A DC-100 GHz Bandwidth and 20.5 dB Gain Limiting Amplifier in 0.25µm InP DHBT Technology

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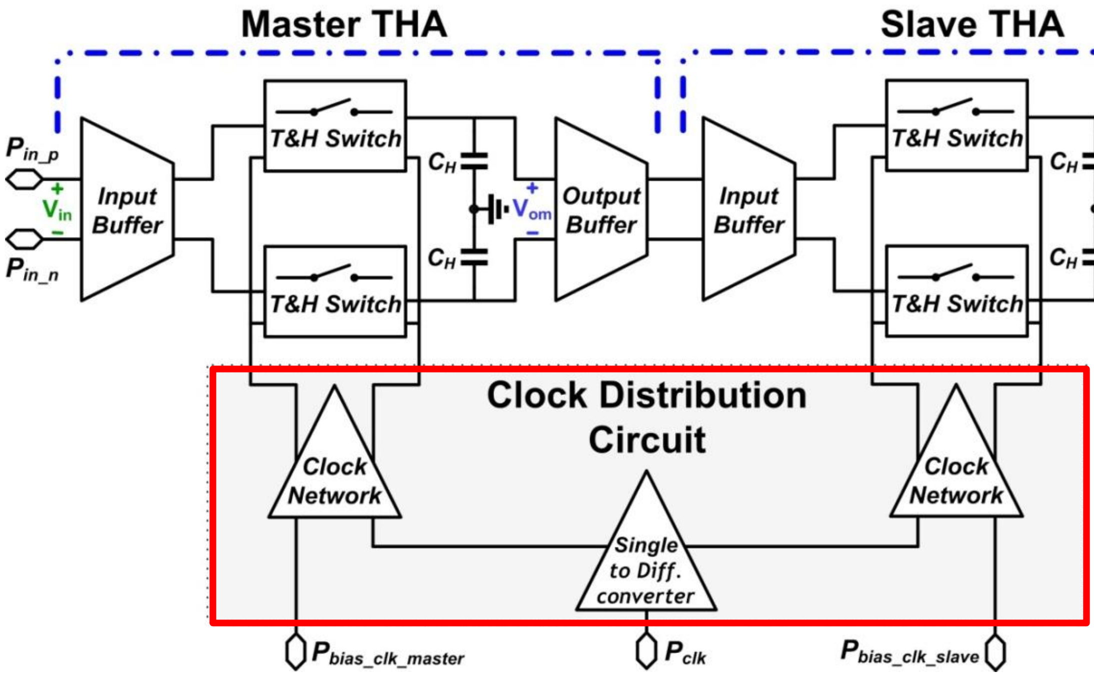
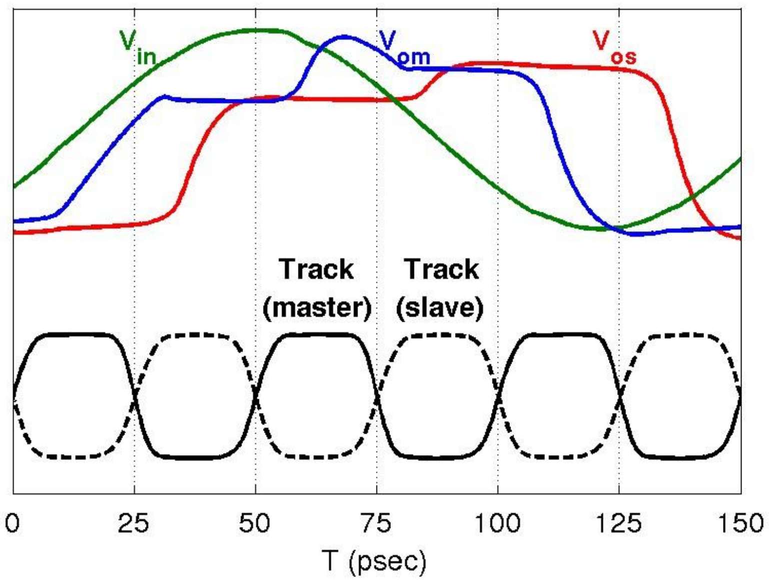
Outline

- **Application and Motivation of the work**
- **TSC 250nm HBT process overview**
- **Block diagram & schematic of the circuit**
- **Layout & EM modeling**
- **Measurement results and comparison table**

Motivation - I

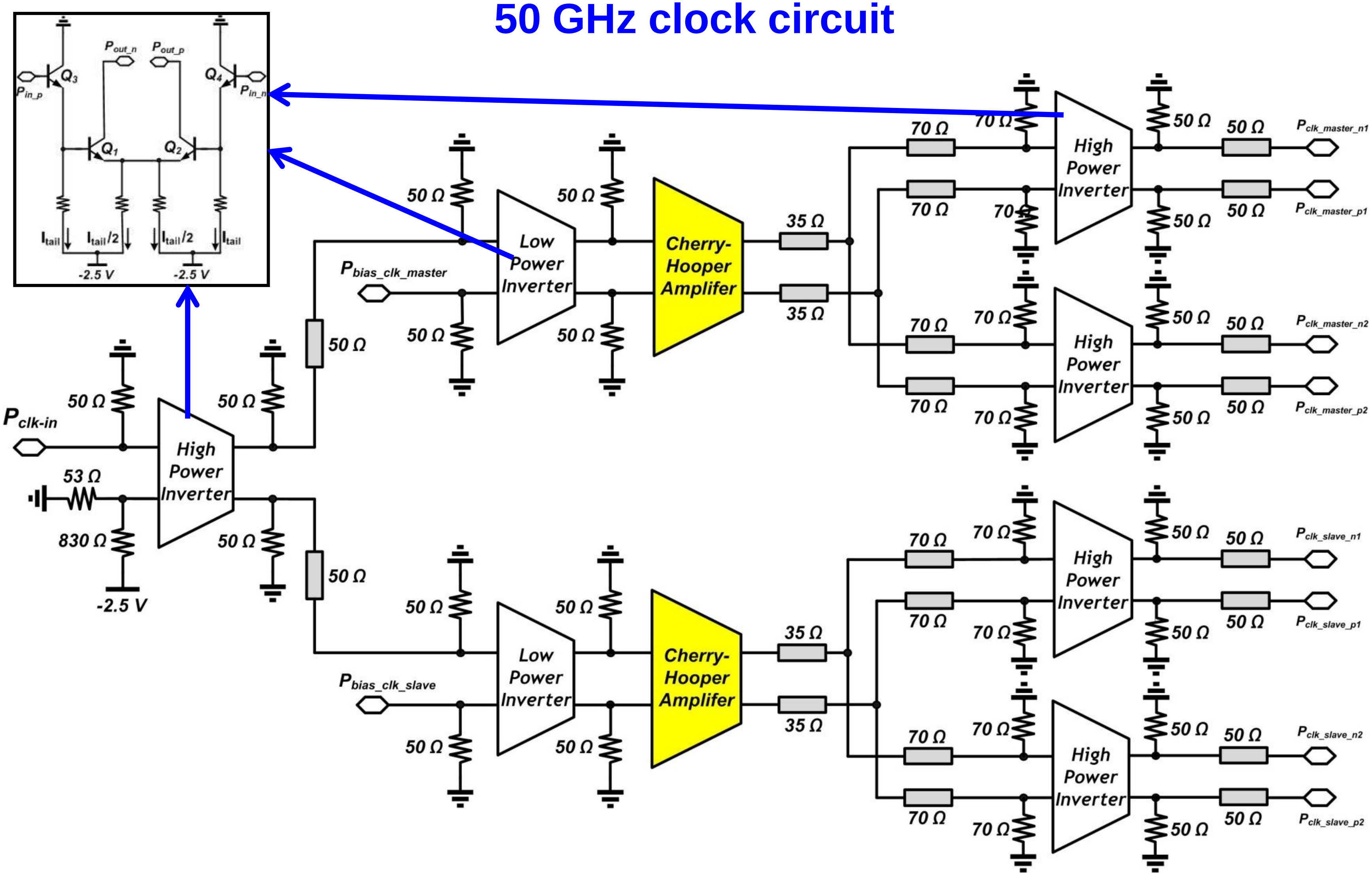




50 GSample/sec Sample & Hold circuit

Motivation - II

50 GHz clock circuit



Applications - I

- **High speed optoelectronic signal conversion requires broadband receivers**

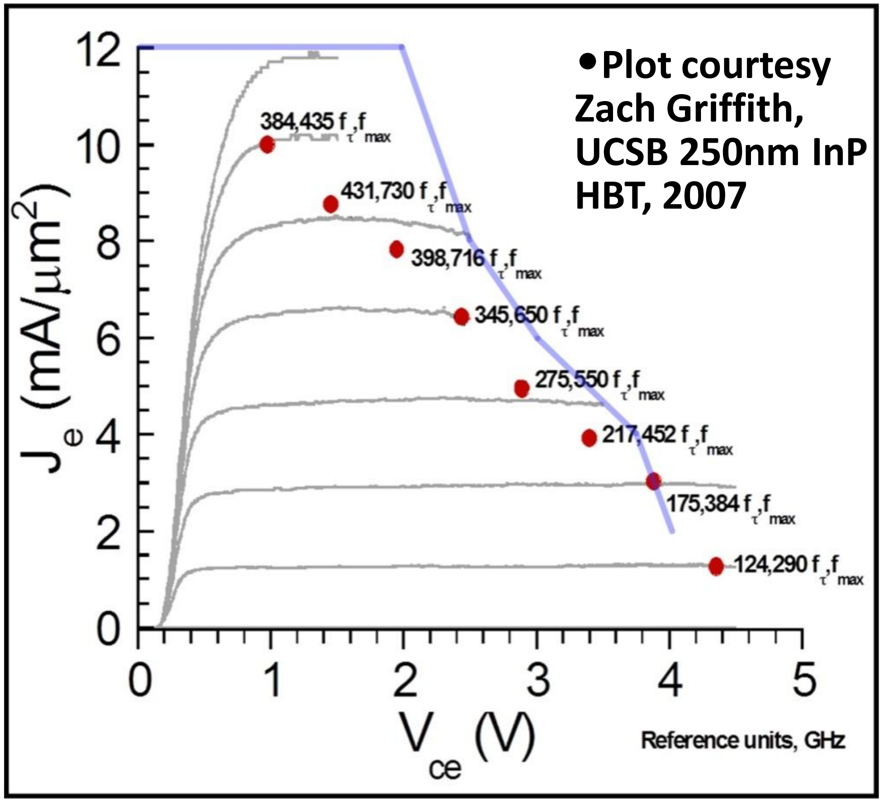
- **Limiting amplifiers are the key components in these receivers in order to:**

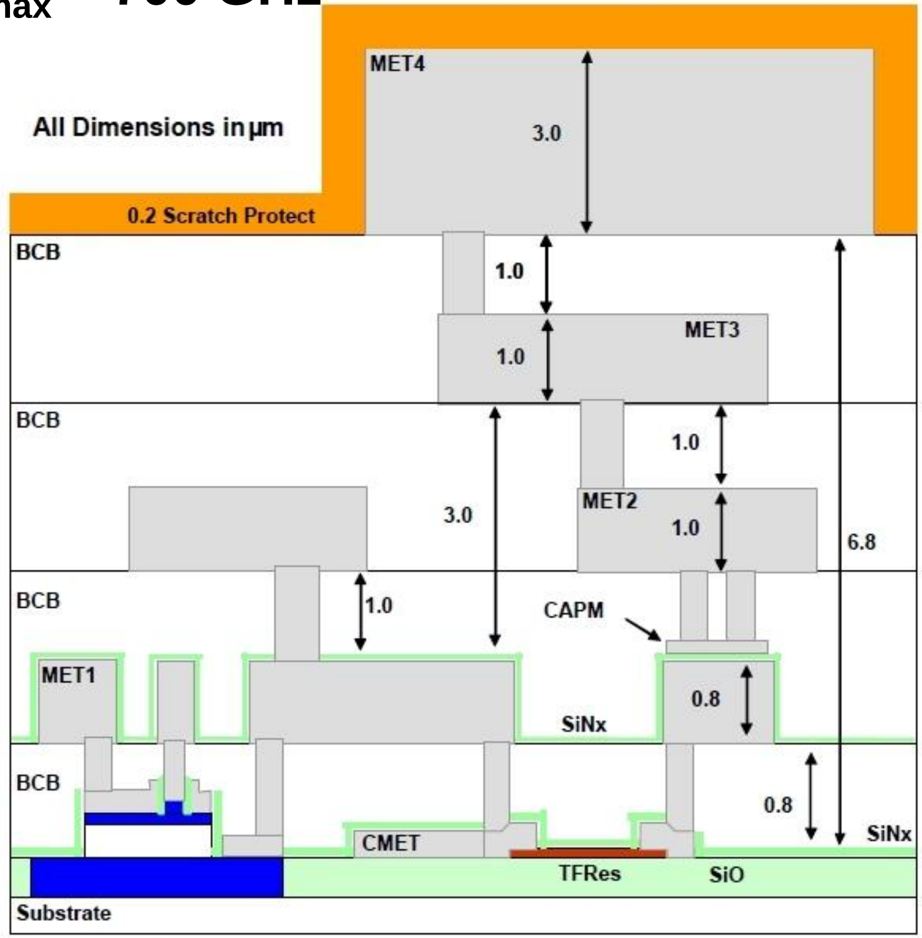
  ✓ **Provide a low input sensitivity and sufficient gain to achieve saturated output levels from small-signal inputs which enables reliable decision making**

  ✓ **Provide a wide bandwidth to achieve short rise and fall times in order to provide an output signal with minimum distortion**

TSC 250nm InP HBT process

- Four metal interconnect stack
- Peak bandwidth of f_t=400 GHz & f_{max} = 700 GHz
- MIM caps of 0.3 fF/µm^2
- Thin-film resistors 50 Ω/square





Representative cross-section of TSC250 IC technology. Drawing is not to scale.

Modified Cherry-Hooper stage [1-3]

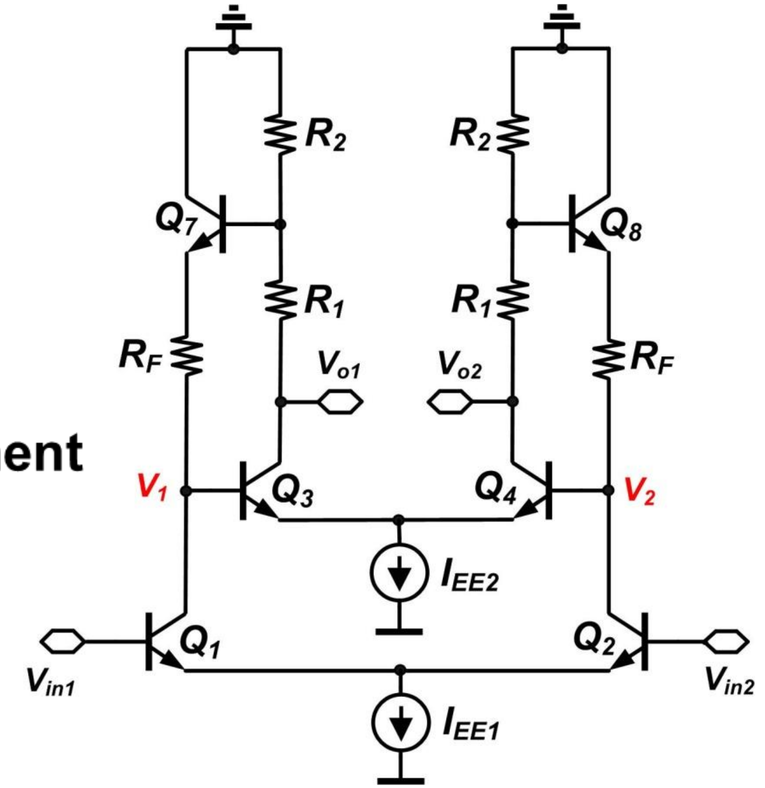
Large signal behavior:

$$V_{o1} - V_{o2} \cong (R_1 + R_2) I_{EE2} \cdot \tanh\left(\frac{V_2 - V_1}{2V_T}\right)$$

- **Conventional C-H amp. gain ≈ $g_{m1\text{-}2} R_F$**

Modified C-H amp. provides gain enhancement

by a factor of $\left(1 + \frac{R_2}{R_1}\right)$ while $0 < \frac{R_2}{R_1} < 2.5$



[1] Y. M. Greshishchev et al., “A 60-dB gain, 55-dB dynamic range, 10-Gb/s broad-band SiGe HBT limiting amplifier,” IEEE JSSC, vol.34, no.12, pp. 1914-1920, Dec. 1999.

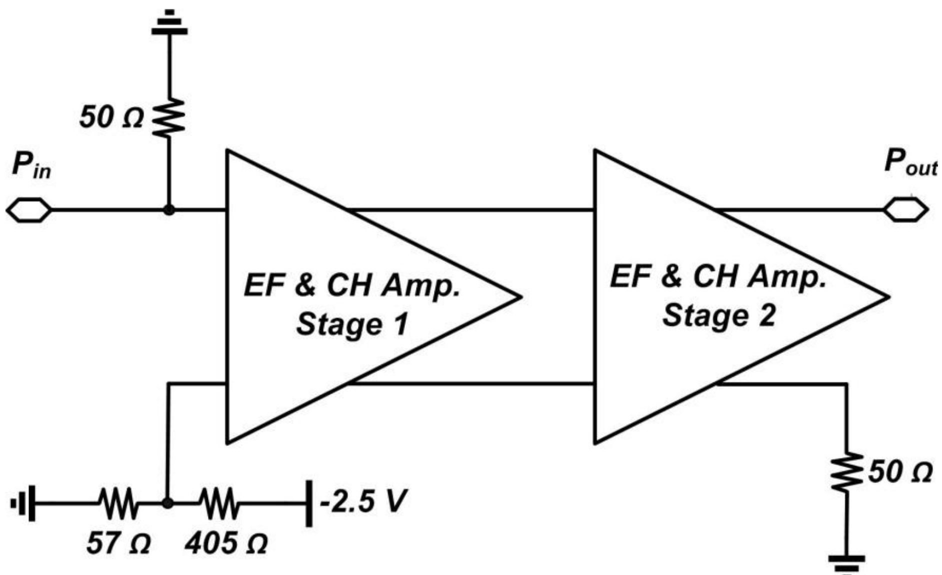
[2] K. Ohhata et al., “Design of a 32.7-GHz bandwidth AGC amplifier IC with wide dynamic range implemented in SiGe HBT,” IEEE JSSC, vol.34, no.9, pp. 1290-1297, Sep. 1999

[3] C. D. Holdenried et al., “Analysis and design of HBT Cherry-Hooper amplifiers with emitter-follower feedback for optical communications,” IEEE JSSC, vol.39, no.11, pp. 1959-1967, Nov. 2004.

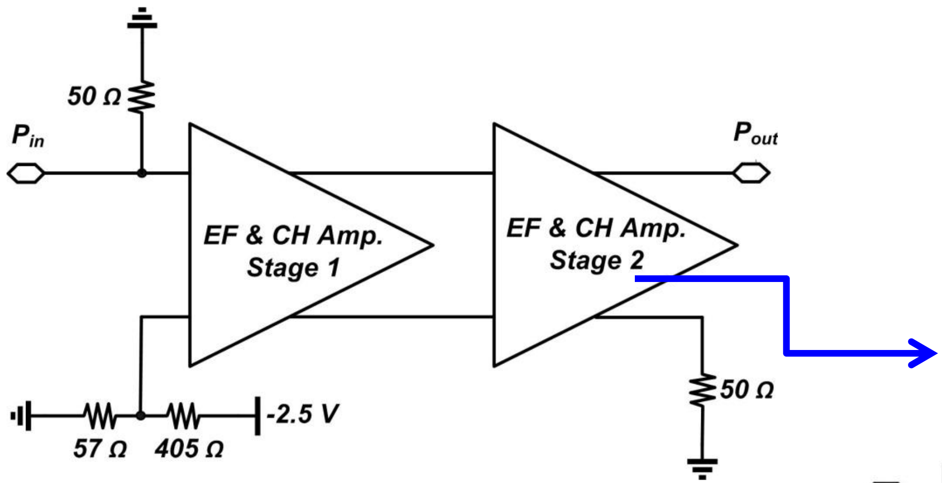
Block Diagram

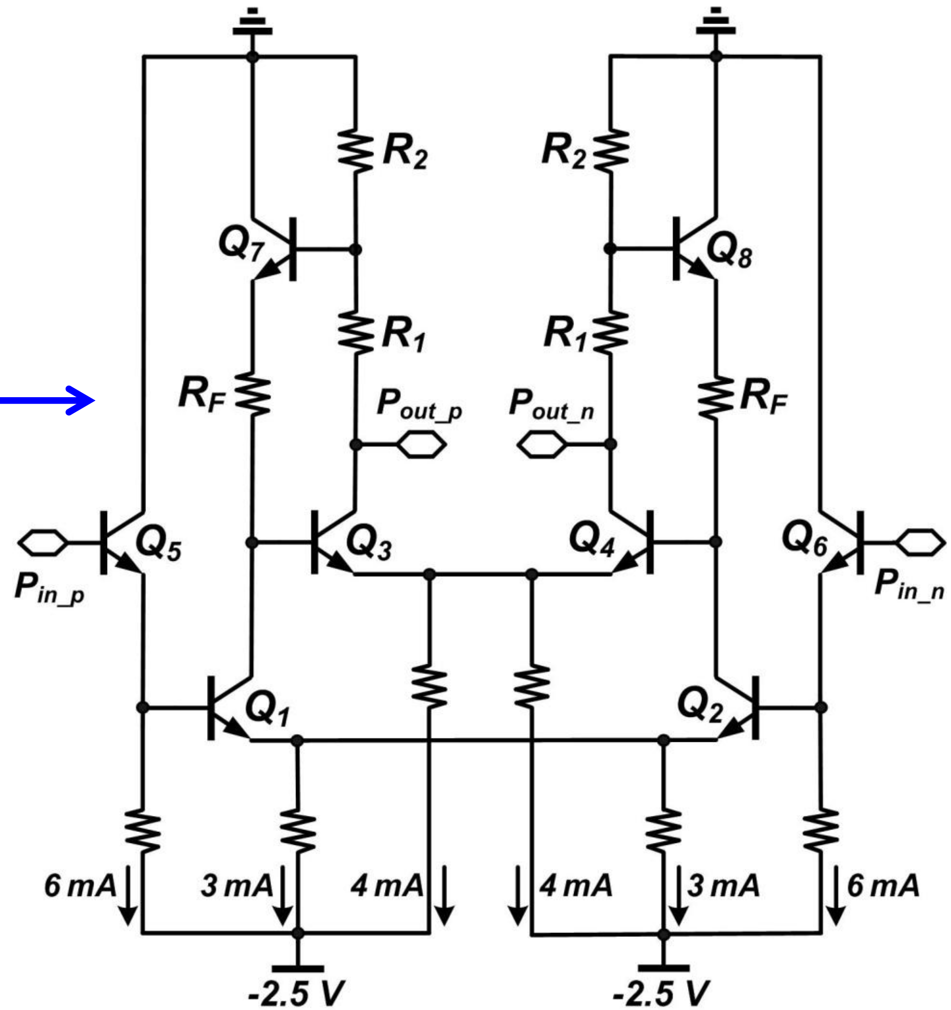
Single-ended gain and BW measurements have be chosen due to unavailability of 4-port s-param measurement for frequencies > 67 GHz

⟶ ~6dB gain has been added to get the differential equivalent



Schematic





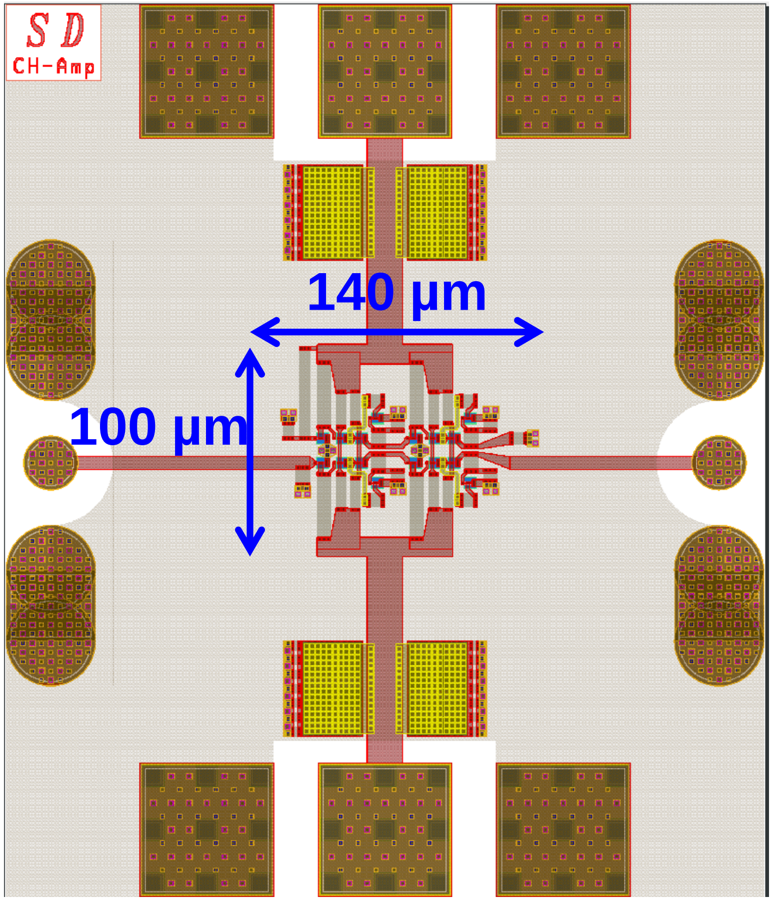
R_1 =30 Ω

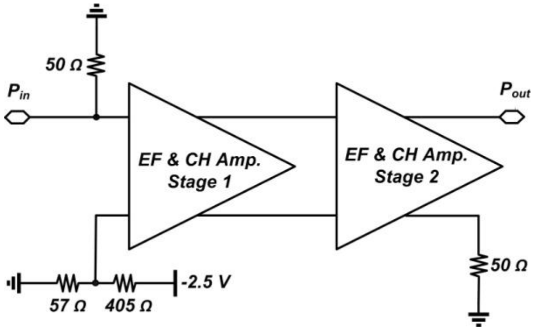
R_2 =50 Ω

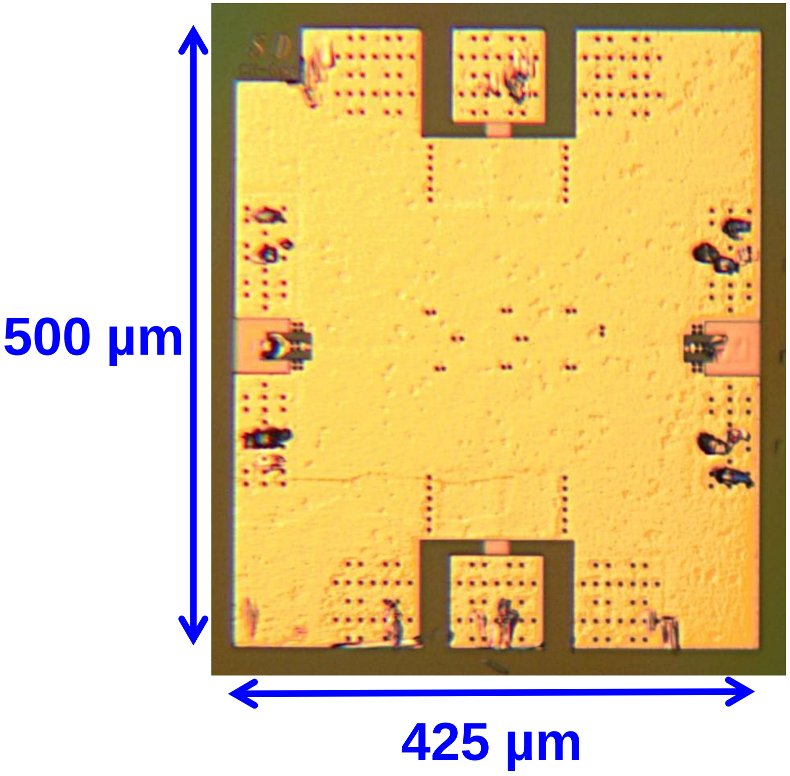
R_F =40 Ω

$Q_{1\text{-}8}$ =3x0.25 µm

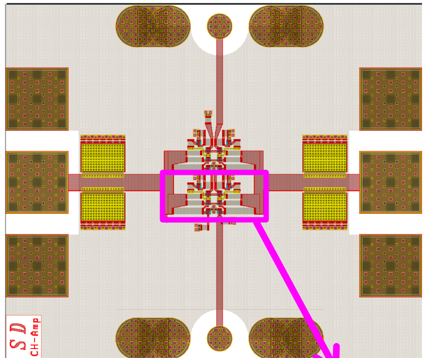
Compact layout

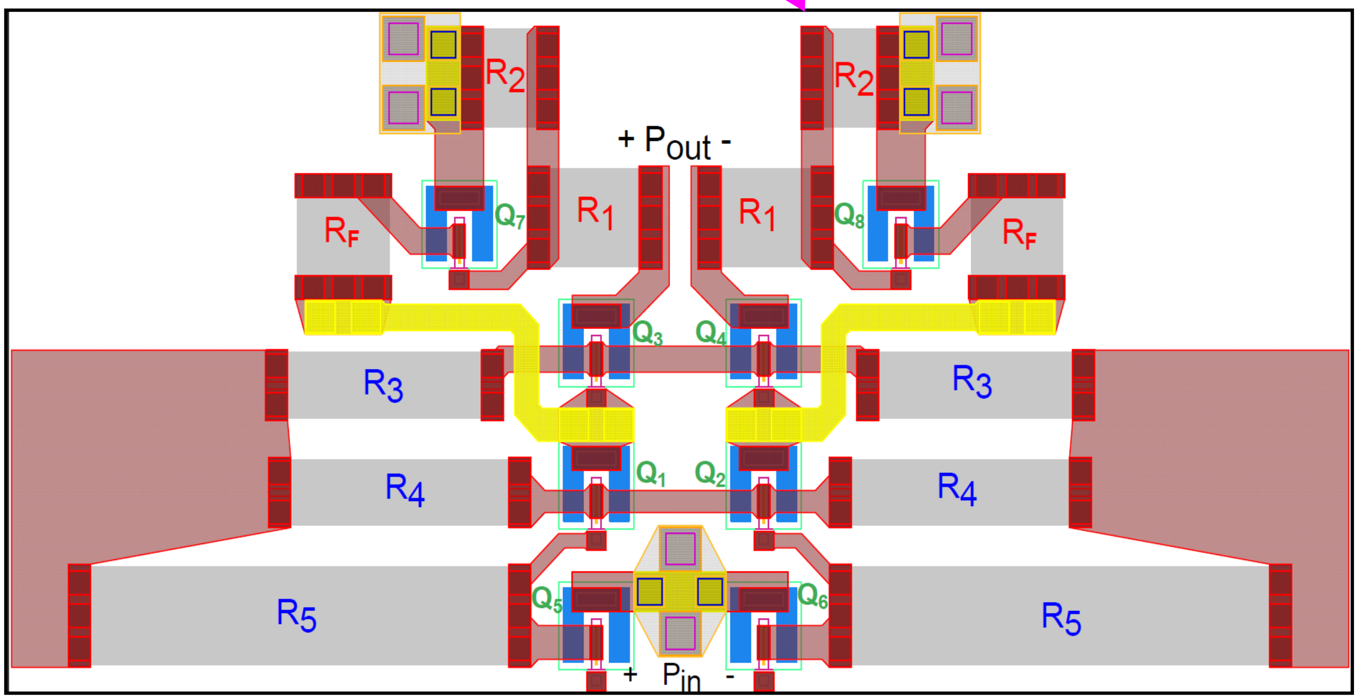


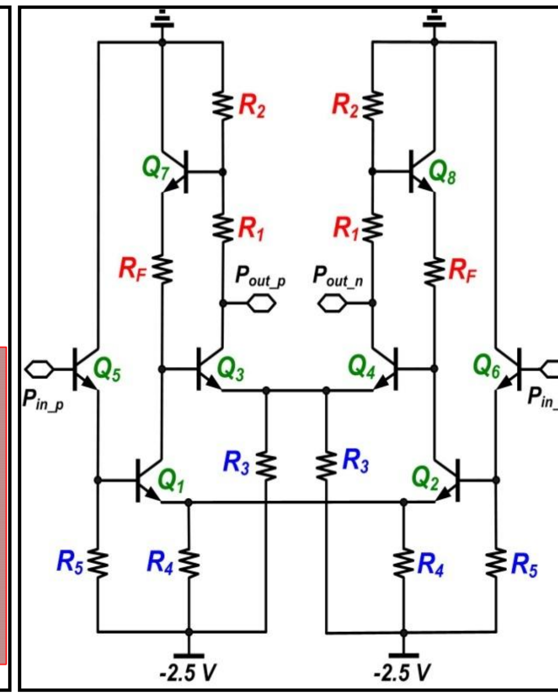




Symmetric layout

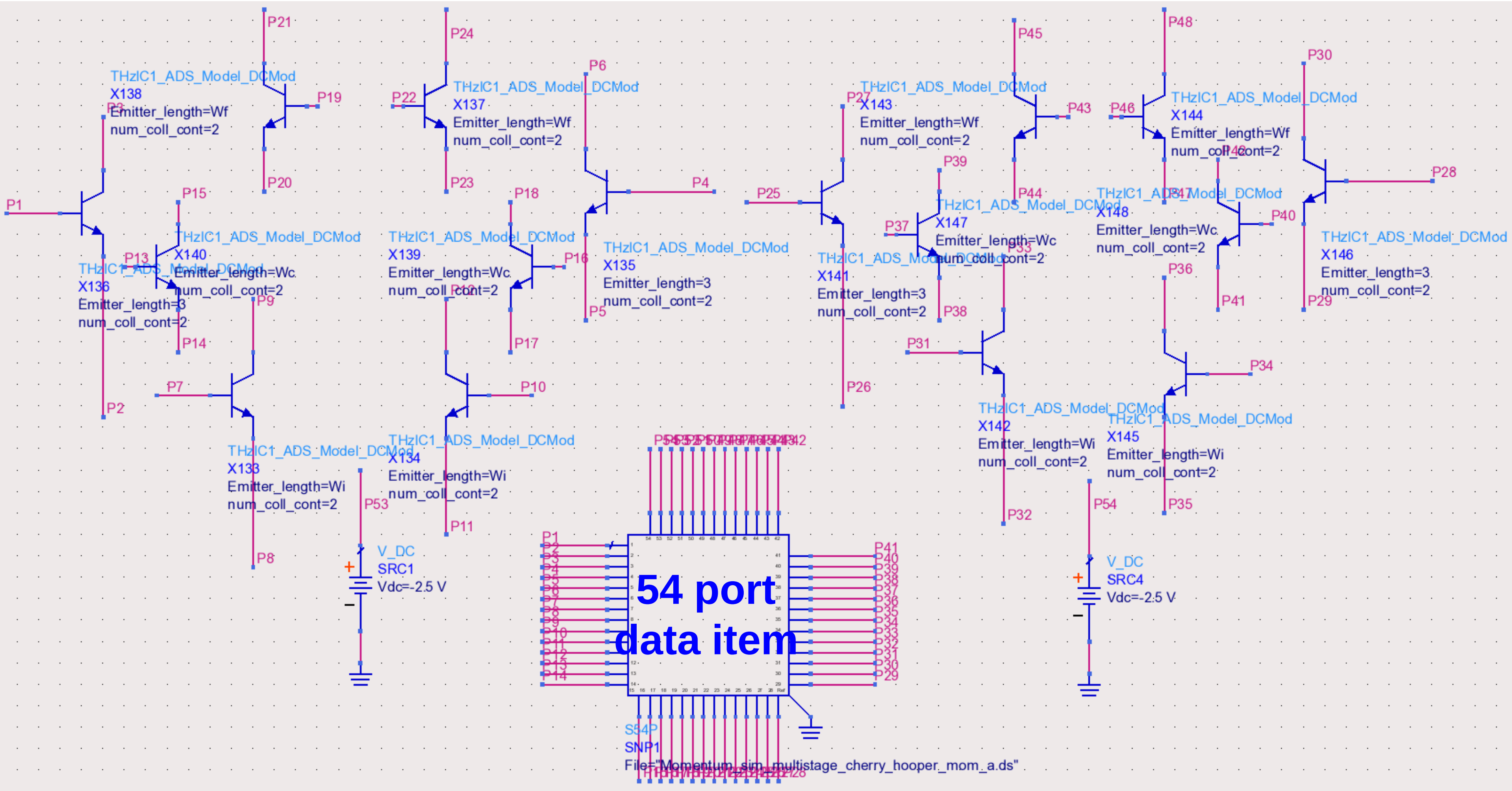






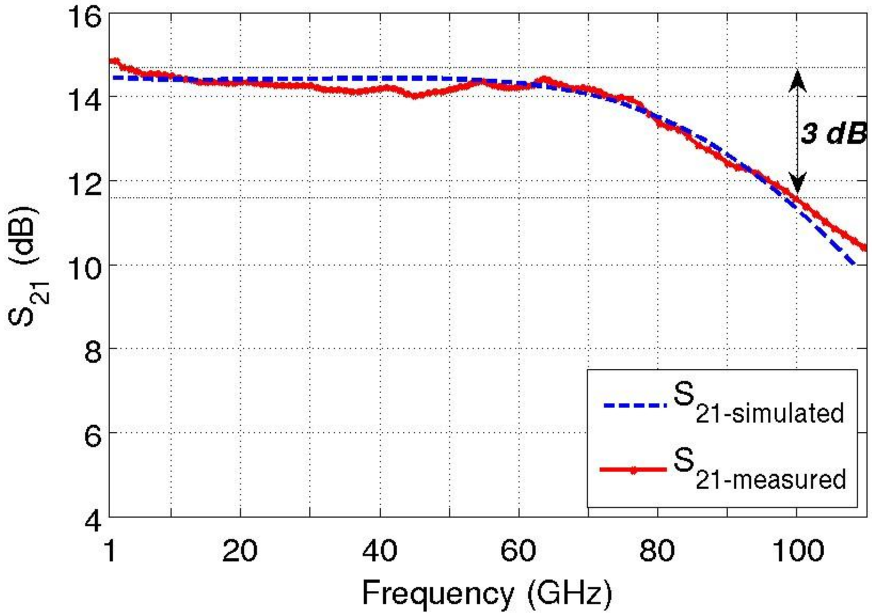
EM Simulation

Whole chip has been modeled using ADS momentum EM simulator

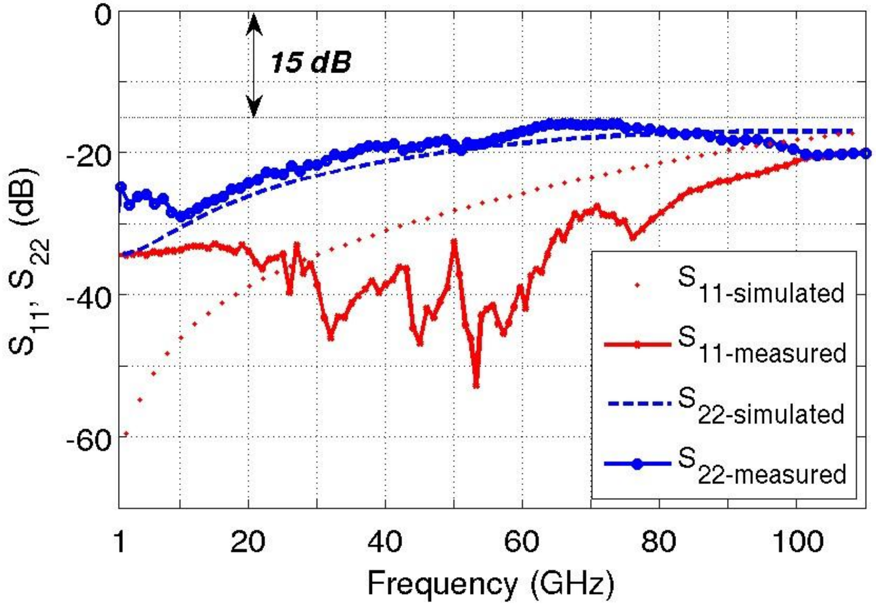


S-parameter measurement results - I

Single-ended insertion loss



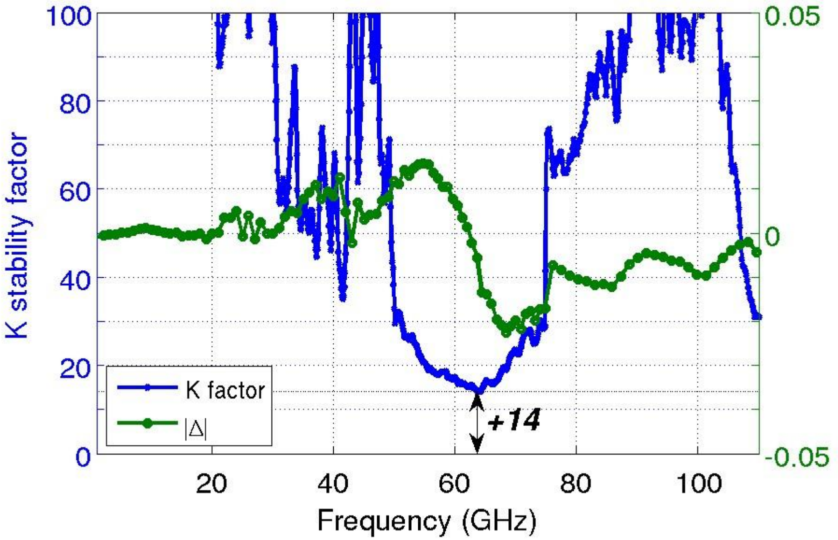
Single-ended input and output return loss



- **S_{21}=14.5 dB , 3dB BW = 100 GHz**
- **S_{21} gain ripple < ±0.5 dB**
- **S_{11}< -20 dB , S_{22}< -15 dB**

S-parameter measurement results - II

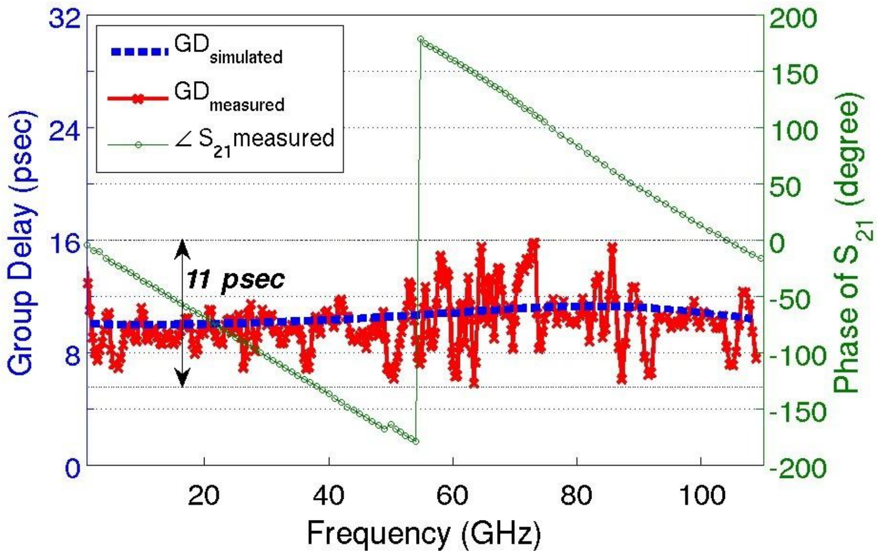
Rollet Stability factor



$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

Group Delay



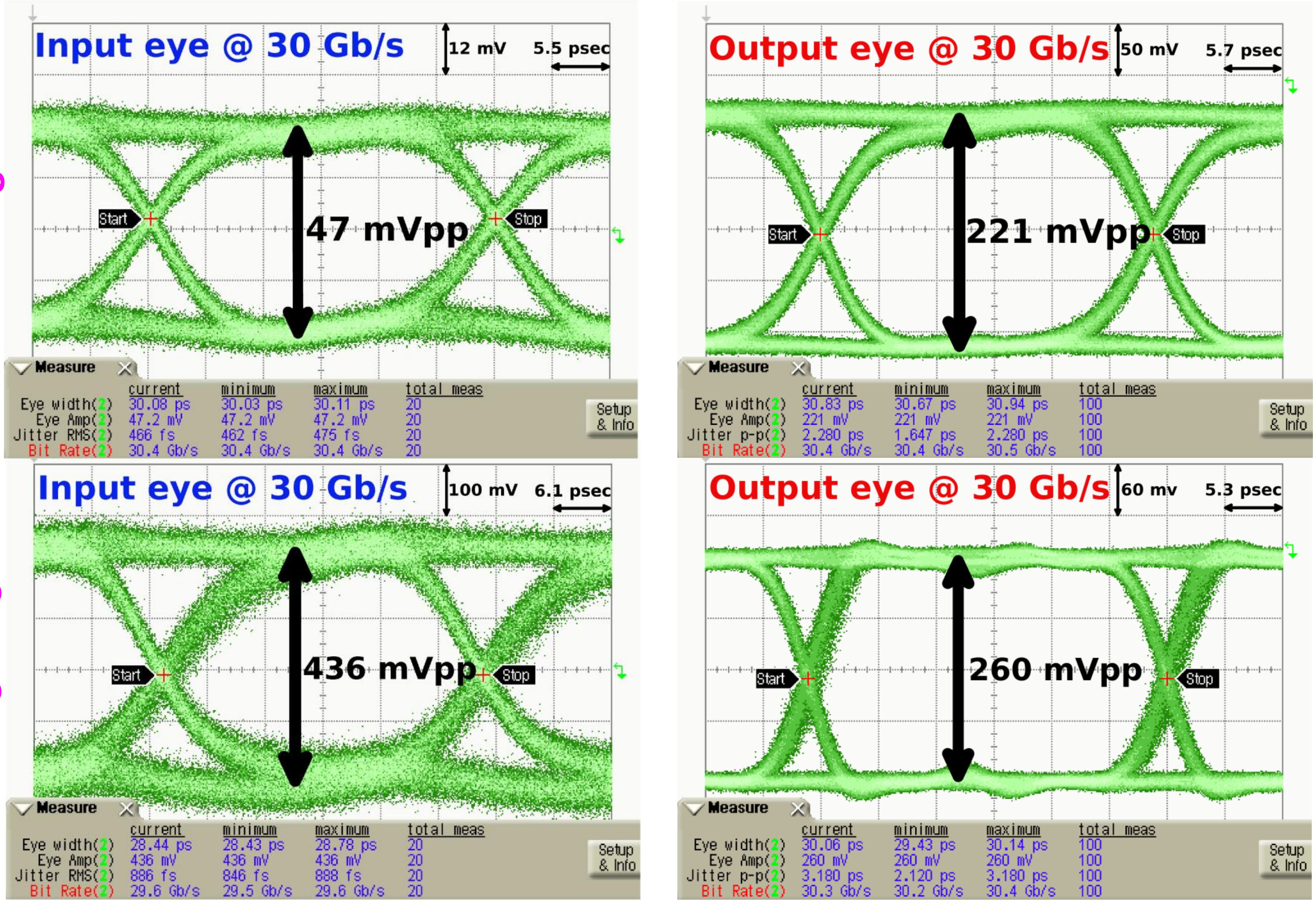
$$\tau_{Group\ Delay} = -\frac{d\varphi}{d\omega} = -\frac{d\theta}{df \cdot 360^{\circ}}$$

Group delay ≈ 9 psec
Group delay variation = 11 psec

Eye diagrams @ 30 Gb/s

Small Signal

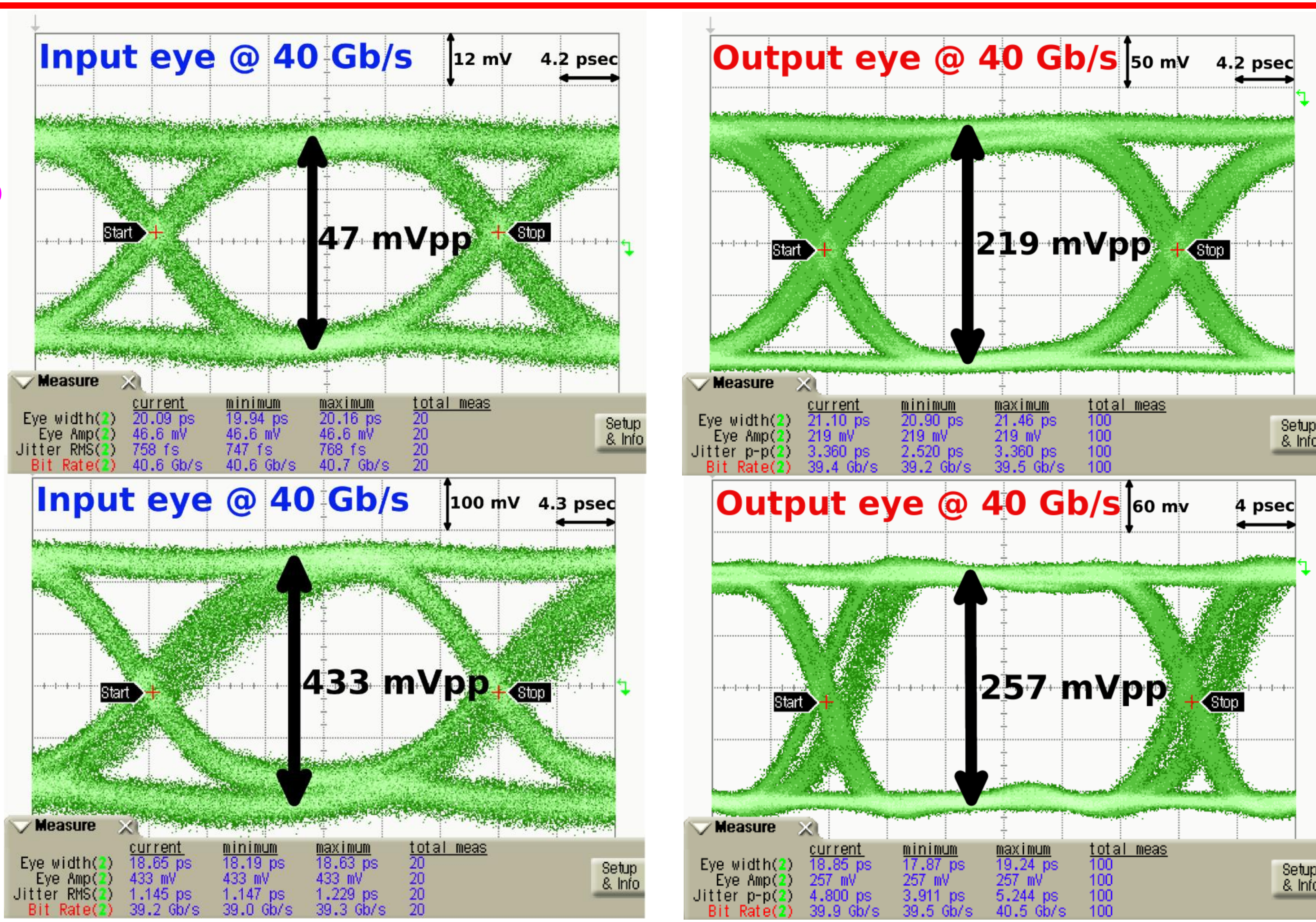
Large Signal



Eye diagrams @ 40 Gb/s

Small Signal

Large Signal



Comparison table

COMPARISON TO SIMILAR BROADBAND AMPLIFIERS REPORTED IN THE LITERATURE.

Ref.	Gain$_S$* (dB)	Gain$_D$** (dB)	BW† (GHz)	GBW‡ (GHz)	IRL$^\perp$ (dB)	ORL$^\top$ (dB)	GR$^\diamond$ (dB)	GD§ (psec)	Supply (V)	Power (mW)	Area (mm^2)	GBW/P$_{DC}$ (GHz/mW)	Archit-ecture	Process
[1]	11	-	90	320	>5	>7	2.4	-	2.5	210	1.28	1.52	DA[1]	0.12μm SOI CMOS
[4]	7	13	81	362	>7	>7	>5	-	5.5	495	1.17	0.73	DA[1]	SiGe f_T=200 GHz
[5]	10	16	62	391	>11	>3	>3	-	-5	775	0.3	0.51	EF & DP[2]	SiGe f_T=200 GHz
[6]	14	20	84	840	>7	>7	4	±32	-5.5	990	0.63	0.85	EF & CA[3]	0.18μm SiGe
[7]	-1	5	62	110	>14	-	>3	-	2.5	125	-	0.88	EF & CH[4]	0.13μm SiGe
[8]	10	-	102	323	>8	>9	<2	±6	2	73	0.29	4.42	DF & CW[5]	0.12μm SiGe
[9]	24	30	43	1360	>7	>7	>2	±10	-4	500	0.7	2.72	EF & CH[4]	1μm InP SHBT
[11]	15	21	44	494	>6	>10	<2	-	5.2	458	0.66	1.08	EF & CH[4]	InGaAs-InP HBT
[12]	15	-	67	729	>7	>10	>2	±10	3.5	133	0.09	5.50	-	0.5μm InP DHBT
[13]	21	-	120	1350	-10	-10	3	±15	-	610	2	2.21	DA[1]	InP DHBT
[14]	10	16	110	694	>5	>5	>3	-	-4	304	0.95	2.28	EF & CH[4]	0.25μm InP HBT
This work	14.5	20.5	100	1060	>20	>15	1	±5.5	-2.5	145	0.21	7.31	EF & CH[4]	0.25μm InP DHBT

* Measured single-ended S_{21} gain, ** Inferred differential S_{21} gain, † 3-dB bandwidth of S_{21}, ‡ Inferreded differential S_{21} gain $\times$ its 3-dB bandwidth, $^\perp$ Input return loss, $^\top$ Output return loss, $^\diamond$ Total S_{21} gain ripple, § Group delay variation of S_{21}, [1] Distributed amplifier, [2] Emitter follower & differential pair, [3] Emitter follower & cascode stage, [4] Emitter follower & Cherry-Hooper stage, and [5] Darlington feedback amplifier & constructive wave amplifier.

Thank you for your listening