30% PAE W-band InP Power Amplifiers using Sub-quarter-wavelength Baluns for Series-connected Power-combining

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***Abstract* — We present high-efficiency W-band power amplifier (PA) ICs with a new series-connected power-combining technique using sub-quarter-wavelength transmission-line baluns. The PAs are implemented in a 0.25µm InP HBT process. At 86GHz, a single-stage PA exhibits 30.4% peak PAE, 20.37dBm P_{out} and 23GHz 3dB-bandwidth. A two-stage PA exhibits 30.2% PAE, and 23.14dBm P_{out}. These values of PAE represent a 1.2:1 improvement in the state-of-the-art for E- and W-band PAs having similar RF output powers.**

***Index Terms* — W-band power amplifiers, power-added-efficiency, sub-quarter-wavelength baluns, InP HBT device.**

I. Introduction

High efficiency W-band power amplifiers (PAs) are required for future high-speed communications and high-resolution radar/imaging systems. High power allows large signal transmission coverage, while high efficiency extends battery life, saves energy and reduces cost. W-band PA design is challenging because of limited transistor bandwidth and because power-combining networks are lossy and occupy considerable die area [1-3].

With GaN W-band PAs [1-2], where the high FET breakdown voltage allows >10V supplies, 530mW/mm^2 output power per unit IC die area has been reported, as has 24.7% power-added efficiency (PAE) at 206mW output power and 20.0% PAE at 1.8W [1-2]. InP HBTs have higher power-gain cutoff frequencies- greater than 1THz f_{max}- hence higher W-band power gain is available than in GaN. Consequently, despite the lower 2.5~3V supply voltages [4], the efficiency of W-band InP PAs can exceed levels currently demonstrated in GaN. High PAE and output powers approaching 1W are feasible in W-band InP HBT power amplifiers.

Efficient output power combining techniques are necessary both for high PAE and for high output power per unit die area. Whether they use quarter-wavelength (λ/4) line sections, i.e. Wilkinson combiners, or sub-quarter-wavelength lines, classic corporate output power-combiners have high attenuation and occupy large IC die areas [1-2]. Power combiners using transformers [3] or baluns can occupy smaller die areas, but attenuation, imbalances between ports, and low transformer coupling-factors present design challenges which impair efficiency.

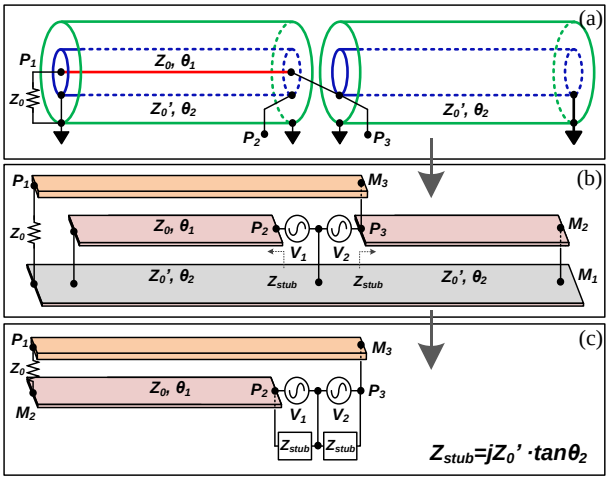

Fig. 1. A new sub-quarter-wavelength balun using (a) triaxial cables, (b) three-metal interconnects and (c) its equivalent-circuit model showing series-connected power-combining.

Here we report high performance PAs using a new sub-quarter-wavelength balun for series-connected power-combining (Fig. 1). We review the InP HBT IC process in Section II. The power-combiner is described in Section III, and the PA design procedure is described in Section IV. Section V presents measured results.

II. InP Device and IC Process

The W-band PA ICs reported in this paper are designed using 0.25µm InP HBTs with a breakdown voltage BV_{CEO}=4.5V. An HBT-cell having four fingers, each 0.25x6µm^2, exhibits 590GHz f_{max} and 350GHz f_τ at J_E=6mA/µm^2 emitter current density. The IC process has three levels of gold interconnects, as shown in Fig. 1 (b), where vias provide access from the top layer M_3 (3µm thickness) to the bottom two layers M_2 and M_1 (each has 1µm thickness). The three metal layers are separated by BCB (ε_r=2.7) dielectric layers M_3-M_2 (5µm thickness) and M_2-M_1 (1µm thickness), respectively. MIM capacitors of

0.3fF/μm^2 and thin film resistors of 50Ω/square are incorporated for matching and biasing.

III. SUB-QUARTER-WAVELENGTH BALUNS

The output power-combiner is similar to a wideband Marchand balun, but unlike the Marchand design [5], uses line sections much shorter than $\lambda_g/4$, a quarter of a guide wavelength. In this sub-quarter-wave design, power-combining losses are greatly reduced simply because of greatly reduced transmission-line length. The required die area is similarly reduced. The sub-quarter-wave design introduces shunt inductive loading at the ports connecting to the transistors, loading which is tolerated by absorbing it into the amplifier output tuning network, thereby tuning the transistor output capacitance. To maintain phase balance, an identical balun is used on the PA input.

A. Series-connected Power-combining Baluns

The proposed balun structure can be analyzed by considering *triaxial* cable and *triplate* transmission-lines (Fig. 1). The *triaxial* cable in Fig. 1 (a) consists of an inner-conductor (red), mid-conductor (blue) and outer-conductor (green) which correspond to the metal planes M_3, M_2 and M_1, in Fig. 1 (b) and (c), respectively. In the coaxial structure, conductor M_2 shields conductor M_1 from conductor M_3, hence the balun eigenmodes are the voltages between M_1 and M_2, with characteristic impedance Z_0 selected to be 50Ω, and the voltage between M_2 and M_3, with characteristic impedance Z_0', which can be arbitrary. In the *triplate* configuration, the conductor M_2 is made much wider than the conductor M_3, so as to again shield M_3 from M_1. The M_1-M_2 (impedance Z_0') and M_2-M_3 (impedance Z_0) voltage differences then again become the normal modes of the structure.

The balun output power-combiner (Fig. 1 (b)) is now clearly and simply understood using the equivalent circuit of Fig. 1 (c), where the voltage sources V_1 and V_2, connected to balun ports P_2 and P_3 respectively, are connected in series between conductors M_2 and M_3, the 50Ω transmission-line connected to the 50Ω amplifier load. Voltage sources V_1 and V_2 are also loaded by the shunt-stub impedance $Z_{stub} = jZ_0' \cdot \tan\theta_2$ associated with the short-circuited transmission-line stubs between M_1 and M_2. Given the series connection, V_1 and V_2 are each individually loaded by the parallel combination of 25Ω and the inductive shunt impedance Z_{stub}.

In class-A power amplifier design, highest output power and highest collector/drain efficiency are obtained if the transistor is loaded in a LR parallel network whose resistive part $R_{L,opt} = (V_{\max} - V_{\min})/I_{\max}$ is the ratio of maximum transistor voltage swing to maximum transistor current, and whose inductive part $j\omega L = -1/j\omega C_{out}$,

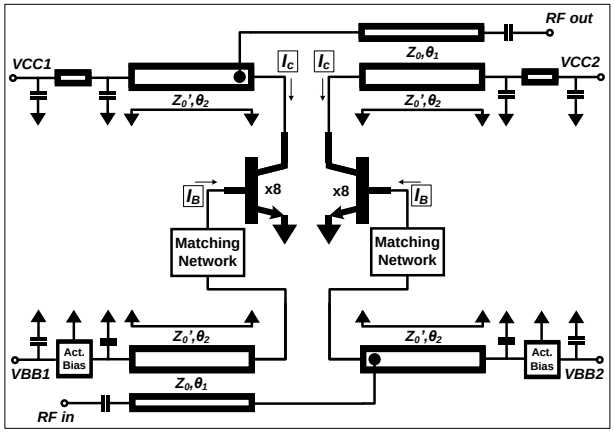

Fig. 2. The single-stage PA circuit schematic.

where C_{out} is the transistor output capacitance. Design therefore consists of adjusting the HBT junction area, and hence $I_{\max}$, until $R_{L,opt} = 25\Omega$, and then subsequently adjusting the balun length θ_2 until $Z_{stub} = -1/j\omega C_{out}$.

In these designs using 2:1 baluns, each of the two HBT power cells has 2:1 larger junction area, and 2:1 larger $I_{\max}$, than a device sized to directly drive 50Ω with appropriate shunt inductive tuning. The total output power is therefore increase 4:1. We have also designed and fabricated, and are presently testing, PA designs with 4:1 series-connected baluns. In simulations, these provide a 16:1 increase in output power.

B. Balun Design in Real ICs

The *triaxial* cable for the proposed balun concept is designed using the Teledyne Scientific Company's IC process, which supports three-metal interconnects as shown in Fig. 1 (b). This metal stack is not optimum for the proposed balun structure, because the M_3-M_2 distance of 5μm is higher than the M_2-M_1 distance of 1μm, and the metal stacks lead non-negligible E-fields between M_3-M_1. In order to solve this problem, two sidewalls adjacent to M_3 are used with dense arrays of via$_{23}$ supporting the functionality of the *triaxial* cable. The top-metal M_3 (width w_3=12μm) and the second-metal M_2 (width w_2=42μm) with the sidewalls (M_3-M_3 spacing of 5μm) produce a Z_0=50Ω. The other characteristic impedance Z_0'=55Ω between M_1-M_2 is implemented using 3μm slot-type spacing transmission-line due to the small distance of 1μm between M_1-M_2.

In order to verify the operation and the performance of the proposed balun, test structures of two back-to-back baluns have been designed and fabricated, and their insertion losses have been measured at frequencies of 80, 90, and 100GHz with different values of capacitors (103, 78, and 65fF). The measured results verify the predictions with the insertion loss less than 0.6dB which is achieved from one balun as small as ~λ/16.

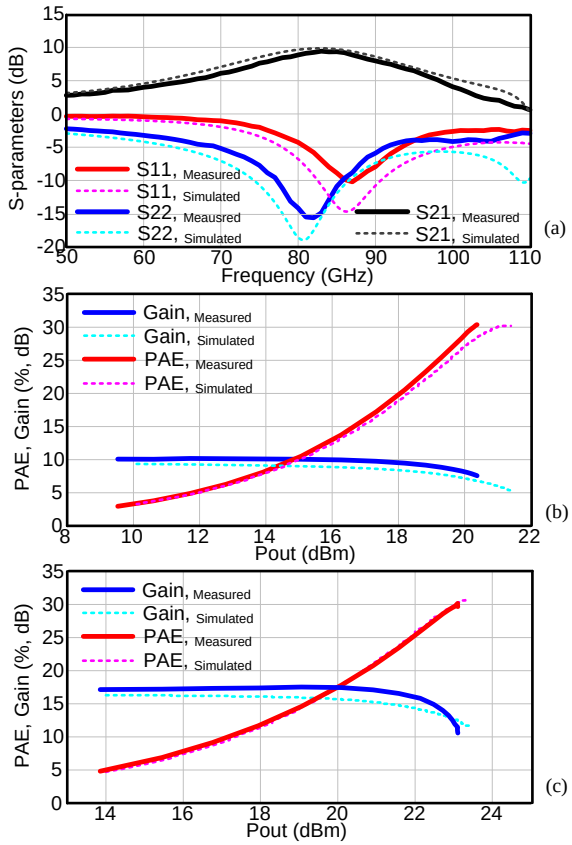

Fig. 3. Measured and simulated PA results: (a) S-parameter results for the single-stage PA, (b) PAE and gain vs. output power for the single-stage PA and (c) PAE and gain vs. output power for the two-stage PA.

IV. Power Amplifier IC Designs

The high-efficiency W-band single-stage and two-stage 2:1 series power-combined PAs have been designed using the sub-quarter wavelength *triplate* transmission-line baluns as the single-stage PA schematic diagram shown in Fig. 2. 2x4-finger scaled HBT cells have been selected for a DC current with 25mA, which is slightly lower than a class-A bias in order to maintain the speed of transistors and achieve higher PAEs. The cells have an optimum load impedance R of 25Ω, which is an appropriate value for a 2:1 impedance transformation to an un-balanced input and output load of 50Ω. Since the outputs of the PA-cells contain a parasitic collector-emitter capacitance C_{out} of ~90fF, the shrunk balun can fit into the output of PA cells without any other matching components.

The center frequency of 84GHz is targeted for the PA designs where the electrical length of $\theta_2=\lambda/4$ (400μm) on the slot-type transmission-lines can be decreased to the electrical length of $\theta_2<\lambda/16$ (91μm). Decoupling capacitors of about 1.8pF between M_2-M_1 are used on the ending edges of the input and output baluns in order to provide RF shorts while maintaining DC bias feeds to the PA input and output. Moreover, semi- λ/4 lines with additional bypass capacitors are used on the bias lines to prevent external bias circuit effects. The differential (or push-pull) operation is achieved by having the identical baluns on the input and output while the input of the HBT cells are properly matched to the differential ports of the input balun in order to obtain maximum power transmission. Active bias circuits using an emitter buffered bias topology with two stacked diodes and one resistor to V_{BB} are utilized for the thermal stability and slightly lower bias operation than a class-A [6]. The two-stage PA has been also designed by the back-to-back connection of the single-stage amplifier with a DC blocking capacitor.

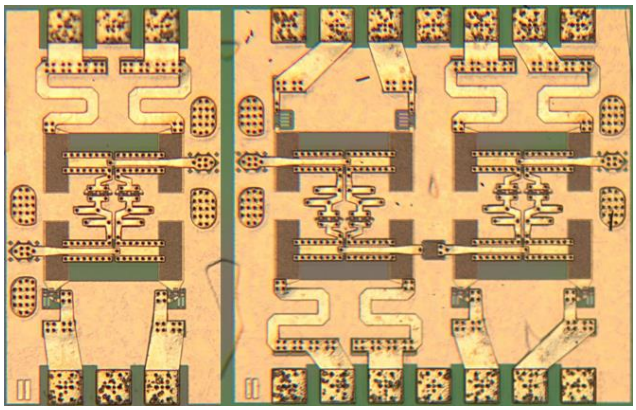

Fig. 4. Die photo of the single-stage and two-stage PAs.

V. IC Characterizations

The two sets of designed and fabricated PA ICs have been measured on the wafer. Small-signal s-parameters on wafer were measured using an Agilent 8510 XF VNA system for single-stage measurements from 50 to 110GHz. A Cascade W-band calibration substrate was used to perform an LRRM probe-tip calibration for these measurements. For large-signal power measurements, high frequency signal was generated with a QuinStar frequency triple and amplified with a Spacek power amplifier (SPW12-10). The set-up was capable of providing ~19mW of power on-wafer at 86GHz. Output power was measured using a Virginia Diodes Erickson PM-4 power meter. The reported power measurements were corrected for the loss of the output probe and connecting waveguide (~1.6dB).

A. Single-stage power amplifier

The performance of the single-stage PA was measured and compared to the simulation results as shown in Fig. 3 (a) and (b). The DC bias points of V_{CC}=2.5V, I_C=50mA, and I_B=2mA are set for the PA measurements. Measured

TABLE I – SUMMARY OF RECENT W-BAND POWER AMPLIFIERS

Ref.	Technology	Freq. (GHz)	f_{max} / f_t (GHz)	BW_{3dB} (GHz)	Max. S_{21} (dB)	P_{out} (dBm)	Peak PAE (%)	V_{DD} or V_{CC} (V)	Area (mm^2)	mW /mm^2	Topology
[1]	0.14μm GaN HFET	94	230 / 97	-	~6	23.14	24.7	12	-	-	Unit-Cell
[1]	0.14μm GaN HEMT	93.5	230 / 97	~10	~18	33.30	19.0	14	-	-	Three-stage 8-way Power-combining
[2]	0.15μm GaN HEMT	91	-	~7	~16	30.79	>20	17.5	2.25	530	Three-Stage Cascades
[3]	0.13μmSiGe BiCMOS	62	-	>10	20.6	20.10	18	1.8	0.72	142	Three-stage 4-way Transformer Balun
This work	0.25μm InP HBT	86	590 / 350	23	9.4	20.37	30.4	2.5	0.37	294 (723)	2-way Series-connected Power-combining Balun
		86	590 / 350	-	17.5	23.14	30.2	3.0	0.67	307 (497)	Two-stage 2-way Series-connected Power-comb.

small-signal s-parameter results, as represented in Fig. 3 (a), exhibit a maximum S_{21} of 9.4dB at 83GHz with a 3-dB bandwidth of 23GHz (72-95GHz). The input power has been swept from -0.5 to 12.8dBm in order to obtain the output power of 9.50 to 20.4dBm at 86GHz as shown in Fig. 3 (b). The single-stage PA exhibits a peak PAE of 30.4% at an output power of 20.4dBm (108.8mW). Fig. 4 (left) shows the IC image of the single-stage PA, with a total chip area of 448x816μm^2 and core area (excluding DC and RF pads) of 295x510μm^2 which exhibits a power density (output powers/active chip area) of 723mW/mm^2.

B. Two-stage power amplifier

The two-stage (back-to-back) PA performance has been also measured and compared to the simulation results as shown in Fig. 4 (c). DC bias points for the first stage are V_{CC}=3V and I_C=30mA, and for the second stage are V_{CC}=3V and I_C=50mA. Under RF signal drive, the operating voltage can exceeds the BV_{CEO}, and the PA could support a DC bias of 3.0V. Large signal performance for the two-stage PA has also been measured at 86GHz where the PA shows a peak PAE of 30% at an output power of 23.14dBm (206mW). The PA IC has been designed within a total area of 824x816μm^2 and a core area of 670x618μm^2 which represents a power density of 497mW/mm^2. Fig. 4 (right) is a photo image for the fabricated two-stage PA IC.

Table-I shows the comparison of the results for the recent high performance PAs at the frequencies around W-band [1-3]. The PA ICs, reported in this paper, have achieved the record PAE of 30.2% with 3-dB bandwidth of 23GHz and high power density of 723mW/mm^2 using the high speed 0.25μm InP HBT technology and the proposed novel sub-quarter-wavelength balun structure.

VI. CONCLUSIONS

We have reported W-band InP power amplifier (PA) ICs designed with 0.25μm InP HBT technology. Using a new proposed efficient power combining technique of a sub-quarter-wavelength balun, the two-stage PA IC achieved 30% PAE at an output power of 23.14dBm while the single-stage PA exhibits a wide 3-dB bandwidth of 23GHz as well as high power density of 723mW/mm^2.

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