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Citation: Appl. Phys. Lett. **103**, 203502 (2013); doi: 10.1063/1.4831683
View online: http://dx.doi.org/10.1063/1.4831683
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Reduction of leakage current in $In_{0.53}Ga_{0.47}As$ channel metal-oxide-semiconductor field-effect-transistors using $AlAs_{0.56}Sb_{0.44}$ confinement layers

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(Received 3 October 2013; accepted 1 November 2013; published online 14 November 2013)

We compare the DC characteristics of planar $In_{0.53}Ga_{0.47}As$ channel MOSFETs using $AlAs_{0.56}Sb_{0.44}$ barriers to similar MOSFETs using $In_{0.52}Al_{0.48}As$ barriers. $AlAs_{0.56}Sb_{0.44}$, with ~1.0 eV conduction-band offset to $In_{0.53}Ga_{0.47}As$, improves electron confinement within the channel. At gate lengths below 100 nm and $V_{DS} = 0.5$ V, the MOSFETs with $AlAs_{0.56}Sb_{0.44}$ barriers show steeper subthreshold swing (SS) and reduced drain-source leakage current. We attribute the greater leakage observed with the $In_{0.52}Al_{0.48}As$ barrier to thermionic emission from the N + $In_{0.53}Ga_{0.47}As$ source over the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterointerface. A 56 nm gate length device with the $AlAs_{0.56}Sb_{0.44}$ barrier exhibits 1.96 mS/μm peak transconductance and SS = 134 mV/dec at $V_{DS} = 0.5$ V. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4831683]

Driven by the potential for improved on-current over Si, $InAs/In_xGa_{1-x}As$ and $In_xGa_{1-x}As$ channel materials are being investigated to replace Si in future generations of CMOS VLSI.[1–6] To date, most reported III-V MOSFETs grown lattice-matched to InP use $In_{0.52}Al_{0.48}As$ lower electron confinement (barrier) layers. For this barrier layer, the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ conduction band offset is approximately 0.52 eV.[7] In the heavily doped source and drain regions, at $4 \sim 8 \times 10^{19}$ cm^{-3} doping, the electron Fermi level, E_f, is ~0.3–0.4 eV above the conduction band edge of $In_{0.53}Ga_{0.47}As$, leaving the $In_{0.52}Al_{0.48}As$ conduction band energy, $E_{c,b}$, only ~0.1–0.2 eV above this Fermi level. This small barrier energy is insufficient to fully confine electrons in the channel; the thermionic emission current density over the barrier can be approximated by

$$J_{th} \approx q(kT/m^*)^{1/2} N_c \exp((E_f - E_{c,b})/kT), \qquad (1)$$

where $N_c = 2 \times 10^{17}$/cm^3 effective density of states of $In_{0.53}Ga_{0.47}As$ and $m*$ is the electron effective mass. Given a 0.2 eV barrier, this thermionic current is approximately 5 μA/μm^2. Given both small (<100 nm) separations between the N+ source and drain, and significant (~500 mV) drain-source bias voltage, the drain-source field is large, and electrons thermally emitted from the N+ source into the $In_{0.52}Al_{0.48}As$ barrier layer are then carried under high field to the drain.

We here show that barrier leakage can be the dominant source of off-state leakage current in short-channel InGaAs MOSFETs with $In_{0.52}Al_{0.48}As$ barriers and small separations between the N+ source and drain. The magnitude of barrier leakage will depend in detail upon the MOSFET's source-drain structure; presence of an $In_{0.52}Al_{0.48}As$ upper barrier layer between the $In_{0.53}Ga_{0.47}As$ channel and the N+ $In_{0.53}Ga_{0.47}As$ source and drain will reduce the electron density within the channel, increasing $(E_{c,b} - E_f)$ and thereby reducing the thermionic leakage,[1] while in other reported III-V MOSFETs the separation between the N+ source and drain is significantly greater than the gate length.[2]

In this letter, we demonstrate $In_{0.53}Ga_{0.47}As$ MOSFETs with an $AlAs_{0.56}Sb_{0.44}$ barrier layer, grown lattice-matched to an InP substrate, and compare its DC characteristics to that of similar MOSFETs using $In_{0.52}Al_{0.48}As$ confinement layers. The $In_{0.53}Ga_{0.47}As/AlAs_{0.56}Sb_{0.44}$ conduction-band offset is ~1.0 eV, providing much greater suppression of barrier leakage current than provided by an $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterointerface. At gate lengths below 100 nm, and for 0.5 V drain-source bias voltage, the MOSFETs with $AlAs_{0.56}Sb_{0.44}$ barriers show steeper subthreshold swing and reduced off-state drain-source leakage current. A 56 nm gate length device shows 1.96 mS/μm transconductance and 134 mV/dec subthreshold swing, both measured at $V_{DS} = 0.5$ V.

The epitaxial layer structures (Figure 1) were grown on semi-insulating InP substrates using solid-source molecular beam epitaxy. Sample A consists of a 400 nm non-intentionally doped (N.I.D.) $In_{0.52}Al_{0.48}As$ buffer layer, a 3 nm Si-doped (1.3×10^{19} cm^{-3}) $In_{0.52}Al_{0.48}As$ pulse doping layer, and a 10 nm $In_{0.53}Ga_{0.47}As$ channel. Sample B consists of a 375 nm N.I.D. $In_{0.52}Al_{0.48}As$ buffer layer, a 25 nm N.I.D $AlAs_{0.56}Sb_{0.44}$ bottom barrier layer, a 3 nm Si-doped (1.3×10^{19} cm^{-3}) $In_{0.52}Al_{0.48}As$ pulse doping layer, a 3 nm N.I.D $AlAs_{0.56}Sb_{0.44}$ spacer layer, and a 10 nm $In_{0.53}Ga_{0.47}As$ channel, with details of $AlAs_{0.56}Sb_{0.44}$ growth as described in Ref. 8. To characterize the interface quality of $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As/AlAs_{0.56}Sb_{0.44}$ heterojunctions, InGaAs single quantum well double heterostructures (DH) with 5 nm and 10 nm well thickness were grown and investigated. The detailed structures were presented in Ref. 8. The measured Hall

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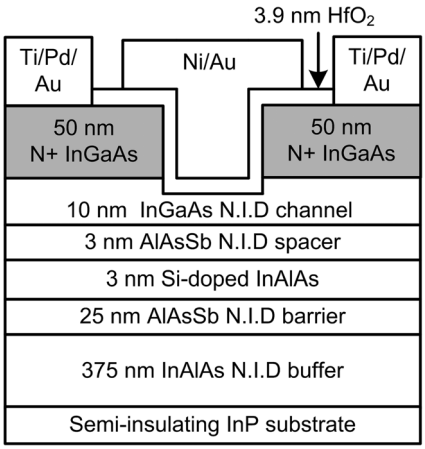

FIG. 1. Structure of sample B ($AlAs_{0.56}Sb_{0.44}$ barrier). The pulse doping layer is 3 nm, 1.3×10^{19} cm^{-3} Si-doped $In_{0.52}Al_{0.48}As$. In sample A, the two $AlAs_{0.56}Sb_{0.44}$ layers are omitted and the $In_{0.52}Al_{0.48}As$ buffer layer is 400 nm thick. (N.I.D. = non-intentionally doped).

mobilities are summarized in Table I. The electron mobility for a 10 nm InGaAs quantum well is about ~9500 $cm^2/V{\cdot}s$ at room temperature for both DHs with InAlAs barriers and AlAsSb barriers. As reducing the well thickness from 10 nm to 5 nm, the electron mobility significantly decreased and was lower for InGaAs/AlAsSb DHs than for InGaAs/InAlAs DHs. The decrease in mobility could be the result of stronger interface scattering associated with the higher conduction band offset of AlAsSb barriers,[9] or a rougher interface for InGaAs grown on a higher aluminum content barrier layer.[10–12]

To fabricate MOSFETs, hydrogen silsesquioxane (HSQ) dummy gates were patterned by e-beam lithography, and ~50 nm thick, *n*-type $In_{0.53}Ga_{0.47}As$ (Si: 4×10^{19} cm^{-3}) source-drain layers were regrown by metal organic chemical vapor deposition (MOCVD). After MOCVD regrowth, the dummy gates were removed in buffered HF. Channel surface damage caused by regrowth was then removed by two cycles of digital etching.[13] The final $In_{0.53}Ga_{0.47}As$ channel thickness is ~7.5 nm for both samples. Transistors were then mesa-isolated, were cleaned in buffered HF for 2 min and then in-situ cleaned in an atomic layer deposition (ALD) reactor using alternating cycle of nitrogen plasma and trimethylaluminum pretreatment.[14] Approximately 3.9 nm HfO_2 gate dielectric was then blanket-deposited. Samples were then annealed in forming gas (5% H_2/95% N_2) at 400 °C for 15 min. 35 nm/120nm thermally evaporated Ni/Au gate metal and 20 nm/50nm/100nm Ti/Pd/Au source/drain metal were then deposited and patterned by liftoff. Because $AlAs_{0.56}Sb_{0.44}$ is readily oxidized by air exposure and is etched during the mesa isolation, 0.75 μm mesa etch undercut is observed at the edge of the bottom barrier in the final devices. The final gate width determined by scanning electron microscope is ~23.5 μm (25 μm as drawn) for sample B.

TABLE I. Comparison of Hall mobility between InGaAs/InAlAs and InGaAs/AlAsSb double heterostructures (detailed structures depicted in Ref. 8).

Well thickness (nm)	Barrier layer	N_s, 300 K (10^{12} cm^{-2})	μ, 300 K ($cm^2/V \cdot s$)
10	InAlAs	2.28	9530
10	AlAsSb	2.40	9541
5	InAlAs	2.28	6785
5	AlAsSb	2.13	4777

Figure 2 shows the transfer characteristic of sample A and sample B, at 58 nm and 56 nm gate lengths (L_g) respectively. At $V_{DS} = 0.5$ V, sample A shows 2.2 mS/μm peak transconductance and 242 mV/dec subthreshold swing (SS), while sample B shows 1.96 mS/μm peak transconductance and 134 mV/dec SS. The drain-source leakage current (I_{DS} at, *e.g.*, $V_{GS} = -0.2$ to -0.4 V) is significantly reduced in sample B. The slightly reduced transconductance of sample B may be due to reduced mobility arising from stronger interface roughness scattering of InGaAs/AlAsSb heterojunction.[8] As a function of gate lengths, threshold voltages are 0.1–0.15 V more positive for sample B, possibly a result of the increased eigenstate energy in the InGaAs channel, also due to stronger quantum confinement.

Figures 3(a) and 3(b) compare the subthreshold characteristics of samples A and B as a function of gate lengths. With sample A (InAlAs barrier), the off-state drain leakage current (I_{DS} at, *e.g.*, $V_{GS} = -0.2$ to -0.4 V) increases rapidly as L_g is reduced from 558 nm to 131 nm and 58 nm, particularly for $V_{DS} = 0.5$ V. At short gate lengths, 130 nm and 56 nm L_g, sample B (AlAsSb barrier) exhibits much smaller off-state leakage than sample A. For $L_g < 200$ nm, sample B shows considerably smaller subthreshold swing as shown in Figure 3(c). Sample B shows a residual off-state leakage of

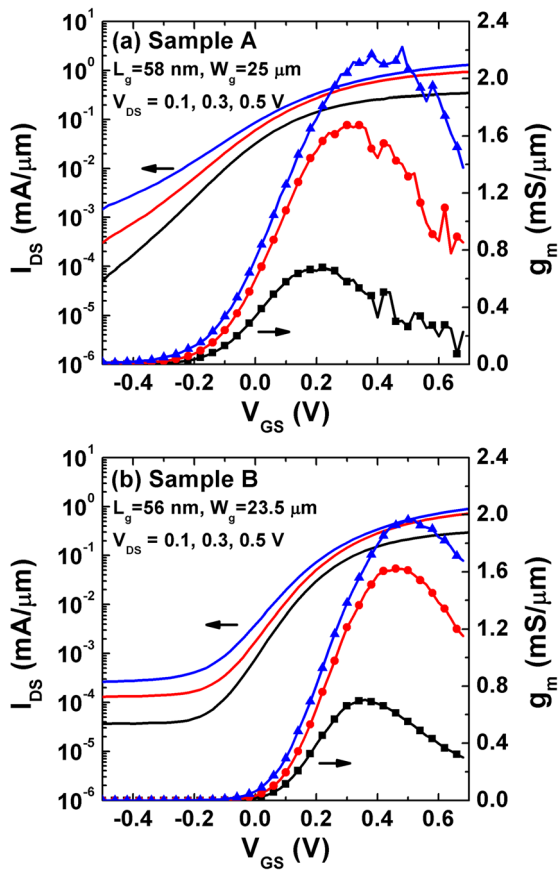

FIG. 2. Transfer characteristics of (a) sample A with $L_g = 58$ nm and (b) sample B with $L_g = 56$ nm at V_{DS} of 0.1, 0.3, and 0.5 V.

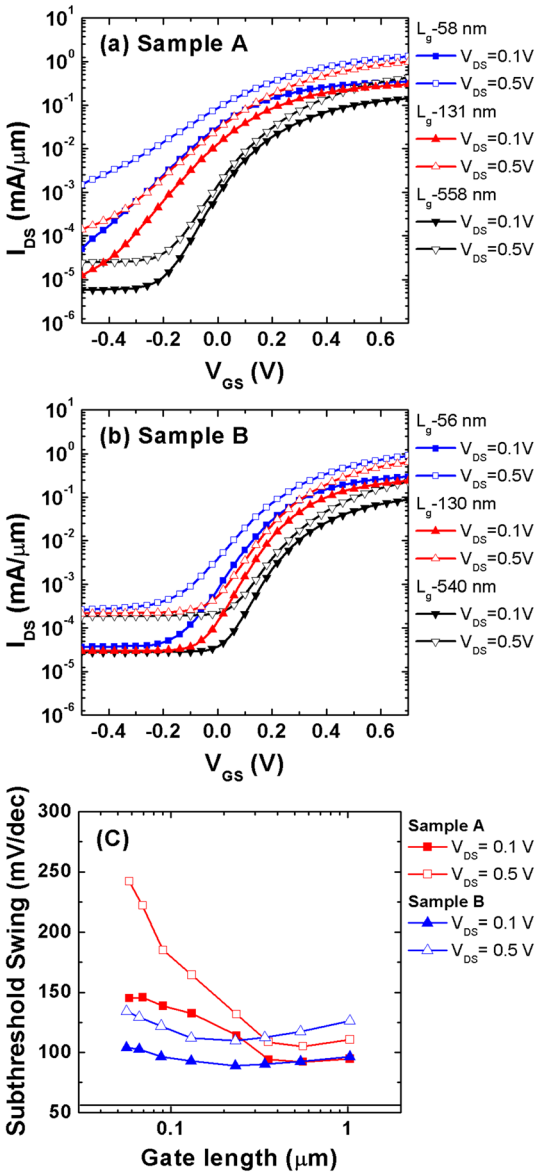

FIG. 3. Subthreshold characteristics (a) of sample A with $L_g = 58$, 131, and 558 nm and (b) of sample B with $L_g = 56$, 130, and 540 nm. (c) Subthreshold swing vs. L_g for sample A and sample B at $V_{DS} = 0.1$ V and $V_{DS} = 0.5$ V.

3–4 $\times 10^{-5}$ mA/μm at $V_{DS} = 0.1$ V and 2–3 $\times 10^{-4}$ mA/μm at $V_{DS} = 0.5$ V. This background leakage has an approximately linear (Ohmic) variation with V_{DS}, and is only weakly dependent upon the gate length; on other experimental samples, we have observed similar background leakage when the isolation mesa etch depth is insufficient.

Off-state drain leakage current arising from simple electrostatics (excessive channel or gate dielectric thickness) or from source-drain or band-band tunneling would not show the strong observed dependence upon the energy offset of the lower barrier. Leakage by thermal emission from the N+ source over the channel-barrier interface should however show a strong dependence upon the barrier energy, consistent with Figures 2 and 3. Figure 4 shows a computed energy band diagram drawn vertically through the MOSFET regrown N+ $In_{0.53}Ga_{0.47}As$ source (Si-doped: 4×10^{19} cm^{-3}), through the un-doped $In_{0.53}Ga_{0.47}As$ channel, and into $In_{0.52}Al_{0.48}As$ or $AlAs_{0.56}Sb_{0.44}$ bottom barrier layer. The band diagram is calculated by self-consistent 1-D Schrödinger and Poisson

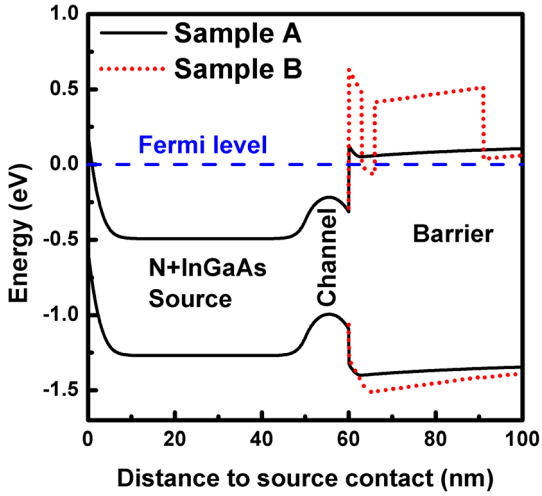

FIG. 4. Energy band diagram of sample A ($In_{0.52}Al_{0.48}As$ barrier) and sample B ($AlAs_{0.56}Sb_{0.44}$ barrier) with raised N+ InGaAs source/drain (Si-doped: 4×10^{19} cm^{-3}), drawn on a vertical line passing through the N+ source, the InGaAs channel, and the InAlAs or AlAsSb bottom barrier. Given the high source doping, the InAlAs barrier energy lies only ~0.1–0.2 eV above the Fermi energy, while AlAsSb barrier provides ~0.6–0.7 eV carrier confinement.

equation. The conduction band energy and valence band energy of $AlAs_{0.56}Sb_{0.44}$ barrier are linearly interpolated from unstrained AlAs and AlSb layers without considering bowing parameter. As shown in Figure 4, the electron Fermi level lies ~0.4 eV above the conduction band of the N+ source and ~0.2 eV above that of the un-doped InGaAs channel. The $In_{0.52}Al_{0.48}As$ layer provides only ~0.1–0.2 eV barrier above the electron Fermi level, insufficient to strongly suppress thermal emission from the N+ source. Using an oxide barrier,[5] or a wide band-gap semiconductor barrier will potentially reduce this barrier leakage current. Replacement of the $In_{0.52}Al_{0.48}As$ barrier with $AlAs_{0.56}Sb_{0.44}$ increases the barrier energy by ~0.5 eV, and should suppress this thermal emission by ca. $10^8 : 1$.

In summary, we have demonstrated planar $In_{0.53}Ga_{0.47}As$ MOSFETs with a wide band-gap $AlAs_{0.56}Sb_{0.44}$ barrier layer. A device with 56 nm gate length shows the peak transconductance about 1.96 mS/μm and SS = 134 mV/dec, both at $V_{DS} = 0.5$ V. Replacing the $In_{0.52}Al_{0.48}As$ barrier with $AlAs_{0.56}Sb_{0.44}$ greatly reduces the drain-source leakage current, which we attribute to suppression of the carrier injection from the N+ InGaAs source into the back barrier.

The authors gratefully acknowledge support for this work by the Semiconductor Research Corporation through the Nonclassical CMOS Research Center (Task ID 1437.009). A portion of this work was performed in UCSB nanofabrication facility, which is part of the NSF-funded NNIN network.

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