High Transconductance Surface Channel $In_{0.53}Ga_{0.47}As$ MOSFETs Using MBE Source-Drain Regrowth and Surface Digital Etching

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Outline

- **Motivation: Why III-V MOSFETs?**
- **Key Design Considerations**

  - Device Structure : Gate-last with S/D regrowth

  - Damage during regrowth : surface digital etching
- **Process Flow**
- **Measurement Results**

  - I-V Characteristics

  - TLM measurement
- **Conclusion**

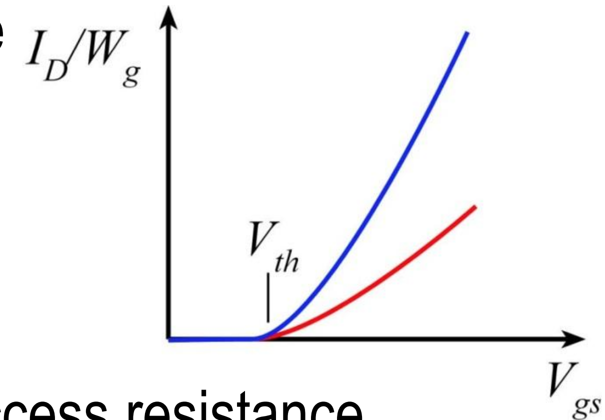
Why III-V MOSFETs in VLSI ?

more transconductance per gate width

more current (at a fixed V_{dd})$\longrightarrow$ IC speed

or reduced V_{dd} (at a constant I_{on})$\longrightarrow$ reduced power

or reduced FET widths$\longrightarrow$ reduced IC size



increased transconductance from:

low mass$\longrightarrow$ high injection velocities

lower density of states$\longrightarrow$ less scattering

higher mobility in N+ regions $\longrightarrow$ lower access resistance

Other advantages

heterojunctions$\longrightarrow$ strong carrier confinement

wide range of available materials

epitaxial growth$\longrightarrow$ atomic layer control

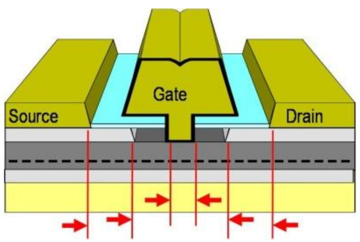
Key Design Considerations

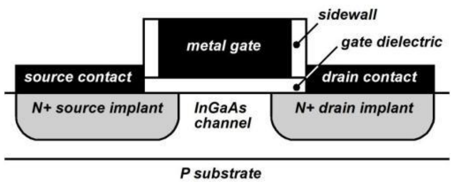
Device structure:

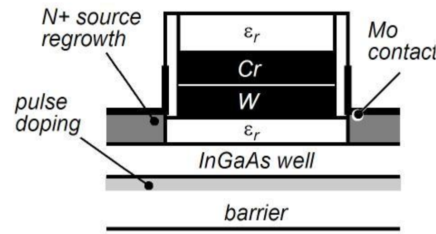
Scalability (sub 20 nm-L_g,<30 nm contact pitch) : self-aligned S/D, very low ρ_c [2)]

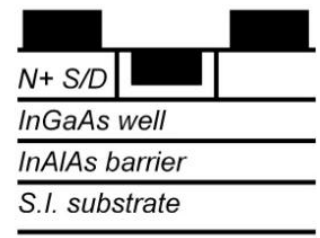
Carrier supply*:* heavily doped N+ source region[3)]

Shallow junction*:* regrown S/D[3)] or Trench-gate









Channel Design:

Thinner wavefunction depth*:* Thin channel, less pulse doping.

More injection velocity*:* high In-content channel[4)]

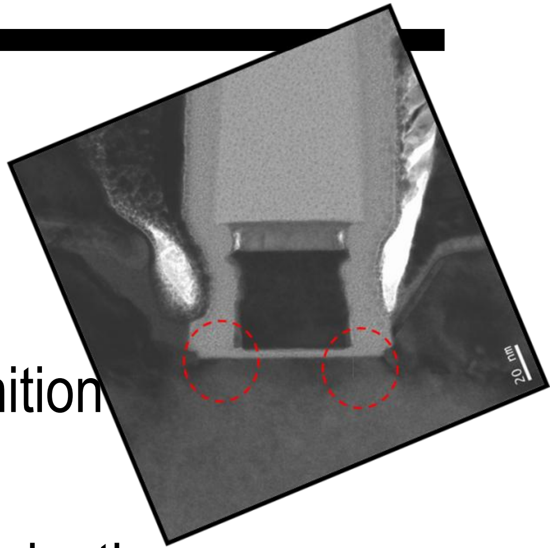
Gate Dielectric:

Thinner EOT *:* scaled high-k dielectric

Low D_{it} *:* surface passivation[5)], minimized process damage[6)]

1) M. Wistey et al. EMC 2009; 2) A. Baraskar et al. IPRM 2010 ; 3) U. Singisetti et at. EDL 2009 ;
4) S. Lee et al. EDL 2012 (accepted); 5) A. Carter et at. APEX 2011; 6) G. Burek, et al, JVST 2011.

Device Structure : Gate-Last process



A. Carter et at., DRC 2011

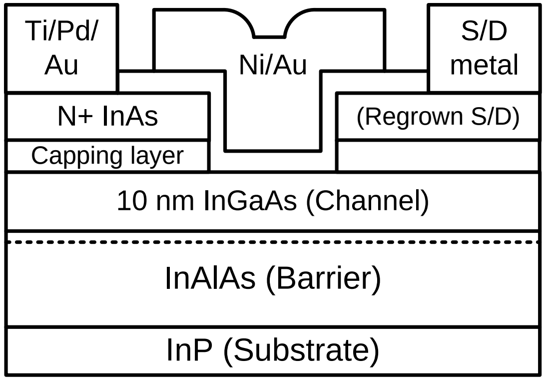
Gate-First

Fully self-aligned transistor at nm dimensions

Process damage during gate metal deposition and definition

Large ungated region: High pulse doing
➔ Large leakage current and increase in wavefunction depth

Gate-Last (substitutional-gate)



Low-damage process: Thermal gate metal,
No plasma process after gate dielectric deposition

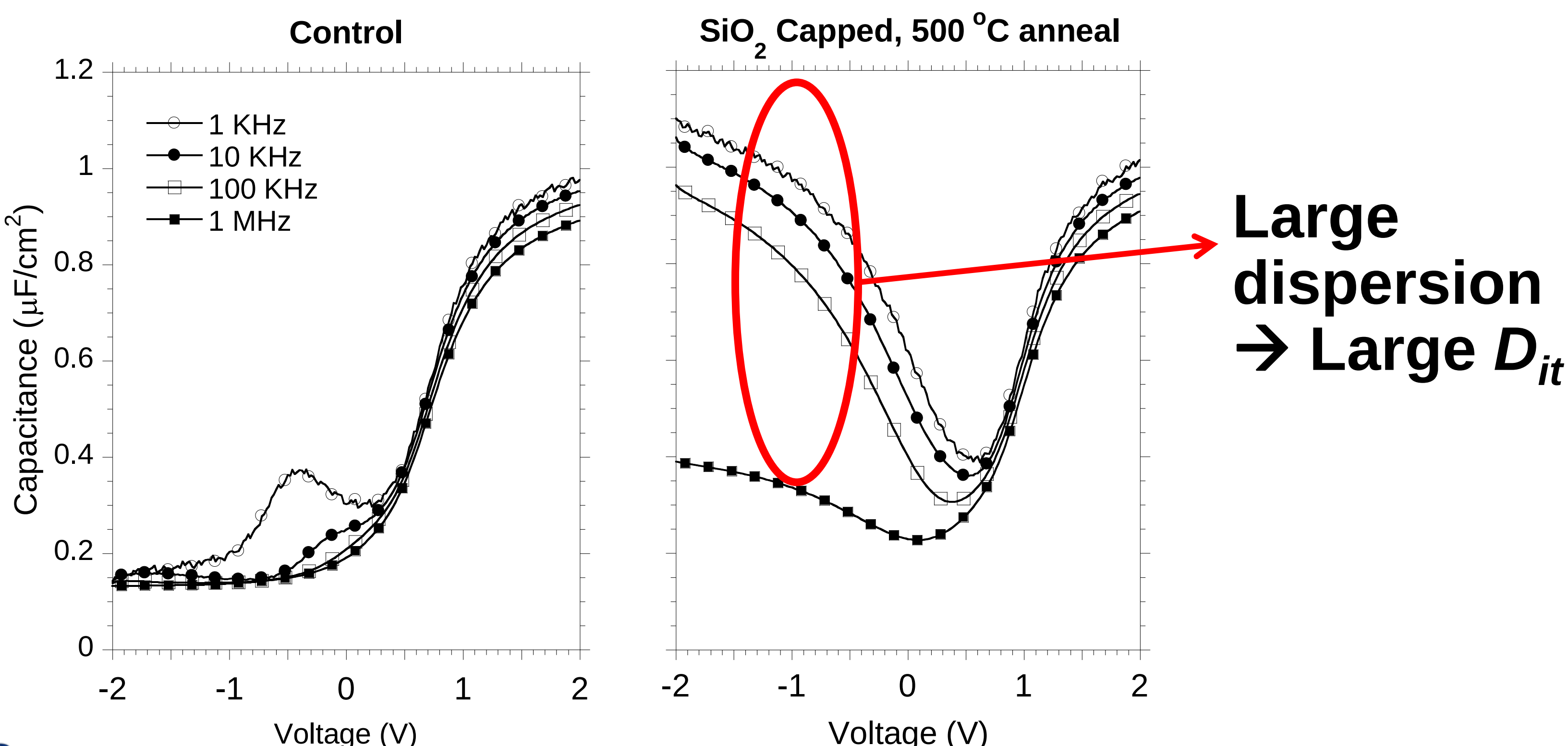
Rapid turn-around ➔ rapid learning.

Evidence of Surface Damage During Regrowth

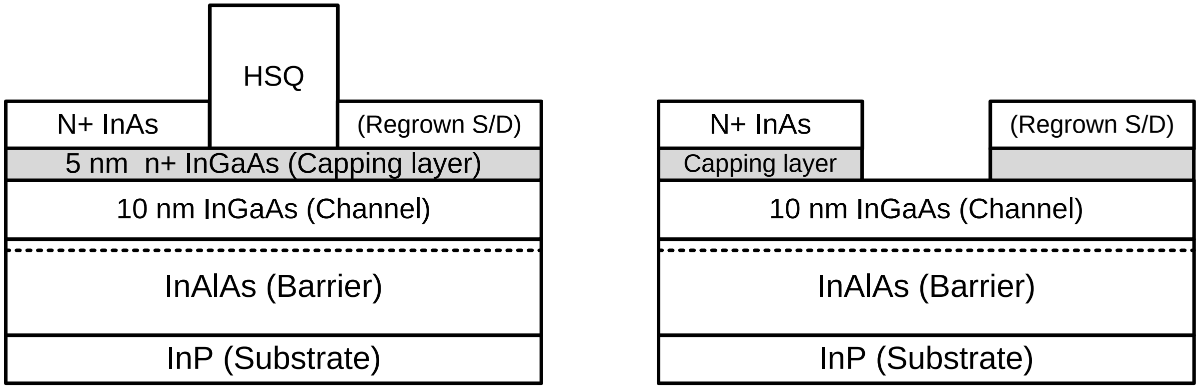
Long-channel FETs: consistently show >100 mV/dec. subthreshold swing
Indicates high D_{it} despite good MOSCAP data. Suggests process damage.

Experiment: SiO_2 capping + high temp anneal + strip → MOSCAP Process

Finding: large degradation in MOSCAP dispersion.
Confirms process damage hypothesis.



Post-Regrowth Surface Digital Etching for Damage Removal



- **Surface removed by digital etch process**

  2' in BOE (dummy gate removal) ,

  # cycles: 15' UV ozone (surface oxidation)

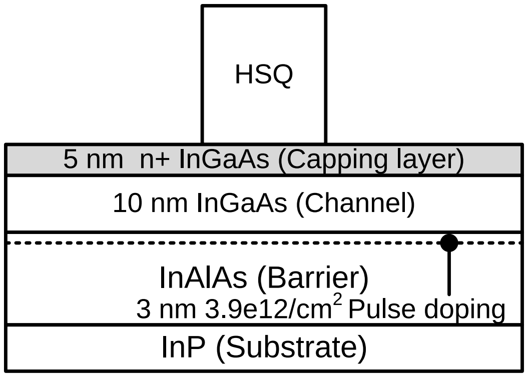
  1' dilute HCl (native oxide removal)

  ➔ 13 - 15 Å/cycle, ~0.16 nm RMS roughness

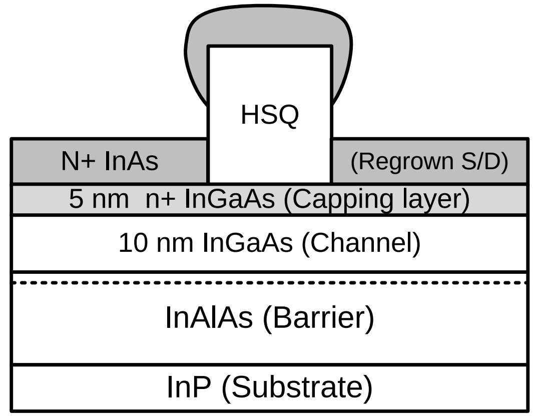
- **Etch significantly improves subthreshold swing and g_m**

- **Using this technique, we can easily thin the channel thickness.**

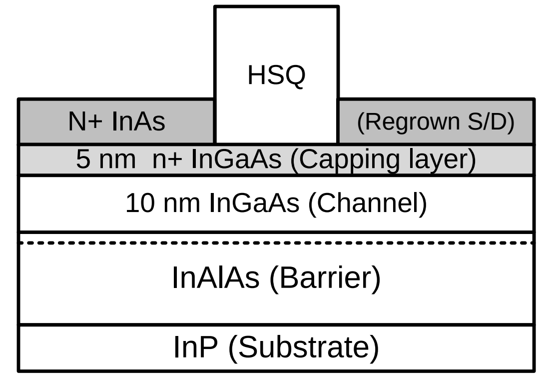
Process Flow



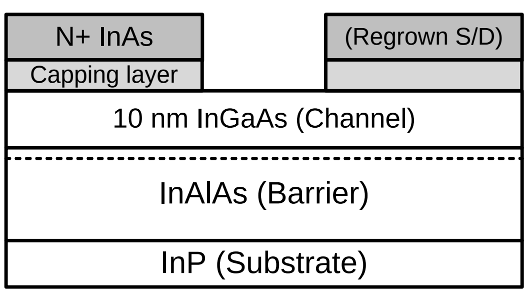
- Epitaxial layer growth
- Dummy gate definition



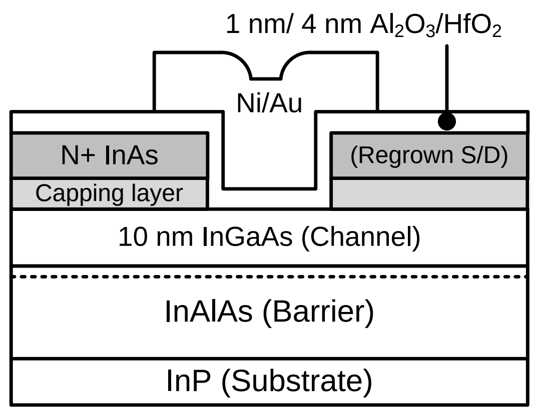
- InAs Source/Drain regrowth



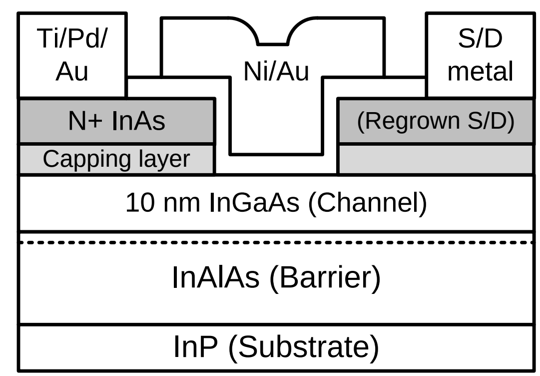
- Mesa isolation
- InAs debris wet-etching



- Dummy gate removal
- Capping layer digital etching

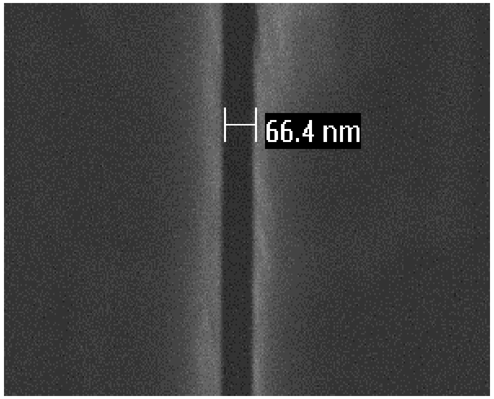


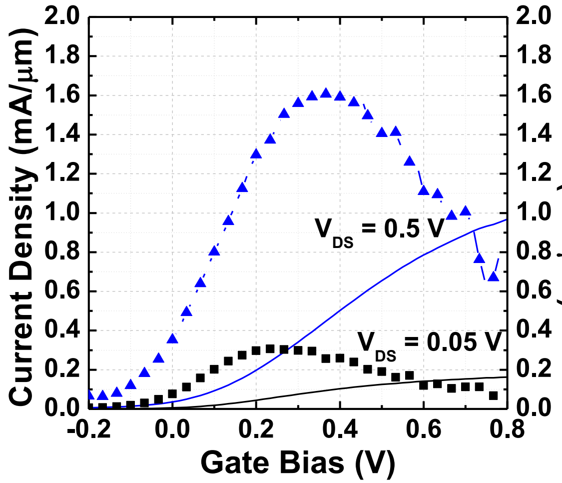
- High-k deposition
- Annealing
- Gate metal deposition

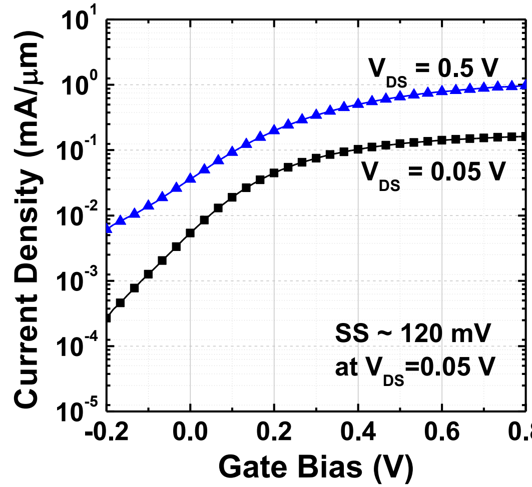


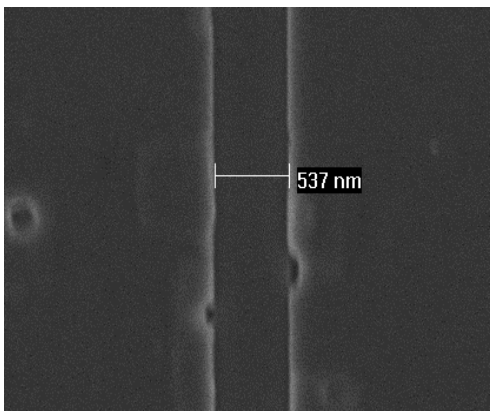
- S/D metal deposition

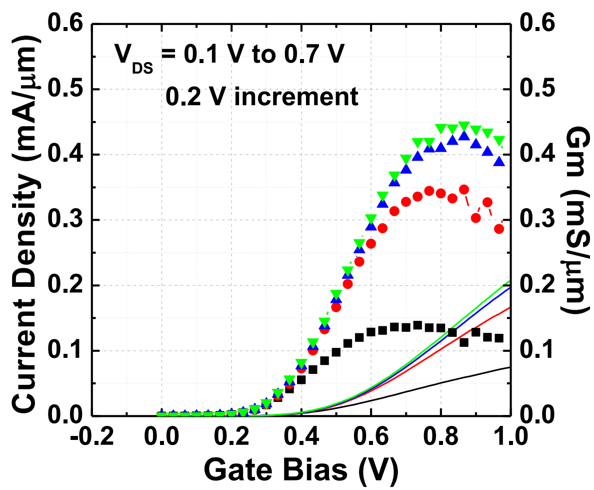
I-V Characteristics for short and long channel devices

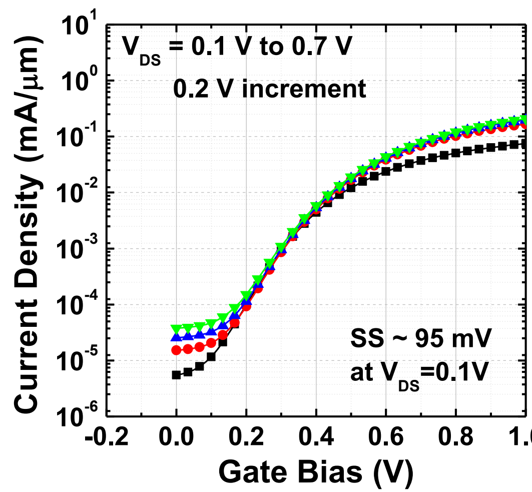








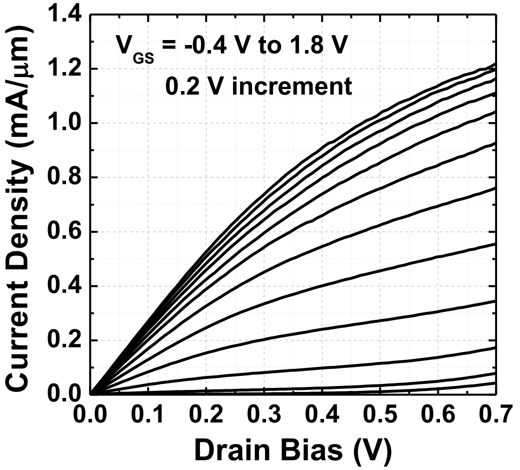


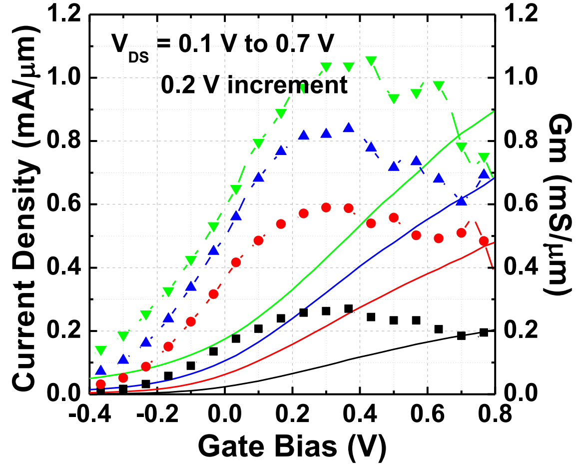


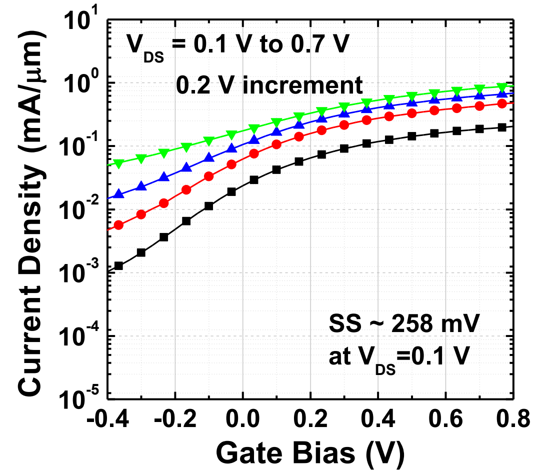
- 1.6 mS/μm at V_{ds}=0.5 V for a 65 nm-L_g device.
- 95 mV/dec SS for a 530 nm-L_g device.

Comparison with a control sample (short channel)

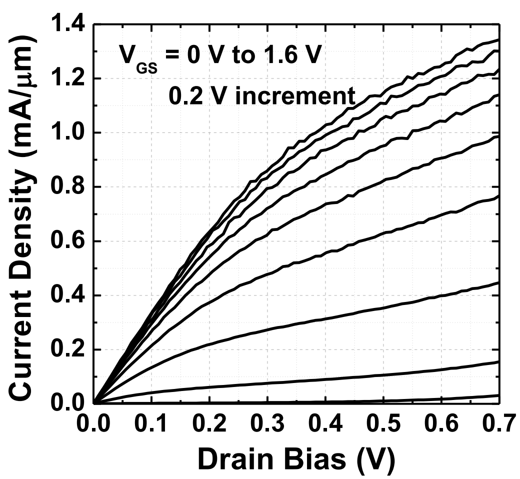
Control : without capping layer and surface digital etching, 75 nm-Lg

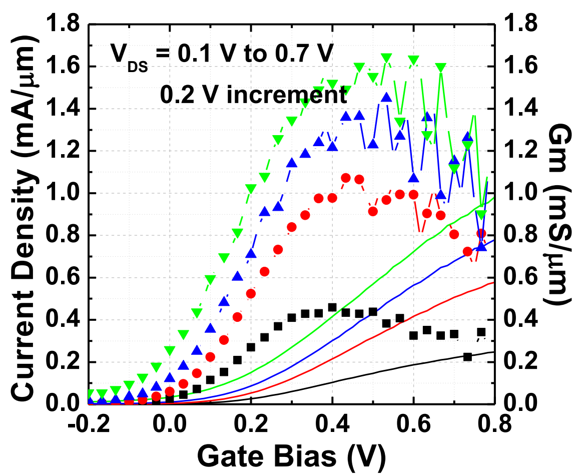


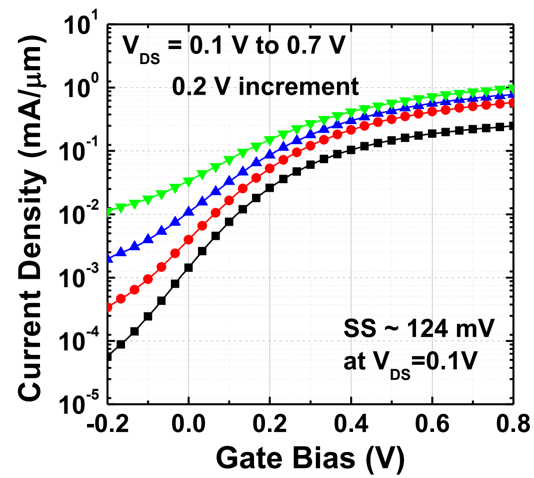




Experimental : with surface digital etching , 75 nm-Lg



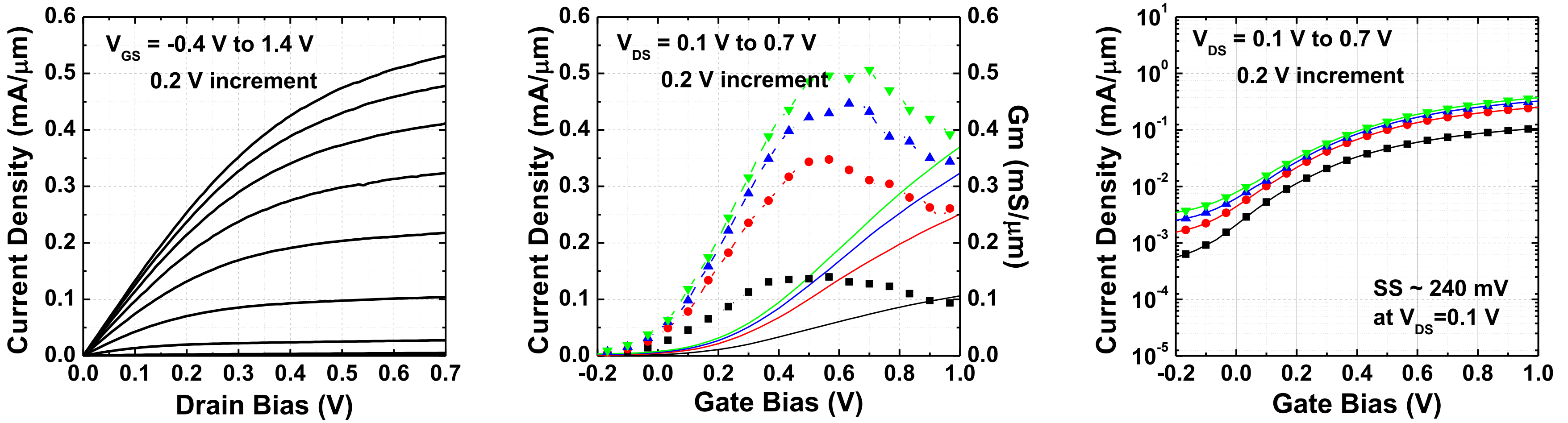




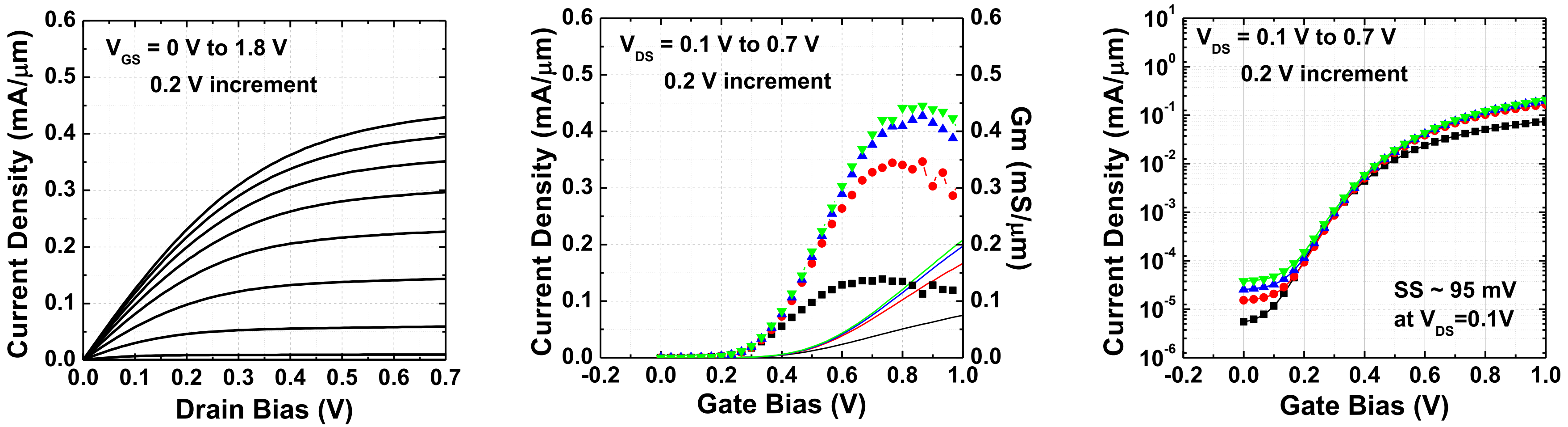
- ~75 % increase in peak transconductance at V_{ds} = 0.5 V
- significantly better short channel characteristic with surface digital etching

Comparison with a control sample (long channel)

Control : without surface digital etching, 500 nm-Lg

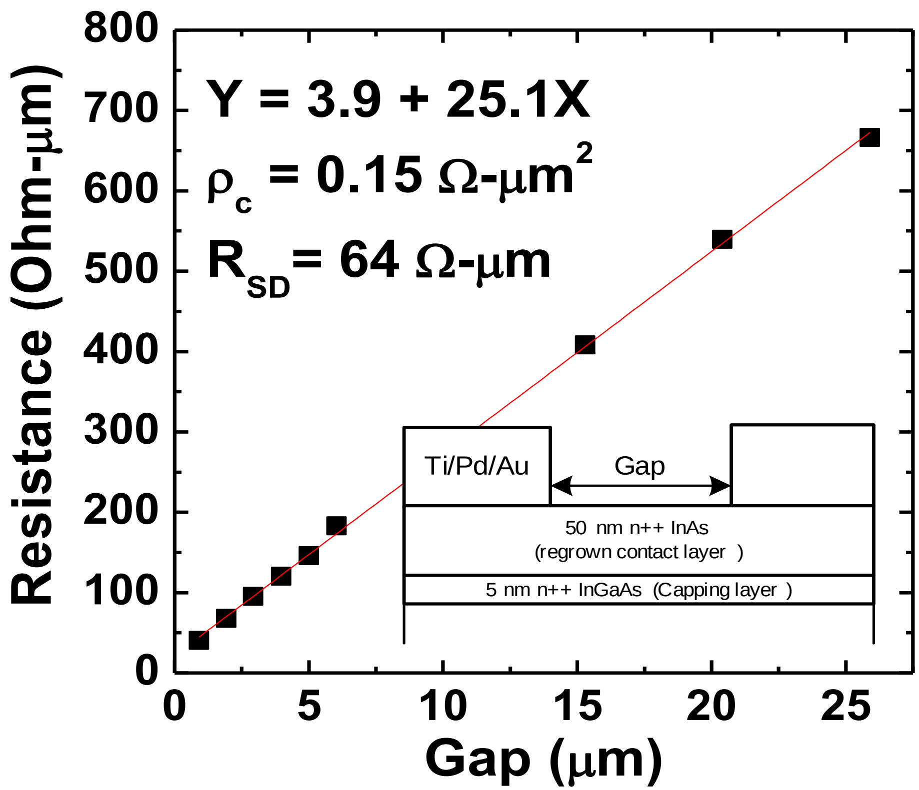


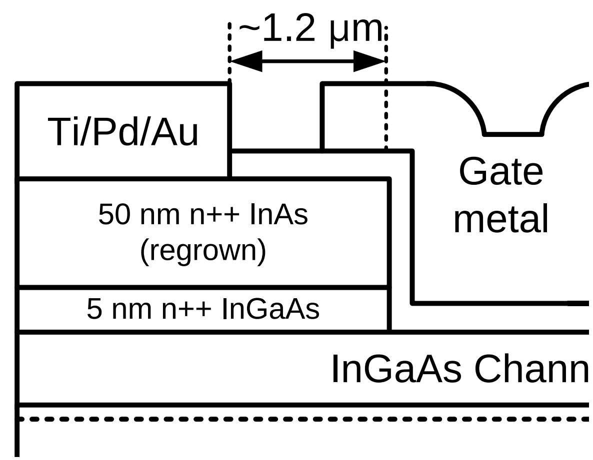
Experimental : with surface digital etching, 535 nm-Lg



- Similar on-state characteristics (~0.4 V Vt shift)
- Better short channel effect

TLM Measurement for S/D metal contact





- **0.15 ohm-μm² Contact resistivity and 25 ohm/sq. sheet resistance.**
- **64 ohm-μm S/D access resistance (~5 % transconductance degradation)**

Conclusion

- Using digital etching, damaged surface can be effectively removed in a nanometer precision without etch-stop.
- The removal of the damaged surface significantly improves both on- and off-state performance.
- g_m = 1.6 mS/μm at V_{ds}=0.5 V for a 65 nm-L_g device
  95 mV/dec for a 530 nm-L_g device
- InAs regrown S/D provides very low contact resistivity of 0.15 ohm-μm^2 .

Thanks for your attention!
Questions?

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