A 220GHz Solid-State Power Amplifier MMIC with 26.8dB S_{21} Gain, and 55.5mW P_{out} at 17.0dB Compressed Gain

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***Abstract* — A 220GHz solid-state power amplifier MMIC is presented, simultaneously demonstrating 55.5mW output power P_{out} at 17.0dB compressed gain (1.12mW P_{in}). The maximum saturated P_{out} is 60mW at 14.0dB compressed gain (2.36mW P_{in}). This 3-stage, 4-cell amplifier has 26.8dB S_{21} gain at 220GHz, with 3-dB small-signal bandwidth from at least 210GHz to 235GHz. P_{DC} is 3.38W. Amplifier cells were fabricated from a 250nm InP HBT technology, jointly with a substrate-shielded, thin-film microstrip wiring environment using BCB. The 55-60mW P_{out} is achieved by combining four amplifier cascode cells. The use of three gain stages significantly relaxes the RF source power requirements, where only 1.12mW P_{in} is needed to achieve 55.5mW P_{out}, and 2.36mW P_{in} to achieve 60mW fully saturated P_{out}. This represents at least 5-6dB gain improvement to state-of-the-art for 220GHz SSPAs when operated at similar output powers. Over 20GHz bandwidth, at least 50mW P_{out} is observed from 205-225GHz.**

I. Introduction

Future synthetic aperture radars and high resolution imaging systems will benefit from the continued development of solid-state power amplifiers (SSPA), where recently there has been active interest to increase the saturated output power at 220GHz. These high-power signals may be used to drive multiplier chains for THz applications, or to drive higher power vacuum tube amplifiers around the 220GHz low-loss free space propagation window. For many wireless applications, significant output power will be necessary at 220GHz and above to overcome attenuation due to weather events.

The highest output power reported at 220GHz operation is from an InP HBT technology having 90mW P_{out} (8.2dB compressed gain) from a single SSPA MMIC, measured by RF wafer probing [1]. The highest output power reported for an InP HEMT technology is 75mW (10-11dB compressed gain) in a waveguide-block package [2]. For these amplifiers, while the output power is appreciable, the amount of gain at these power levels is small, where a pre-driver amplifier would be required if these parts were used in system applications. Continued advancements in InP HBT gain and bandwidth at the 250nm node make is possible to realize high-mm- and sub-mm-wave amplifiers with higher amounts of gain without compromising or risking amplifier stability.

In this paper, a 3-stage, 4-cell InP HBT SSPA MMIC is reported using cascode InP HBT gain cells, and 1:4 and 4:1 power dividers and combiners in a low-loss, substrate shielded thin-film microstrip wiring environment. At 17.0dB compressed gain, P_{out} = 55.5mW (1.12mW P_{in}), and at 14.0dB compressed gain, P_{out} = 60mW (2.36mW P_{in}). The SSPA exhibits 26.8dB S_{21} gain at 220GHz and 3-dB small signal bandwidth from at least 210GHz to 235GHz. P_{DC} is 3.38W. The use of three gain stages significantly relaxes the RF source power requirements for high saturated output power, where only 1.12mW P_{in} is needed to achieve 55.5mW P_{out}, and 2.36mW P_{in} to achieve 60mW fully saturated P_{out}. This represents at least a 5-6dB gain improvement to state-of-the-art for 220GHz SSPAs when operated at similar output powers. Over 20GHz bandwidth, at least 50mW P_{out} is observed from 205-225GHz.

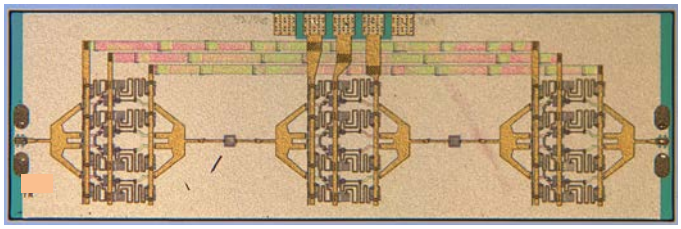

Fig. 1 IC Micrograph of the 220GHz, 3-stage, 4-cell InP HBT solid-state power amplifier MMIC. Dimension: 2.24mm × 0.71-mm.

II. MMIC Power Amplifier Design

A single power amplifier (PA) cell was designed having a cascode topology using a 24um emitter length (L_e) CE HBT and 24um L_e CB HBT. A detailed description of the device topology, DC performance, and RF performance (gain and stability at 220GHz) of these 250nm InP HBT cells from Teledyne Scientific has been reported in [3]. Figure-2 shows a detailed circuit schematic of the PA cell containing the RF tuning networks and DC bias approach. The DC bias is provided to the HBTs using quarter-wave transmission lines, thus appearing as an open-circuit at the HBT near and at the design frequency. The input of the amplifier cell is matched to 50-Ohm Z_o for highest small- and large-signal RF gain. The output of the PA cell is matched such that the CB HBT collector voltage and current would swing along a class-A load-line which is coincident with the high performance operating area of the transistor [3]. The operating load-line end-points are defined at the HBT saturation voltage $0.9V_{CE}$ at

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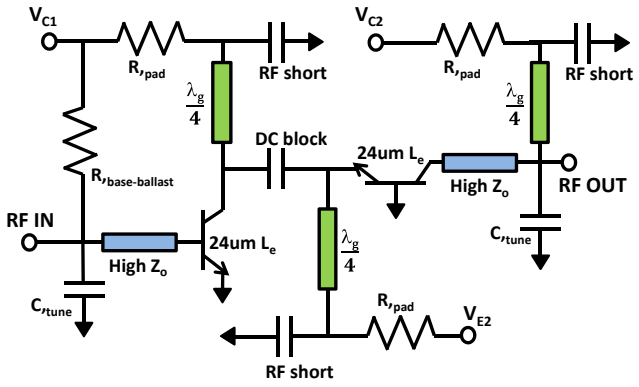

Fig. 2 Schematic of a 220GHz power amplifier cascode cell.

highest current density $J_{max} = J_{Kirk} = 9mA/um^2$, and at $3.8V_{CE}$ and $1.5mA/um^2$ where the transistor still has appreciable MAG/MSG gain at 220GHz. For the CB HBT, its DC bias was selected at $2.35V_{CE}$ and $5.5mA/um^2$ J_e (33mA I_C).

Amplifier circuits were simulated in Agilent Advanced Design System (ADS) using the Agilent-HBT model for the Teledyne Scientific 250nm HBT technology. All interconnects, transmission lines, MIM capacitors, probe pads, and power splitters/combiner structures were designed using ADS Momentum, a 2.5-D electromagnetic simulator.

Thin film microstrip transmission lines were formed using the lowest metal interconnect layer as DC and RF ground potential, and the upper three metal interconnect layers for signal transmission. Substrate shielded, non-inverted thin-film microstrip wiring was selected to minimize interconnect inductance between the ground plane and the emitter terminal for the common-emitter (CE) HBT, and between the ground plane and the base terminal for the common-base (CB) HBT. This is especially important for the common-base HBT, as additional inductance at the base causes significant reduction to amplifier stability margin. Use of a substrate-shielded ground plane eliminates (or at least keeps very small) signal coupling between PA cells through the 12.8-ε_r InP substrate. For amplifiers with high gain, unintentional signal feedback through the substrate to preceding stages can potentially cause the amplifier to oscillate. Minimal ground return inductance provided by the large, continuous ground plane helps to permit the amplifier to be broadband. It also allows accurately predicted passive networks at high-mm-, sub-mm-wave frequencies by the EM simulator because the ground return currents are more accurately determined.

Figure-3 shows a circuit block-diagram of the SSPA MMIC. For each amplifier stage, the RF signal is split to the cascode cells, amplified, and then recombined before being transmitted to the next stage. To satisfy the objectives of this design (>25dB S_{21} gain and >50mW P_{out}), three stages of gain and a 4-way splitter/combiner network were selected and designed. In figure-1, the divider/combiner structures are clearly identified. Through iterative design by EM simulation, fabricated test structures have shown low loss (0.6-0.7dB),

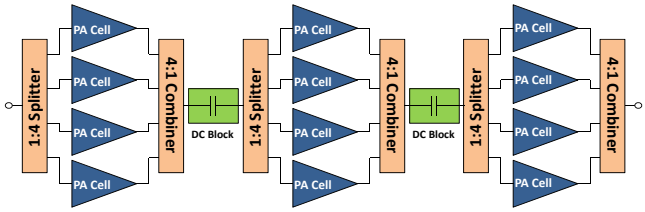

Fig. 3 Circuit block diagram of the 3-stage, 4-cell SSPA MMIC.

and excellent amplitude and phase matching between the four arms. Further details associated with similar splitter/combiner structures have been reported in [4]. The amplifier gain stages are identical – the was done to ensure that the output stage is provided with sufficient RF input power so as to generate the greatest amount of output power P_{out} from the overall MMIC. While this approach will generate highest SSPA P_{out}, excess DC power is consumed, thus lowering the MMIC power added efficiency (PAE).

Lastly, for this multi-stage design, simple shunt R-C bypass networks (series 250fF + 5Ohms) are used along the DC bus lines to provide isolation between stages and dampen/suppress any standing waves that may be unintentionally stimulated.

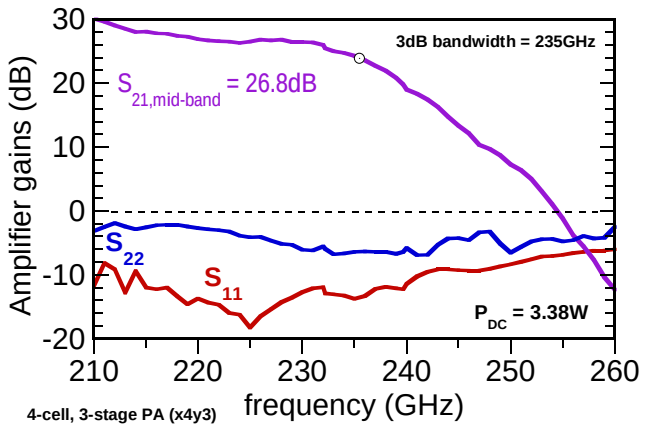

Fig. 4 S-parameters of the 3-stage, 4-cell SSPA MMIC. The SSPA shows 26.8dB S_{21} gain at 220GHz and a bandwidth greater than 210-235GHz.

III. Experimental Results

On-wafer SSPA MMIC S-parameter measurements were performed by 210-325GHz OML T/R frequency extender modules, controlled by an Agilent 8510C VNA. GGB WR03 waveguide coupled probes were used for wafer probing. For all measurement results discussed here, they were performed on a 4" diameter, full-thickness (25-mil) InP wafer without backside metal. LRRM probe-tip calibration was performed using WinCal XE calibration software. The amplifier P_{DC} is

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3.38W. At a DC bias of V_{C1} = 2.75V, I_{C1} = 462mA, V_{C2} = 2.35V, I_{C2} = 443mA, V_{E2} = -2.2V, and I_{E2} = 462mA, the S_{21} gain of the 3-stage, 4-cell SSPA MMIC at 220GHz is 26.8dB. Figure 4 shows the measured S-parameters for the amplifier. The 3-dB bandwidth extends from at least 210GHz to 235GHz. Note from figure-4 there is no evidence that parasitic modes are being excited in the electrically thick InP substrate – this observation verifies that amplifier stages are well isolated from the InP through the use of the substrate-shielded, non-inverted microstrip wiring environment.

For large-signal measurements, a Virginia Diodes Inc. amplifier multiplier chain (AMC, 16× multiplier) is used for power sweep testing of the SSPA MMIC from 205-235GHz. Output power was measured by an Erickson PM4 sub-mm-wave power sensor. Power data was corrected, taking into account the insertion loss of the RF wafer probes, short waveguide lengths, and a waveguide transition to the power sensor.

Using identical DC bias conditions from RF testing, the 3-stage, 4-cell SSPA MMIC demonstrates 55.5mW output RF power P_{out} with 17.0dB compressed gain at 220GHz (1.12mW P_{in}). This corresponds to 1.61% power added efficiency (PAE). Figure 5 summarizes the power measurements from 205-235GHz. The data strongly suggests the output load-line has tuned downward from 220GHz (design target) to ~210GHz – a shift of less than 5%. For 2.0mW P_{in} at 220GHz, the amplifier P_{out} is 59mW (1.68% PAE) and the compressed gain is 14.7dB. From 205-225GHz, the SSPA MMIC P_{out} is ≥ 50mW. At all frequencies measured across the bandwidth of the VDI source, the amplifier demonstrated no oscillations or unstable behavior. Like with the S-parameter measurements, this observation verifies that stages are well isolated through the use of the substrate-shielded, non-inverted microstrip wiring environment.

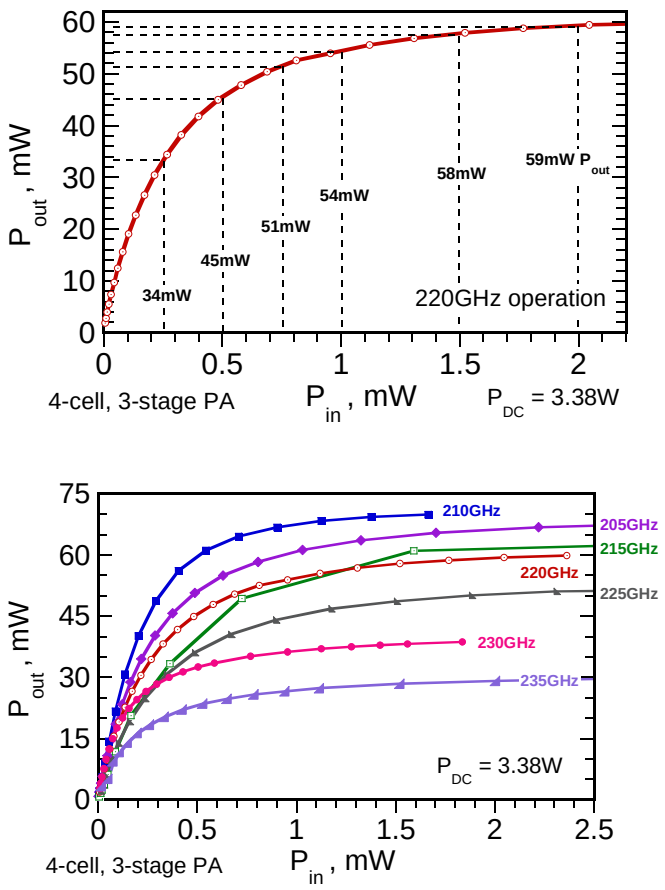

Fig. 5 A 220GHz power sweep (top) shows that the SSPA provides 60mW maximum saturated output power P_{out}. Power sweeps at frequencies between 205-235GHz (bottom) shows > 50mW P_{out} from 205-225GHz.

IV. Conclusions

A 220GHz solid-state power amplifier MMIC has been presented, demonstrating 26.8dB S_{21} gain, and 55.5mW P_{out} at 17.0dB compressed gain. The maximum saturated P_{out} at 220GHz is 60mW at 2.36mW P_{in}. From 205-225, the SSPA MMIC shows P_{out} > 50mW. This work represents a significant improvement to state-of-the-art at these high-mm-wave frequencies for SSPA MMICs, where stable, high gain operation has been demonstrated from a single MMIC. Optimization of the stages preceding the output driver amplifier will improve PAE and the thermal management required when these amplifiers are packaged.

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IV. References

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