

A 600 GHz InP HBT Amplifier Using Cross-Coupled Feedback Stabilization and Dual-Differential Power Combining

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Abstract — We report a 600 GHz amplifier with > 30 dB peak gain, based on 12 cascaded differential common-base (CB) stages, in a 130 nm InP HBT process. Three consecutive CB stages are grouped as a unit gain block, sharing a common bias current. Each CB stage is stabilized by cross-coupled capacitive feedback. Output powers from two differential branches are combined through a 4-way combiner, resulting in a 4× increase in power compared to a single single-ended output stage. On-wafer testing in WR-1.5 band (500-750 GHz) shows that the amplifier exhibits > 20 dB of gain up to 620 GHz, with +2.8 dBm of saturated output power at 585 GHz, while consuming 455 mW.

Index Terms — Terahertz, hetero-junction bipolar transistors, amplifiers, cross-coupled feedback, power combining.

I. INTRODUCTION

Sub-millimeter-wave and lower terahertz (THz) frequency bands covering 300 GHz to 1 THz have emerging applications in security/medical imaging systems, radar, chemical/bio sensors, and high-rate data communications. Various THz transceiver building blocks up to 670 GHz have been reported in indium phosphide-based (InP) high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) [1-4]. In this paper, the design and testing of an InP-HBT based 600 GHz amplifier is presented, as an essential building block in fully-integrated THz transmitters and receivers. The amplifier design exploits differential topology for a 1:2 power splitting, final 4:1 power combining, and individual stage stabilization.

II. INP HBT TECHNOLOGY

The amplifier IC is based on a 130 nm emitter width InP HBT technology. Details of the device technology can be found in [5]. Key features of the process technology are the use of electron-beam lithography and electroplating to form the emitter contact, and the use of dielectric sidewall spacers to form a self-aligned base-emitter junction. Circuits were fabricated on 4-inch InP substrates and the HBT IC process includes thin-film resistors (50 Ohm/sq), MIM capacitors, and 3-levels of gold interconnect (M1-M3). A 7 μm thick BCB layer is used between M2 and M3 to facilitate the formation of low-loss thin-film microstrip lines.

The highly-scaled HBTs support very high current (> 30 mA/μm²) and power (> 50 mW/μm²) densities. The common-

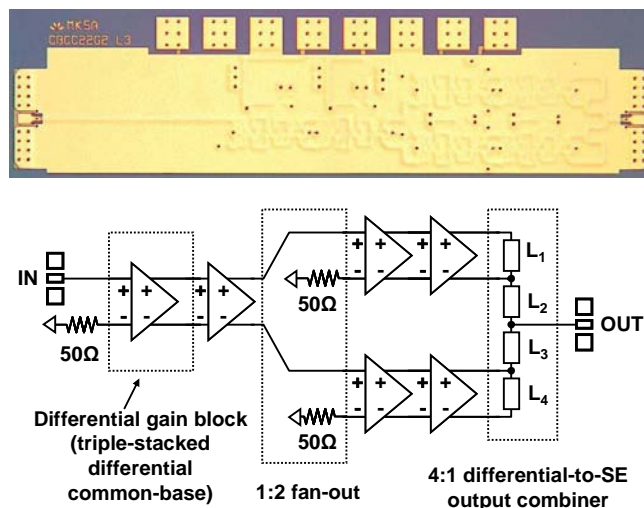


Fig. 1. 600 GHz InP-HBT amplifier: chip photograph (top) and block diagram (bottom). Chip size: 1,360×340 μm².

emitter breakdown of the transistors is $BV_{CEO} = 3.5$ V ($J_E = 10$ μA/μm²). Transistor *S*-parameter measurements are performed using on-wafer extended reference plane microstrip TRL calibration structures and RF figures-of-merit are extracted. A 0.13×2 μm² HBT exhibits a current gain cutoff frequency $f_i = 520$ GHz and a maximum frequency oscillation $f_{max} = 1.1$ THz at $I_C = 6.9$ mA and $V_{CE} = 1.6$ V. Longer emitter length devices exhibit progressively smaller values of f_{max} due to distributed resistance effects along the length of the base mesa.

III. AMPLIFIER CIRCUIT DESIGN

Chip photograph and block diagram of the 600 GHz amplifier is shown in Fig. 1. The amplifier consists of six differential gain blocks and a 4:1 output power combiner. First, overall amplifier architecture will be described, and discussions on the differential gain block will follow.

A. Amplifier Architecture

In general, differential topology makes circuit operation insensitive to common-mode impedances, e.g. bias circuits and via inductance, and thus more tolerant to modeling uncertainties and errors. The differential topology also

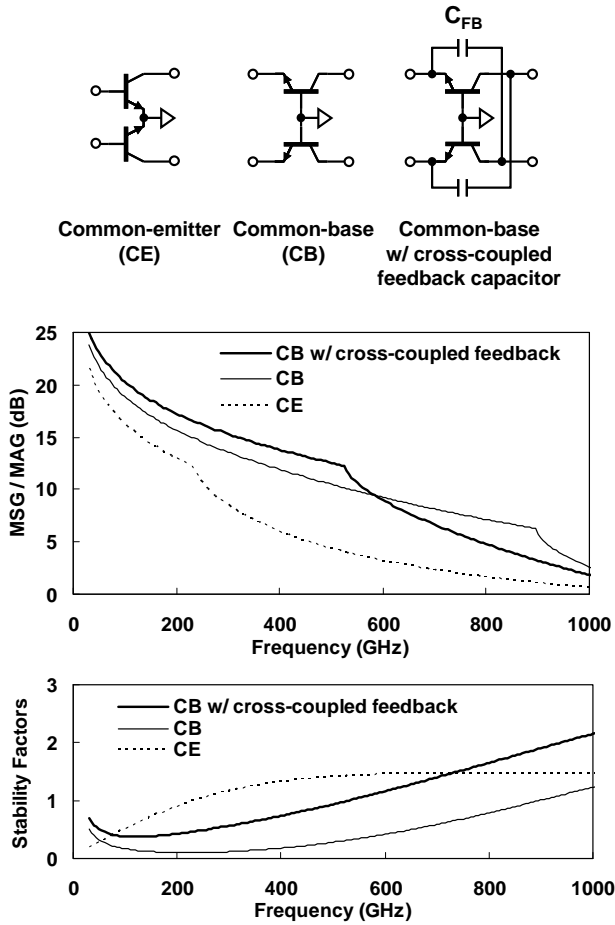


Fig. 2. Comparison of three basic gain blocks: Common-emitter (CE), common-base (CB), and common-base with cross-coupled feedback capacitor (All HBTs are $0.13 \times 3 \mu\text{m}^2$, biased at $J_E = 18 \text{ mA}/\mu\text{m}^2$, $V_{CB} = 0.8 \text{ V}$)

eliminates circuit losses and bandwidth reduction caused by lossy *single-ended* ac-grounds and their internal inductance. In addition, differential topology provides a convenient way of 1:2 signal splitting. As illustrated in the amplifier block diagram (Fig.1 bottom), each single-ended (SE) output of the second gain stage separately drives next-stage differential gain blocks, with their unused input terminated to 50Ω . With a sufficiently low common-mode gain, the differential output of the following blocks will remain reasonably balanced. This 1:2 fan-out approach, based on a SE-to-differential conversion, obviates the use of a passive splitter or balun, thus simplifying design with no bandwidth restriction of the passive counterparts. Four SE outputs of the final-stage gain blocks are combined through a 4:1 combiner, enabling a $4\times$ increase in output power compared to a single SE output stage under the same HBT periphery and bias conditions. In simulation, the 4:1 combiner shows 60-70 % efficiency with optimized L_{1-4} .

B. Unit Differential Gain Block

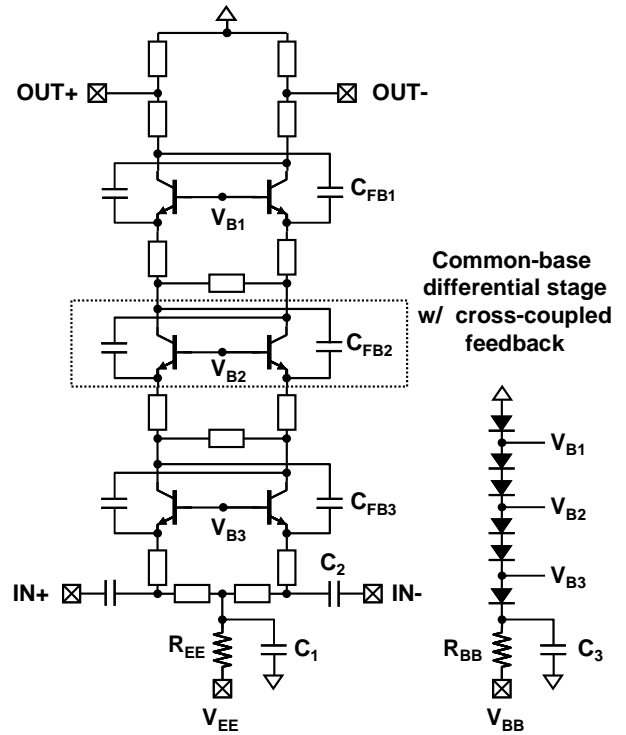


Fig. 3. Unit differential gain block: Three cascaded CB share a common bias current. All HBTs are $0.13 \times 3 \mu\text{m}^2$.

At the design frequency of 600 GHz, a single HBT gain stage in a common-base (CB) configuration exhibits a significantly higher gain than in a common-emitter (CE), i.e. $\text{MSG}/\text{MAG} = 9 \text{ dB}$ versus 3 dB , as shown in Fig. 2, mostly due to CB's smaller Miller capacitance than CE's. A CB stage is, however, substantially unstable compared to a CE stage, i.e. stability factor $K = 0.4$ and 1.5 , respectively, for a CB and CE, respectively. In THz IC designs, there are in general greater uncertainties in active / passive device modeling than in lower frequency designs. Therefore, individual gain stages must be stabilized with a sufficient margin, so that the final multi-stage amplifier can still remain stable in the presence of modeling errors, process variations, and inter-stage coupling (e.g. the stability of a CB stage is sensitive to a small base layout inductance). In this paper, to improve the stability of a CB stage, a cross-coupled capacitive feedback is proposed (Fig. 2), exploiting differential topology. In a differential CB stage, a collector node is in an approximately opposite phase to an emitter of the other HBT, therefore the cross-fed capacitors (C_{FB}) add negative feedback to the gain stage. A small amount of feedback capacitance ($C_{FB} = 0.4 \text{ fF}$) was found to be sufficient for stabilization ($K = 1.2$) with only 0.2 dB reduction in MSG / MAG . In an actual layout, C_{FB} 's are implemented by a M1-M2 overlap capacitance.

Three such cross-coupled CB stages shares a common bias current for a compact layout (Fig. 3), and constitutes a unit gain block in Fig. 1. The entire amplifier circuit is

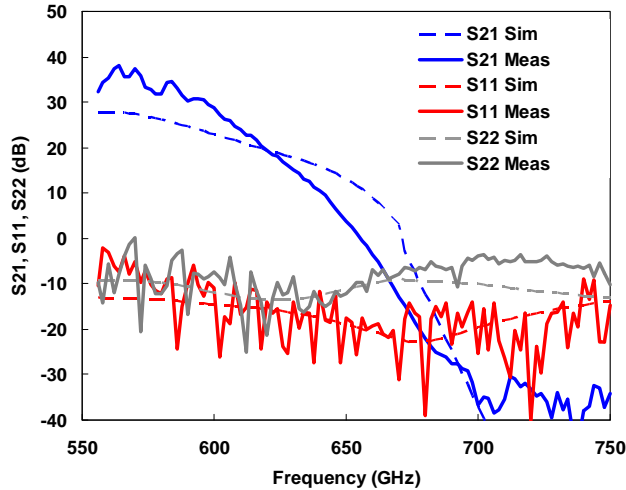


Fig. 4. S-parameters of the 600 GHz amplifier: Measured (solid lines) and simulated (dotted lines).

implemented using inverted microstrip lines to utilize a continuous ground plane on M3.

IV. MEASUREMENT RESULTS

Two-port S-parameters of the fabricated amplifier IC was characterized on-wafer using VDI WR-1.5 VNA extender heads and Dominion WR-1.5 GSG probes. Measured S-parameters show reasonable agreement with simulation (Fig. 4). Measured S21 was greater than 20 dB up to 620 GHz, with peak S21 greater than 30 dB. The amplifier gain remains positive until 655 GHz, dissipating 455 mW of total dc power. All HBTs are $0.13 \times 3 \mu\text{m}^2$, and operate at the emitter current density $J_E = 17\text{-}19 \text{ mA}/\mu\text{m}$ and $V_{CB} = 0.8 \text{ V}$.

Large-signal characteristics of the amplifier were tested using the setup in Fig. 5. Measured saturated output power at 585 GHz was +2.8 dBm (1.9 mW), after correcting for 7.3 dB of output probe loss, with 21 dB of compressed gain (Fig. 6). Measured saturated output power at 565 GHz was +2.7 dBm.

V. CONCLUSION

A 600 GHz amplifier in a 130 nm InP HBT process is presented. The design exploits differential topology for a 1:2 fan-out, 4-way output combining, and cross-feedback stabilization. On-wafer measurement exhibits > 20 dB of gain up to 620 GHz, and +2.8 dBm of saturated output power at 585 GHz. Further power testing at higher frequencies is under way.

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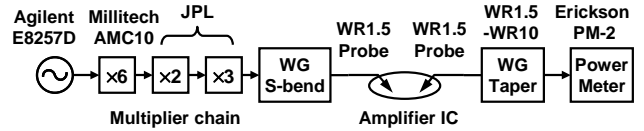


Fig. 5. Power testing setup (560-585 GHz).

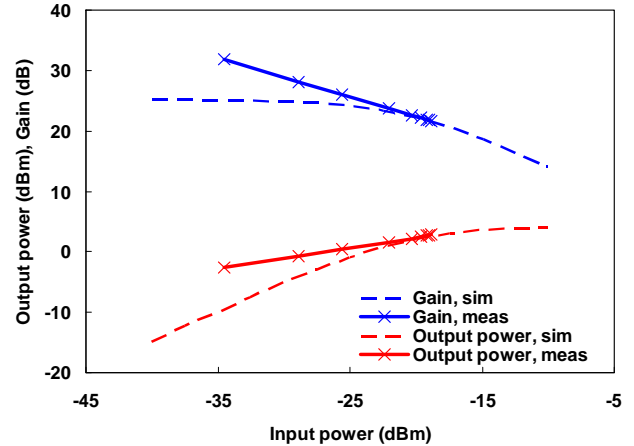


Fig. 6. Large-signal gain and output power characteristics at 585 GHz: Measured (solid lines) and simulated (dotted lines). All input and output waveguide / probe losses are de-embedded.

D. Palmer (Program Manger, DARPA). The views, opinions and/or findings contained in this article are those of the author and should not be interpreted as representing the official views or policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the Department of Defense. This work was in part performed at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with Teledyne Scientific Company.

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