THz Technologies: Transistors, ICs, Systems

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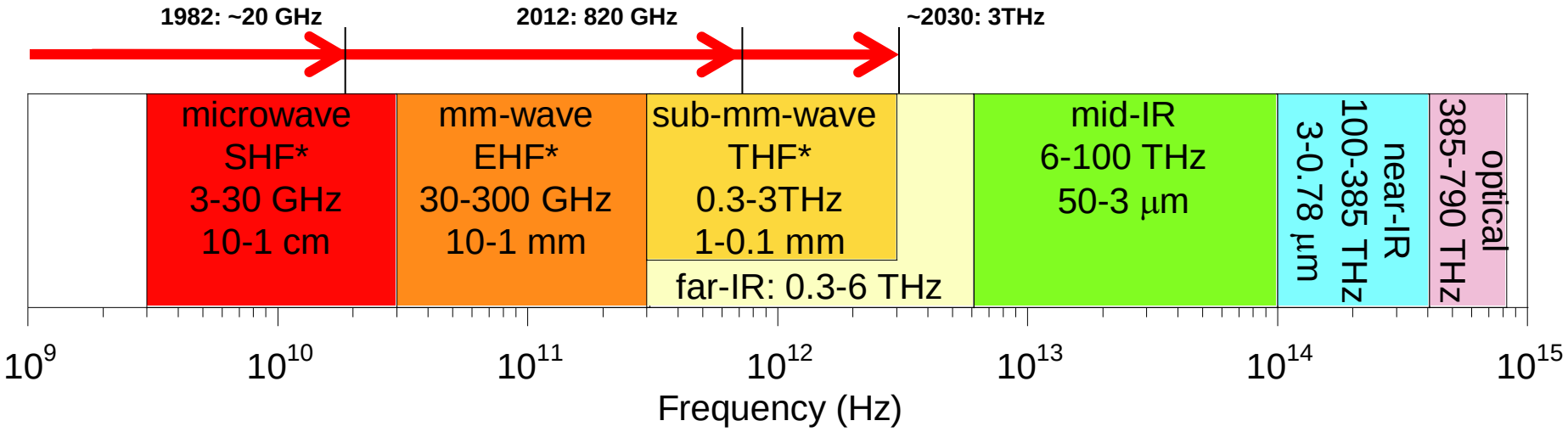
DC to Daylight. Far-Infrared Electronics

How high in frequency can we push electronics ?

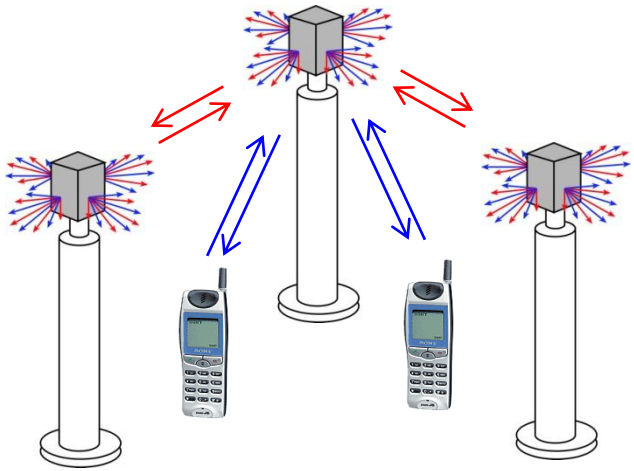
*ITU band designations

** IR bands as per ISO 20473

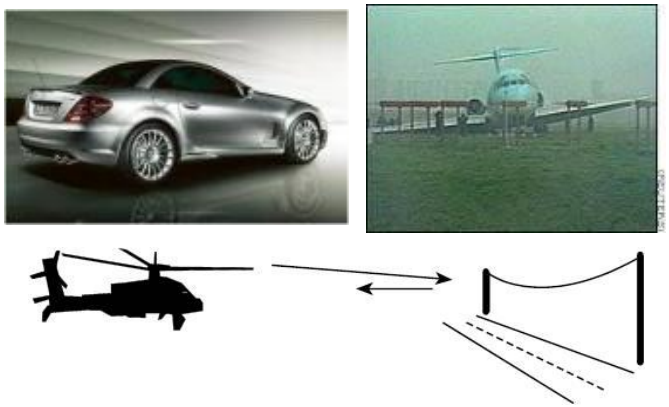


...and what we would be do with it ?

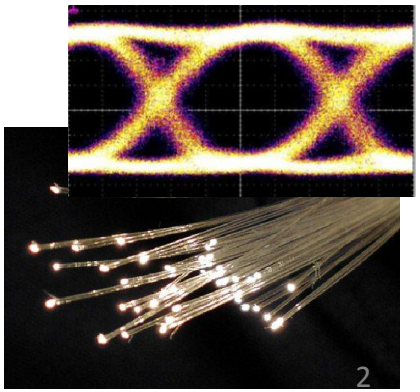
100+ Gb/s wireless networks



Video-resolution radar
→ fly & drive through fog & rain

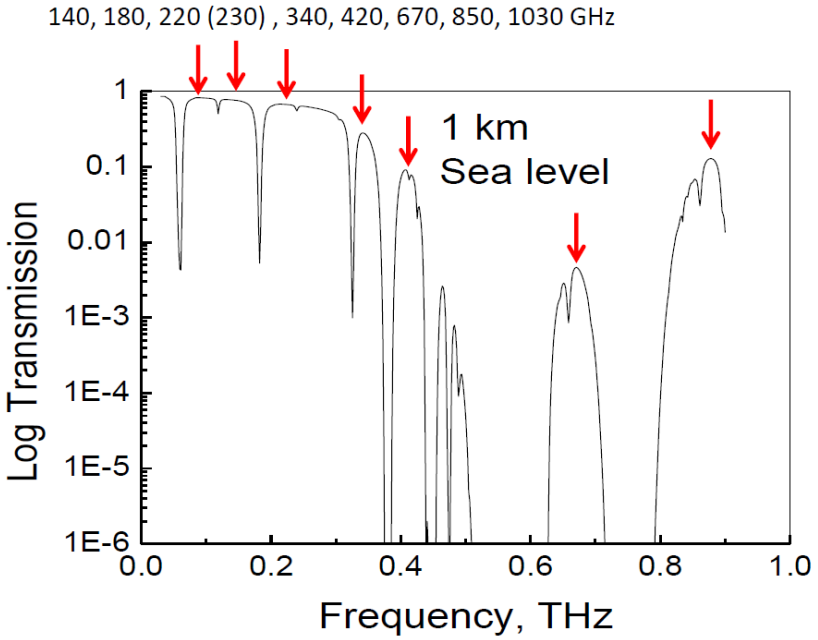


near-Terabit optical fiber links



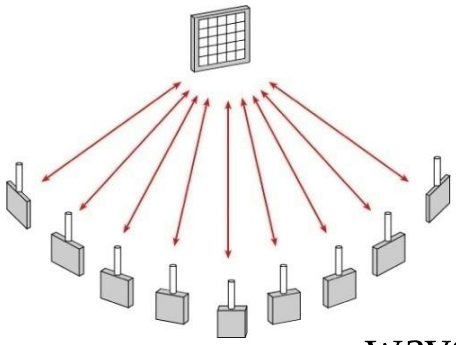
100-1000 GHz Wireless Has High Capacity

very large bandwidths available

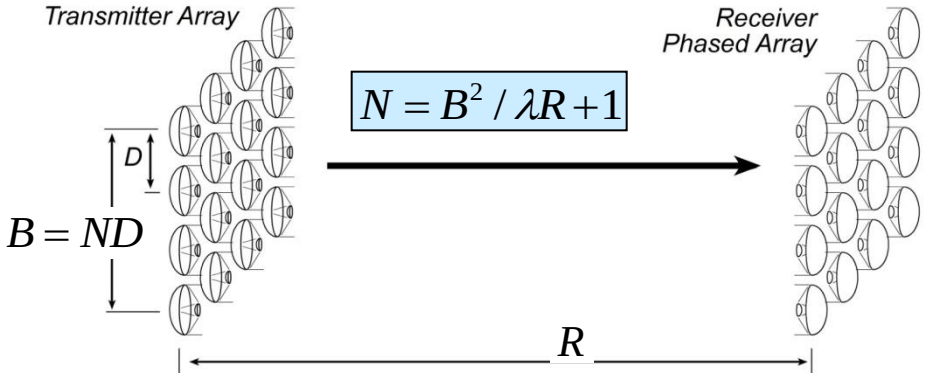


short wavelengths→ many parallel channels

Sheldon IMS 2009
Torkildson : IEEE Trans Wireless Comms. Dec. 2011.



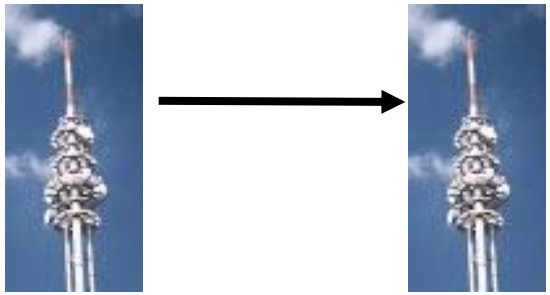
$$\text{angular resolution} \approx \frac{\text{wavelength}}{\text{array width}}$$



$$\#\text{channels} \propto (\text{aperture area})^2/(\text{wavelength}\cdot\text{distance})^2$$

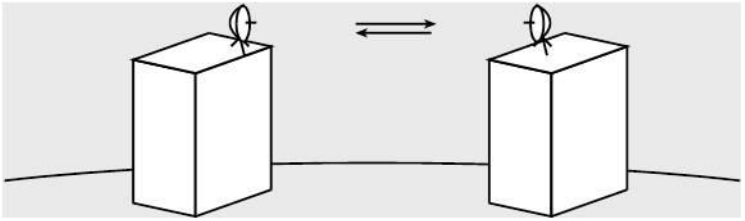
100-1000 GHz Wireless Needs Phased Arrays

isotropic antenna → weak signal →short range



$$\left(\frac{P_{received}}{P_{transmitted}}\right) \propto \left(\frac{\lambda^2}{R^2}\right) e^{-\alpha R}$$

highly directional antenna → strong signal, but must be aimed

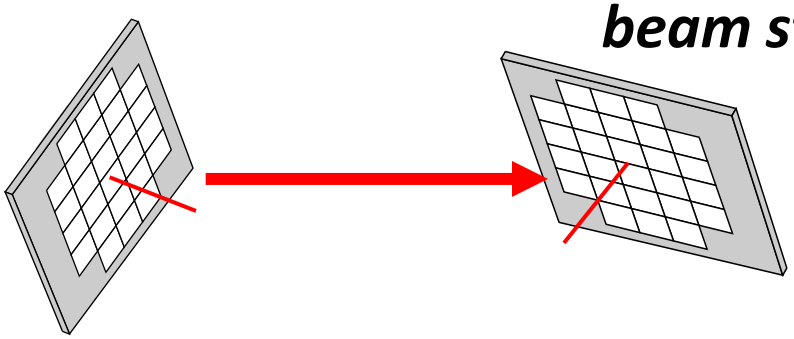


$$\left(\frac{P_{received}}{P_{transmitted}}\right) \propto D_t D_r \left(\frac{\lambda^2}{R^2}\right) e^{-\alpha R}$$

no good for mobile

must be precisely aimed →too expensive for telecom operators

beam steering arrays → strong signal, steerable

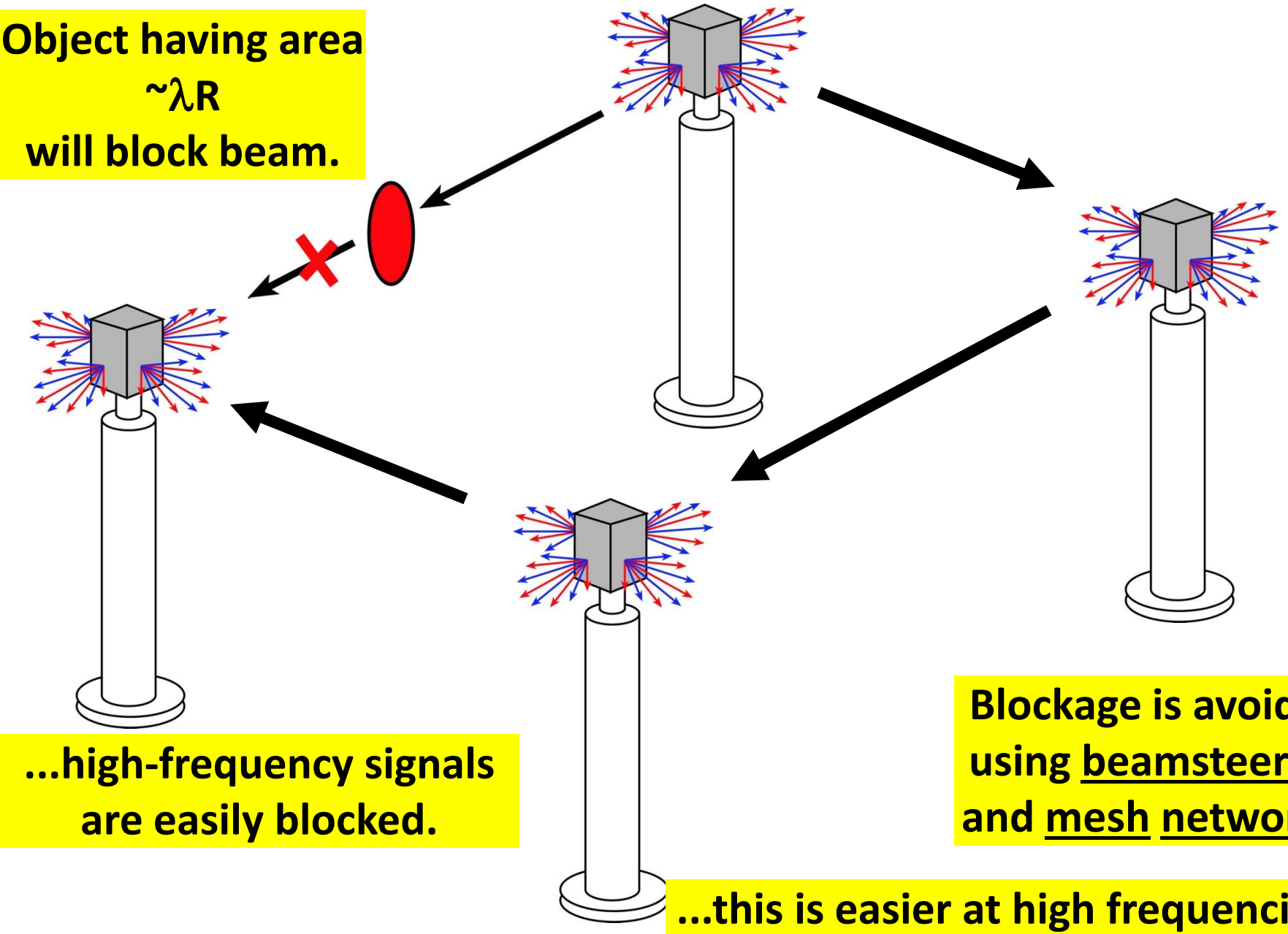


$$\frac{P_{received}}{P_{transmit}} \propto N_{receive} N_{transmit} \frac{\lambda^2}{R^2} e^{-\alpha R}$$

32-element array → 30 (45?) dB increased SNR

100-1000 GHz Wireless Needs Mesh Networks

Object having area ~λR will block beam.

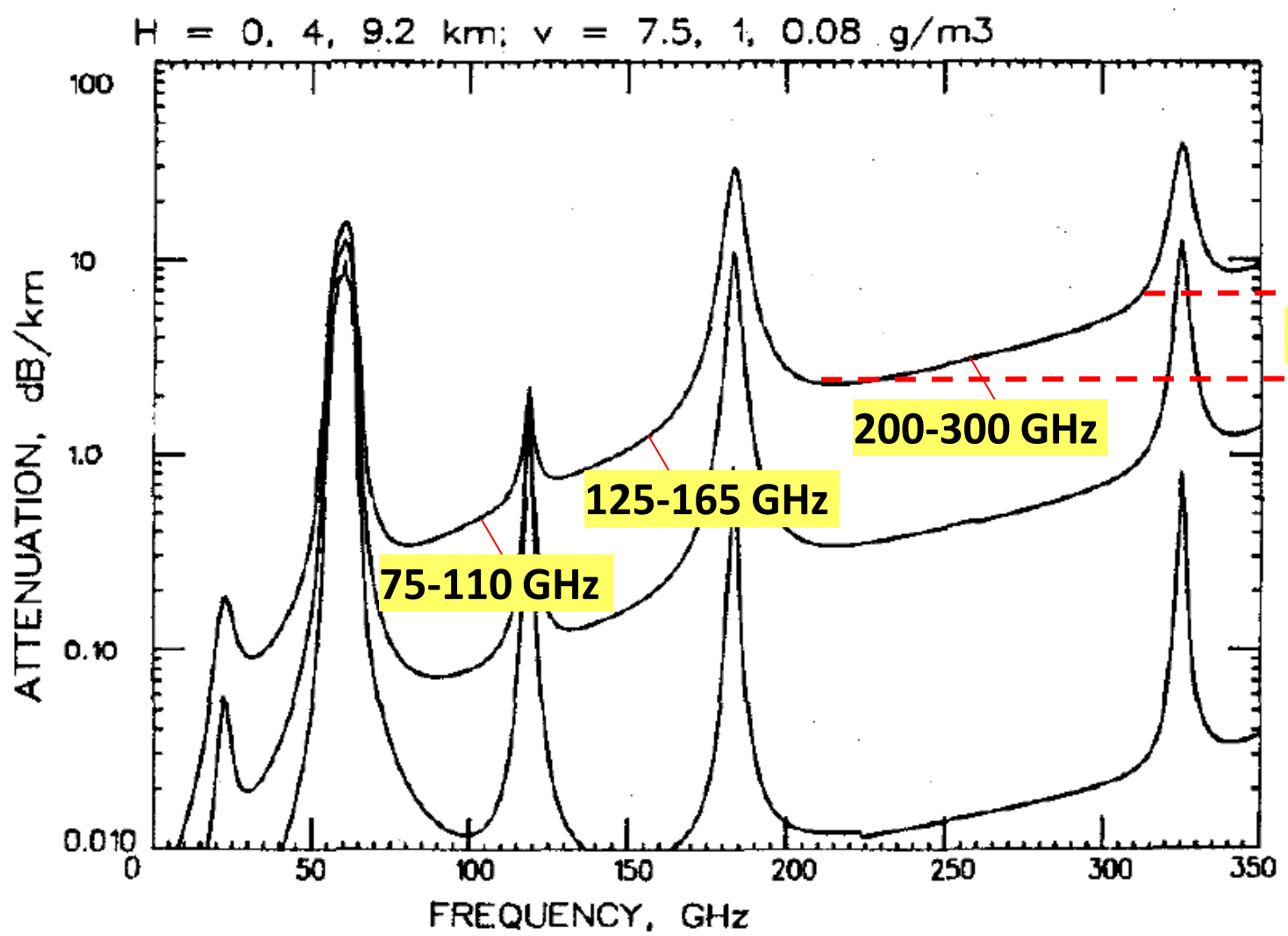


...high-frequency signals are easily blocked.

Blockage is avoided using beamsteering and mesh networks.

...this is easier at high frequencies.

100-1000 GHz Wireless Has Low Attenuation ?

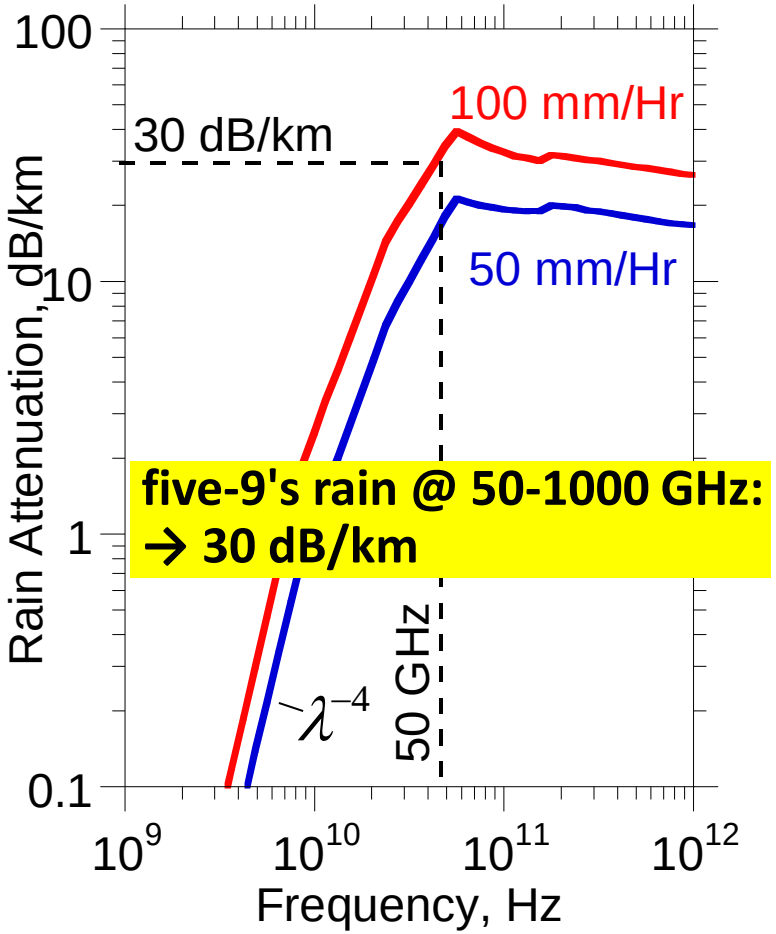


Wiltse, 1997 IEEE Int. APS Symposium, July

Low attenuation on a sunny day

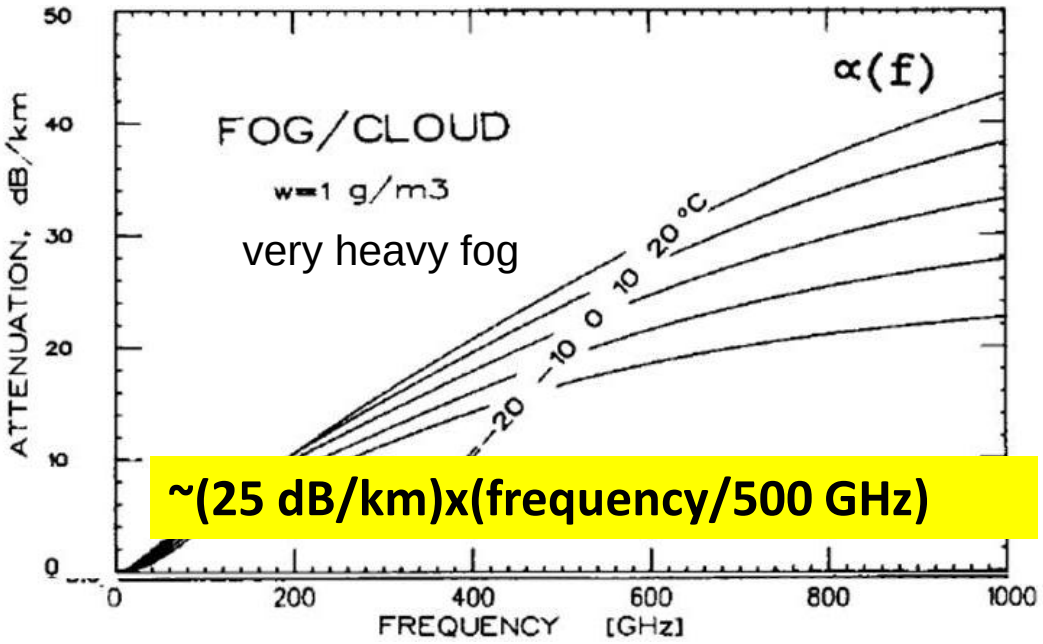
100-1000 GHz Wireless Has High Attenuation

High Rain Attenuation



five-9's rain @ 50-1000 GHz:
→ 30 dB/km

High Fog Attenuation

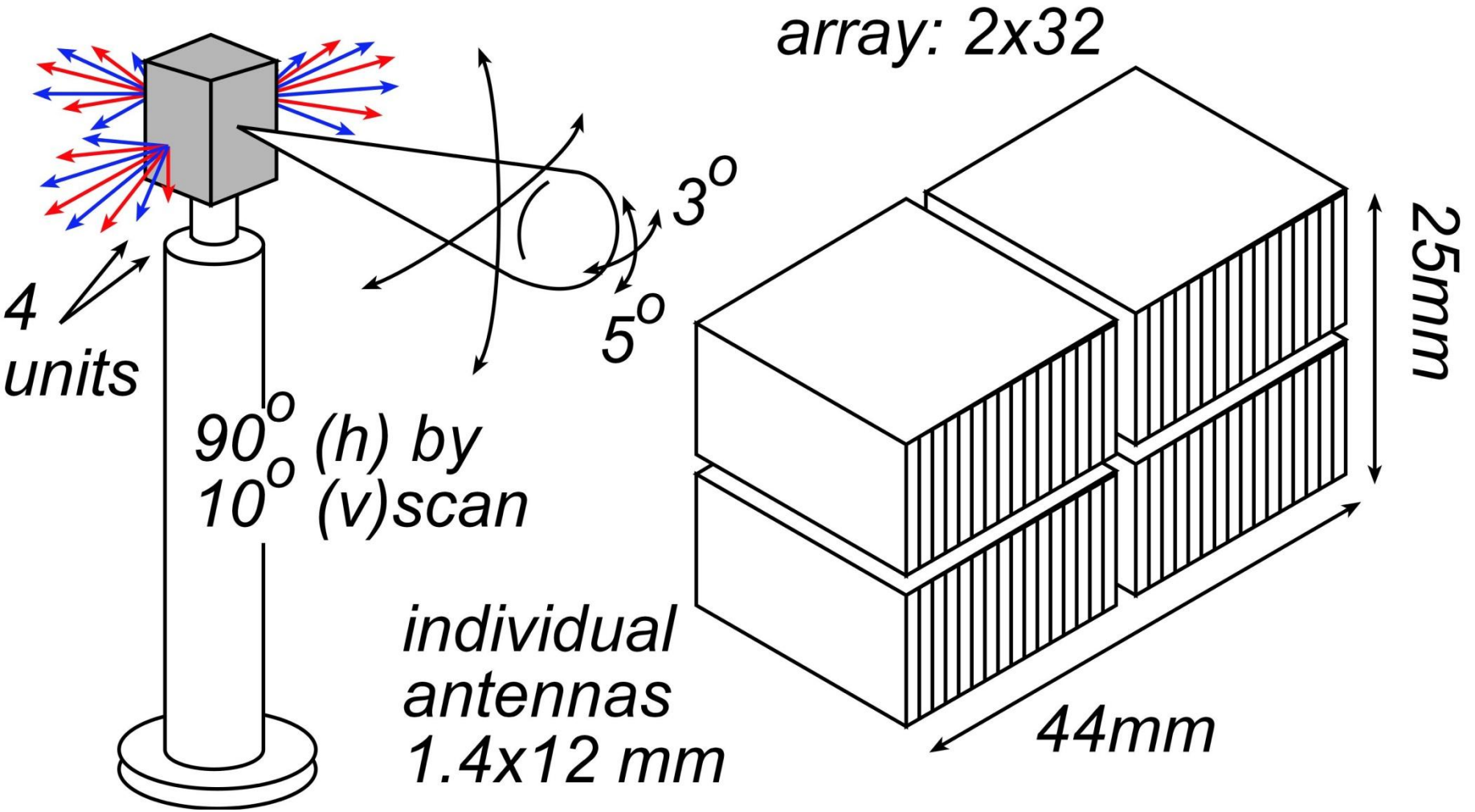


~(25 dB/km)x(frequency/500 GHz)

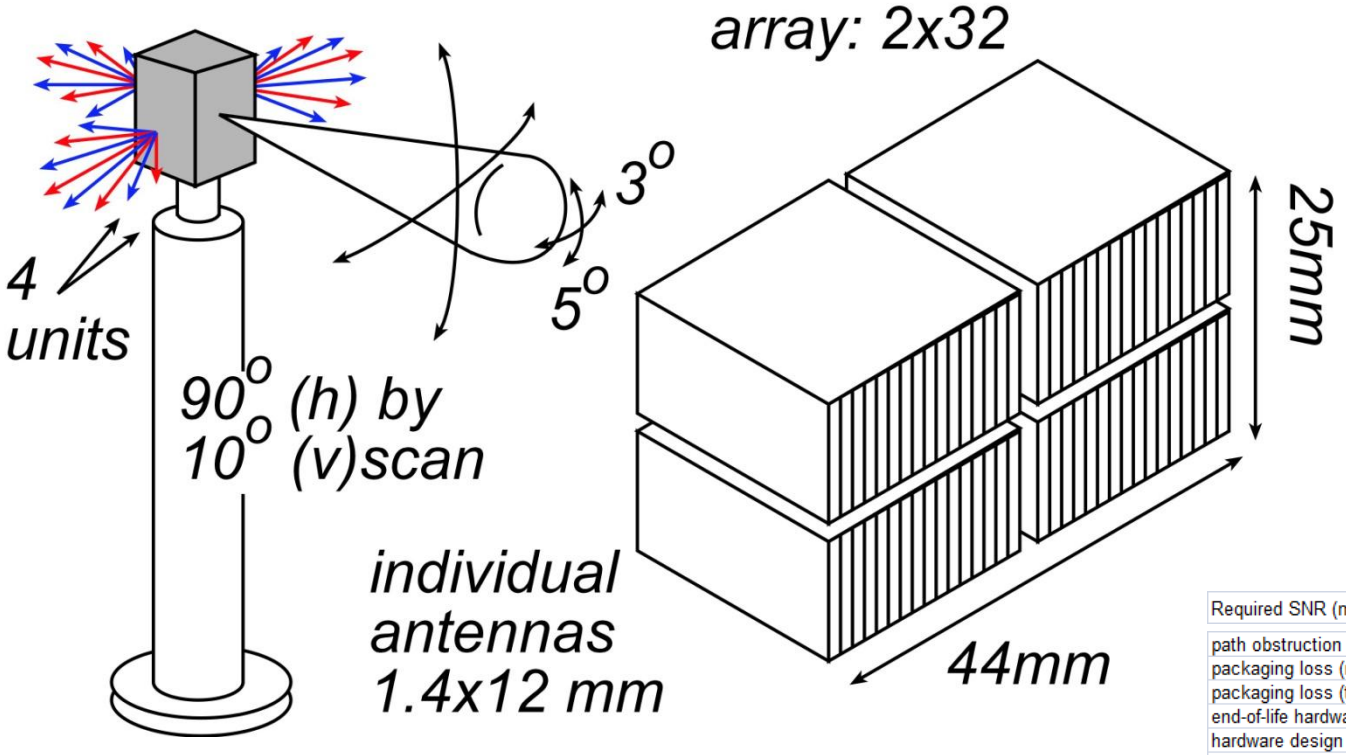
50-500 GHz links must tolerate ~30 dB/km attenuation

Olsen, Rogers, Hodge, IEEE Trans Antennas & Propagation Mar 1978 Liebe, Manabe, Hufford, IEEE Trans Antennas and Propagation, Dec. 1989

140 GHz, 10 Gb/s Adaptive Picocell Backhaul



140 GHz, 10 Gb/s Adaptive Picocell Backhaul



Required SNR (measured as Eb/No)	6.8	dB
path obstruction loss (foliage, glass)	5.00	dB
packaging loss (receiver)	3	dB
packaging loss (transmitter)	3	dB
end-of-life hardware degradation	3	dB
hardware design margin	3	dB
beam aiming loss (edge of beam)	3	dB
systems operating margin	10	dB
PA backoff for OFDM	7.00E+00	dB

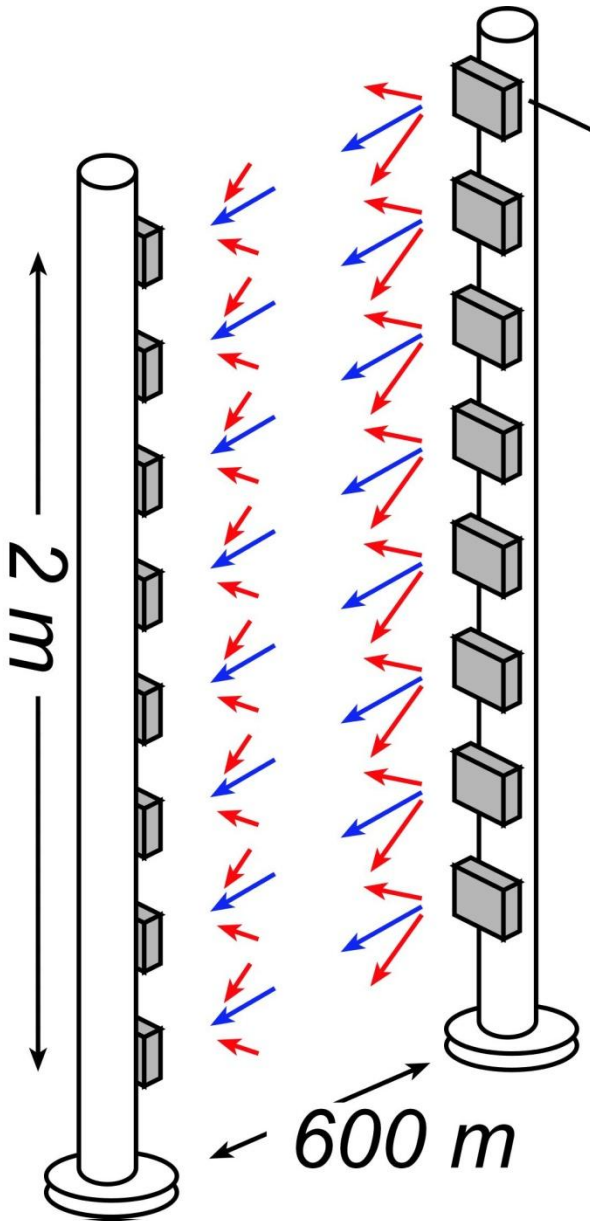
350 meters range in five-9's rain

Realistic packaging loss, operating & design margins

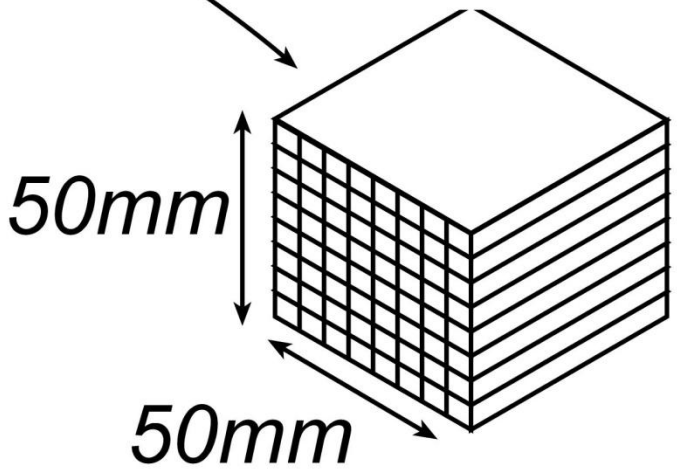
PAs: 24 dBm P_{sat} (per element)→ GaN or InP

LNAs: 4 dB noise figure → InP HEMT

340 GHz, 160 Gb/s MIMO Backhaul Link



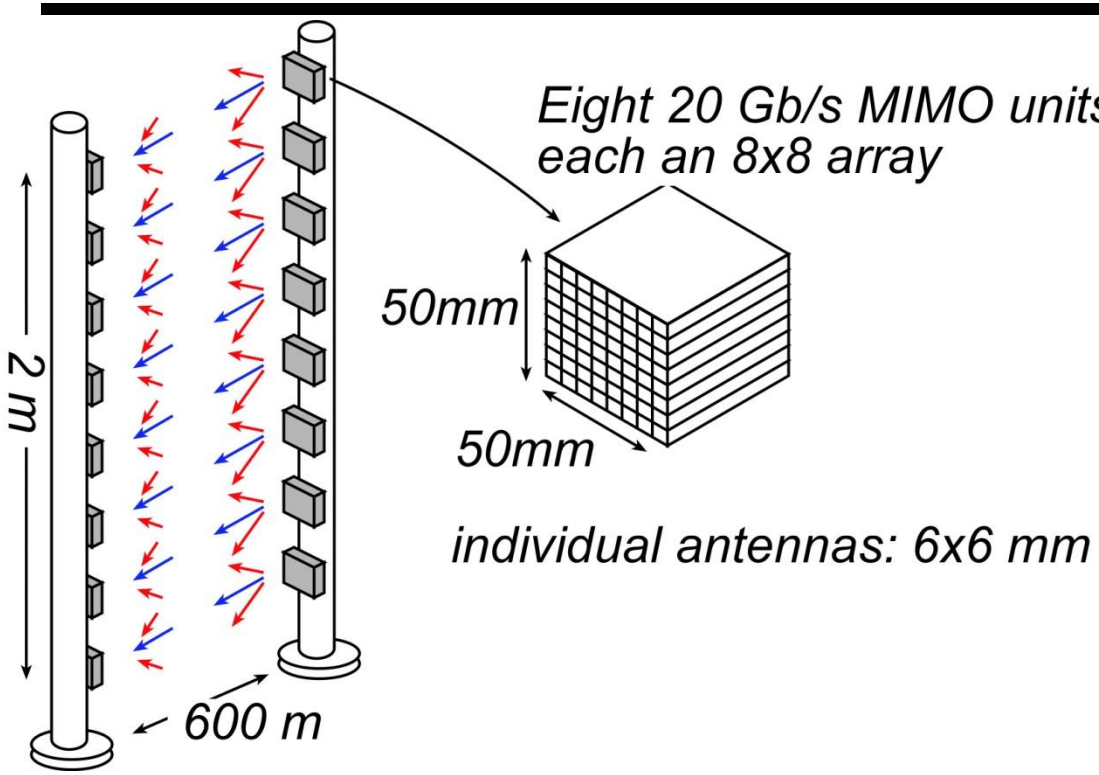
Eight 20 Gb/s MIMO units: each an 8x8 array



individual antennas: 6x6 mm

→ 1° beamwidth; 8° beamsteering

340 GHz, 160 Gb/s MIMO Backhaul Link



1º beamwidth; 8º beamsteering

600 meters range in five-9's rain

Realistic packaging loss, operating & design margins

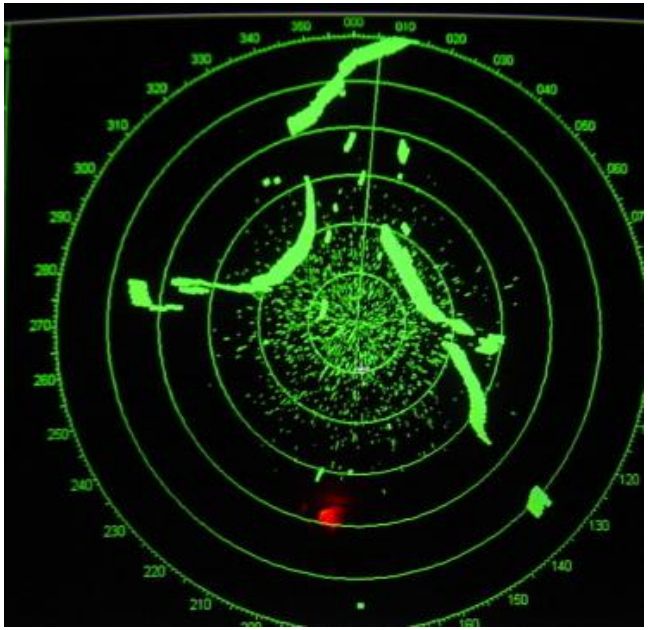
PAs: 21 dBm P_{sat} (per element)→ InP

LNAs: 7 dB noise figure → InP HEMT

400 GHz frequency-scanned imaging radar

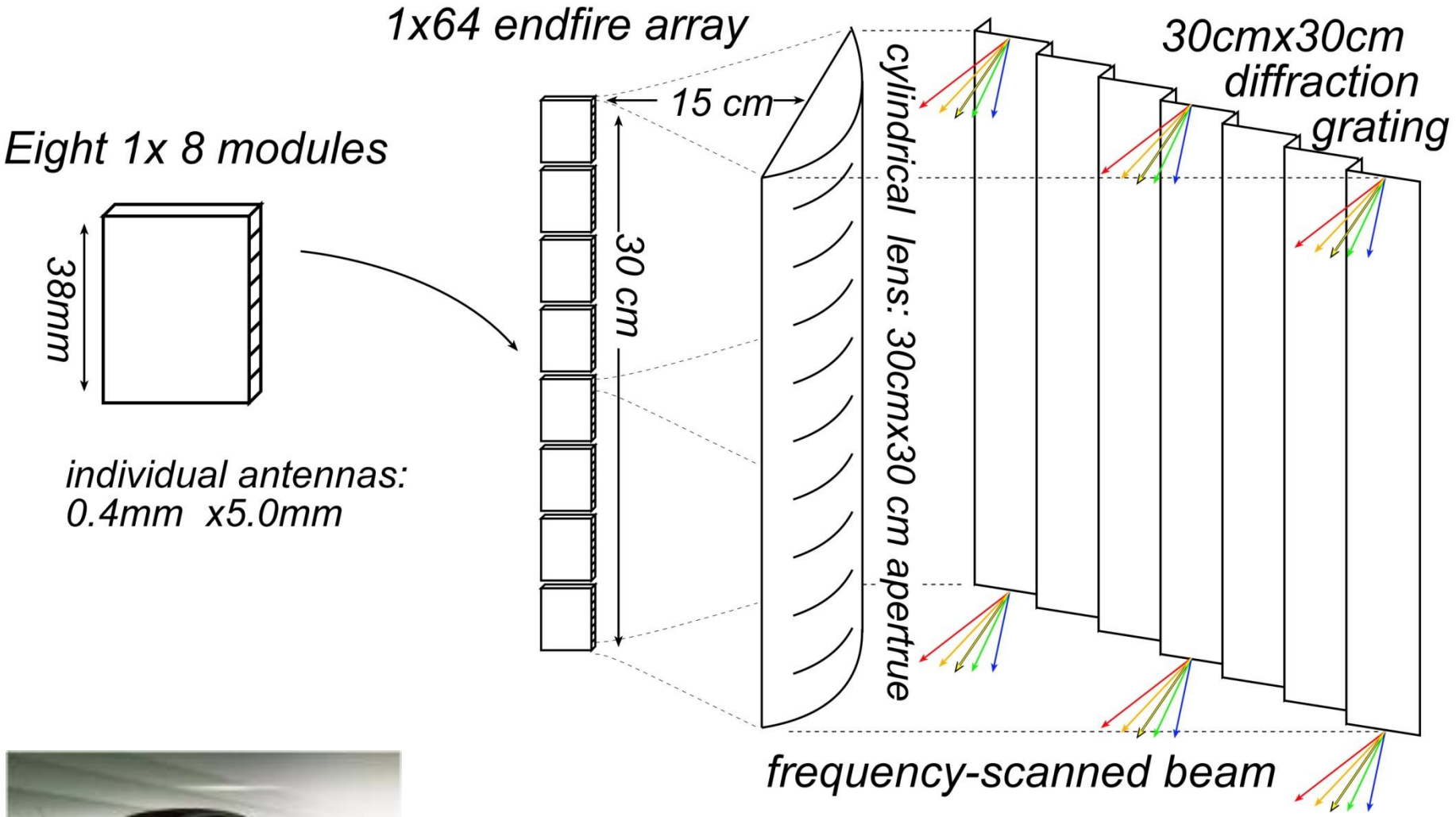
What your eyes see-- in fog

What you see with X-band radar



What you would like to see

400 GHz frequency-scanned imaging car radar



400 GHz frequency-scanned imaging car radar

Range: see a basketball at 300 meters (10 seconds warning) in heavy fog
(10 dB SNR, 28 dB/km, 1 foot diameter target, 65 MPH)

Image refresh rate: 60 Hz

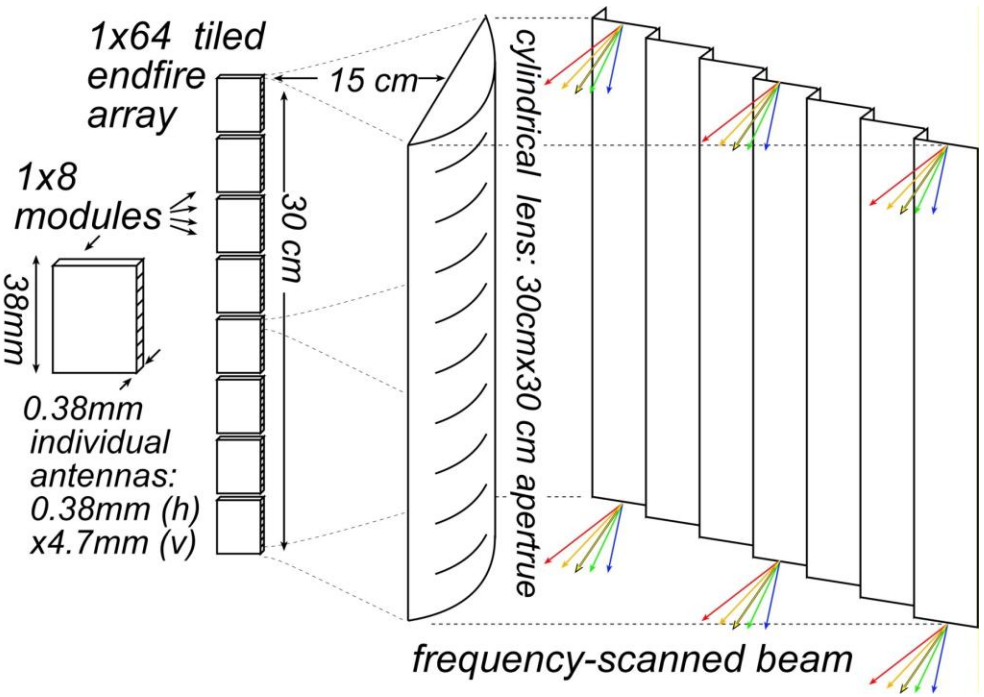
Resolution 64×512=32,800 pixels

Angular resolution: 0.10 degrees

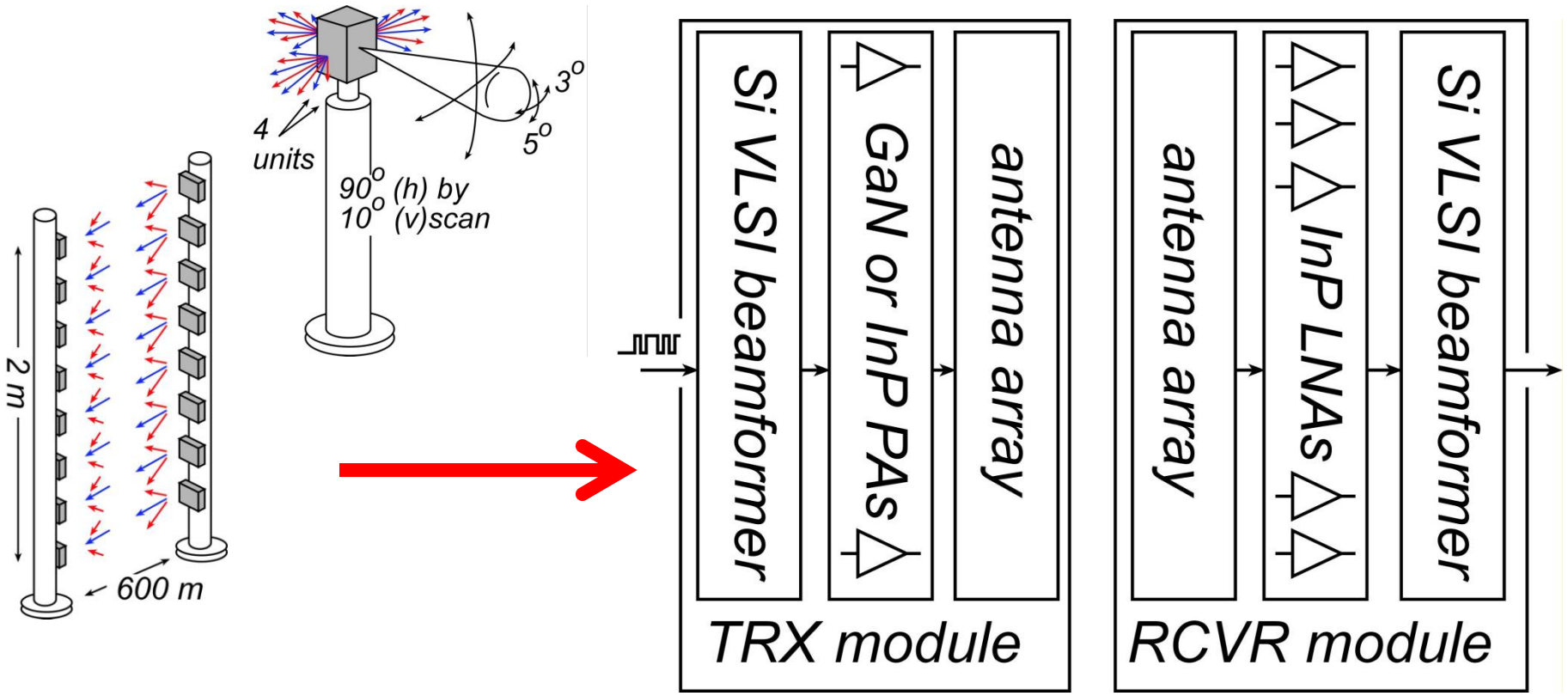
Angular field of view: 9 by 97 degrees

Aperture: 12" by 12"

Component requirements:
10 mW peak power/element,
3% pulse duty factor
6.5 dB noise figure,
5 dB package losses
5 dB manufacturing/aging margin



100-1000 GHz Wireless Transceiver Architecture

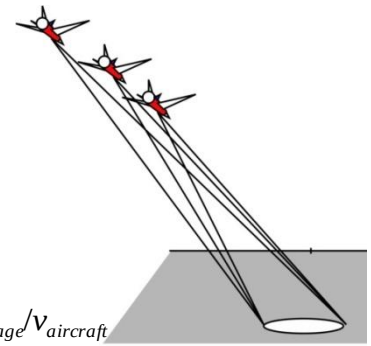


III-V LNAs, III-V PAs → power, efficiency, noise
Si CMOS beamformer→ integration scale

...similar to today's cell phones.

RADAR / Imaging Needs Watts of Power, Low Noise Figure

220 GHz video-rate synthetic aperture radar



$$\text{Azimuthal resolution } \delta_a = \lambda R f_{image}/v_{aircraft}$$

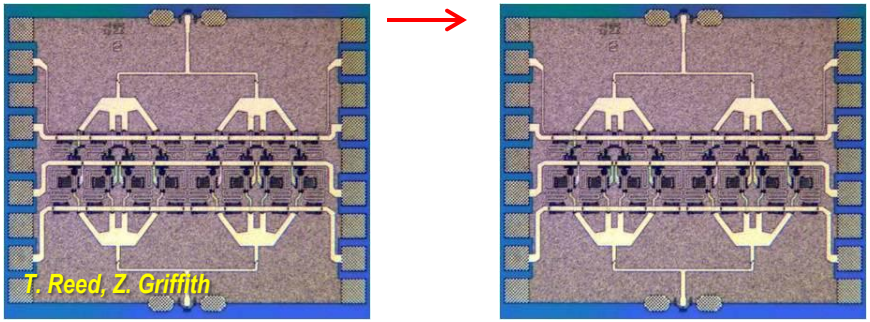
$$\text{SNR} = \frac{P_{trans}}{kTFf_{image}} \frac{1}{4\pi R^2} \frac{LH}{\lambda^2} \cdot \delta_a \delta_r \sin\psi \cdot \rho \cdot \frac{LH}{4\pi R^2} e^{-2\alpha R}$$

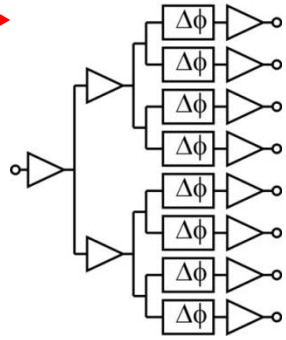
10 Hz video rate.	1 km range
570 x 500 pixel image	100 mm x 44 mm total aperture,
5.5 cm resolution.	32 receive elements.
16 dB SNR	250 m/s aircraft velocity
@ 10% reflectivity.	7 dB/km attenuation

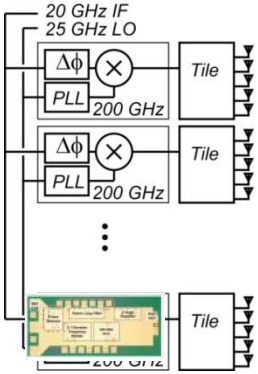
50 W transmitted power. 6 dB noise figure.

...to reach such levels with a solid-state source:

Present 220 GHz, 66 mW PA → Develop 200 mW PA → 8-element array tile IC: 1.6 W → 32 tiles/array → 51 W



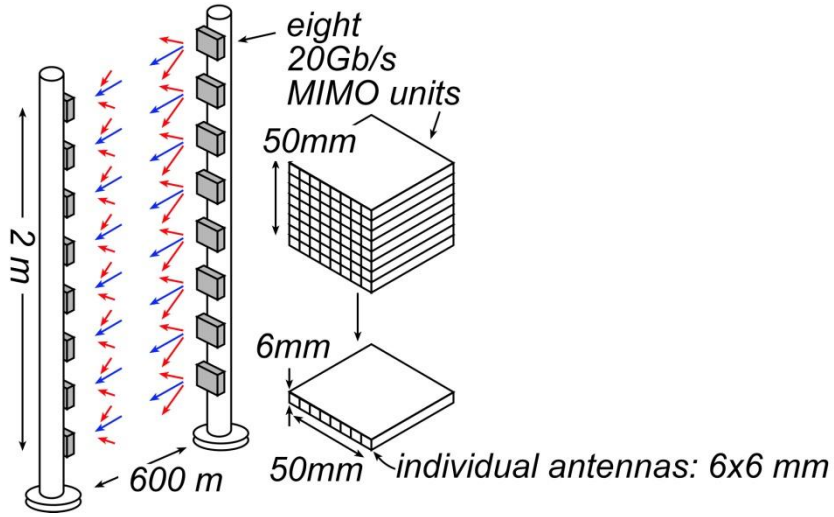


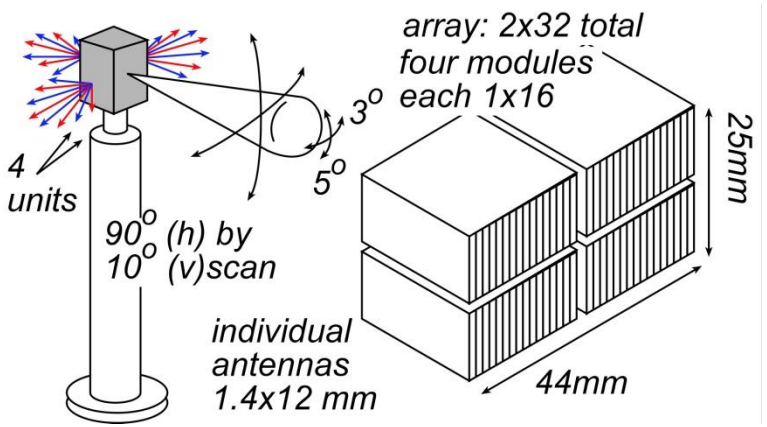


(200 GHz PLL is existing design by M. Seo)

As a function of range, weather, and data rate, effective sub-mm-wave technologies must low noise figure, high transmit power, and/or moderate to large phased arrays

0.1-1 THz Comms Links: No Monolithic Arrays





On-wafer antennas

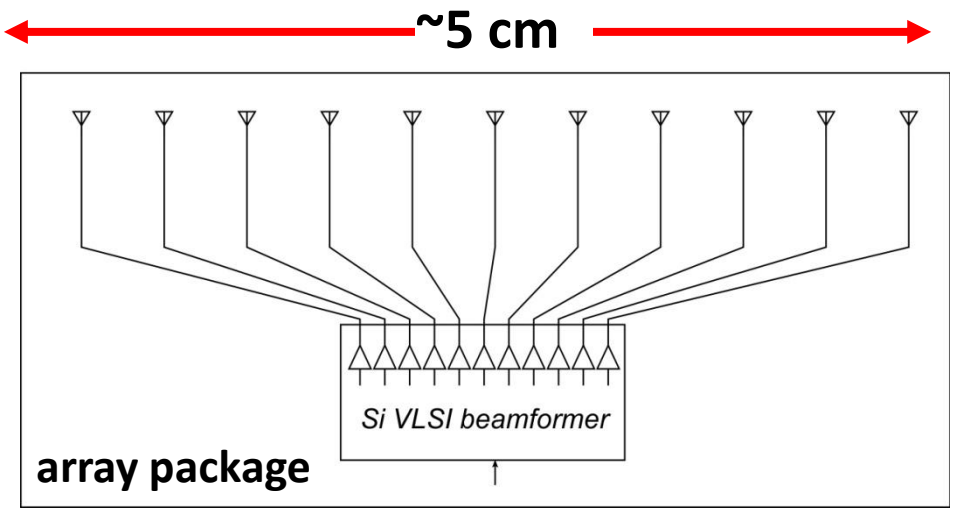
substantial die area, have high losses

For useful directivity, aperture areas are ~ 25 cm^2.

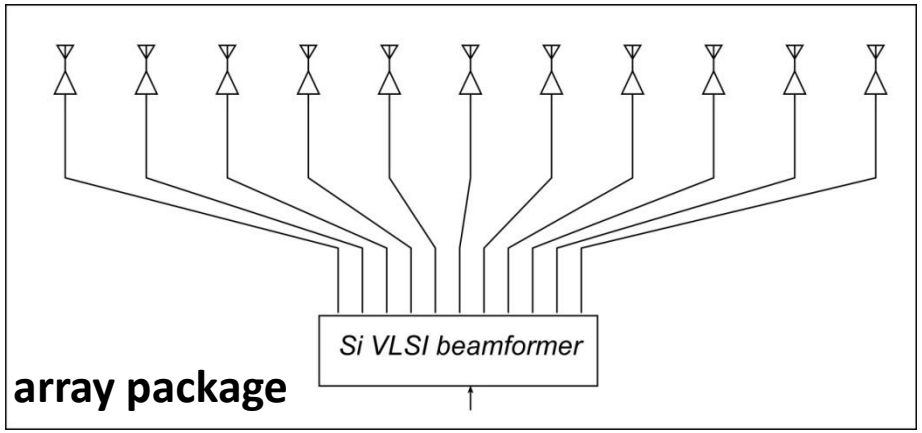
→ vastly too large for an IC

0.1-1 THz Comms Links: Discrete LNAs & PAs

Monolithic PAs & LNAs
- **long lines to antennas**
- **many dB losses on transmit**
- **many dB losses on transmit**
- **degraded noise, degraded power**

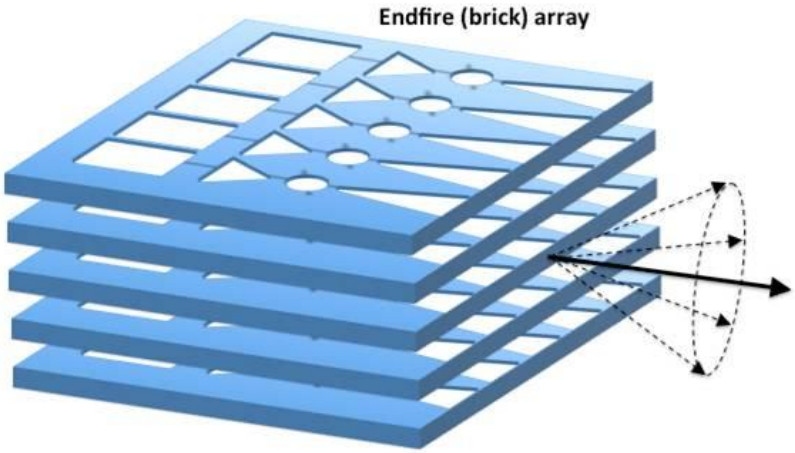


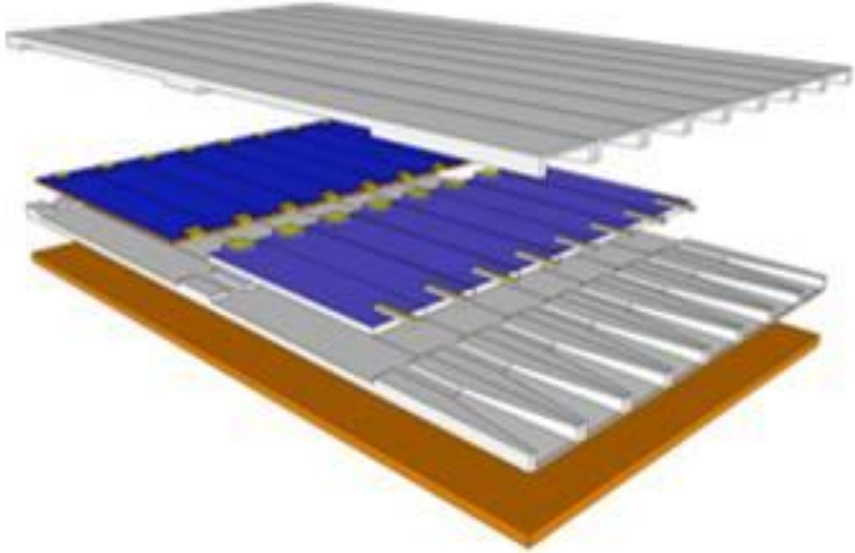
Discrete LNAs and PAs
- **LNAs & PAs: adjacent to antennas**
- **losses no longer impair link**

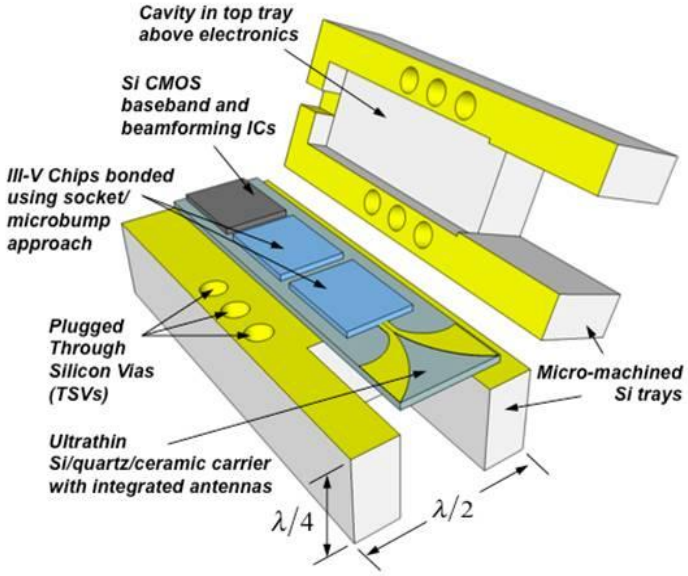


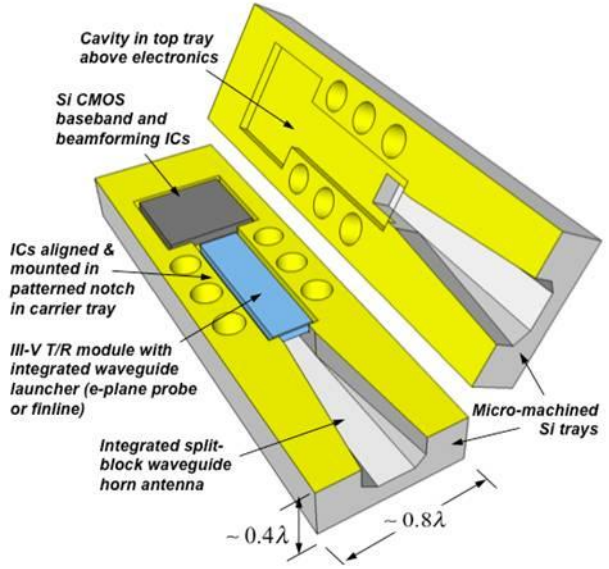
Given that we should not integrate the LNA and PA on the beamformer, it is to our benefit to use high-performance GaN & InP LNAs and PAs.

0.1-1 THz Comms Links: Array Design Concepts



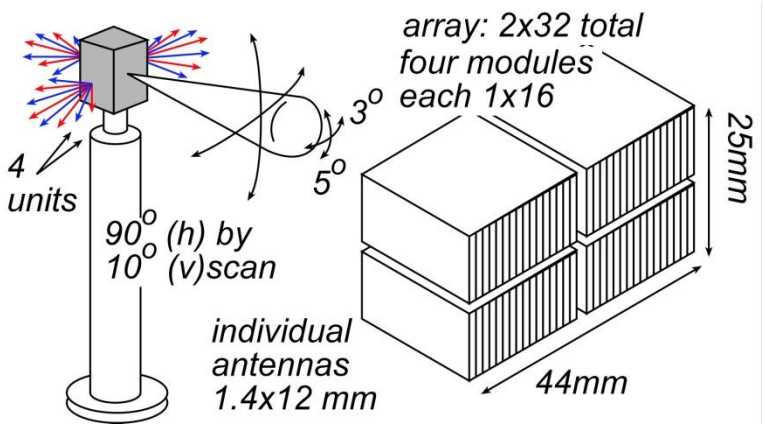






Concepts: Robert York, UCSB

Effects of array size, Transmitter PAE, Receiver F_{min}



200 mW phase shifters in TRX & RCVR, 0.1 W LNAs

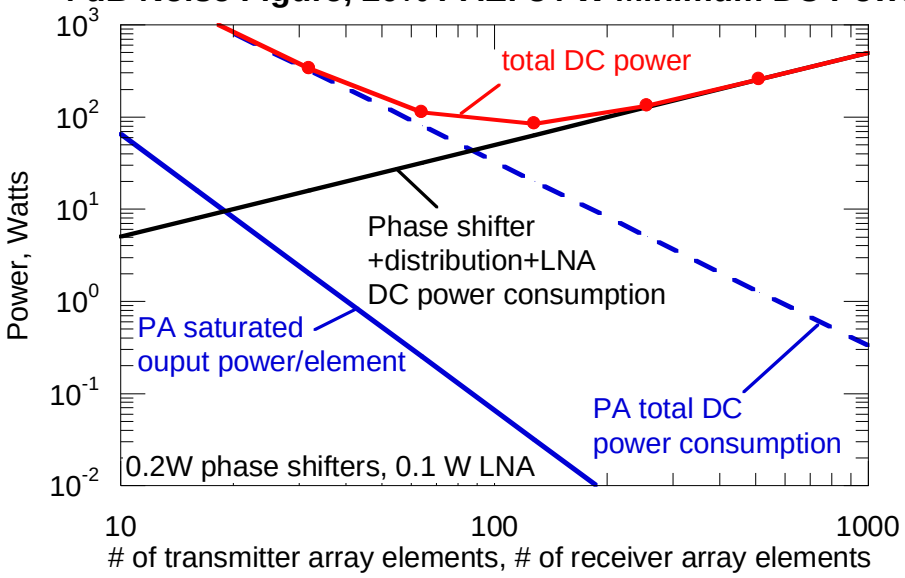
Large arrays:
more directivity, more complex ICs
Small arrays:
less directivity, less complex ICs

→ ***Proper array size minimizes DC power***

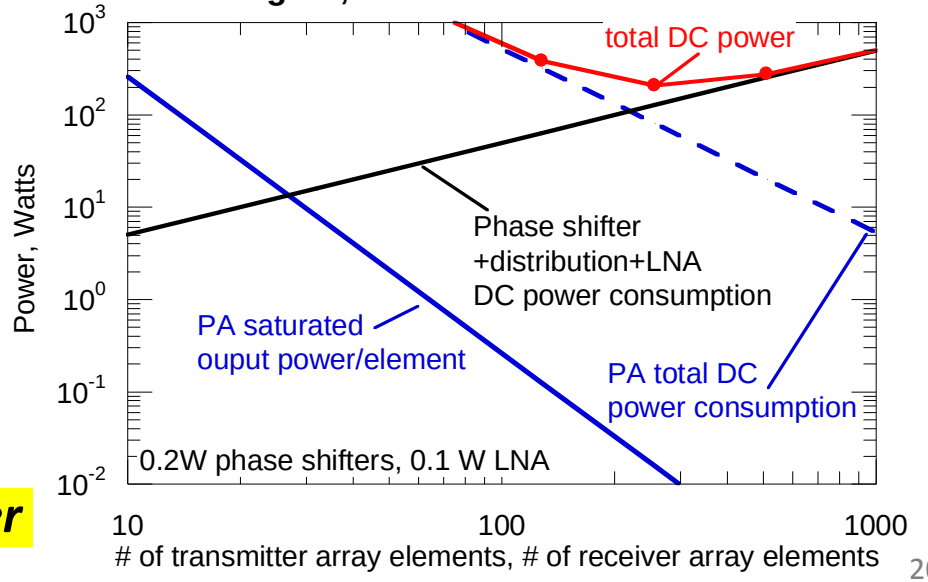
Low transmitter PAE
& high receiver noise
are partially offset using arrays,

but DC power, system complexity still suffer

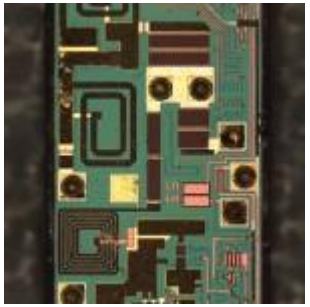
4 dB Noise Figure, 20% PAE: 84 W Minimum DC Power

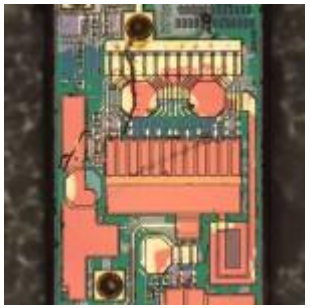


10 dB Noise Figure, 5%PAE: 208 W Minimum DC Power



III-V PAs and LNAs in today's wireless systems...





http://www.chipworks.com/blog/recentteardowns/2012/10/02/apple-iphone-5-the-rf/

Devices for 100-1000 GHz systems: F_{min}, P_{sat}, PAE

LNA noise figure, Power amplifier power & efficiency:
All critically important in radio and radar

InP HBTs: strong THz MSI technology
efficient, high-power PAs,
up/down converters (VCOs, synthesizers, mixers)

InP HEMTs: best THz LNA technology
3 dB more noise → 2:1 more transmit power

GaN HEMTs vs. InP HBTs for power:
breakdown vs. gain→ power vs. PAE.

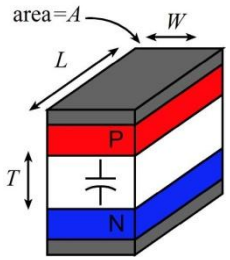
CMOS VLSI:
high bandwidth, high integration scales → bulk of signal processing
poor P_{sat}, PAE, F_{min}.

Harmonic techniques:
multiplication: low power, inefficient, nonlinear (16QAM ?, OFDM ?)
harmonic mixing: high noise figure

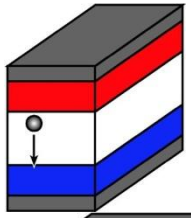
Transistors for 100-1000 GHz systems

Transistor scaling laws: (V,I,R,C,τ) vs. geometry

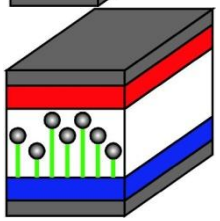
Depletion Layers



$$C = \varepsilon \cdot \frac{A}{T}$$

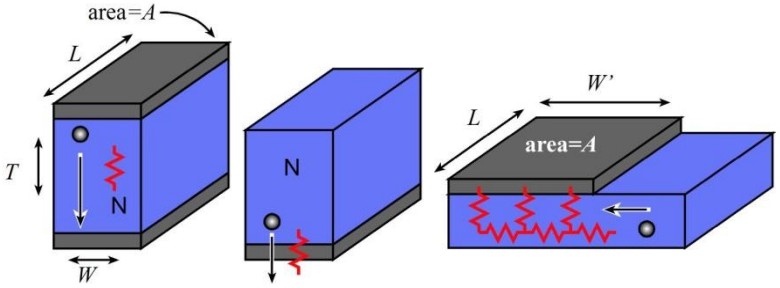


$$\tau = \frac{T}{2v}$$



$$\frac{I_{\max}}{A} = \frac{4\varepsilon v_{sat}(V_{appl} + \phi)}{T^2}$$

Bulk and Contact Resistances

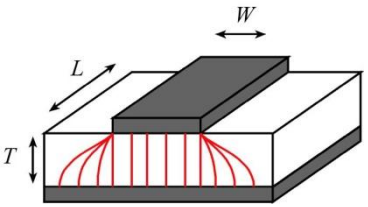


$$R \cong \rho_{contact} / A$$

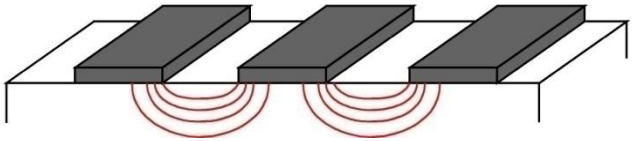
contact terms dominate

Fringing Capacitances

1) FET fringing capacitances
2) IC interconnect capacitances

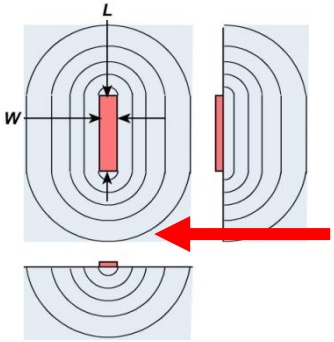


$$C_{finging} / L \sim \varepsilon$$

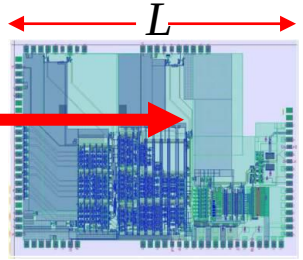


$$C_{finging} / L \sim \varepsilon$$

Thermal Resistance

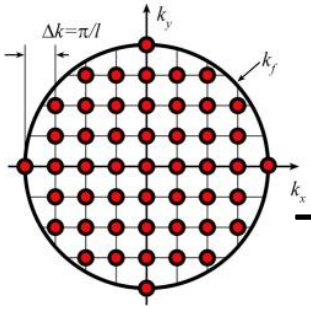


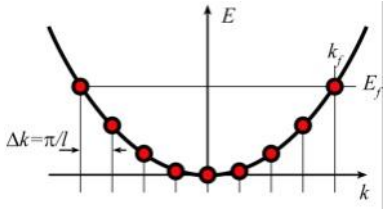
$$\Delta T_{IC} \propto \frac{P_{IC}}{K_{th} L}$$



$$\Delta T_{\text{transistor}} \sim \frac{P}{\pi K_{th} L} \ln\left(\frac{L}{W}\right)$$

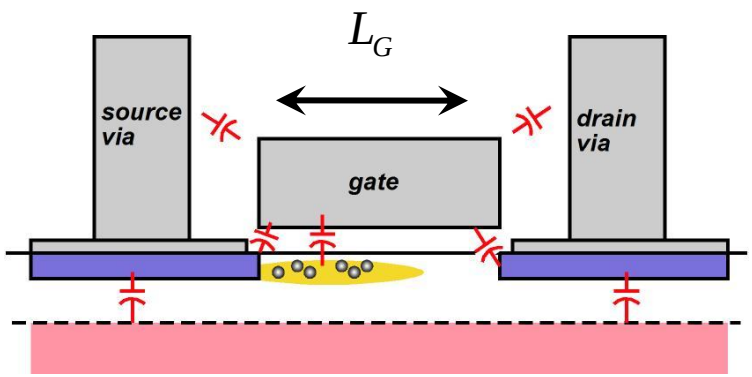
Available quantum states to carry current





→ ***capacitance, transconductance contact resistance***

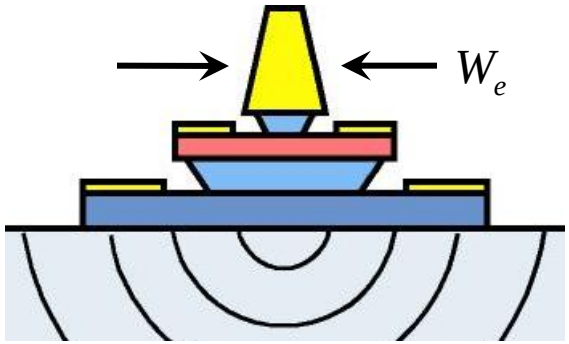
Changes required to double transistor bandwidth



(gate width W_G)

FET parameter	change
gate length	decrease 2:1
current density (mA/μm), g_m (mS/μm)	increase 2:1
transport effective mass	constant
channel 2DEG electron density	increase 2:1
gate-channel capacitance density	increase 2:1
dielectric equivalent thickness	decrease 2:1
channel thickness	decrease 2:1
channel density of states	increase 2:1
source & drain contact resistivities	decrease 4:1

fringing capacitance does not scale → linewidths scale as (1 / bandwidth)



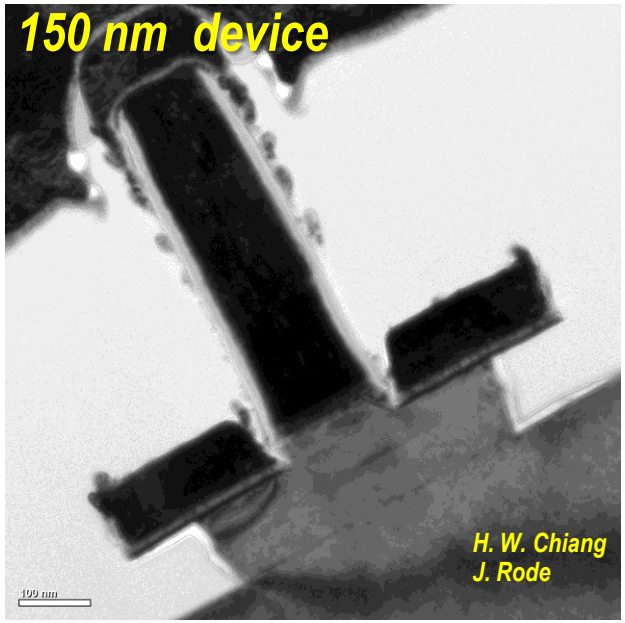
(emitter length L_E)

HBT parameter	change
emitter & collector junction widths	decrease 4:1
current density (mA/μm^2)	increase 4:1
current density (mA/μm)	constant
collector depletion thickness	decrease 2:1
base thickness	decrease 1.4:1
emitter & base contact resistivities	decrease 4:1

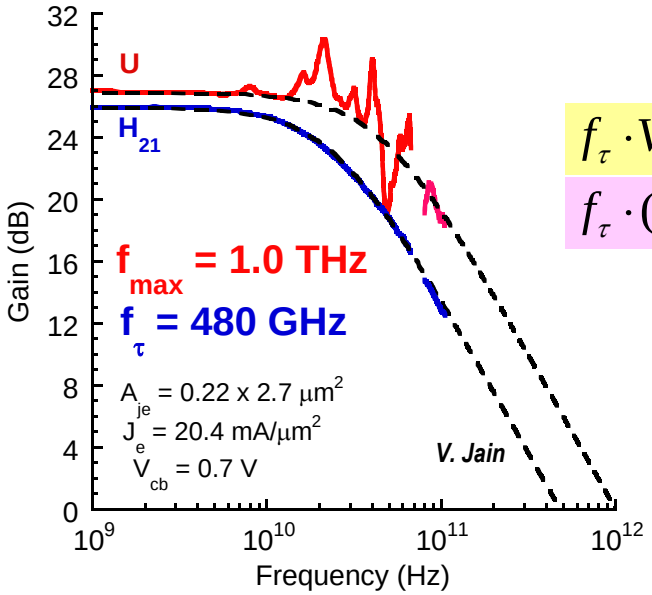
constant voltage, constant velocity scaling

nearly constant junction temperature → linewidths vary as (1 / bandwidth)^2

THz Bipolar Transistors

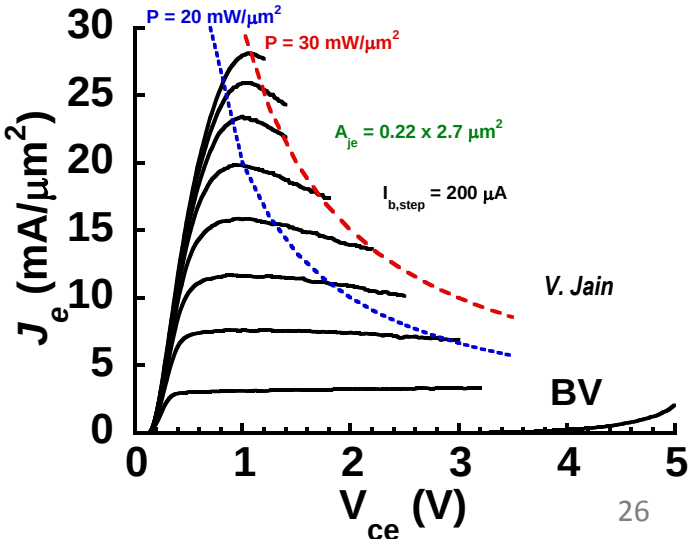


emitter	512	256	128	64	32 nm width
	16	8	4	2	1 Ω·μm² access ρ
base	300	175	120	60	30 nm contact width,
	20	10	5	2.5	1.25 Ω·μm² contact ρ
collector	150	106	75	53	37.5 nm thick,
	4.5	9	18	36	72 mA/μm² current density
	4.9	4	3.3	2.75	2-2.5 V, breakdown
f_τ	370	520	730	1000	1400 GHz
f_{max}	490	850	1300	2000	2800 GHz
power amplifiers	245	430	660	1000	1400 GHz
digital 2:1 divider	150	240	330	480	660 GHz



$$f_\tau \cdot V_{br} \approx 2\,\mathrm{THz}\cdot\mathrm{V}$$

$$f_\tau \cdot (\text{useful } \Delta V) \approx 1.0\,\mathrm{THz}\cdot\mathrm{V}$$



InP HBT: Key Features

512 nm node:

high-yield "pilot-line" process, ~4000 HBTs/IC

256 nm node:

Power Amplifiers: >0.5 W/mm @ 220 GHz

highly competitive mm-wave / THz power technology

128 nm node:

>500 GHz f_τ , >1.1 THz f_{max}, ~3.5 V breakdown

breakdown* f_τ = 1.75 THz*Volts

highly competitive mm-wave / THz power technology

64 nm (2 THz) & 32 nm (2.8 THz) nodes:

Development needs major effort, but no serious scaling barriers

1.5 THz monolithic ICs are feasible.

InP Bipolar Transistor Scaling Roadmap

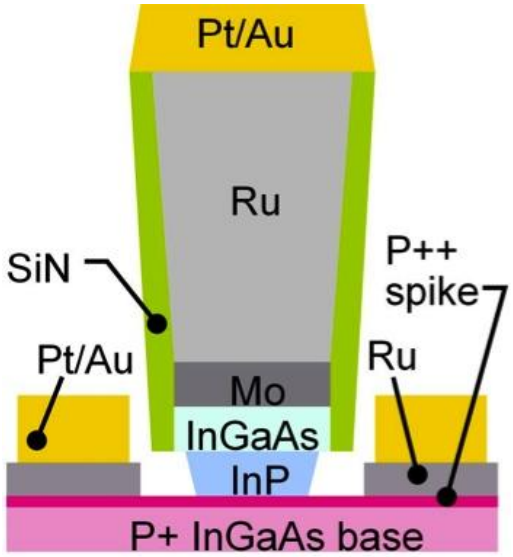
3-4 THz Bipolar Transistors are Feasible.

4 THz HBTs realized by:

Extremely low resistivity contacts

Extreme current densities

Processes scaled to 16 nm junctions



Scaling Node	64	32	16	nm
Emitter Width	64	32	16	nm
Resistivity	2	1	0.5	Ω-μm^2
Base Thickness	18	15	13	nm
Contact width	60	30	15	nm
Contact ρ	2.5	1.25	0.63	Ω-μm^2
Collector Width	180	90	45	nm
Thickness	53	37.5	26	nm
Current Density	36	72	140	mA/μm^2
f_τ	1.0	1.4	2.0	THz
f_{max}	2.0	2.8	4.0	THz

Impact:
efficient power amplifiers
and complex signal processing
from 100-1000 GHz.

InP Field-Effect-Transistor Scaling Roadmap

2-3 THz InP HEMTs are Feasible.

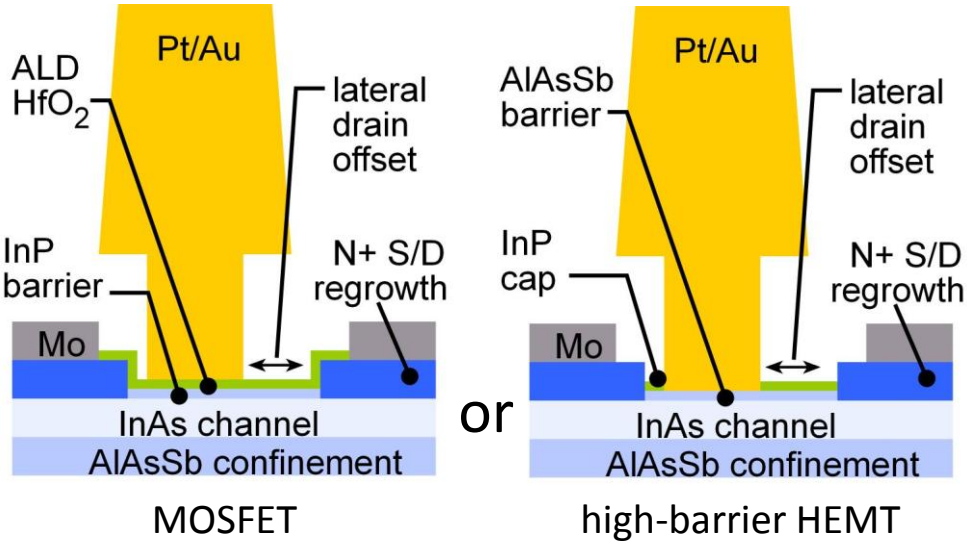
2 THz FETs realized by:

Ultra low resistivity source/drain

High operating current densities

Very thin barriers & dielectrics

Gates scaled to 9 nm junctions



gate length	36	18	9	nm
EOT	0.8	0.4	0.2	nm
well thickness	5.6	2.8	1.4	nm
effective mass	0.05	0.08	0.08	times m_0
# bands	1	1	1	--
S/D resistivity	150	74	37	Ω-μm
extrinisic g_m	2.5	4.2	6.4	mS/μm
on-current	0.55	0.8	1.1	mA/μm
f_τ	0.70	1.2	2.0	THz
f_{max}	0.81	1.4	2.7	THz

Impact:
Sensitive, low-noise receivers from 100-1000 GHz.

3 dB less noise →
need 3 dB less transmit power.

Can we make a 1 THz SiGe Bipolar Transistor ?

Simple physics clearly drives scaling

transit times, C_{cb}/I_c

→ thinner layers, higher current density

high power density → narrow junctions

small junctions→ low resistance contacts

Key challenge: Breakdown

15 nm collector → very low breakdown

Also required:

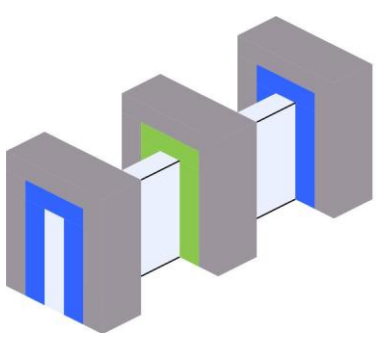
low resistivity Ohmic contacts to Si

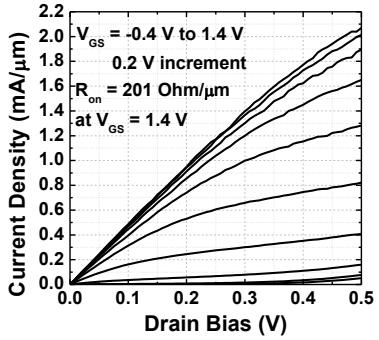
very high current densities: heat

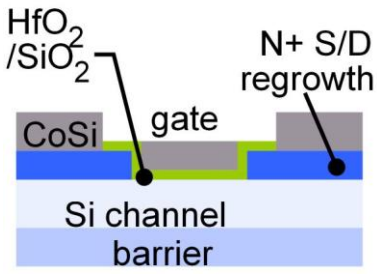
	InP	SiGe	
emitter	64	18	nm width
	2	**0.6**	$\Omega\cdot\mu m^2$ access ρ
base	64	18	nm contact width,
	2.5	**0.7**	$\Omega\cdot\mu m^2$ contact ρ
collector	53	**15**	nm thick
	36	125	$mA/\mu m^2$
	2.75	**1.3?**	V, breakdown
f_τ	**1000**	**1000**	GHz
f_{max}	**2000**	**2000**	GHz
PAs	1000	1000	GHz
digital	480	480	GHz
(2:1 static divider metric)			

Assumes collector junction 3:1 wider than emitter.
Assumes SiGe contacts no wider than junctions

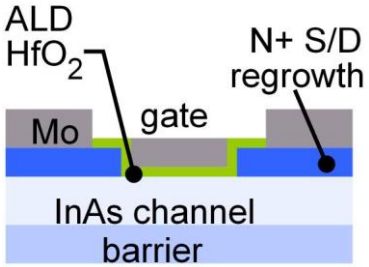
III-V vs. CMOS: A false comparison ?



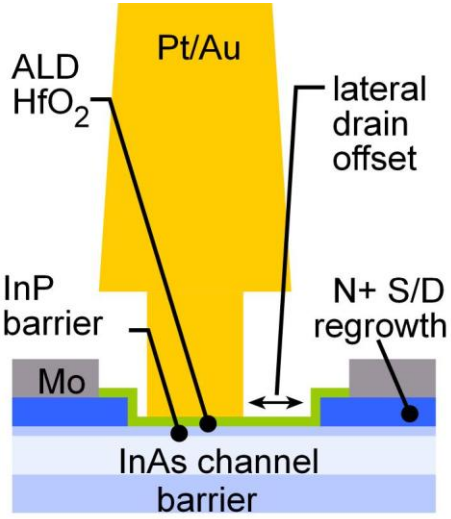




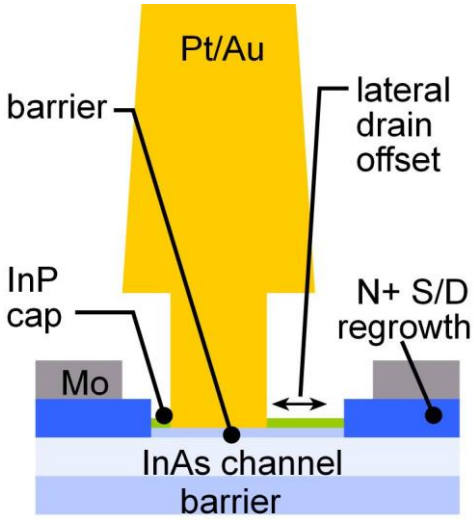
UTB Si MOS



UTB III-V MOS



III-V THz MOS/HEMT



III-V THz HEMT

III-V MOS has a reasonable chance of future use in VLSI

The real THz / VLSI distinction:

Device geometry optimized for high-frequency gain vs. optimized for small footprint and high DC on/off ratio.

0.1-1THz
IC Design

Challenges: 100-1000 GHz IC design

Given: we must use scaled, high-bandwidth transistors

Reduced breakdown is significant, but is not the main problem:

breakdown does not vary as $(\text{bandwidth})^{-1}$

low breakdown is not the only problem

Interconnects and their parasitics

interconnect length should vary as $(\text{frequency})^{-1}$

scaled device footprint: $(g_m / \text{area}) \propto (\text{current} / \text{area}) \propto (\text{frequency})^2$

scaled interconnect pitch: $\propto (\text{frequency})^{-1}$

Interconnects, footprints not scaled

→ large interconnect LC parasitics

Interconnects, footprints scaled

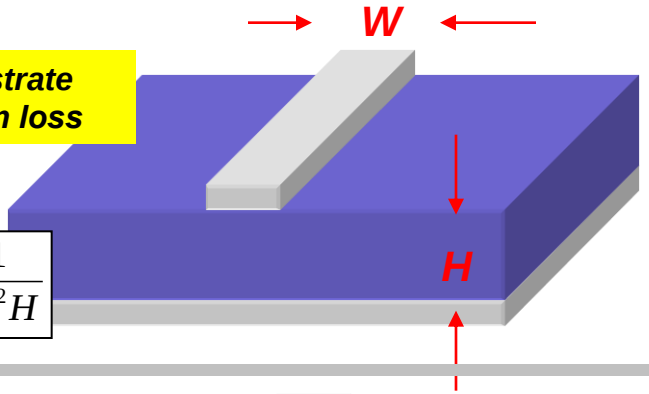
→ large interconnect resistance & skin loss

→ small interconnect burnout current

→ high IC power density

III-V MIMIC Interconnects -- Classic Substrate Microstrip

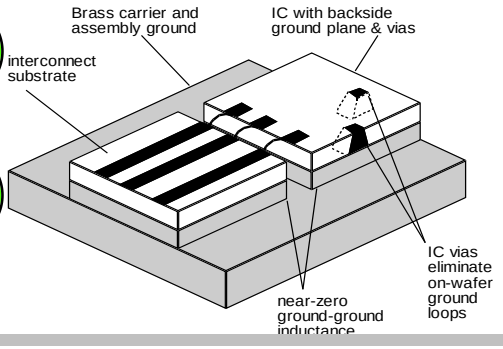
Thick Substrate → low skin loss



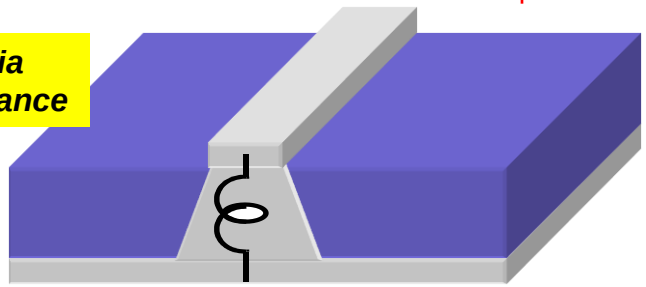
$$\alpha_{skin} \propto \frac{1}{\varepsilon_r^{1/2} H}$$

Zero ground inductance in package

No ground plane breaks in IC

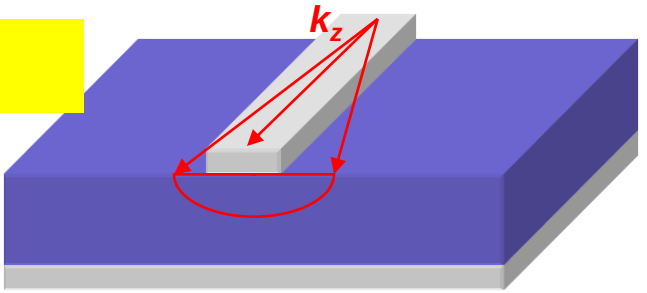


High via inductance



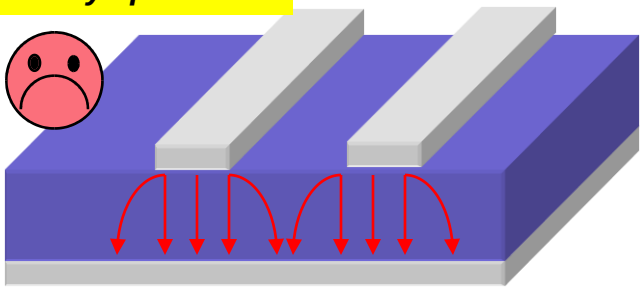
12 pH for 100 μm substrate -- 7.5 Ω @ 100 GHz

TM substrate mode coupling



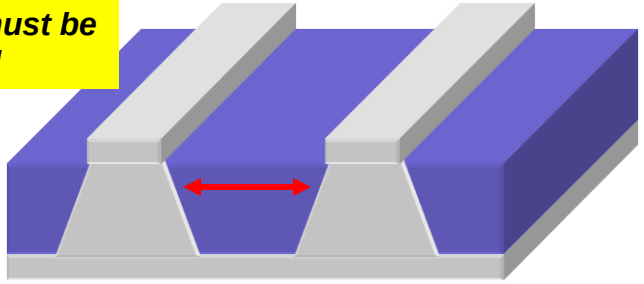
Strong coupling when substrate approaches ~λ_d / 4 thickness

lines must be widely spaced



Line spacings must be ~3(substrate thickness)*

ground vias must be widely spaced

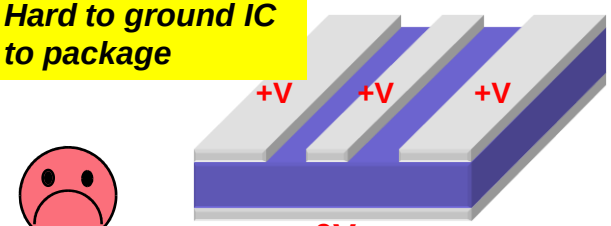


all factors require very thin substrates for >100 GHz ICs
→ lapping to ~50 μm substrate thickness typical for 100+ GHz

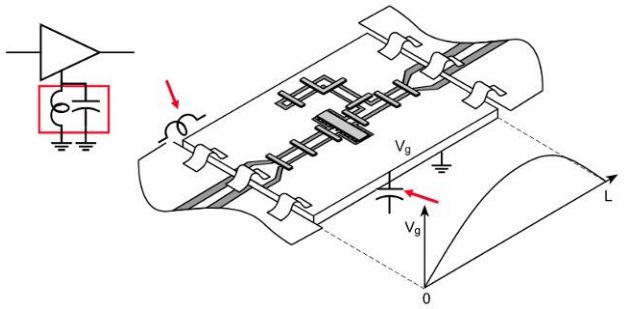
Coplanar Waveguide

No ground vias
No need (???) to thin substrate

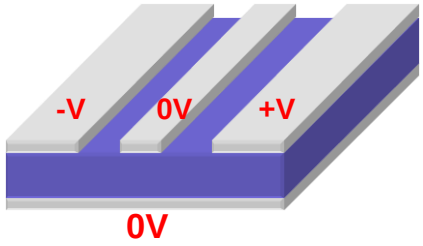
Hard to ground IC to package



Parasitic microstrip mode

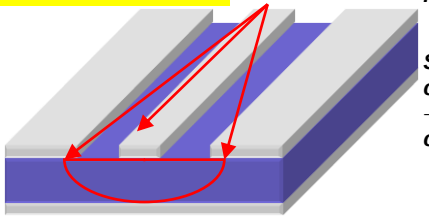


ground plane breaks → loss of ground integrity



Parasitic slot mode

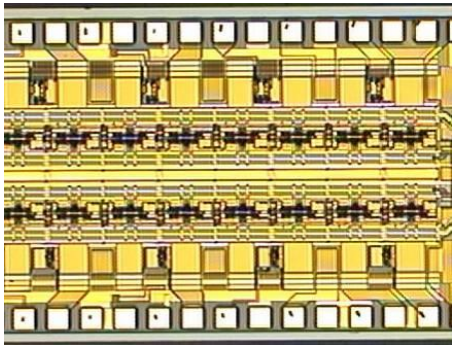
substrate mode coupling or substrate losses



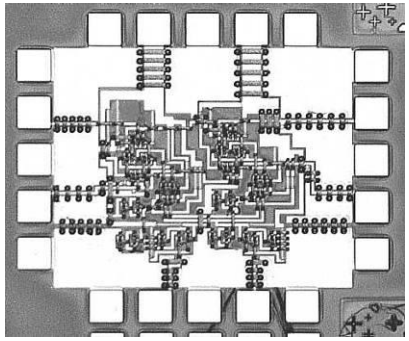
III-V: semi-insulating substrate→ substrate mode coupling

Silicon conducting substrate → substrate conductivity losses

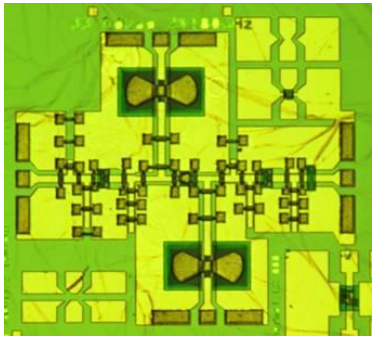
Repairing ground plane with ground straps is effective only in simple ICs
In more complex CPW ICs, ground plane rapidly vanishes
→ common-lead inductance → strong circuit-circuit coupling



40 Gb/s differential TWA modulator driver
note CPW lines, fragmented ground plane



35 GHz master-slave latch in CPW
note fragmented ground plane



175 GHz tuned amplifier in CPW
note fragmented ground plane

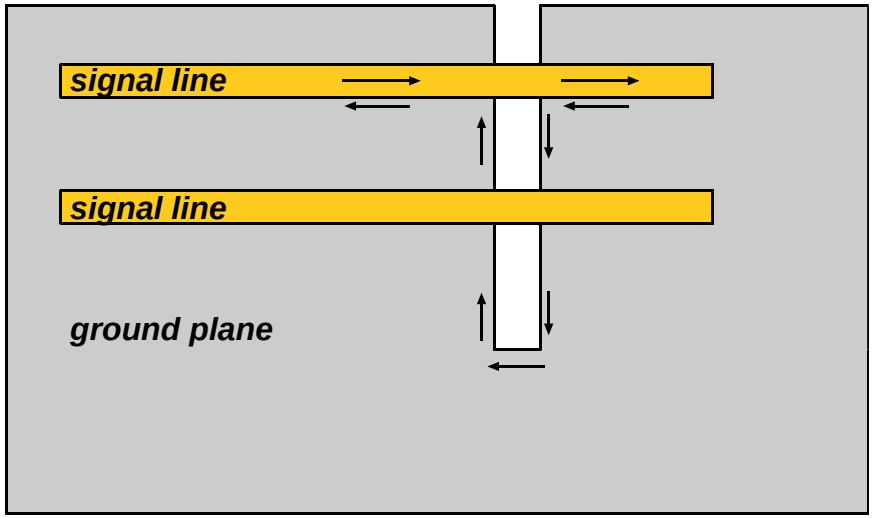
poor ground integrity

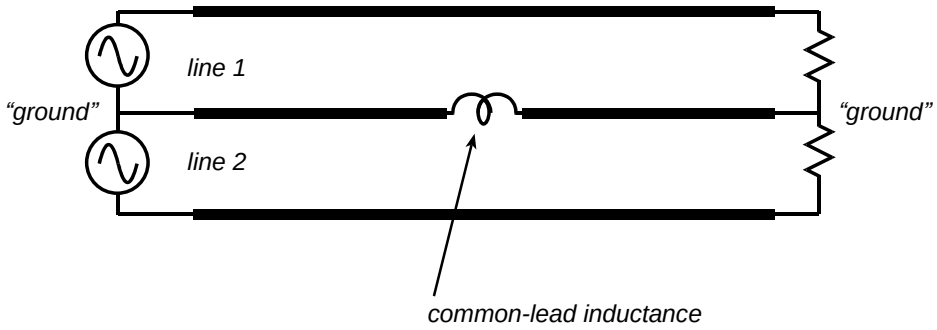
loss of impedance control

ground bounce

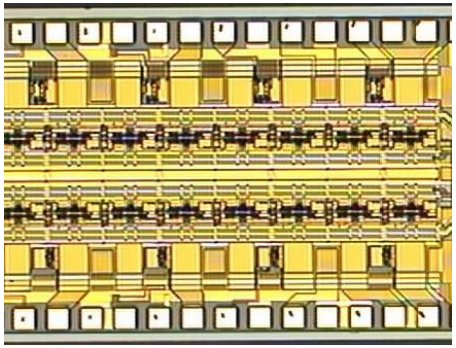
coupling, EMI, oscillation

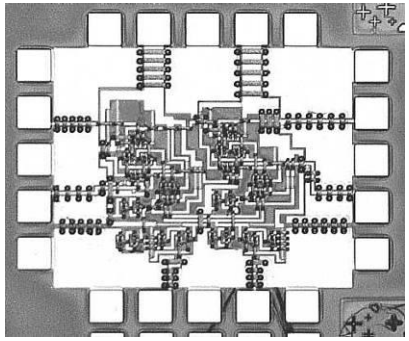
If It Has Breaks, It Is Not A Ground Plane !

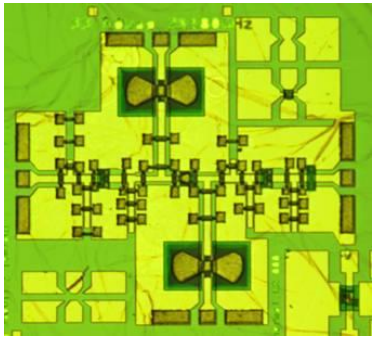




coupling / EMI due to poor ground system integrity is common in high-frequency systems
whether on PC boards
...or on ICs.







III-V MIMIC Interconnects -- Thin-Film Microstrip

narrow line spacing → IC density

no substrate radiation, no substrate losses

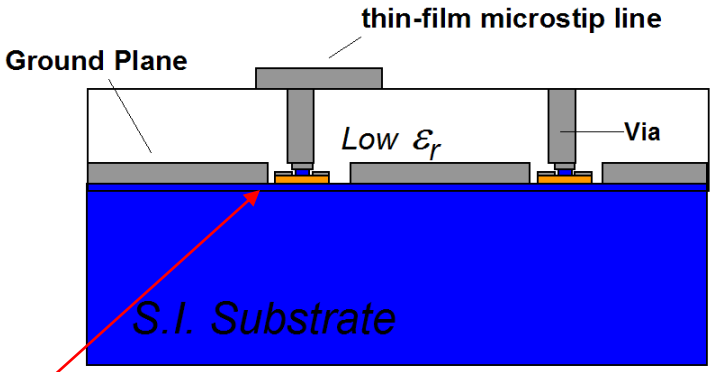
fewer breaks in ground plane than CPW

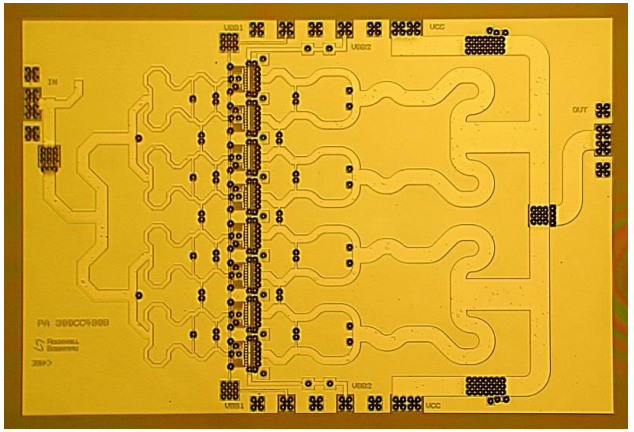
... but ground breaks at device placements

still have problem with package grounding

...need to flip-chip bond

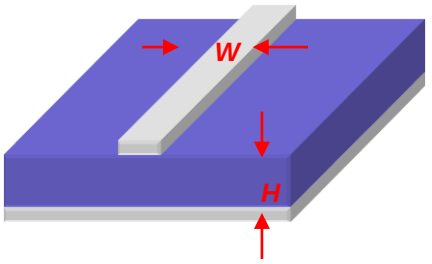
thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines





InP 34 GHz PA
(Jon Hacker , Teledyne)

$$Z_o \sim \frac{\eta_o}{\varepsilon_r^{1/2}}\left(\frac{H}{W+H}\right)$$



III-V MIMIC Interconnects -- Inverted Thin-Film Microstrip

narrow line spacing → IC density

Some substrate radiation / substrate losses

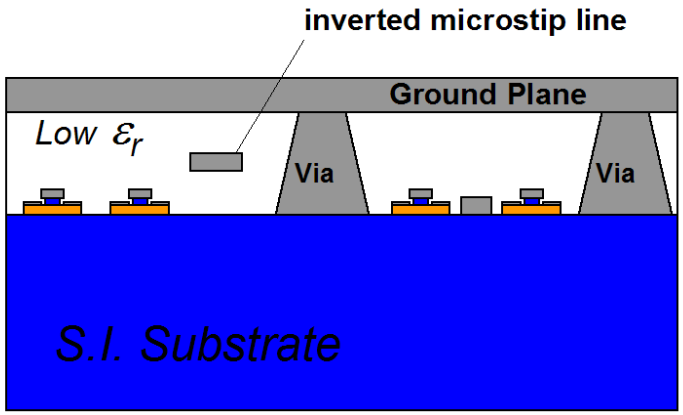
No breaks in ground plane

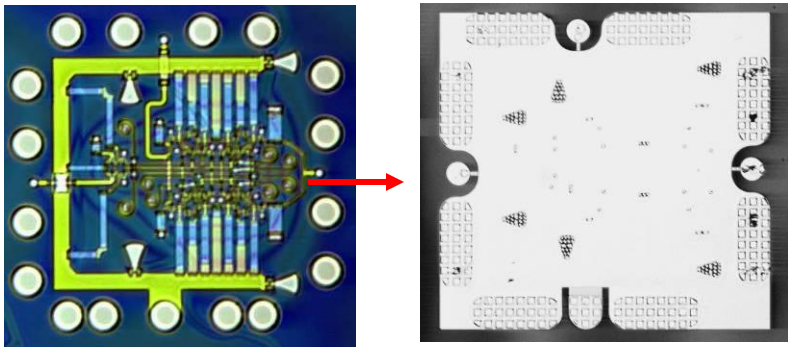
... no ground breaks at device placements

still have problem with package grounding

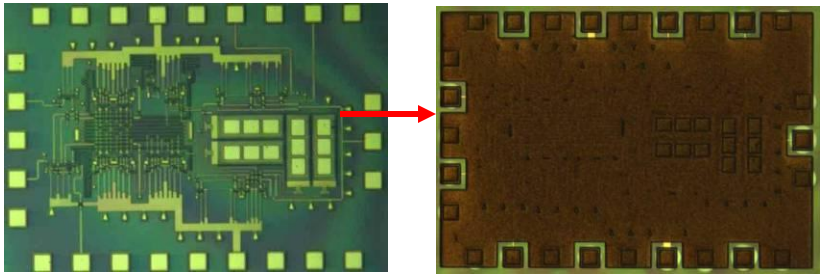
...need to flip-chip bond

thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines





InP 150 GHz master-slave latch



InP 8 GHz clock rate delta-sigma ADC

VLSI mm-wave interconnects with ground integrity

narrow line spacing → IC density

no substrate radiation, no substrate losses

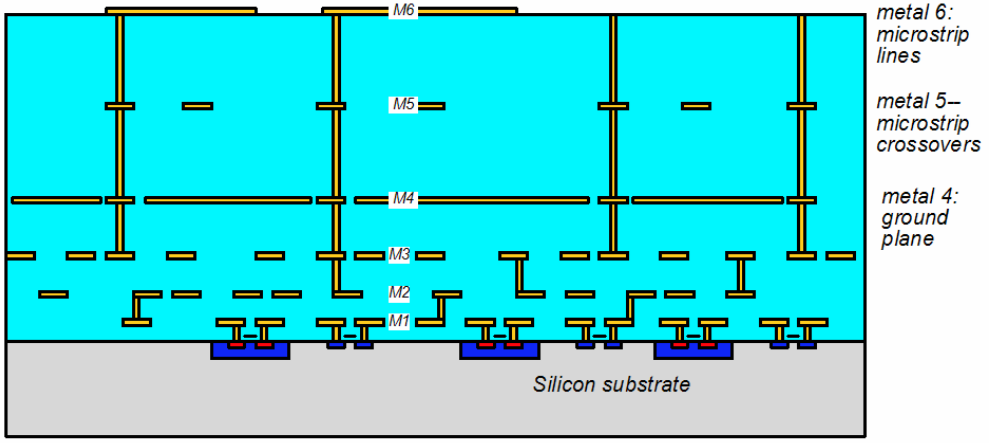
negligible breaks in ground plane

negligible ground breaks @ device placements

still have problem with package grounding

...need to flip-chip bond

thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines



Also:
Ground plane at *intermediate level* permits critical signal paths to cross supply lines, or other interconnects without coupling.
(critical signal line is placed above ground, other lines and supplies are placed below ground)

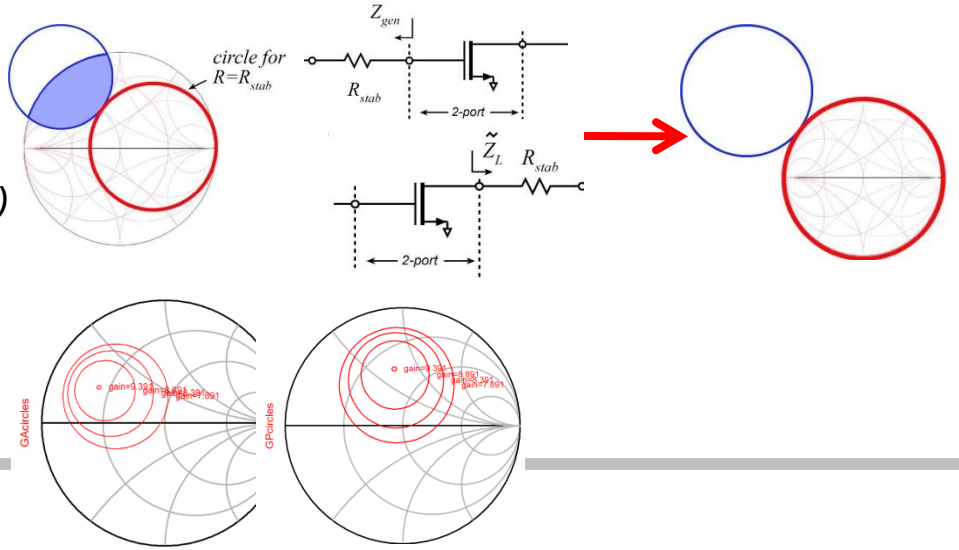
RF-IC Design: Simple & Well-Known Procedures

1: (over)stabilize at the design frequency
guided by stability circles

2: Tune input for F_{min} (LNAs) or output for P_{sat} (PAs)

3: Tune remaining port for maximum gain

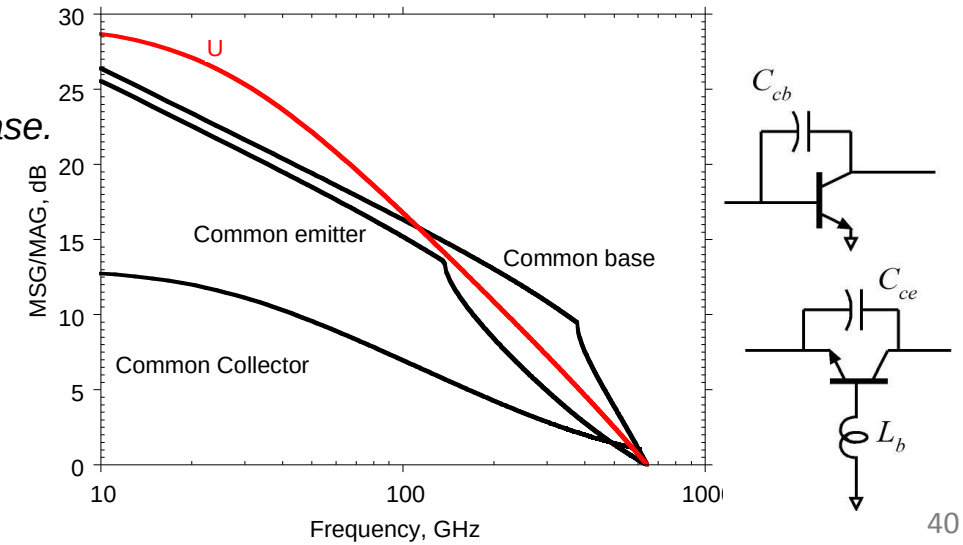
4: Add out-of-band stabilization.



There are many ways to tune port impedances: microstrip lines, MIM capacitors, transformers
Choice guided by tuning losses. No particular preferences.

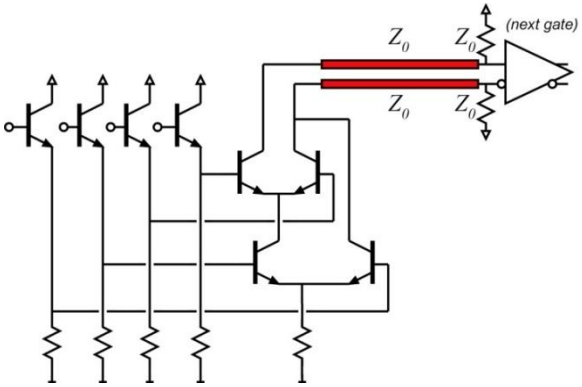
For BJT's, MAG/MSG usually highest for common-base.
→ preferred topology.

Common-base gain is however reduced by:
base (layout) inductance
emitter-collector layout capacitance.

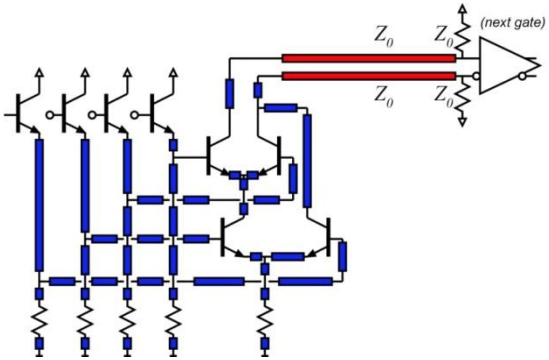


Modeling Interconnects: Digital & Mixed-Signal IC's

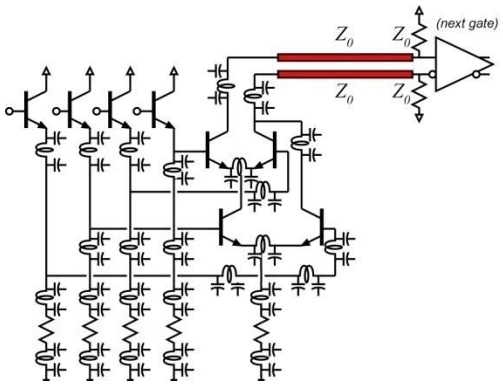
longer interconnects:
lines terminated in Zo → no reflections.



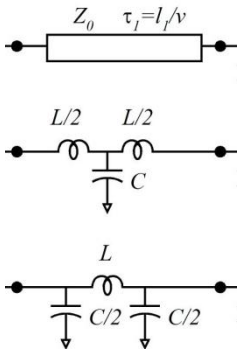
Shorter interconnects:
lines NOT terminated in Zo .
But they are *still* transmission-lines.
Ignore their effect at your peril !



If length << wavelength,
or line delay<<risetime,
short interconnects behave
as lumped L and C.

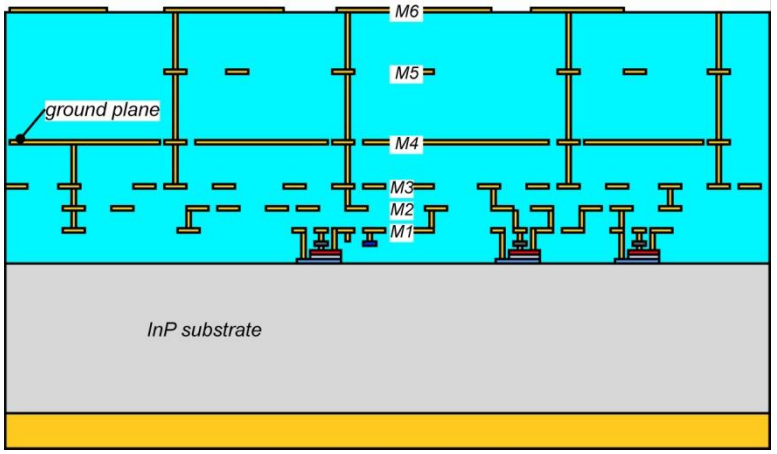


$$L = Z_0 \tau\,,$$
$$C = \tau / Z_0,$$
$$\tau = l / v$$



Design Flow: Digital & Mixed-Signal IC's

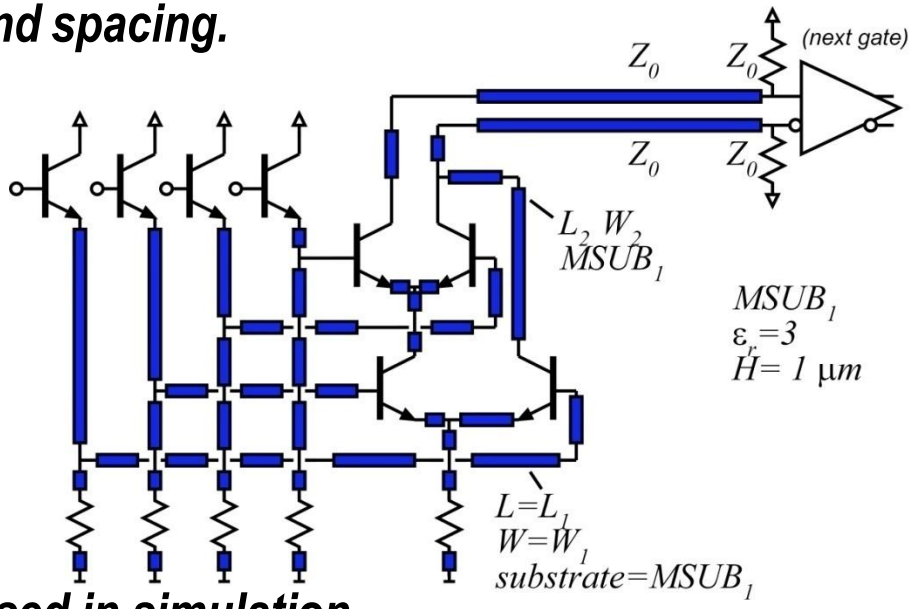
All interconnects: thin-film microstrip environment.
<u>Continuous</u> ground on one plane.



2.5-D simulations run on representative lines.
various widths, various planes
same reference (ground) plane.

Simulation data manually fit to CAD line model
effective substrate ε_r, effective line-ground spacing.

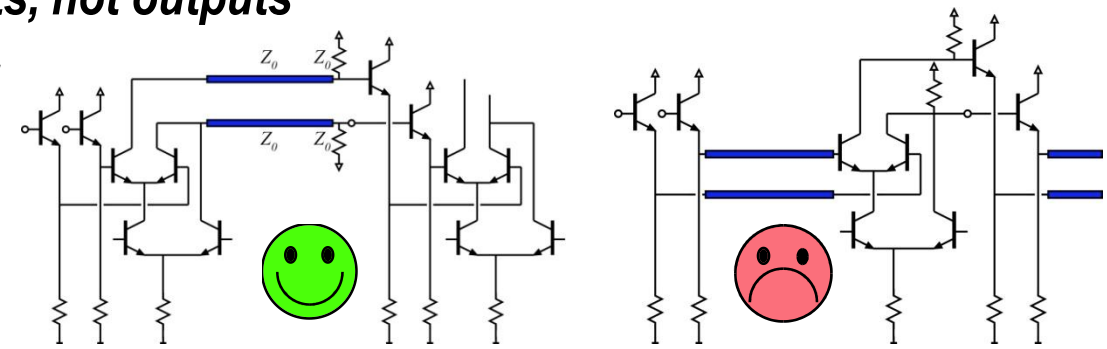
Width, length, substrate of each line entered on CAD schematic.
rapid data entry, rapid simulation.



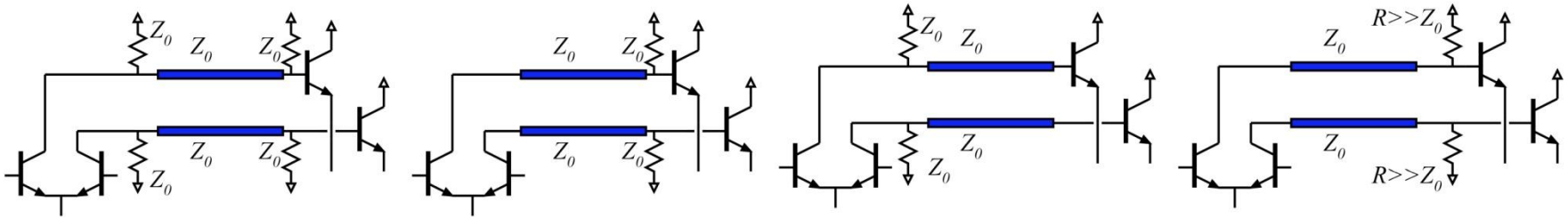
Resistors and capacitors:
2.5-D simulation→ RLC fit
RLC model ---or simulation S-parameters --used in simulation.

High Speed ECL Design

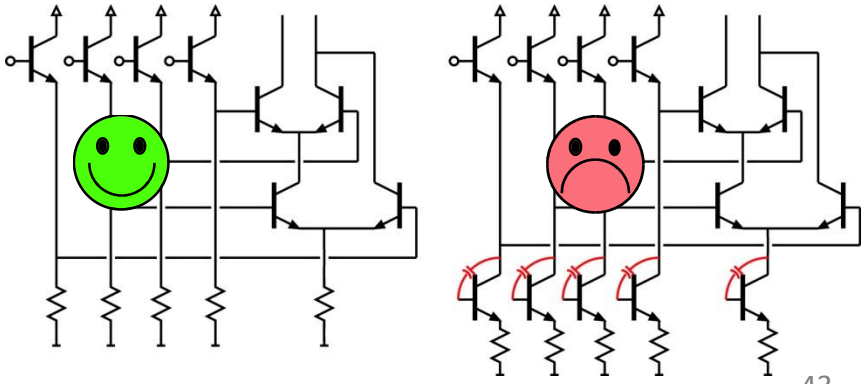
Followers associated with inputs, not outputs
Emitters never drive long wires.
(instability with capacitive load)



Double termination for least ringing, send or receive termination for moderate-length lines, high-Z loading saves power but kills speed.



Current mirror biasing is more compact.
Mirror capacitance→ ringing, instability.
Resistors provide follower damping.

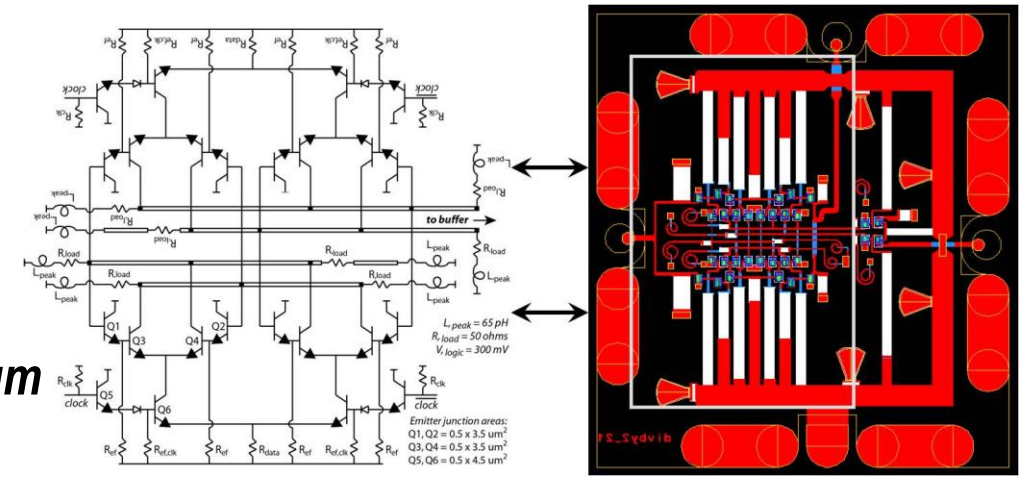


High Speed ECL Design

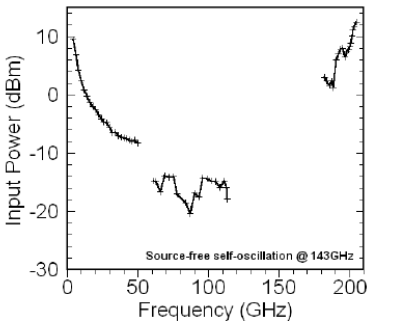
Layout: short signal paths at gate centers, bias sources surround core. Inverted thin film microstrip wiring.

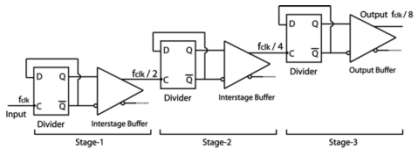
Key: transistors in on-state operate at Kirk limited-current. → minimizes C_{cb}/I_c delay.

Key: transistors designed for minimum ECL gate delay*, not peak (f_τ, f_{max}).
**hand expression, charge-control analysis*

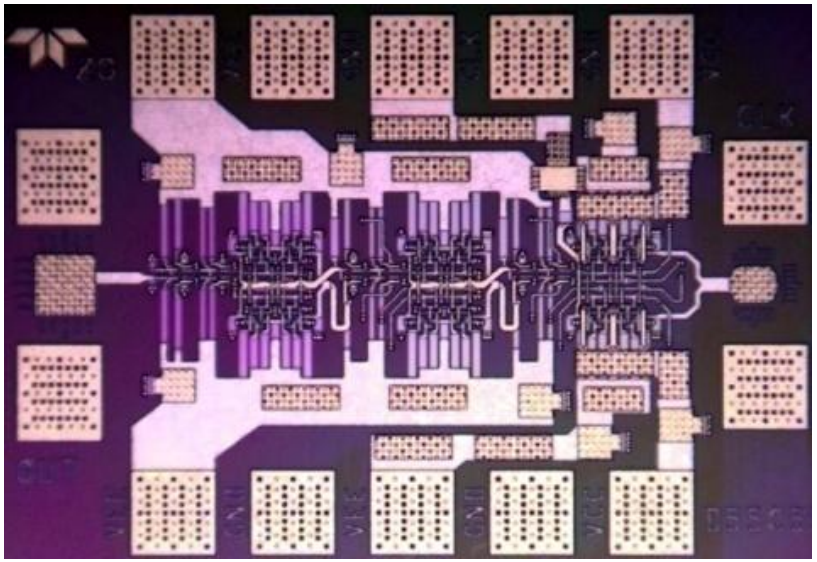


Example: 8:1 205 GHz static divider in 256 nm InP HBT.

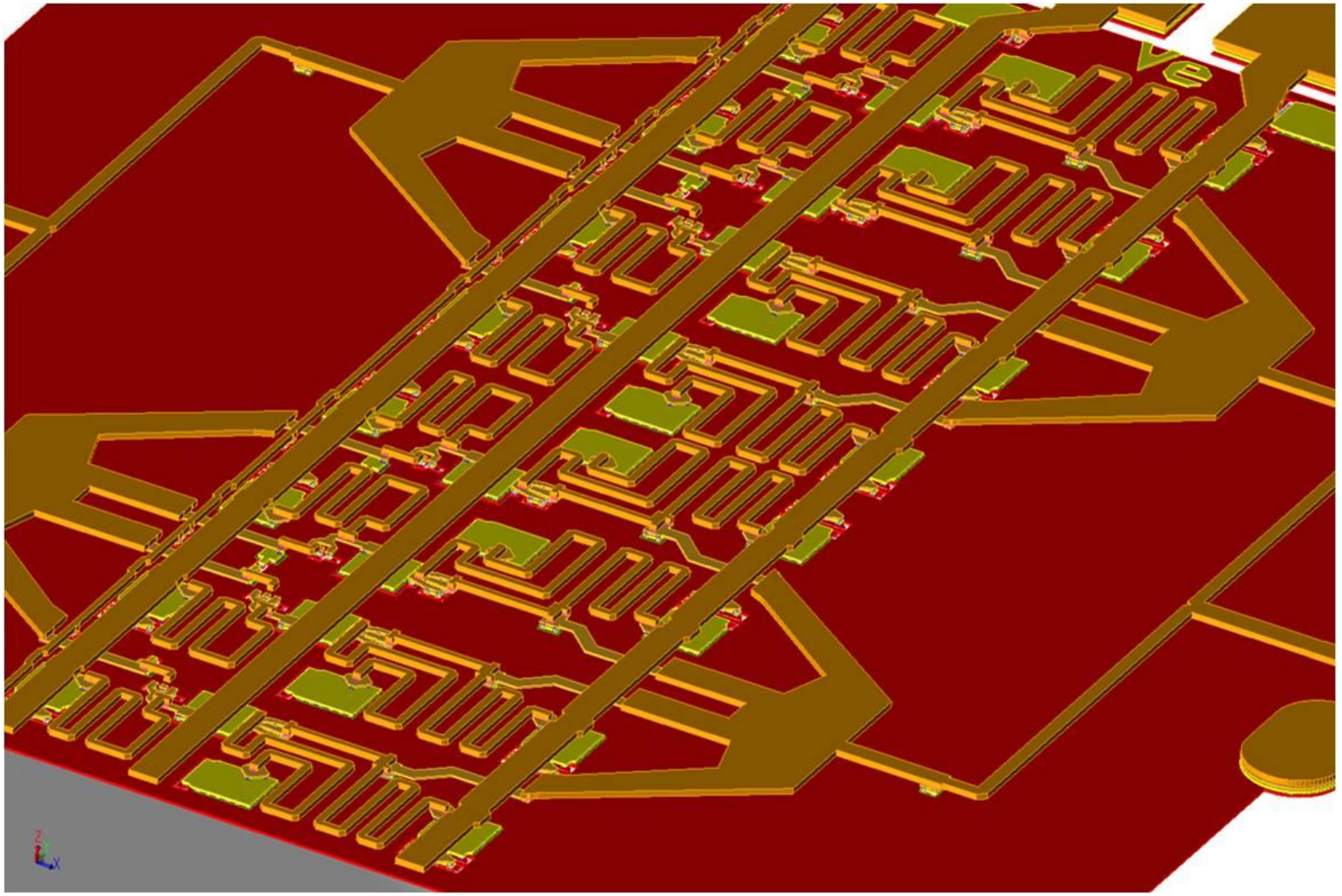




205 GHz divider, Griffith et al, IEEE CSIC, Oct. 2010

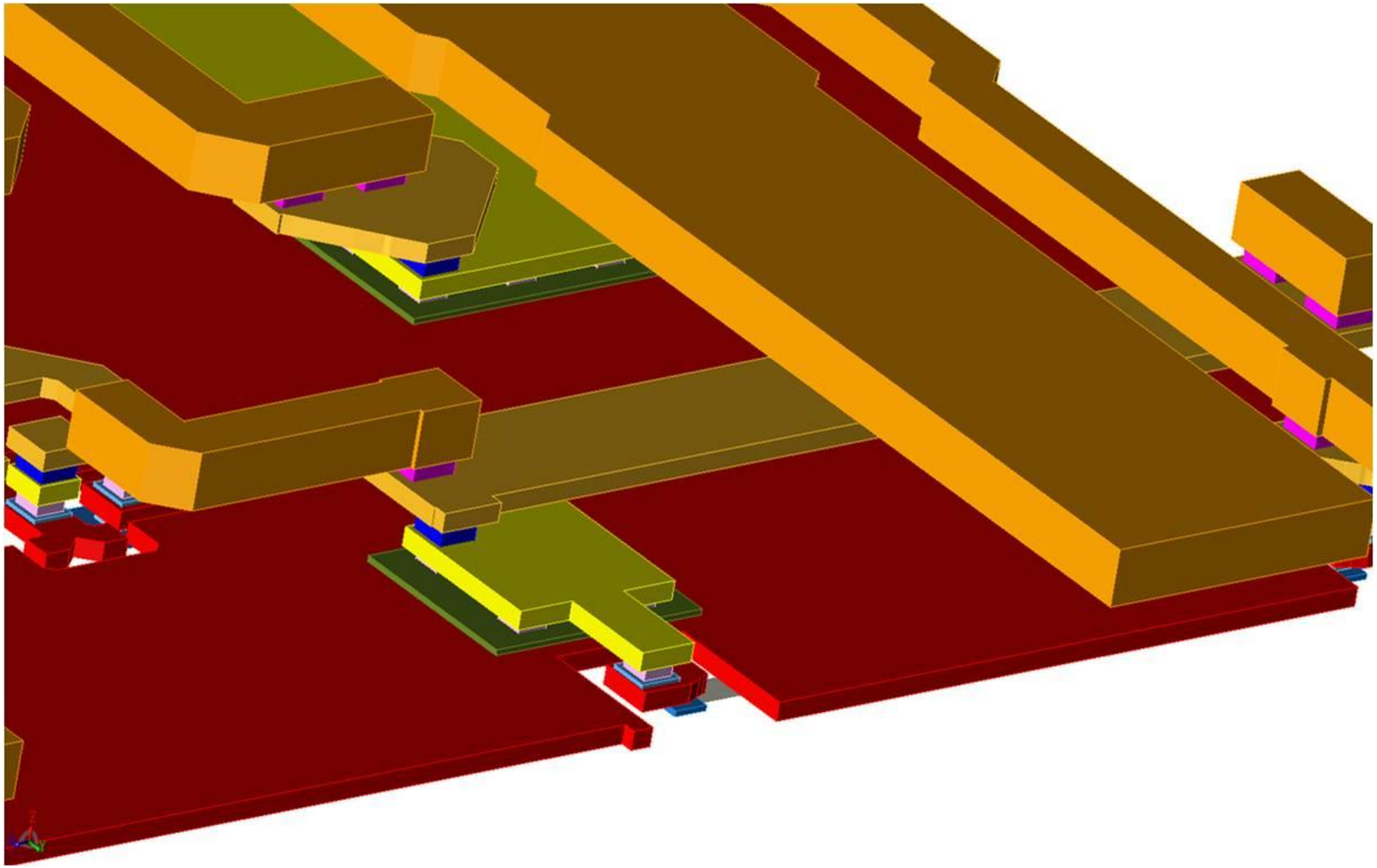


ICs in Thin-Film (Not Inverted) Microstrip



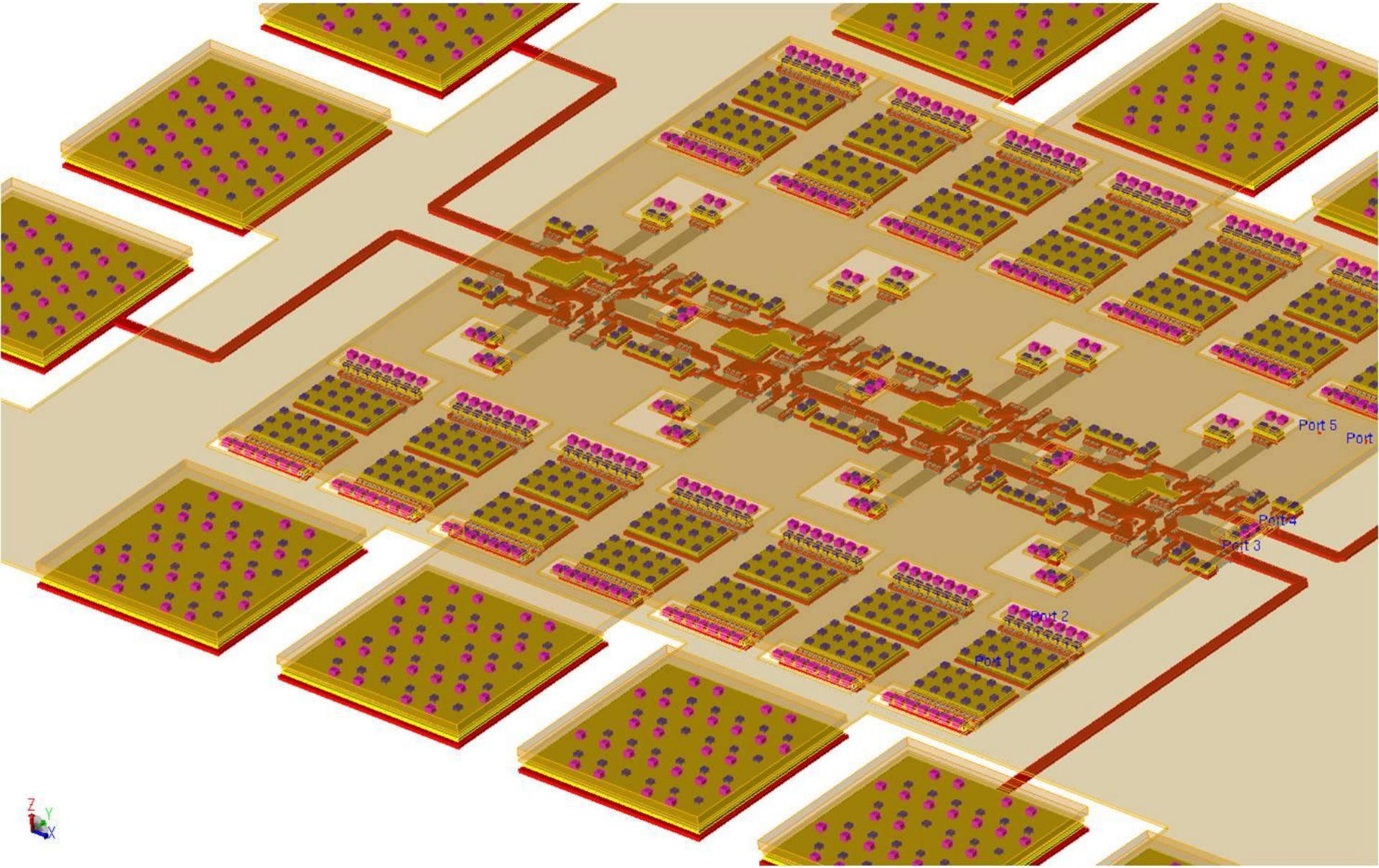
Note breaks in ground plane at transistors, resistors, capacitors

ICs in Thin-Film (Not Inverted) Microstrip



Note breaks in ground plane at transistors, resistors, capacitors

ICs in Thin-Film Inverted Microstrip



100 GHz differential TASTIS Amp. 512nm InP HBT

High Frequency Bipolar IC Design

Digital, mixed-signal, RF-IC (tuned) IC designs----at very high frequencies

Even at 670 GHz, design procedures differ little from that at lower frequencies:

Classic IC design extends readily to the far-infrared.

<u>Key considerations: Tuned ("RF") ICs</u>
Rigorous E&M modeling of all interconnects & passive elements
Continuous ground plane → required for predicable interconnect models.
Higher frequencies→ close conductor planes→ higher loss, lower current

<u>Key considerations: digital & mixed-signal :</u>
Transmission-line modeling of <u>all</u> interconnects
Continuous ground plane → required for predicable interconnect models.
Unterminated lines within blocks; terminated lines interconnecting blocks.
Analog & digital blocks design to naturally interface to 50 or 75Ω.

Design Examples, IC Results

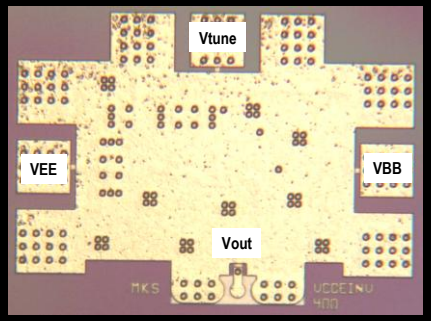
InP HBT Integrated Circuits: 600 GHz & Beyond

TELEDYNE SCIENTIFIC COMPANY
A Teledyne Technologies Company

UCSB

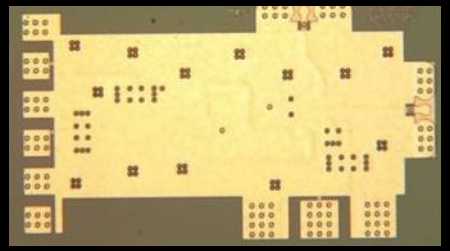
614 GHz fundamental VCO

M. Seo, TSC / UCSB



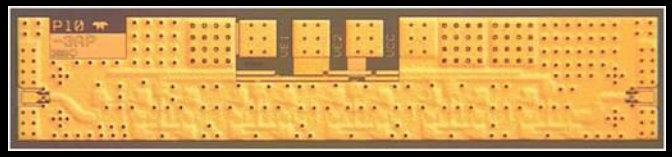
340 GHz dynamic frequency divider

M. Seo, UCSB/TSC
IMS 2010



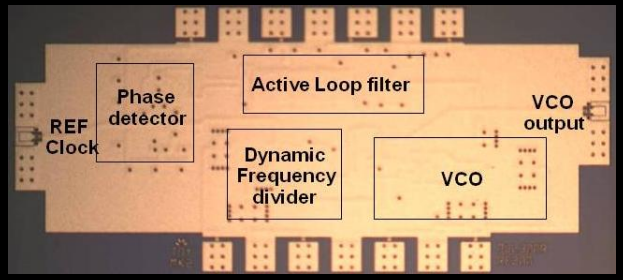
565 GHz, 34 dB, 0.4 mW output power amplifier

J. Hacker, TSC



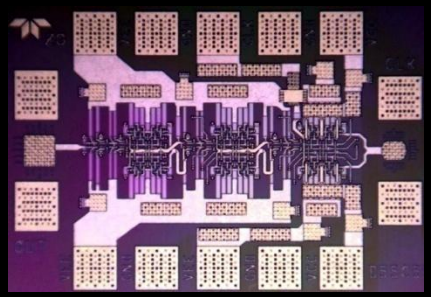
300 GHz fundamental PLL

M. Seo, TSC
IMS 2011



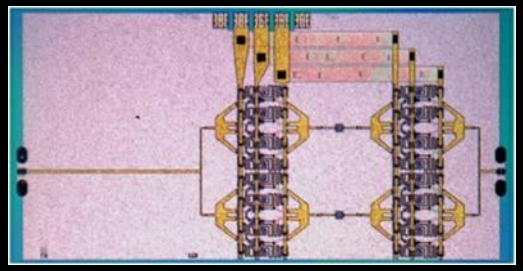
204 GHz static frequency divider (ECL master-slave latch)

Z. Griffith, TSC
CSIC 2010

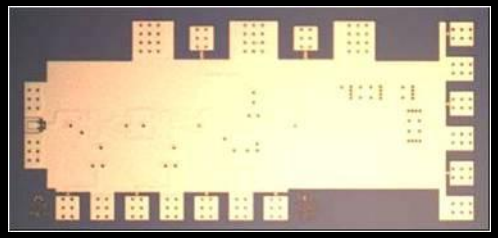


220 GHz 90 mW power amplifier

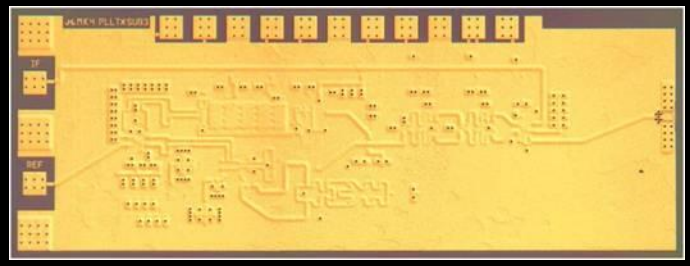
T. Reed, UCSB



Integrated 300/350GHz Receivers:
LNA/Mixer/VCO
M. Seo TSC

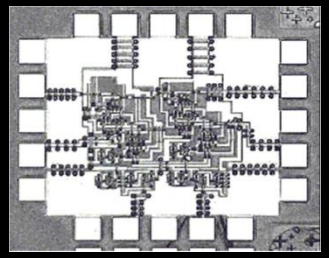


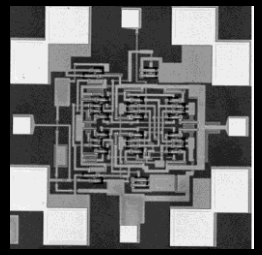
600 GHz Integrated Transmitter
PLL + Mixer
M. Seo TSC



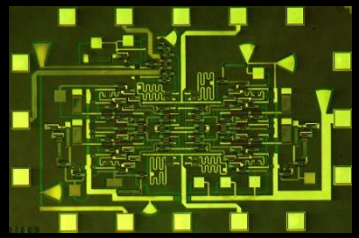
Digital Logic: 30 GHz to 204 GHz in 12 Years

1998: 30 GHz→ 48 GHz

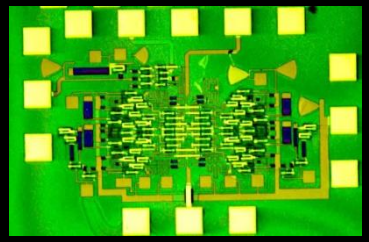




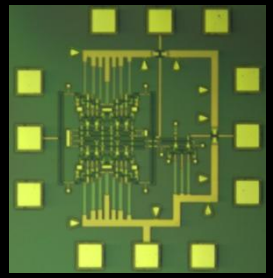
2000: 66 GHz



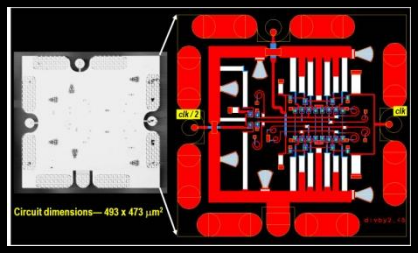
2001: 75GHz



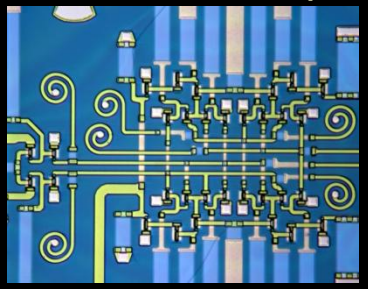
2002: 87GHz



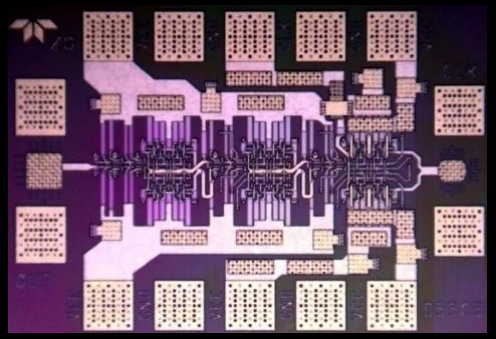
2004: 118 GHz



2004: 142 GHz, 150 GHz

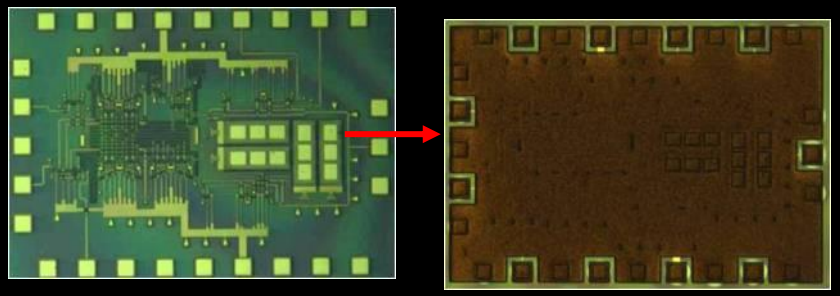


2010: 204 GHz (with Teledyne)

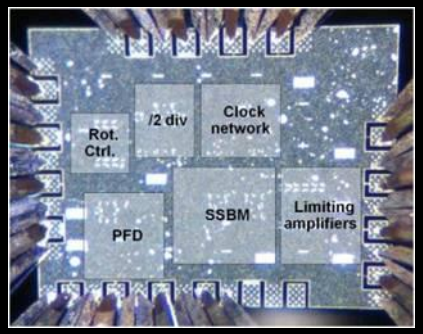


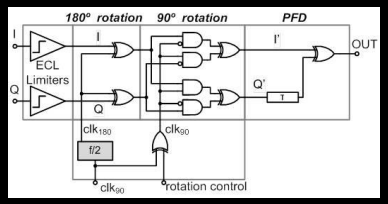
Other InP HBT ICs in Inverted Microstrip

Teledyne InP HBT
256 nm, 512 nm

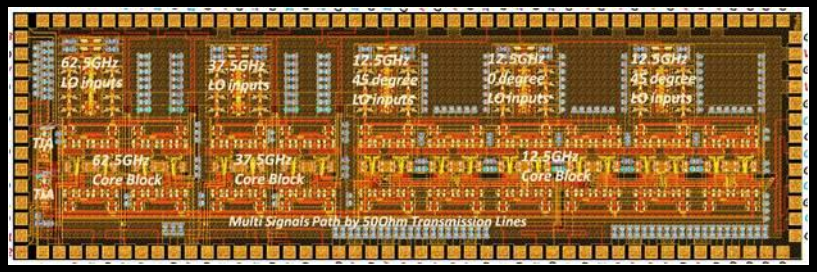


InP 8 GHz clock rate delta-sigma ADC
(Krishnan, IMS 2003)

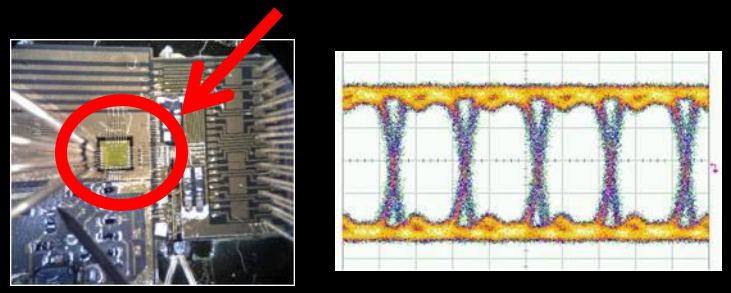




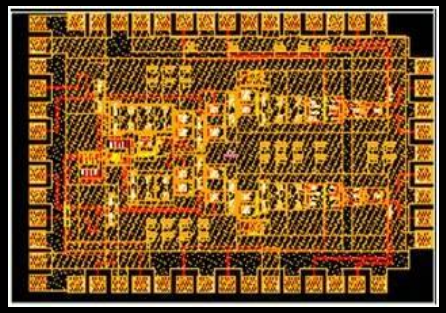
30 GHz digital SSB mixer / PFD for optical PLL
(Bloch, IMS 2012)



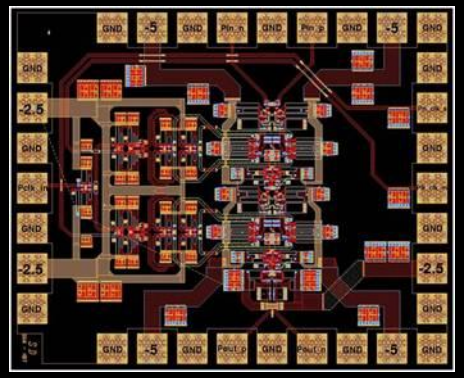
10 Gb/s x 6-channel (+/- 12.5, +/- 37.5, +/- 62.5 GHz)
WDM receiver IC for coherent optical links
(H. Park, being tested)



40 Gb/s coherent optically-phase-locked
BSPK optical receiver (Bloch, Park, ECOC 2012)

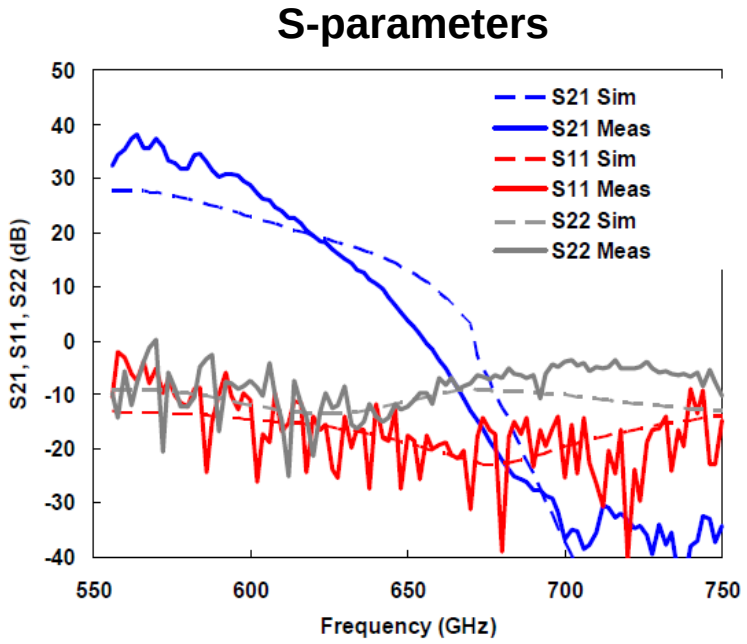


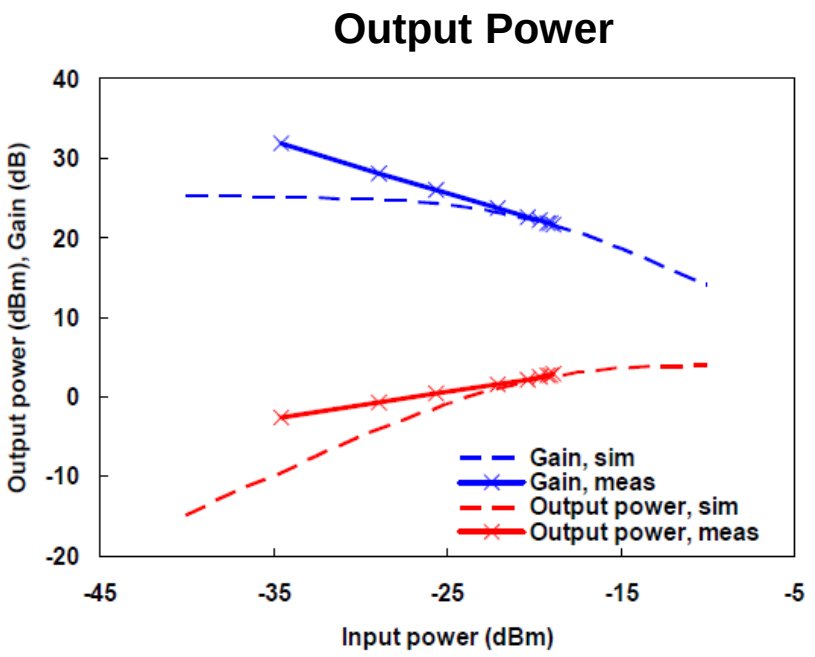
40 Gb/s coherent optically-phase-locked
QPSK optical receiver (E. Bloch, being tested)



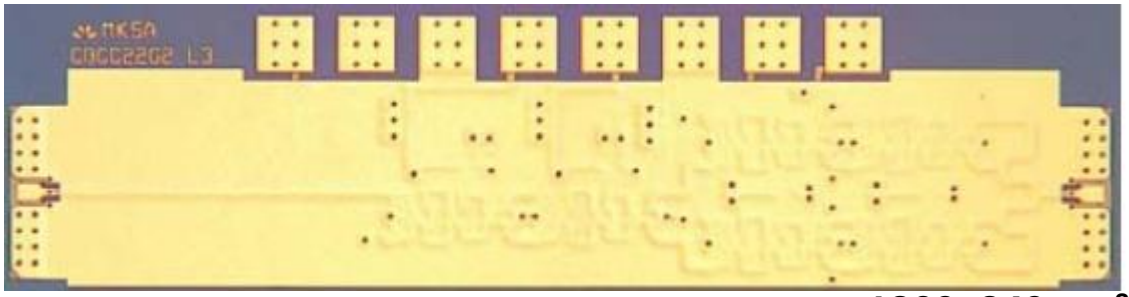
50 GS/s Track/hold and sample/hold amplifiers
Daneshgar, IEEE CSICS Oct. 2012

Teledyne: 600 GHz Common-Base Amplifier IC





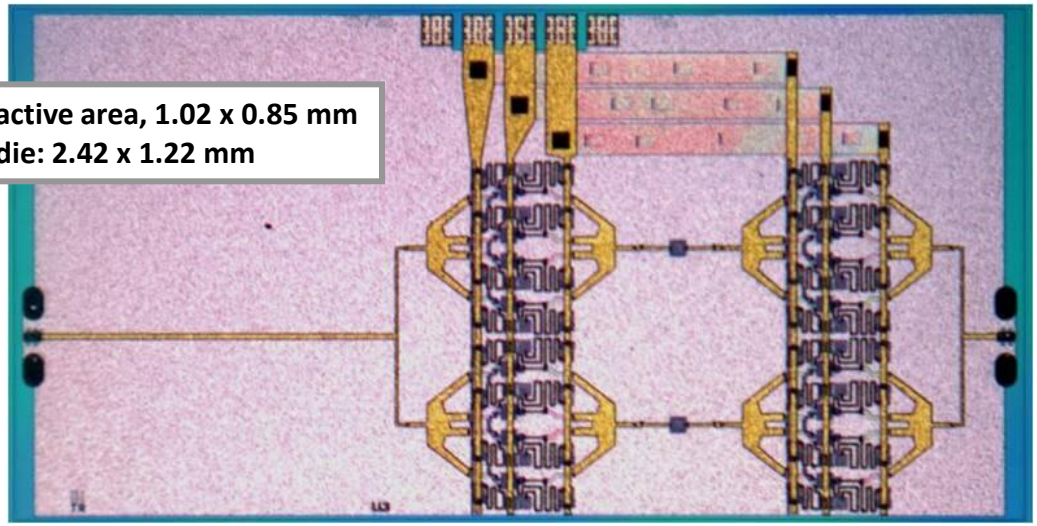
- 12-Stage Common-base using inverted CPW-G architecture
- 2.8 dBm saturated output power
- >20 dB gain up to 620 GHz



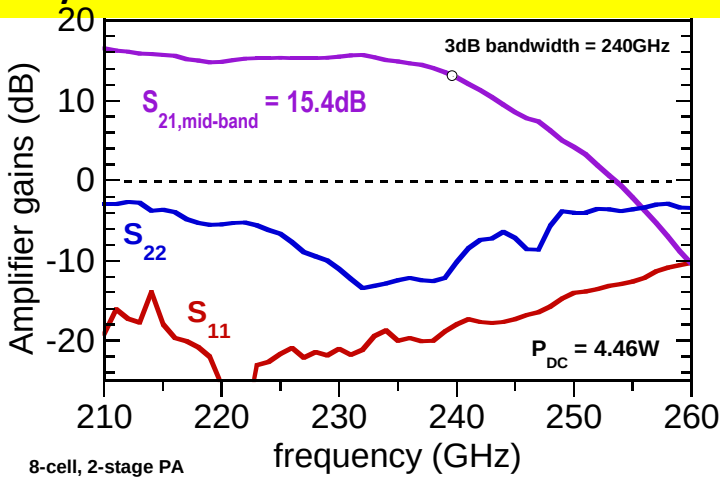
1360x340 μm²

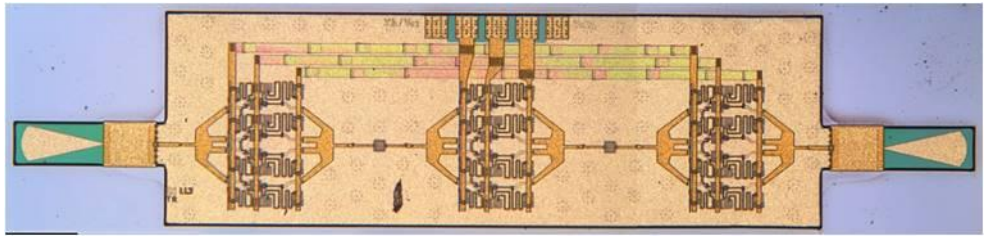
M. Seo *et al*, Teledyne Scientific: IMS2013

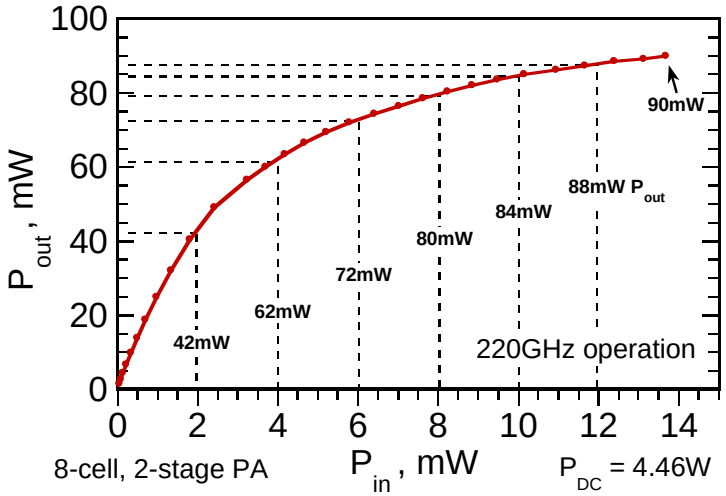
90 mW, 220 GHz Power Amplifier



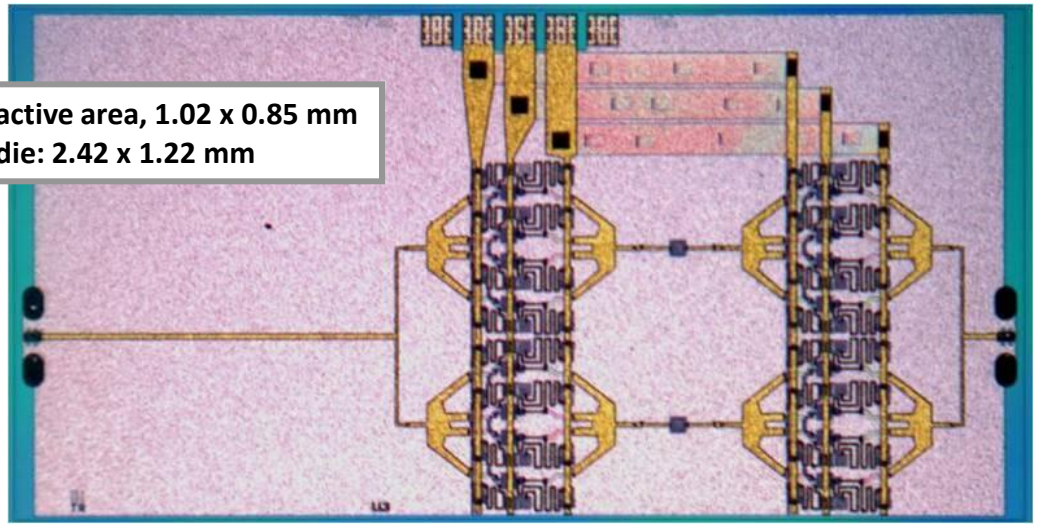
Reed (UCSB) and Griffith (Teledyne): CSIC 2012
Teledyne 250 nm InP HBT



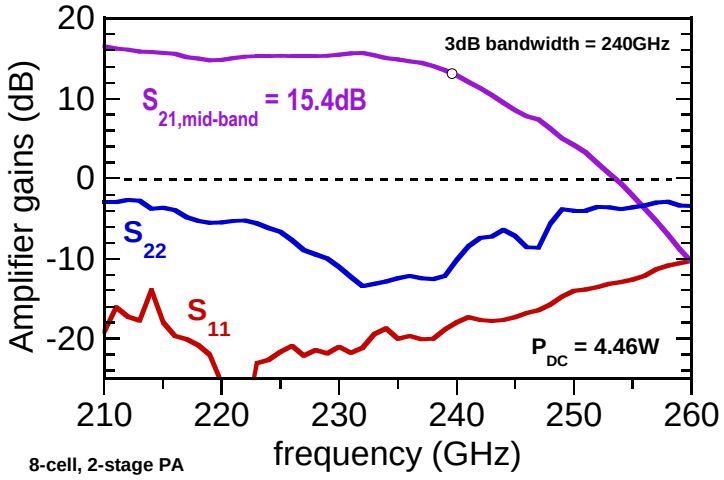




90 mW, 220 GHz Power Amplifier

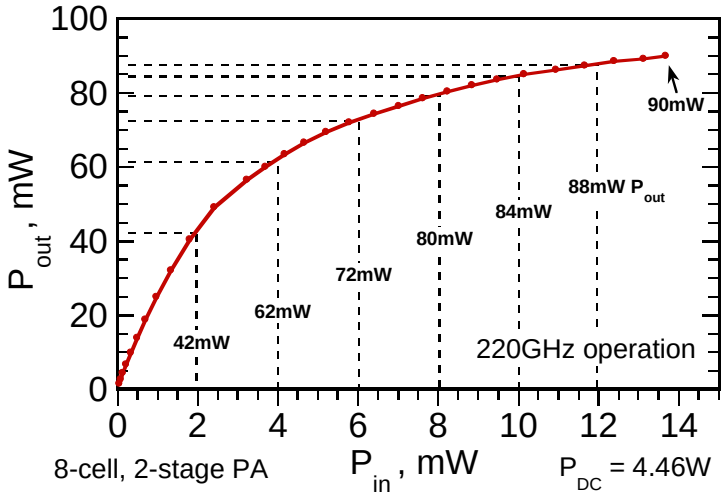


Reed (UCSB) and Griffith (Teledyne): CSIC 2012
Teledyne 250 nm InP HBT

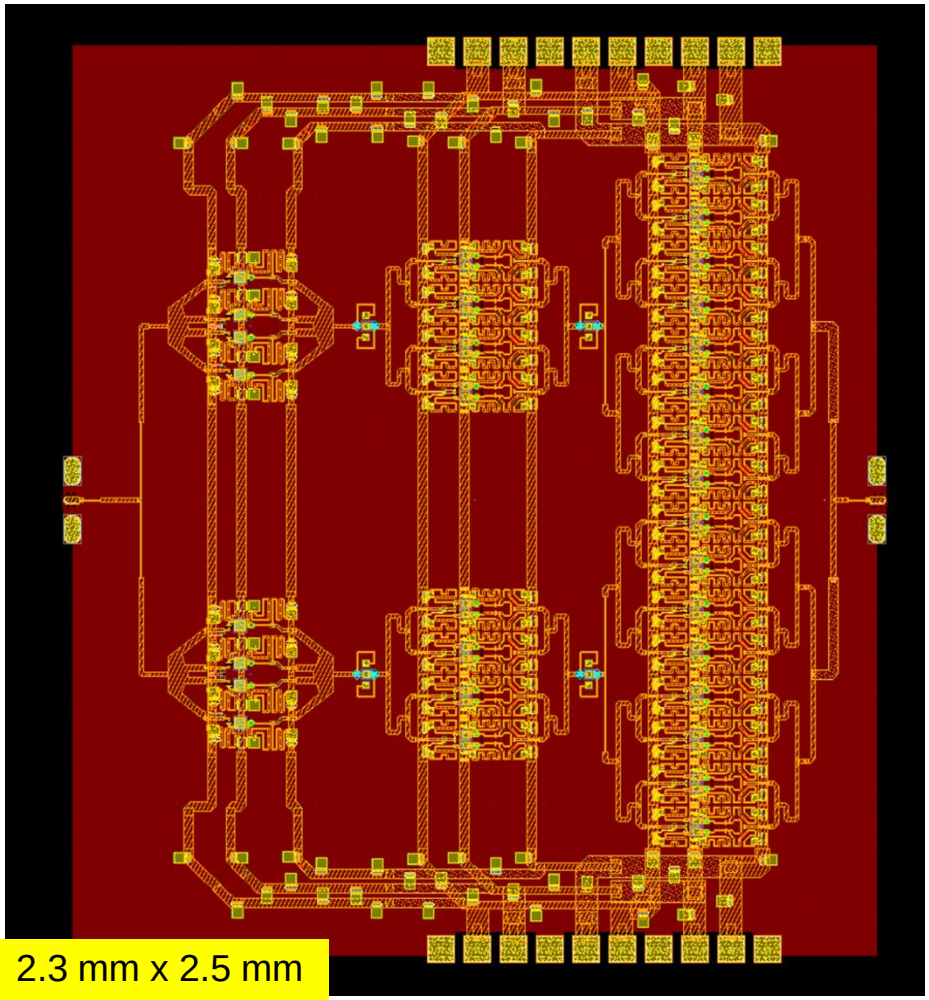


RF output power densities up to 0.5 W/mm @ 220 GHz.

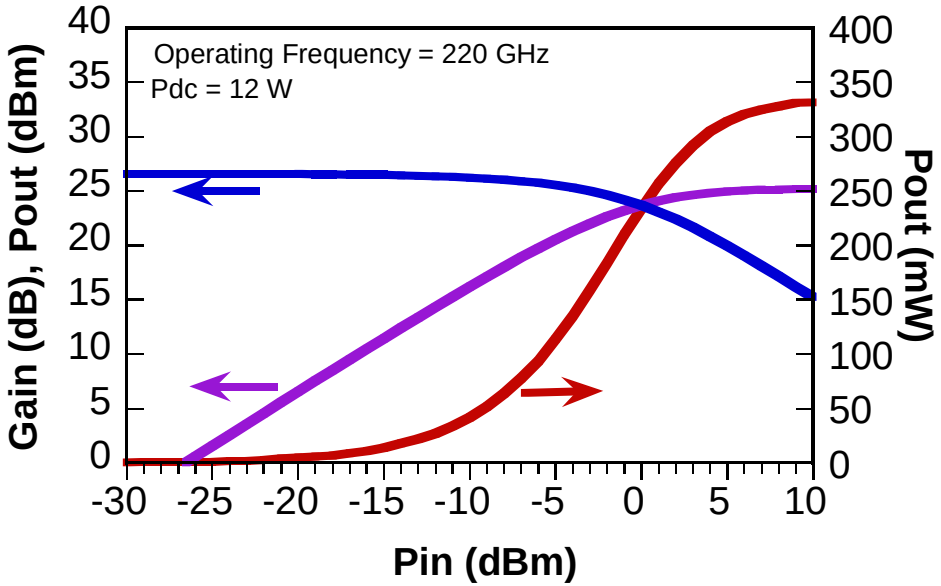
→ InP HBT is a competitive mm-wave / sub-mm-wave power technology.

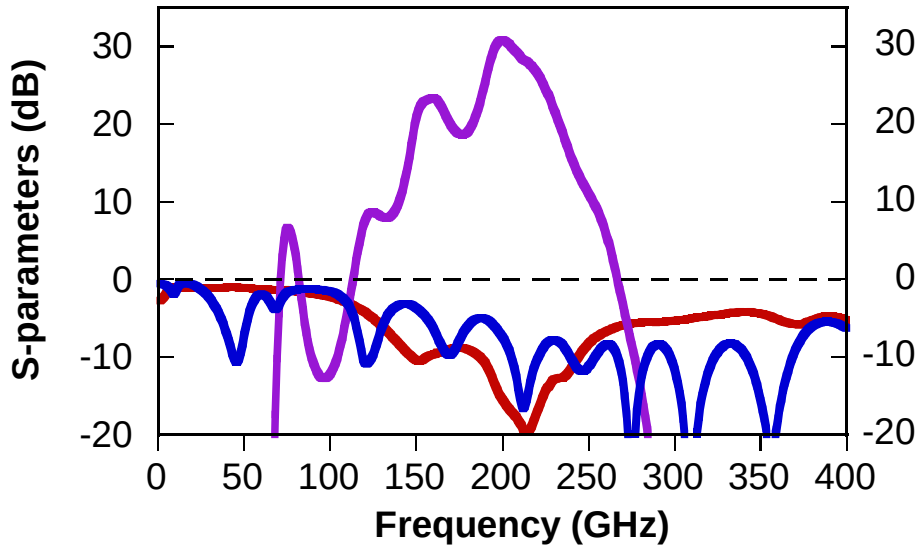


220 GHz 330mW Power Amplifier Design



2.3 mm x 2.5 mm





T. Reed, UCSB
Z. Griffith, Teledyne
Teledyne 250 nm InP HBT

84 GHz Power Amplifier Design #1: 250 nm InP HBT

Simulations:

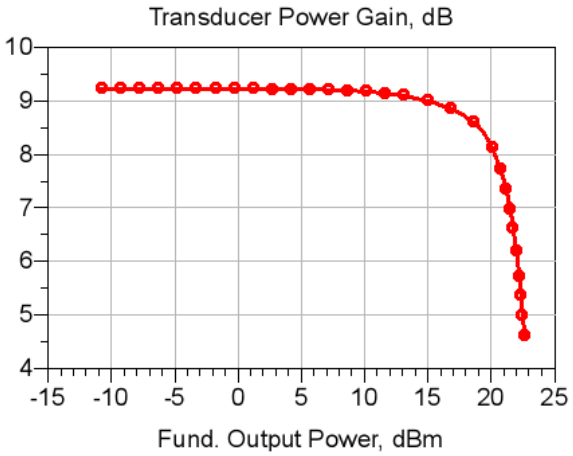
HBT: 16 fingers x 6um x 0.25um= 96 um x 0.25 um

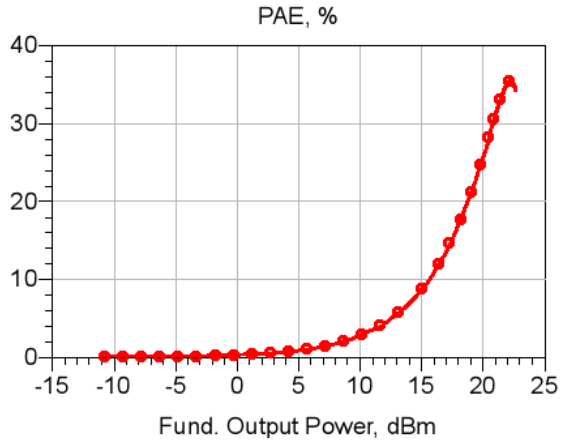
Gain: 9.2dB

PAE: 35%

P_{out}: 22.3 dBm (170 mW) → 1.75 W/mm

Chip size: 450 μm x 780 μm





84 GHz Power Amplifier Design #2: 250 nm InP HBT

Simulations:

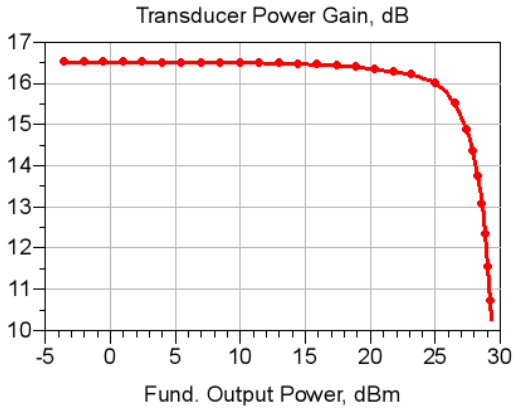
HBT: 96 fingers x 6um x 0.25um= 576 um x 0.25 um

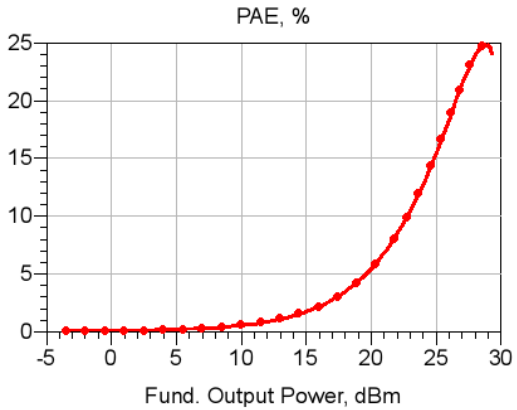
Gain: 16.5dB

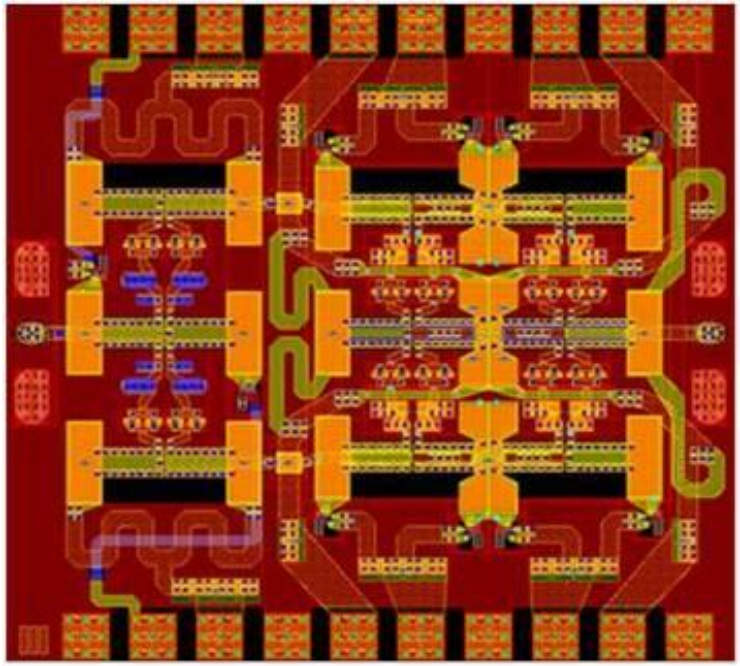
PAE: 24%

P_{out}: 28.8 dBm (760 mW) → 1.3 W/mm

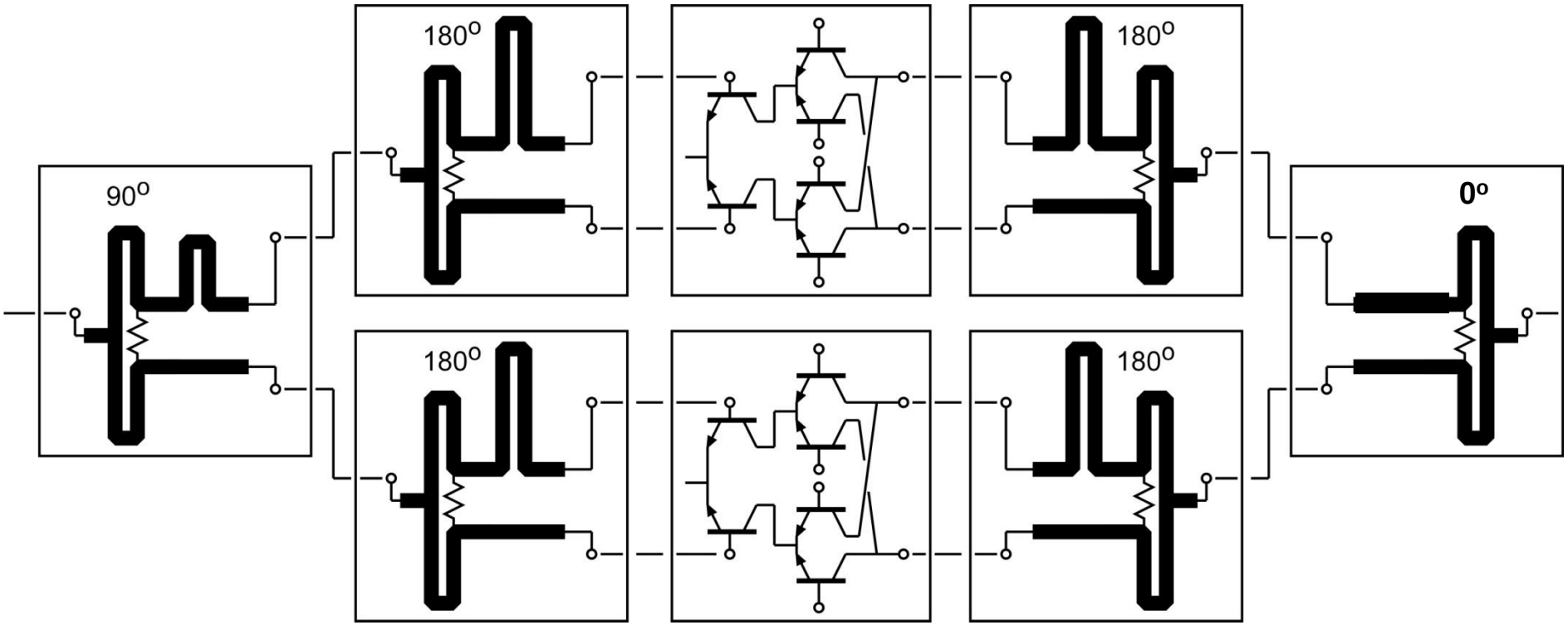
Chip size: 1100 μm x 980 μm



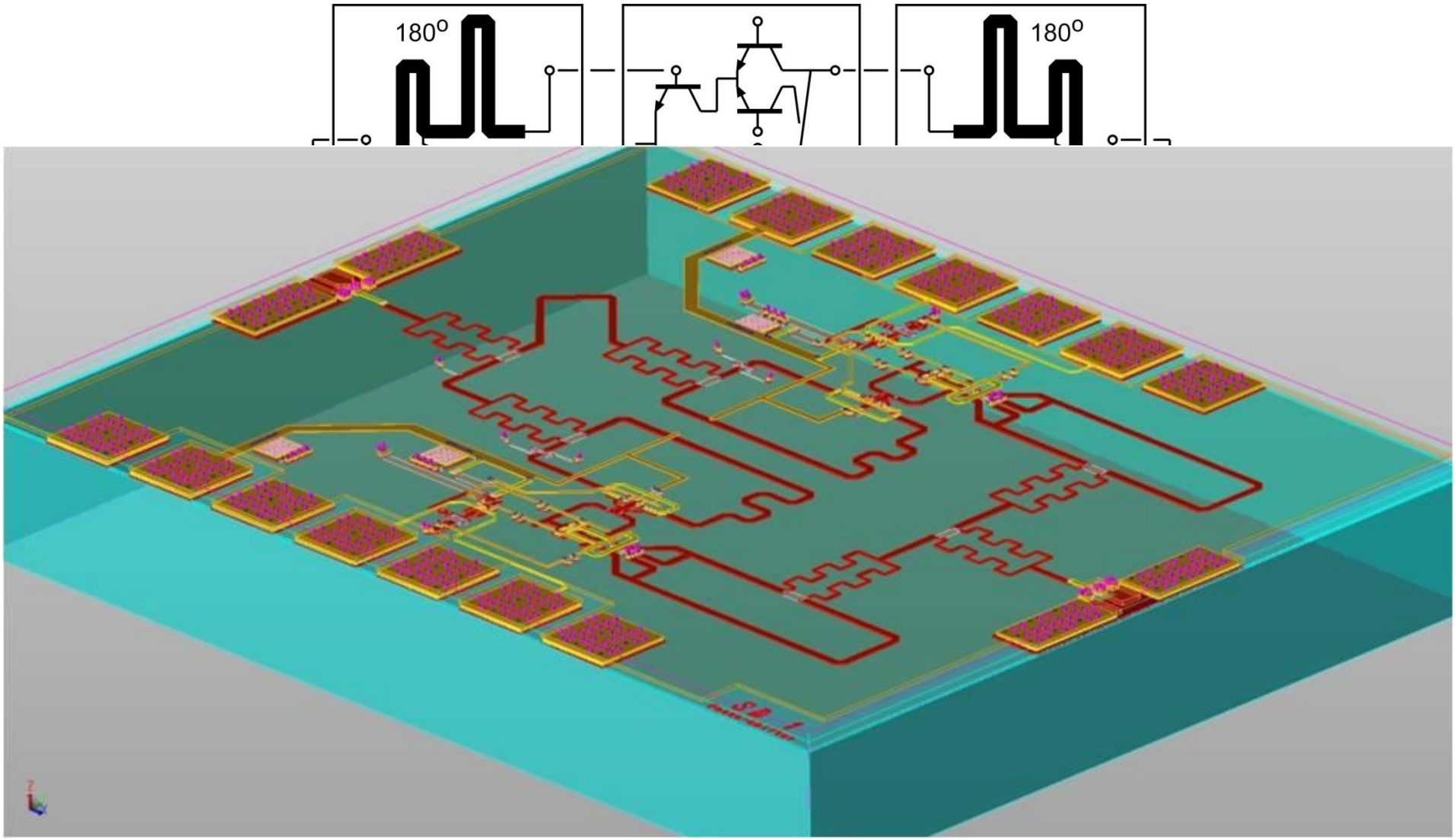




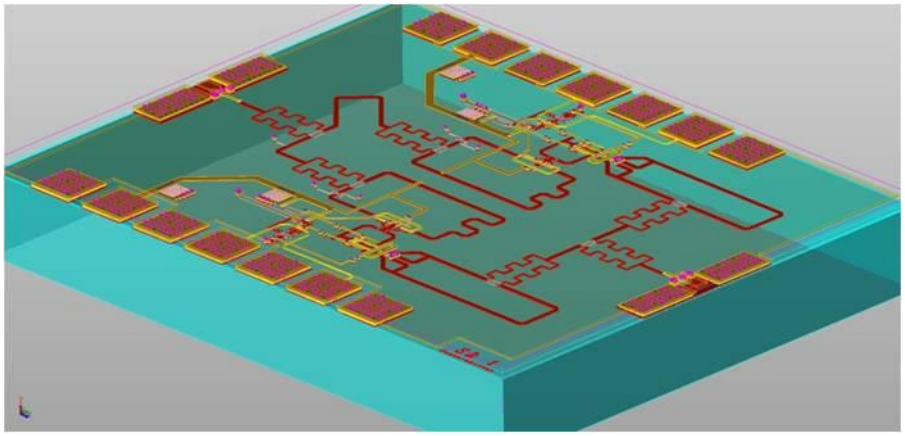
220 GHz Vector Modulator / Phase Shifter Design

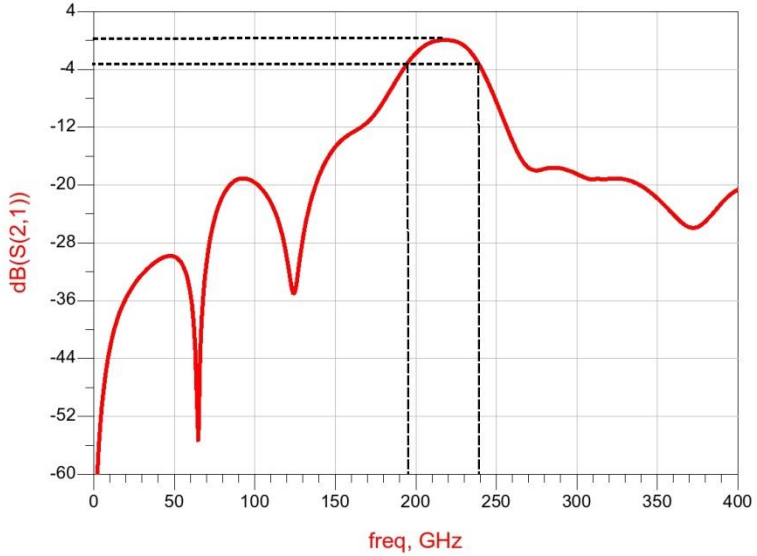


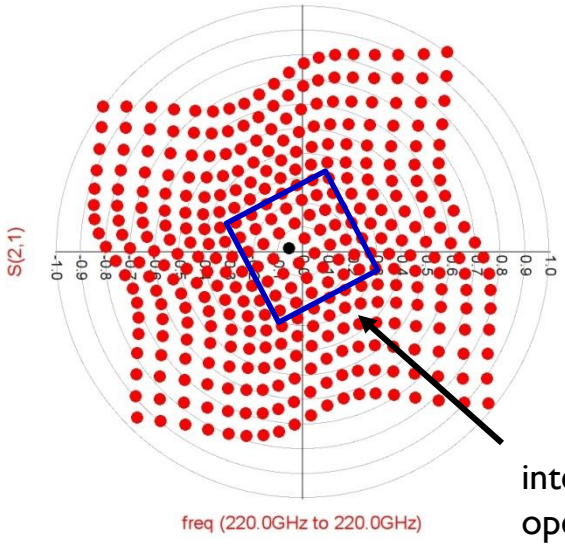
220 GHz Vector Modulator / Phase Shifter Design



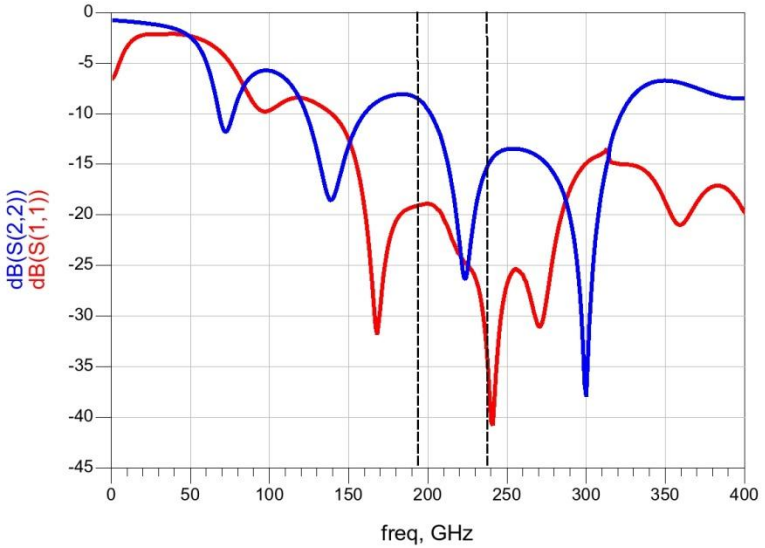
220 GHz Vector Modulator / Phase Shifter Design







intended
operating range



Technology: 256nm InP HBT
9/2012 tapeout; ICs expected 12/2012

THz Electronics for Terabit fiber optics

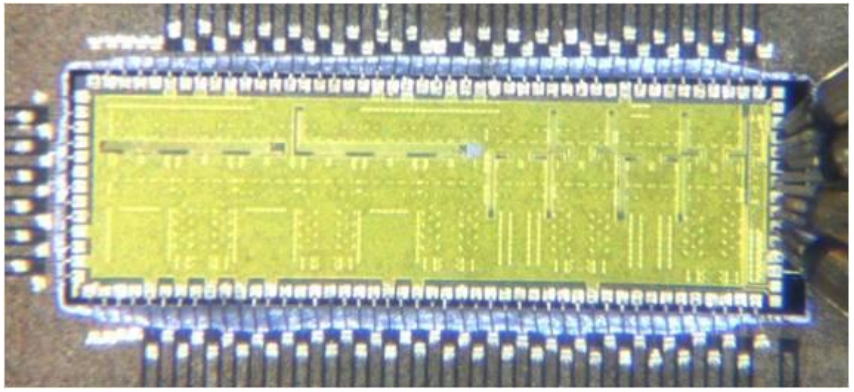
Bandwidth of optical fiber: ~5 THz.
Bandwidth of modern ICs: ~800GHz.

→ With THz transistors, and new IC toplogies,
electrical ICs can access over 1 THz of the optical fiber spectrum

Integrated Circuits for Wavelength Division De-multiplexing in the Electrical Domain

Hyun-chul Park[(1)], Molly Piels[(1)], Eli Bloch[(2)], Mingzhi Lu[(1)], Abirami Sivananthan[(1)], Zach Griffith[(3)], Leif Johansson[(1)], John Bowers[(1)], Larry Coldren[(1)], and Mark Rodwell[(1)]

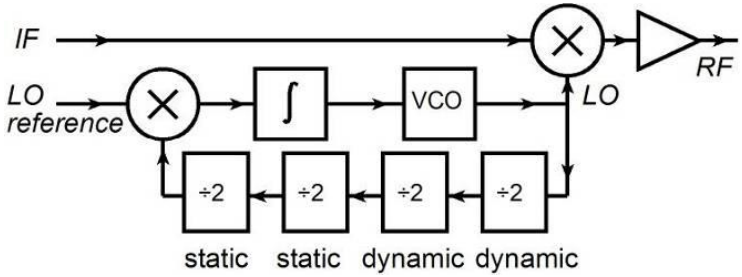
submitted to ECOC 2013



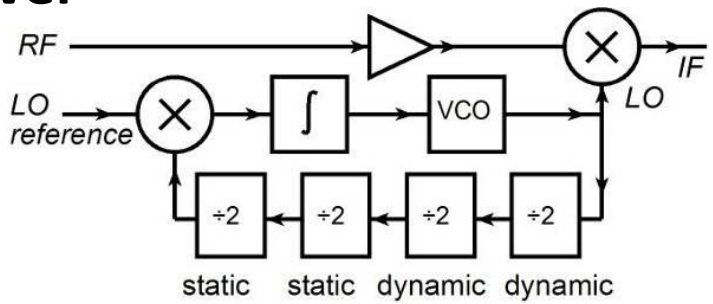
Closing

Where Next ? → 2 THz Transistors, 1 THz Radios.

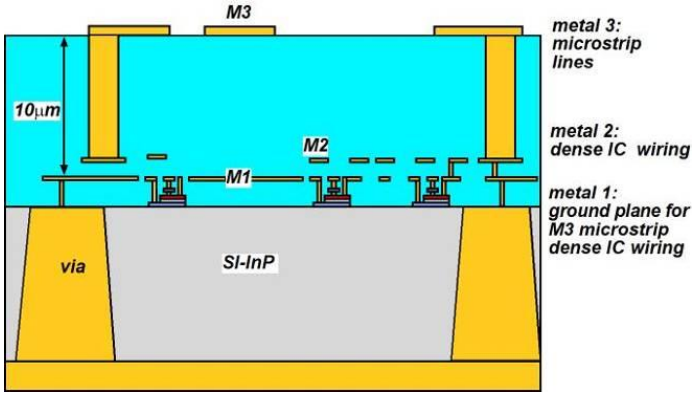
transmitter



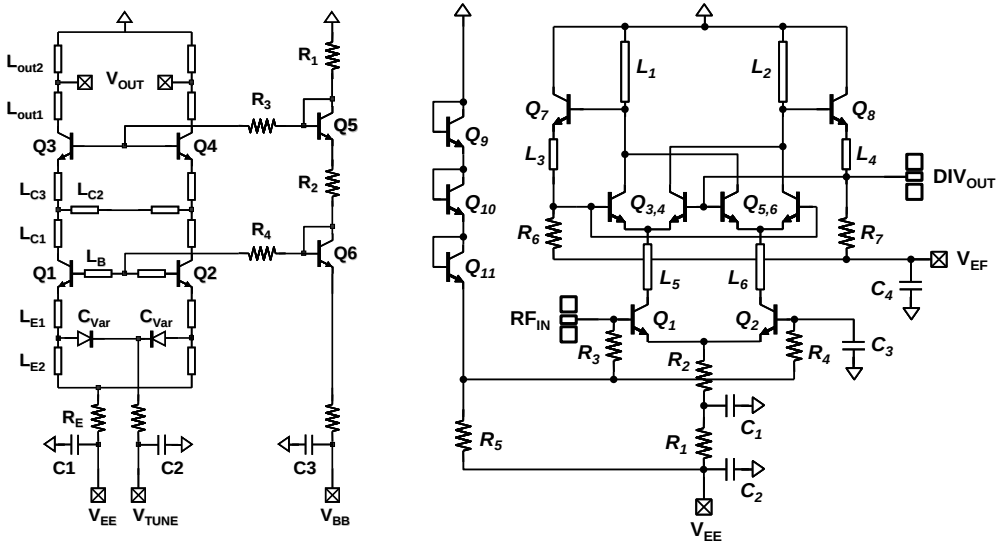
receiver



interconnects

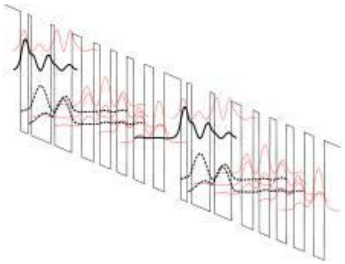


circuits

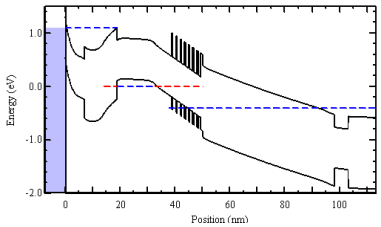


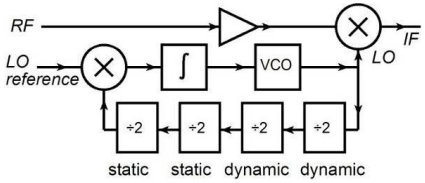
THz and Far-Infrared Electronics

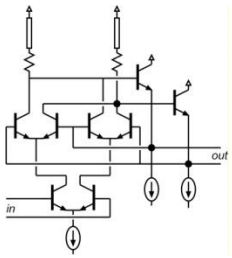
IR today→ lasers & bolometers → generate & detect

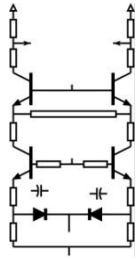


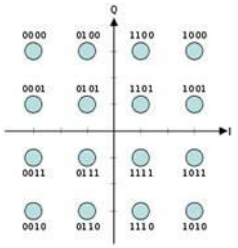
Far-infrared ICs: <u>classic</u> device physics, <u>classic</u> circuit design











Power, power-added efficiency, noise figure are all very important

<u>fundamental-mode operation</u>, <u>not harmonic generation</u>

The transistors will scale to at least 2 THz bandwidths

Even 1-3 THz ICs will be feasible

(backup slides follow)