Performance Impact of Post-Regrowth Channel Etching on InGaAs MOSFETs Having MOCVD Source-Drain Regrowth

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Given low interface trap densities and low access resistances, InGaAs MOSFETs can provide greater on-state current than silicon MOSFETs at the same effective oxide thickness (EOT), and are thus strong candidates for use in VLSI.[1] Transconductance as high as 2.1 mS/µm (V_{ds}=0.5 V) with 115 mV/decade (V_{ds}=0.5 V) subthreshold swing has been reported[2] in planar III-V MOSFETs using a gate recess etch through the N+ InGaAs contact layer. It remains to be established whether the necessary etch depth control can be obtained at VLSI integration scales and 10-20 nm gate lengths. Using self-aligned regrowth of the N+ source and drain, III-V MOSFETs can be fabricated without requiring this gate recess etch;[3] 1.9 mS/µm (V_{ds}=1 V) with 116 mV/decade (V_{ds}=0.05 V) subthreshold swing was reported in a 55 nm L_g InGaAs MOSFET with MOCVD source-drain regrowth.[4] Note that no post-regrowth etching of the channel surface is reported in (4). We have recently found[5] that InGaAs MOSFETs using MBE source-drain regrowth, subthreshold swing and transconductance are substantially improved by removing a 5 nm N+ InGaAs channel cap post-regrowth and immediately prior to gate dielectric deposition, suggesting damage to the channel surface during regrowth. Here, we report similar findings for MOCVD regrowth. We fabricated 65 nm L_g $In_{0.53}Ga_{0.47}As$ surface-channel MOSFETs in a gate-last process with self-aligned raised InGaAs S/D access regions formed by MOCVD regrowth. Removal of ~ 2.4 nm of the channel surface by digital etching improved the transconductance from 1.1 to 1.58 mS/µm (65 nm L_g, V_{ds}=0.5 V), and reduced the subthreshold swing from 326 to 110 mV/dec (1 µm L_g, V_{ds}=0.05 V). These results suggest that substantial surface damage arises, and must be addressed, in MOCVD regrowth III-V MOSFET processes.

The epitaxial layer structure is similar to that found in (3). Approximately 70 nm of PECVD SiO_2 was deposited on the sample for dummy gate formation, gate stripes patterned using electron beam lithography, transferred to the SiO_2 using SF_6/Ar ICP etching. Immediately prior to MOCVD regrowth,[4] the semiconductor surface was oxidized in UV ozone for 30 minutes, and etched in H_2O:HCl. MOCVD regrowth of ~30 nm $In_{0.53}Ga_{0.47}As$ n-type (Si-doped $\sim 4 \cdot 10^{19}\,cm^{-3}$) used TBA, TMI, TMG, and disilane (400 ppm), at 600ºC growth temperature. Devices were isolated using both citric acid:H_2O:H_2O_2 and H_2O_2:H_3PO_4:H_2O. Dummy gates were removed in buffered HF. One sample was exposed to UV ozone for 15 minutes, the InGaAs oxide etched in H_2O:HCl for 1 minute, and oxidized again for 15 minutes. UV ozone-exposed and unexposed samples were then treated with buffered HF prior to dielectric deposition. Each oxidation/etch removed approximately 1.2 nm of $In_{0.53}Ga_{0.47}As$.[5] Samples were then immediately loaded into the atomic layer deposition loadlock. After *in-situ* H_2/TMA treatment,[6] ~1 nm Al_2O_3 and ~4 nm HfO_2 were deposited (EOT ≈ 1.35 nm). Gate metal liftoff was thermally evaporated 50/160 nm Ni/Au. Source/drain region oxide was etched in buffered HF and source-drain metallization was electron beam evaporation of Ti/Pd/Au, 20/60/75 nm.

Further investigating process damage, off-wafer frequency-dependent CV data on 5 nm Al_2O_3 MOS capacitors were measured with one capacitor experiencing 500 ºC anneal in a rapid thermal annealer to simulate source-drain regrowth conditions. The annealed capacitor showed greatly increased frequency dispersion at biases below threshold, suggesting increased interface trap density.[7] 68 nm L_g FETs without channel etching have a threshold voltage of -0.69 V by linear extrapolation, a current density of 0.58 mA/µm at V_{ds} = 0.5 V and $V_{gs} - V_{th}$ = 0.5 V, and peak transconductance of 1.1 mS/µm at a V_{ds} = 0.5 V. 65 nm FETs with channel etching have a threshold voltage of 0.15 V by linear extrapolation, a current density of 0.78 mA/µm at V_{ds} = 0.5 V and $V_{gs} - V_{th}$ = 0.5 V, and peak transconductance of 1.58 mS/µm at V_{ds} = 0.5 V. 1 µm FETs without channel etching have a subthreshold swing of 326 mV/dec at V_{ds} = 0.05 V, compared to 110 mV/dec when the channel is etched. For the digitally etched sample, transmission line measurements of the metal/regrowth interface show 19.8 ohm-micron and 46 ohm/sq for the metal-semiconductor contact resistance and N+ regrowth sheet resistance, respectively. The short- L_g FETs suffer from severe short channel effects, likely due to the large delta doping below the channel. This can be addressed by decreasing or removing the delta doping, more deeply etching the channel, and decreasing the dielectric EOT. Future work will investigate the cause of surface damage.

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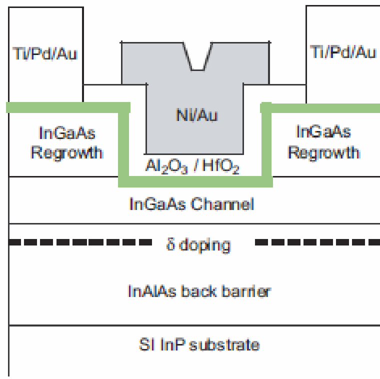


Figure 1: Schematic cross-section of the gate last MOSFET. Green indicates regions digitally etched prior to gate dielectric deposition.

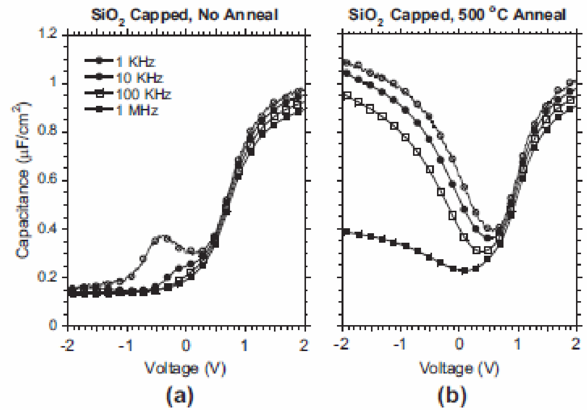


Figure 2: MOSCAP CV epi, SiO_2-capped a) 500°C annealed and (b) not annealed, prior to cap stripping and 5 nm ALD Al_2O_3 deposition.

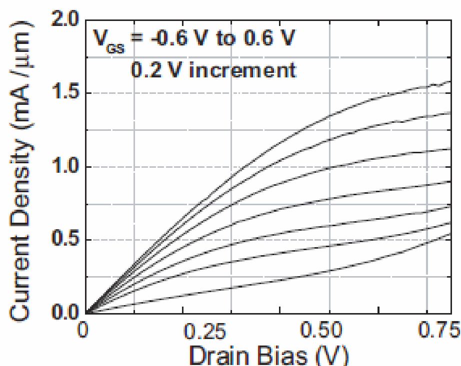


Figure 3: J_{drain} versus V_{ds} for 68 nm L_g / 9.5 μm W_g FET, no channel etching.

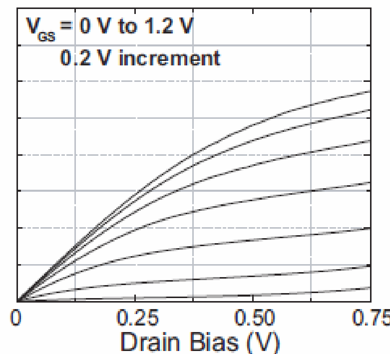


Figure 4: J_{drain} versus V_{ds} for 65 nm L_g / 9.5 μm W_g FET, channel etch applied.

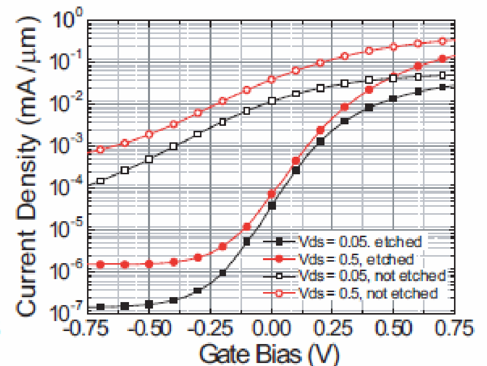
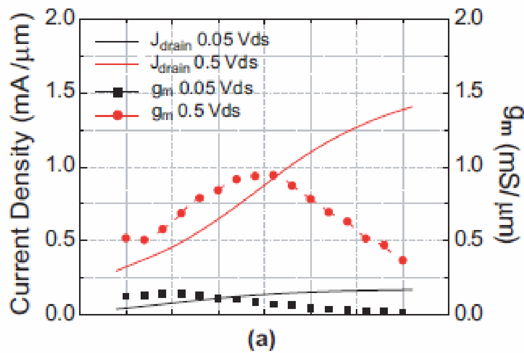


Figure 5: J_{drain} versus V_{gs} for 1 micron L_g FETs, channel etching and no etching.



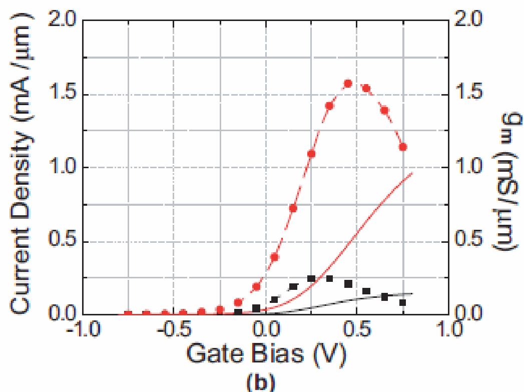
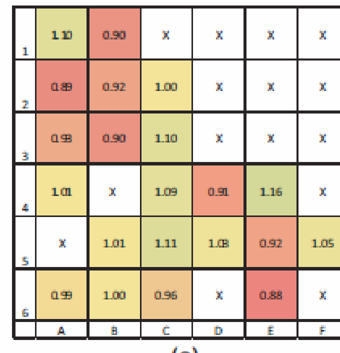


Figure 6: J_{drain} versus V_{gs} for
a) 68 nm L_g FET, no channel etching
b) 65 nm L_g FET, channel etching



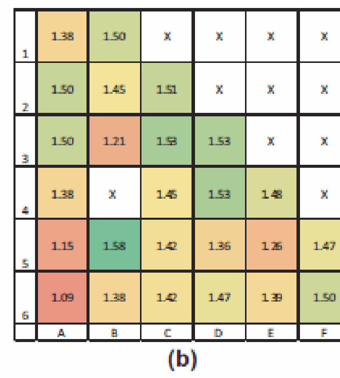
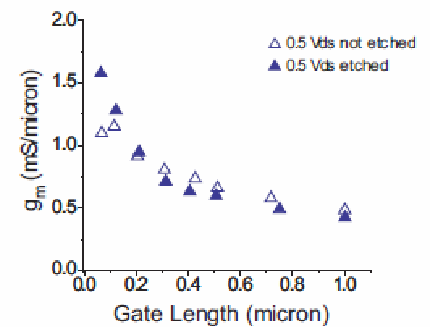


Figure 7: Peak g_m wafer map (mS/micron), V_{ds}= 0.5 V
a) no channel etching, ~ 110 nm L_g
b) channel etching, ~ 65 nm L_g



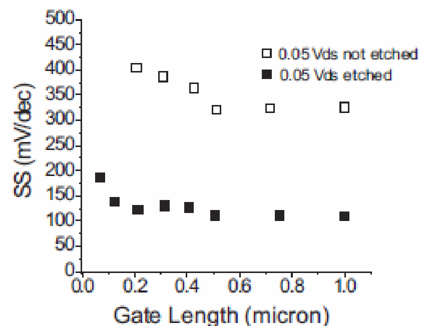


Figure 8: Peak transconductance and minimum subthreshold swing versus gate length for channel etched and not etched samples.