Performance Impact of Post-Regrowth Channel Etching on InGaAs MOSFETs Having MOCVD Source-Drain Regrowth

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Overview

Why III-V for VLSI?

Device Physics and Scaling

Process Flows

Measurements

Conclusions

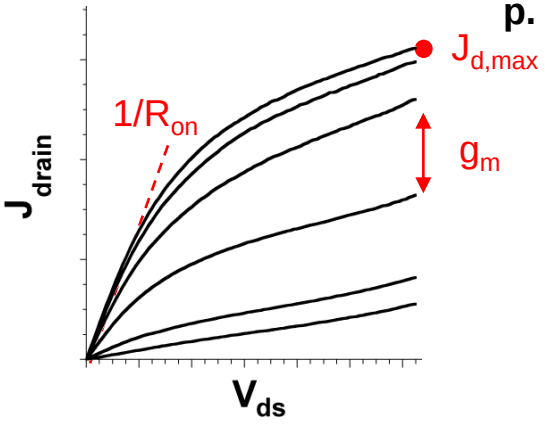
Why III-V VLSI?

Higher electron velocities than Si MOS

For short L_g FETs, $J_{drain} = q \cdot n_{s,channel} \cdot v_{sat}$

Transconductance, $g_m = C_{effective} \cdot v_{sat}$

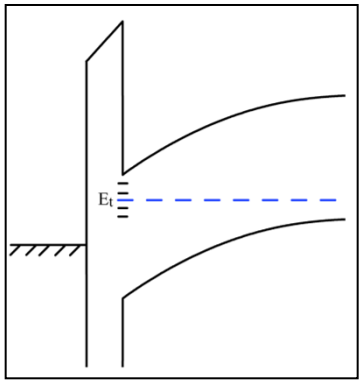
J_d and g_m are key figures of merit in VLSI



However:

J_d and g_m degraded by source large R_{access}

J_d and g_m degraded by interface trap density, D_{it}

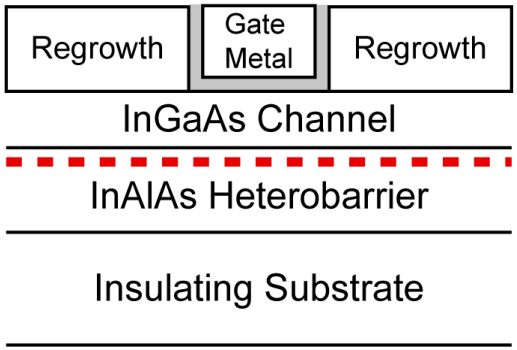


Therefore, we must develop:

Low access resistance source/drain contacts

Thin, high-k, low D_{it} dielectrics on InGaAs

Fully self-aligned process modules



*MOSFETs have been, and always will be, a **materials challenge**.*

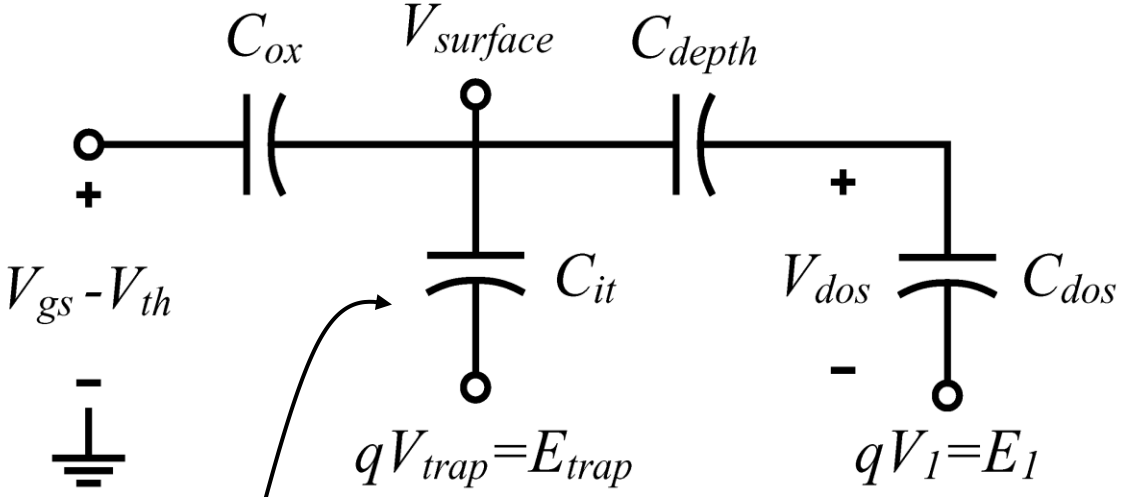
FET Device Physics

$$C_{ox} = \frac{\varepsilon_o \varepsilon_r L_g W_g}{t_{ox}}$$

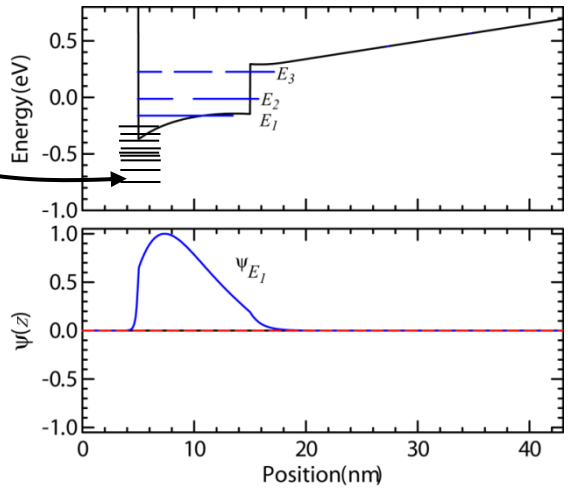
$$C_{depth} \approx \frac{\varepsilon_o \varepsilon_{channel} L_g W_g}{t_{channel}/2}$$

$$C_{dos} = \frac{q^2 g m^*}{2\pi\hbar^2} L_g W_g$$

$$n_{channel} = \frac{C_{dos}}{q}(V_{dos})$$



$$C_{it} = q^2 D_{it} W_g L_g$$

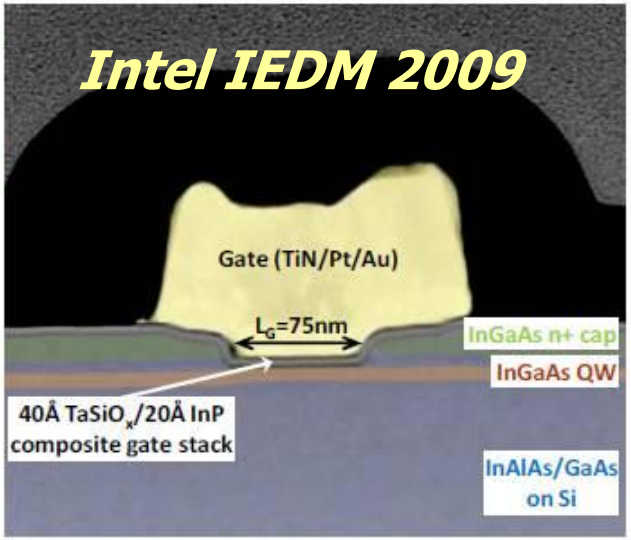


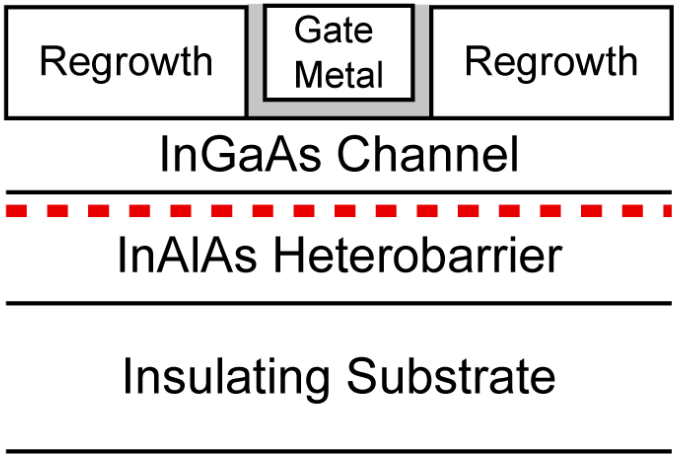
D_{it} problem

- $\uparrow C_{it}$, $\downarrow V_{surface}$
- $V_{surface}$ supplies C_{dos}
- $\downarrow V_{surface}$ =$\downarrow n_{dos}$ in C_{dos}

Electron band diagram: gate-insulator-channel

Candidate III-V Planar Geometries





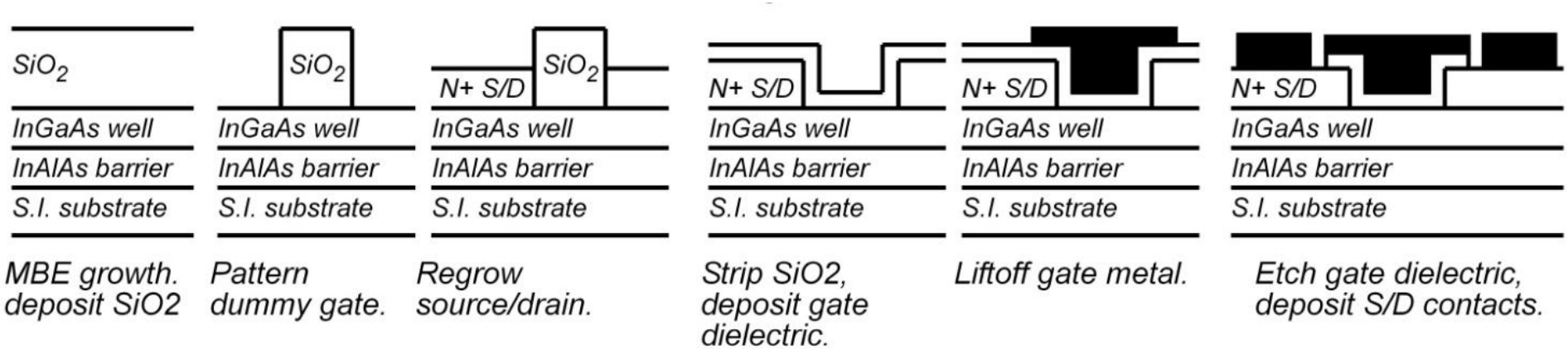
"Trench" MOSFET

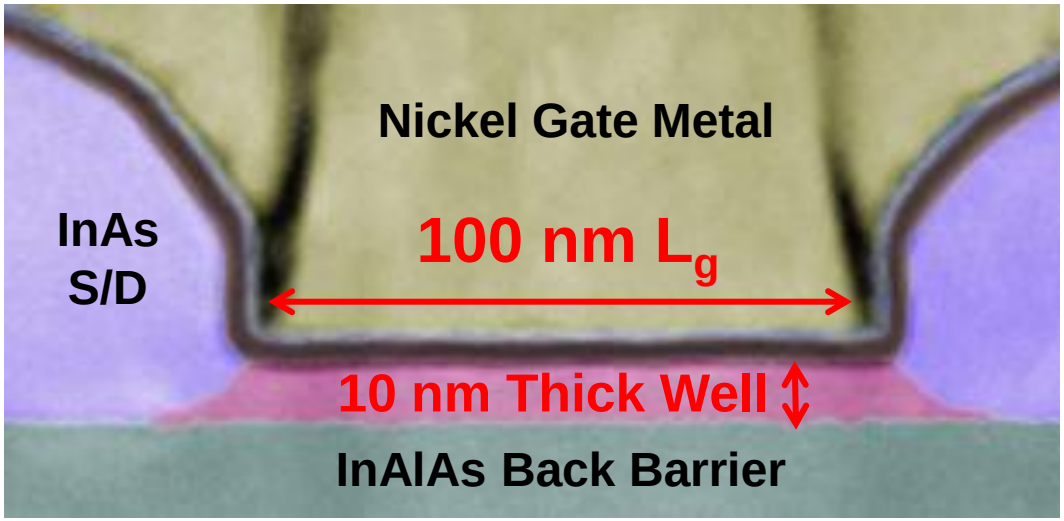
- Leverages HEMT tech.
- Gate oxide → Low I_g ☺
- Small footprint ☺
- **But**
  - **Will the L_g scale?**

Replacement Gate MOSFET

- Easily defined L_g ☺
- Gate oxide ☺
- Small footprint ☺
- **But**
  - **Is RG doping high enough?**

Gate Replacement FET Process Flow



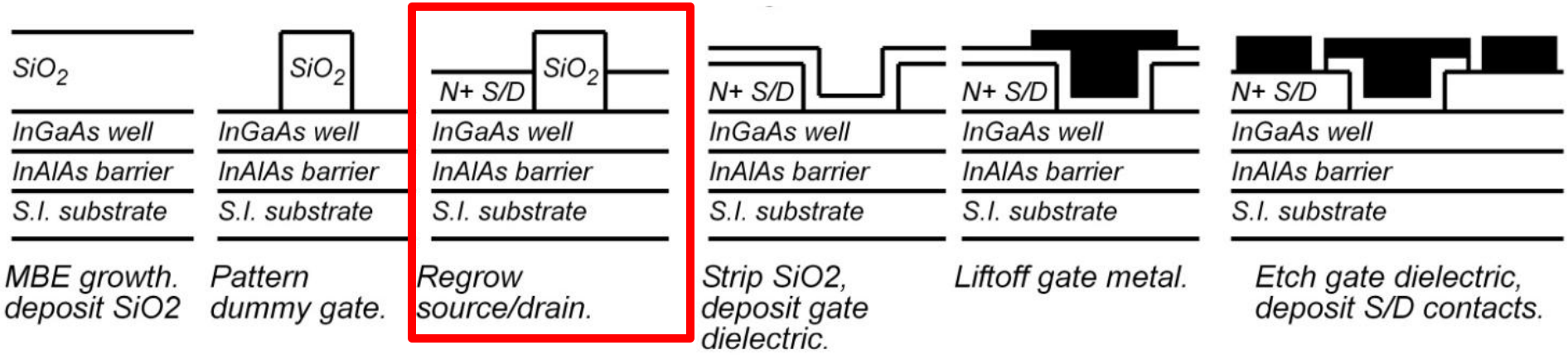


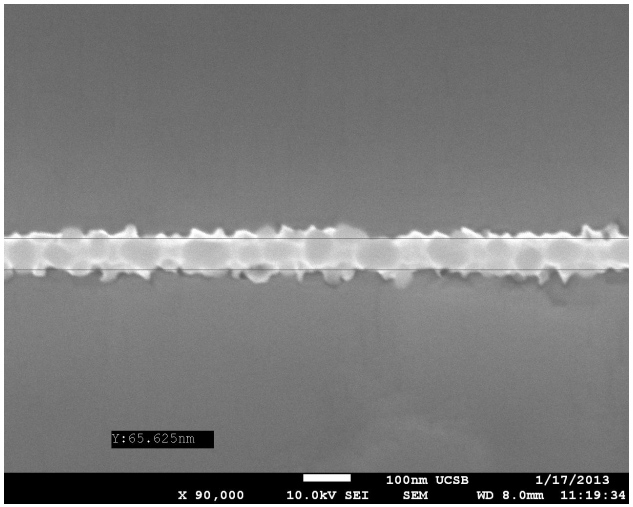
STEM FET cross section, color-coded by chemistry
Figure courtesy Jeremy Law (UCSB)

MBE S/D Regrowth

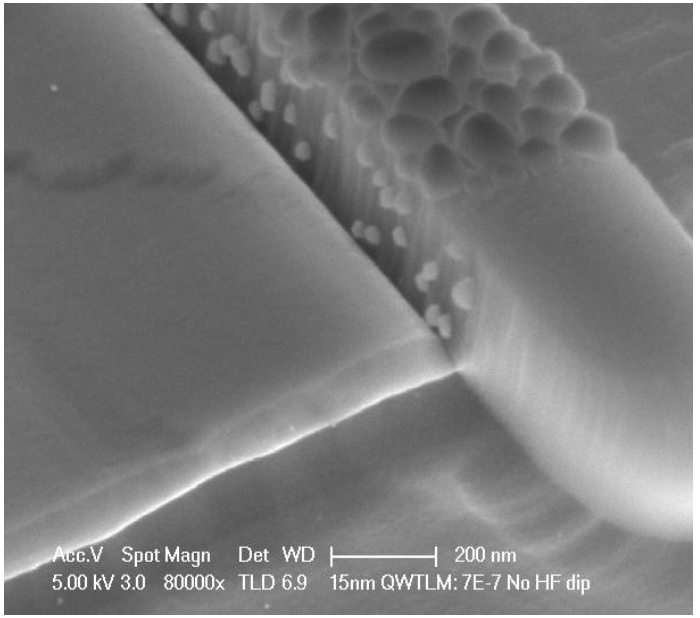
Low-damage process
- Thermal gate metal
- No/Low-damage plasma
- Dielectric post-regrowth

Gate Replacement FET Challenges



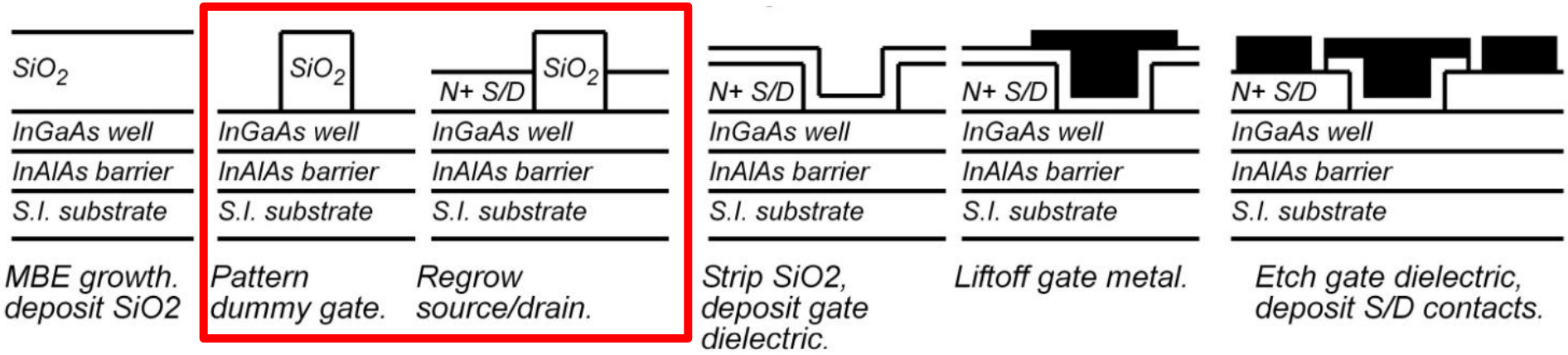


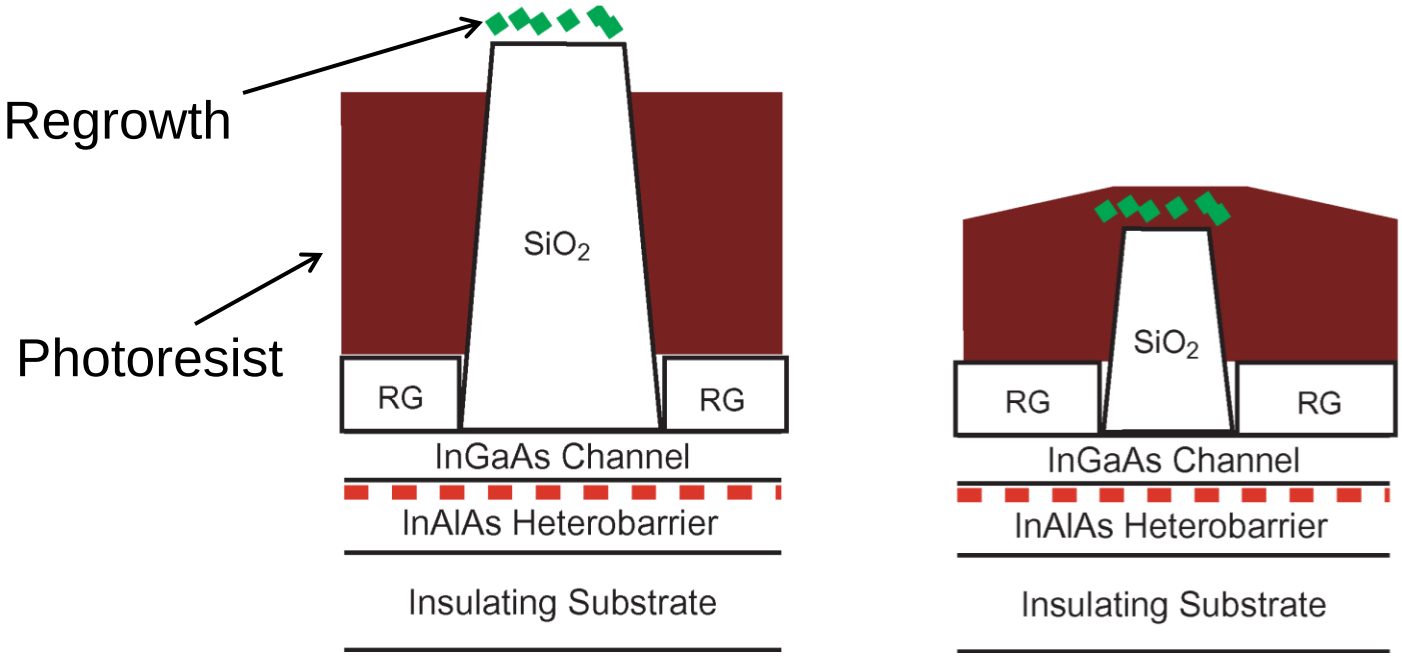
SEM of dummy gate



MBE regrowth is non-selective → requires photoresist planarization

Gate Replacement FET Challenges

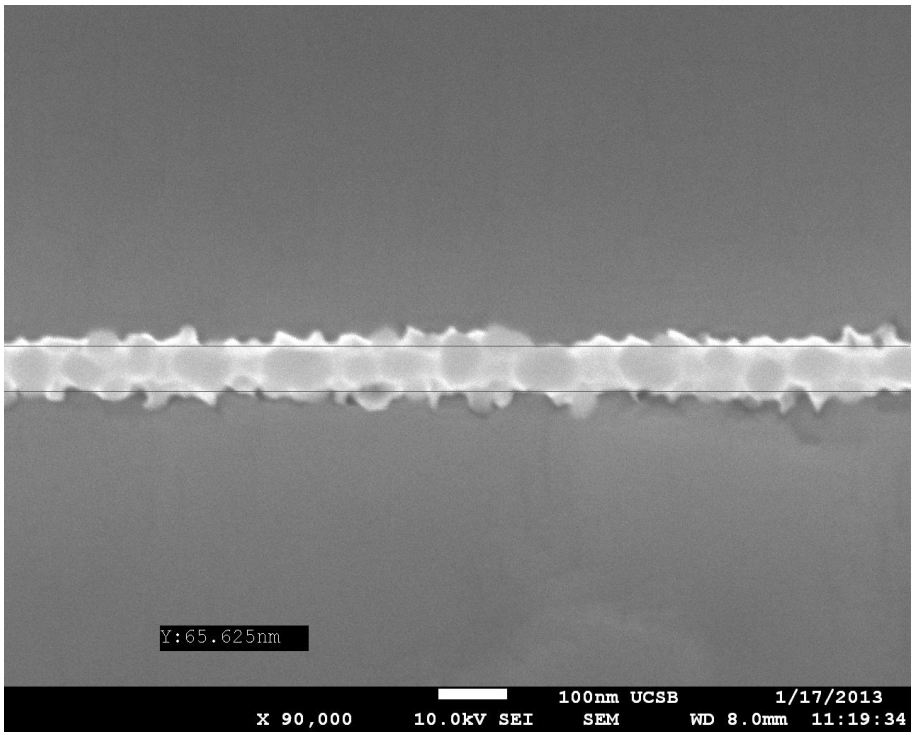




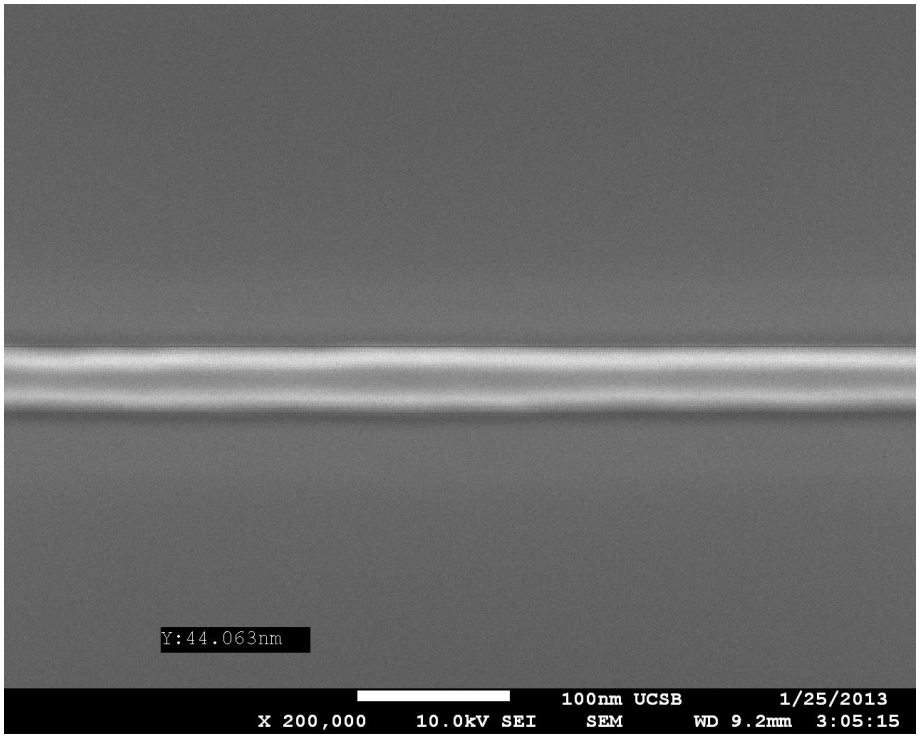
Short dummy gates are hard to planarize, aspect-ratio-limited gate length

Solution: MOCVD S/D Regrowth *

MBE InAs RG



MOCVD InGaAs RG



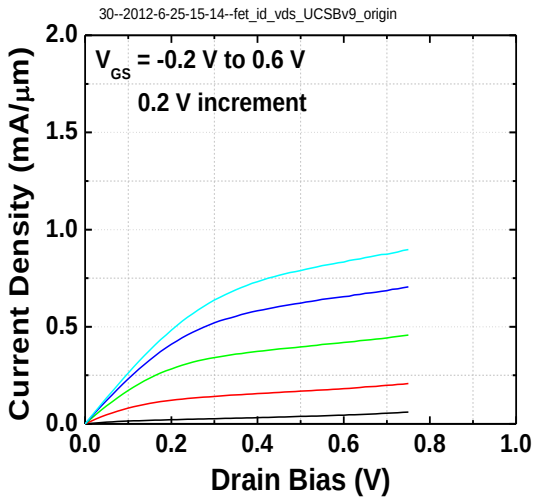
MBE is non-selective to the SiO_2 pillar, while MOCVD is selective!

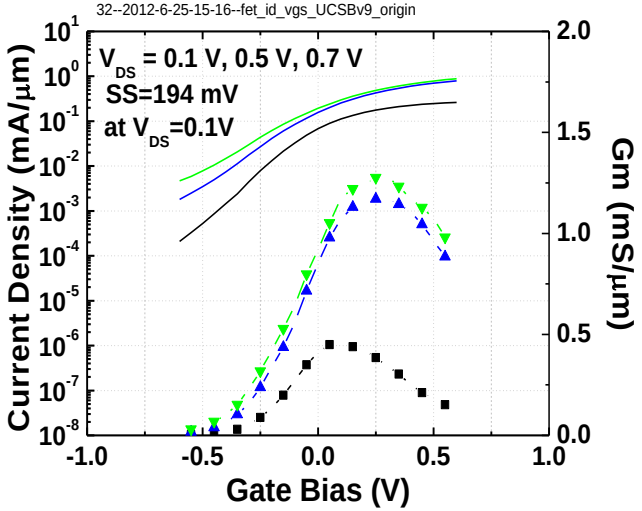
→ PR planarization no longer necessary → short L_g that will not fall over

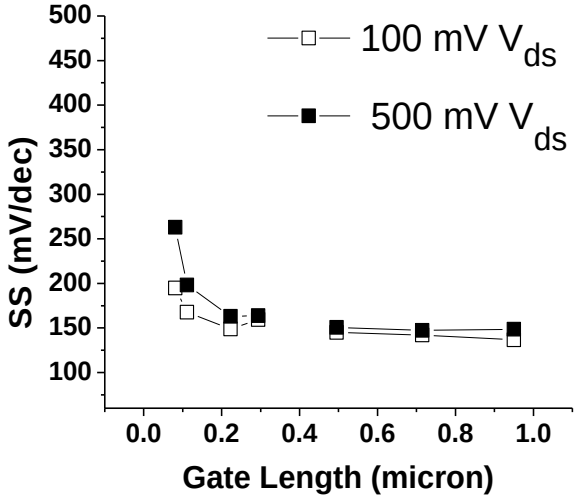
* Terao *et al,* APEX 2011, and Egard *et al*, DRC 2011

MBE Versus MOCVD S/D Regrowth

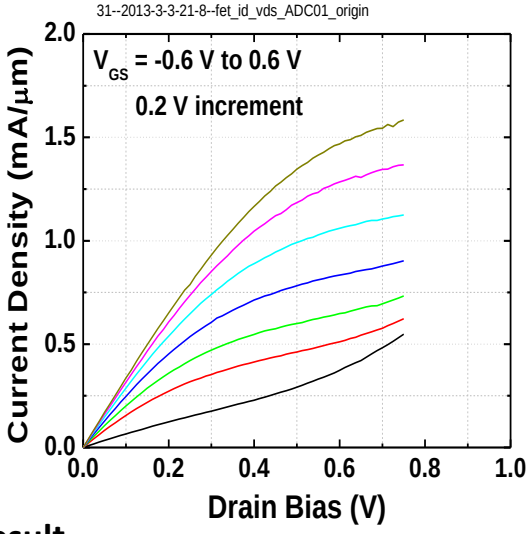
81 nm L_g, (1 nm Al_2O_3/ 4 nm HfO_2), 10 nm channel, MBE InGaAs Regrowth

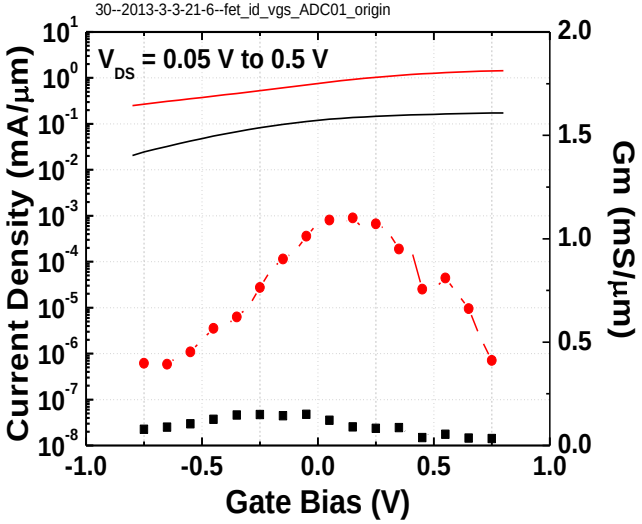


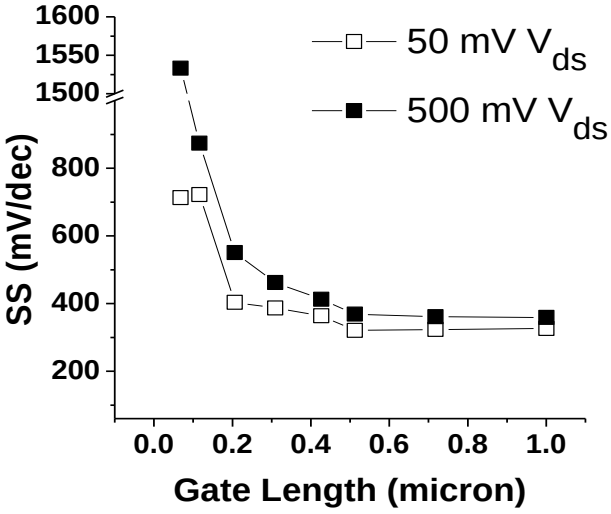




68 L_g, (1 nm Al_2O_3/ 4 nm HfO_2), 10 nm channel, MOCVD InGaAs Regrowth







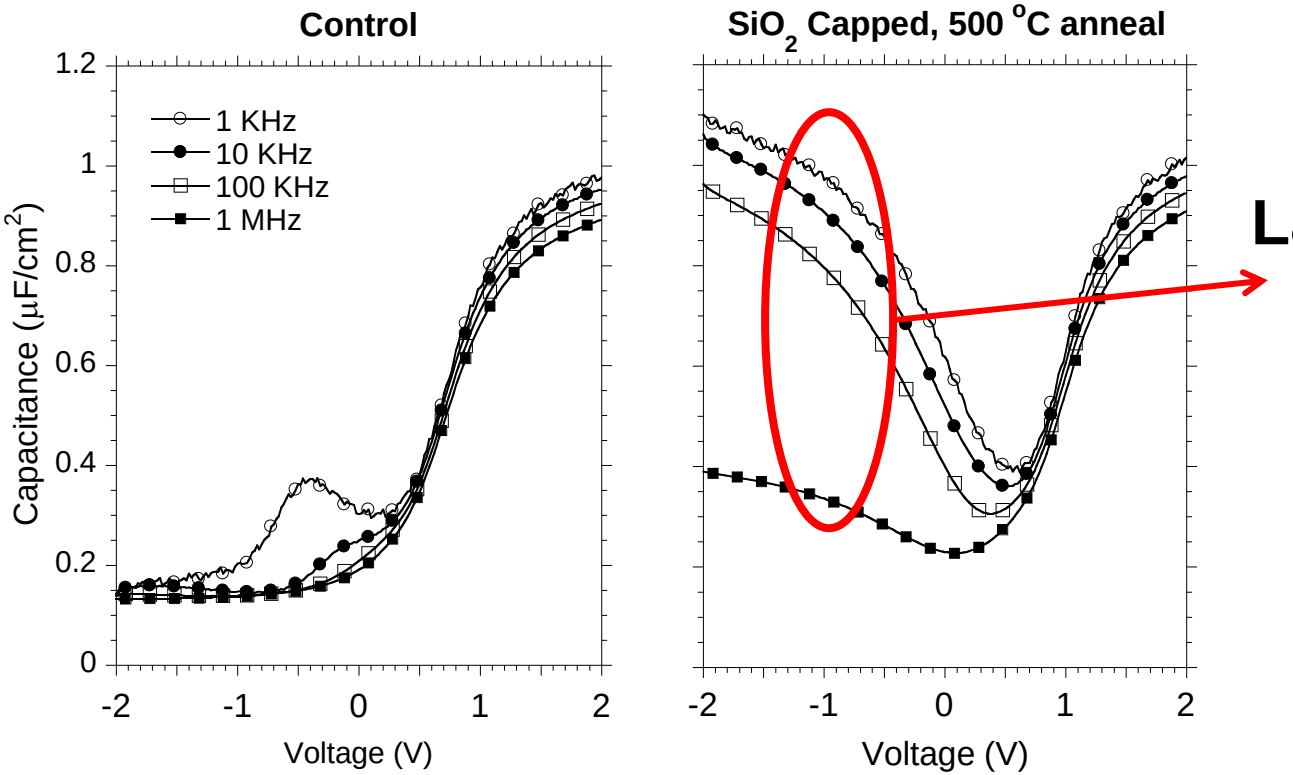
result

Similar on-state performance, but large Vth shift, poor SS, DIBL

Poor subthreshold: Channel Degradation

> 300 mV/dec subthreshold swing → D_{it} ? Channel degradation?

Experiment: SiO_2 capping + high temp anneal + strip → MOSCAP 5 nm Al_2O_3



InP channel capping for RG → large subthreshold swing for FETs ☹

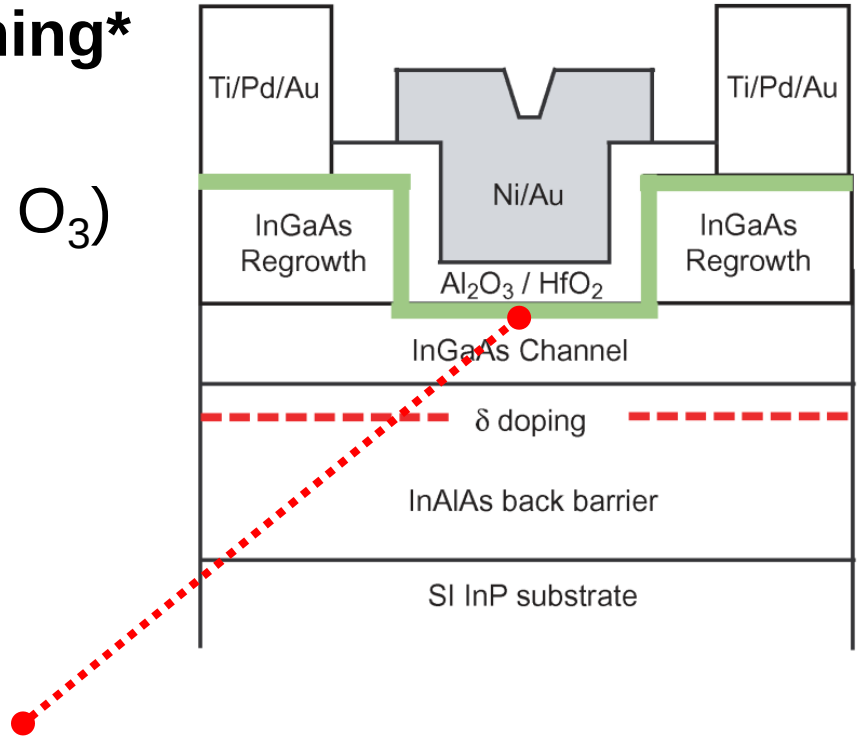
MOCVD: Digital Channel Etching

Digital semiconductor etching*

Before ALD deposition:
- Oxidize channel surface (UV O_3)
- Etch oxide in HCl:DI

Repeat as needed

Etches ~ 1.2 nm per cycle



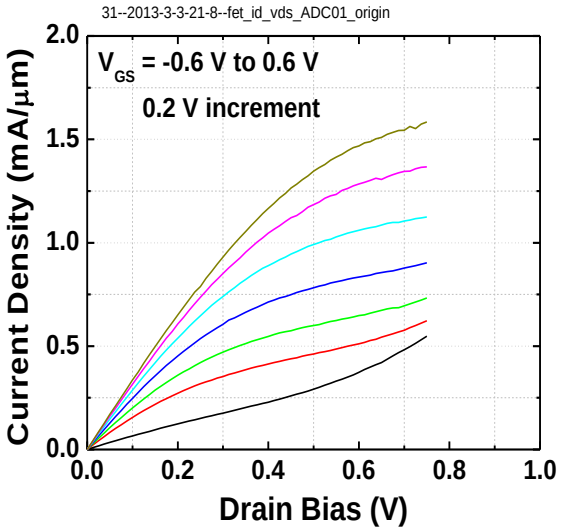
Top-down thin channels → Increase C_{depth}

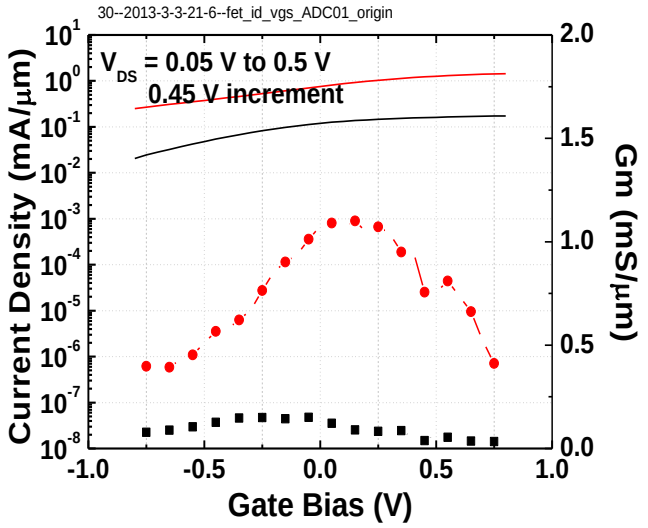
Simultaneous damage removal and body scaling

* S.Lee et al, IPRM 2013

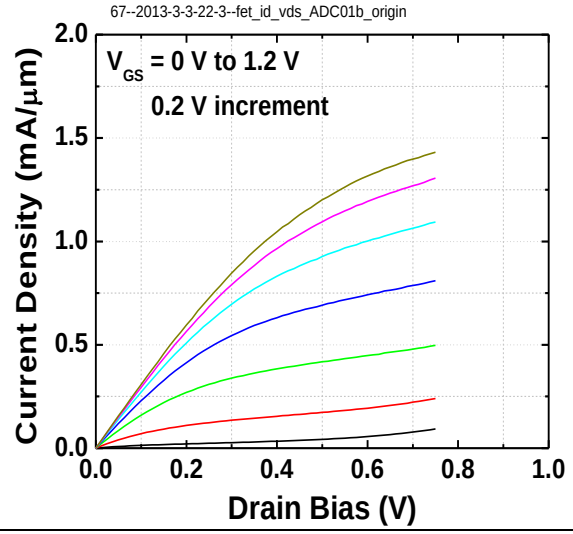
MOCVD RG with Digital Channel Etching

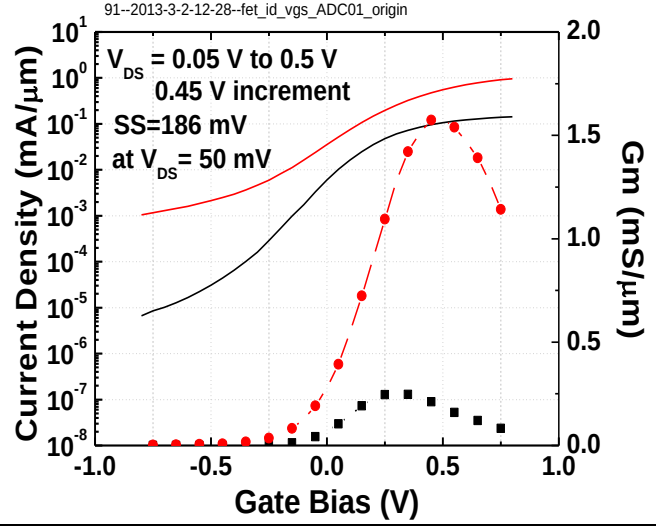
68 nm actual L_g, (1 nm Al_2O_3/ 4 nm HfO_2), No digital etching (~ 10 nm channel)





65 nm actual L_g, (1 nm Al_2O_3/ 4 nm HfO_2) 2 cycles of digital etching (~ 6.5 nm channel)





result

All devices improve with channel etch → thinner channel, remove surface damage

MOCVD RG with Digital Channel Etching

Peak transconductance (mS/micron): 50 nm as drawn gate length, 0.5 V V_{gs}

No Etching (10 nm ch.)

	A	B	C	D	E	F
1	1.10	0.90				
2	0.89	0.92	1.00			
3	0.93	0.90	1.10			
4	1.01	Blank	1.09	0.91	1.16	
5	Open	1.01	1.11	1.03	0.92	1.05
6	0.99	1.00	0.96	Open	0.88	Open

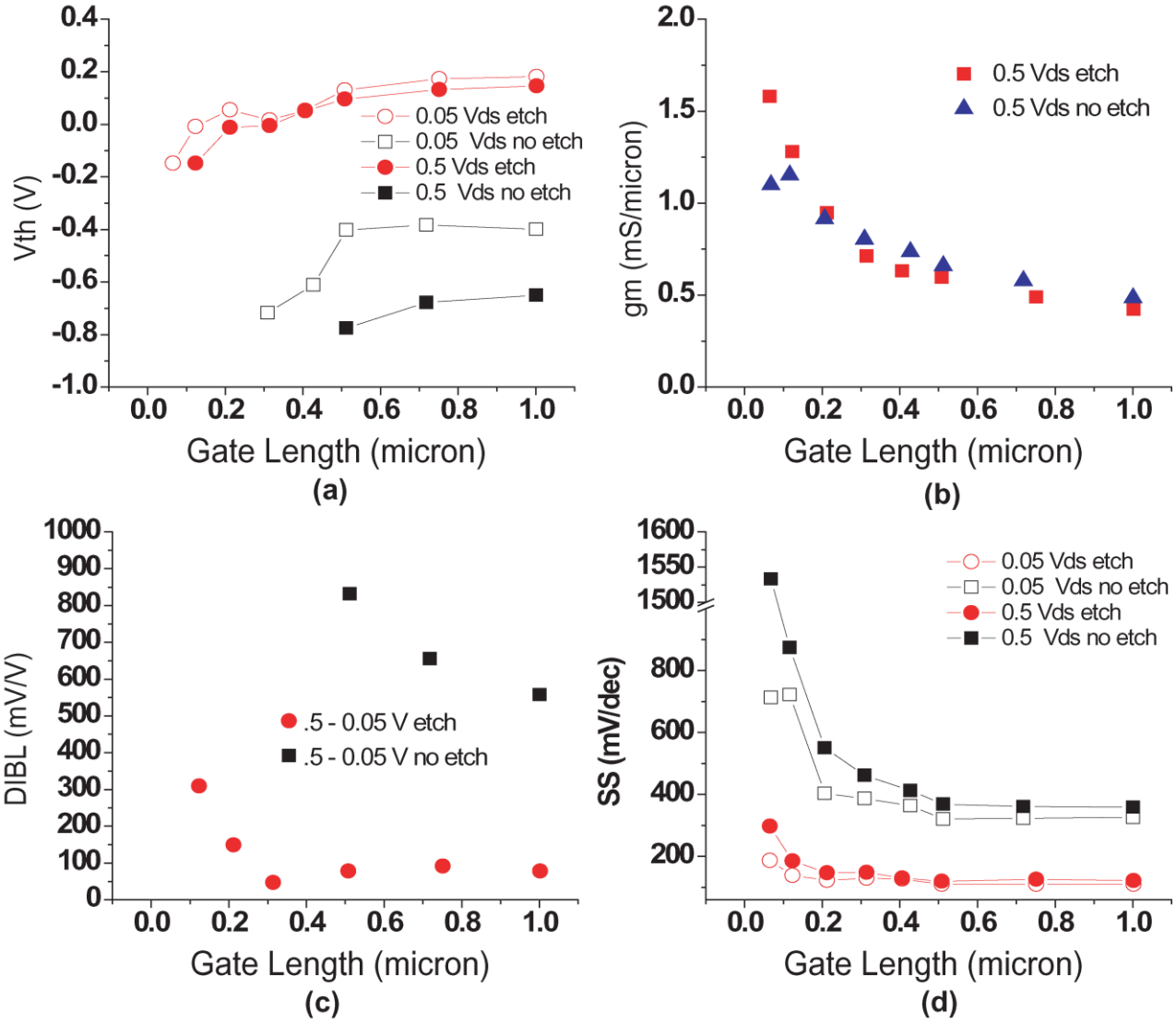
2 Cycle Etching (~6.5 nm ch.)

	A	B	C	D	E	F
1	1.38	1.50				
2	1.50	1.45	1.51			
3	1.50	1.21	1.53	1.53		
4	1.38	Blank	1.45	1.53	1.48	
5	1.15	1.58	1.42	1.36	1.26	1.47
6	1.09	1.38	1.42	1.47	1.39	1.50

result

All devices improve with channel etch → thinner channel, remove surface damage

MOCVD RG with Digital Channel Etching



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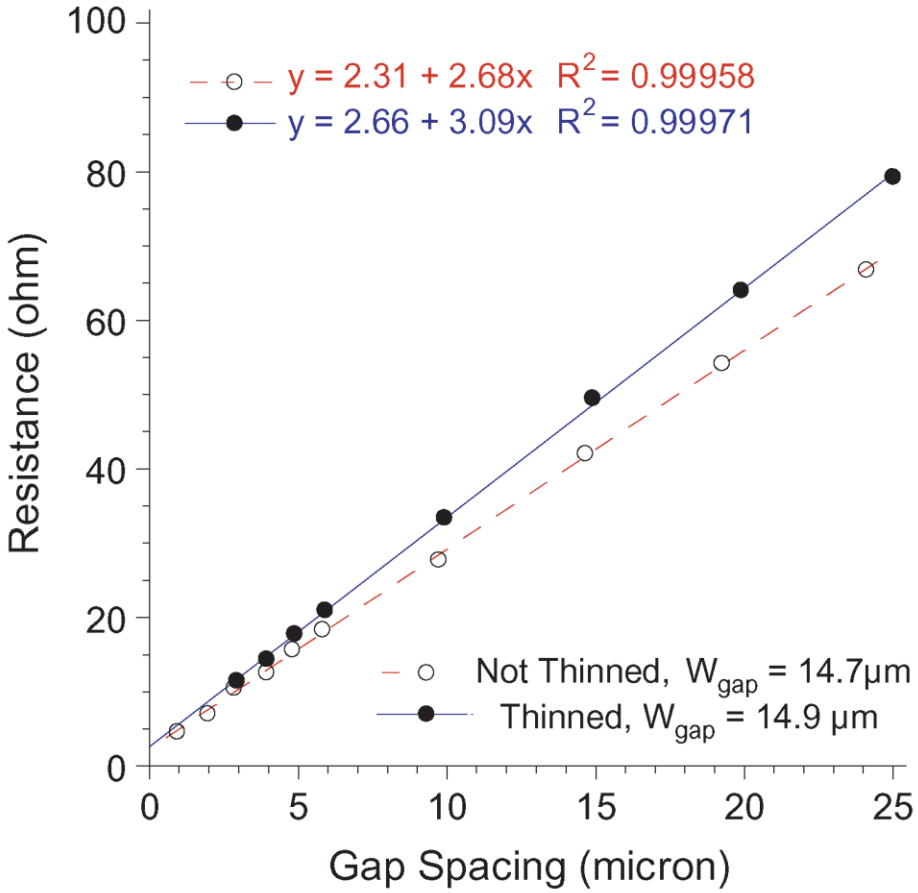
MOCVD RG with Digital Channel Etching



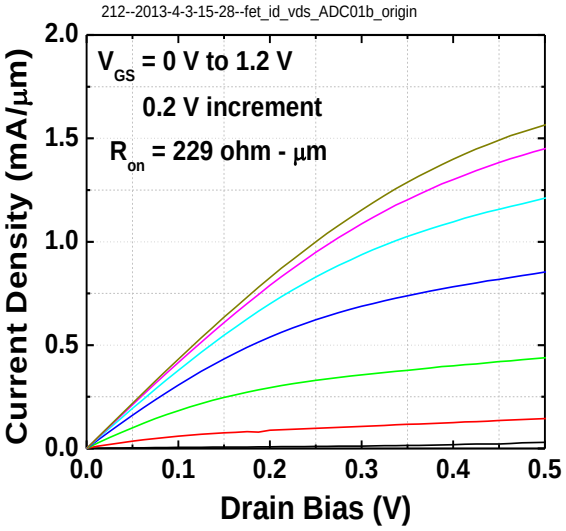
	R_{sh} (ohm/sq)	R_{end}(ohm-µm)	$L_{transfer}$
Not Thinned	39.4	17	430 nm
Thinned	46	19.8	430 nm

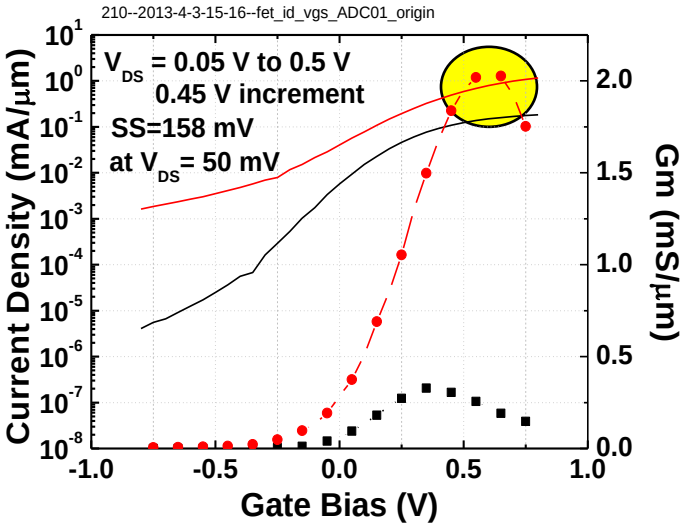
result

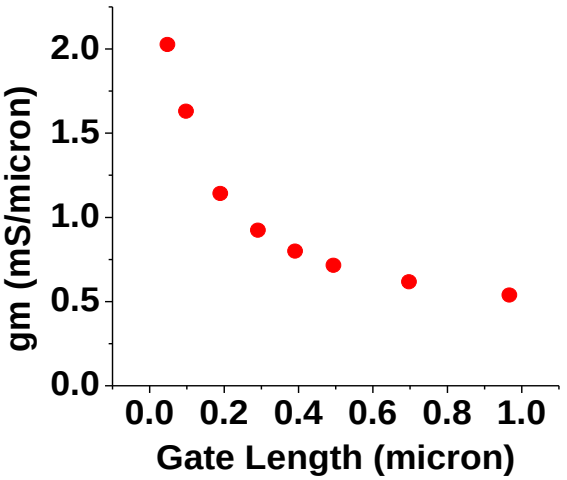
Lower performance for not etched channels not due to metal-RG contact

MOCVD RG: Recent Results

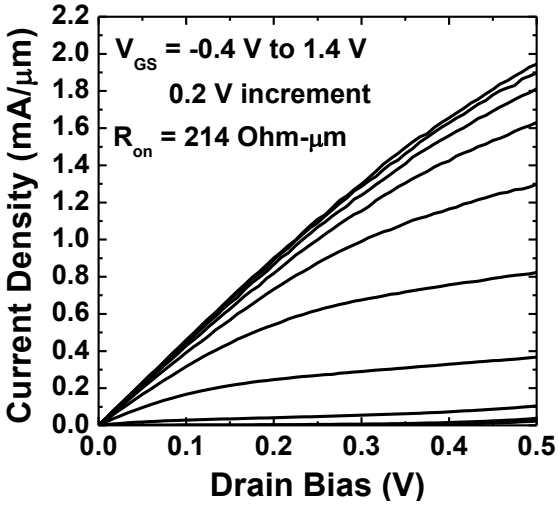
48 nm gate length, ~ 3.8 nm HfO_2, InGaAs with 2 cycle digital etching, p-doped back barrier

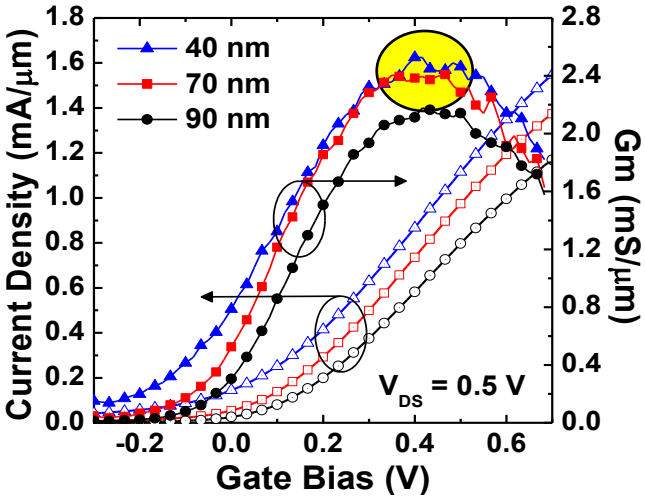


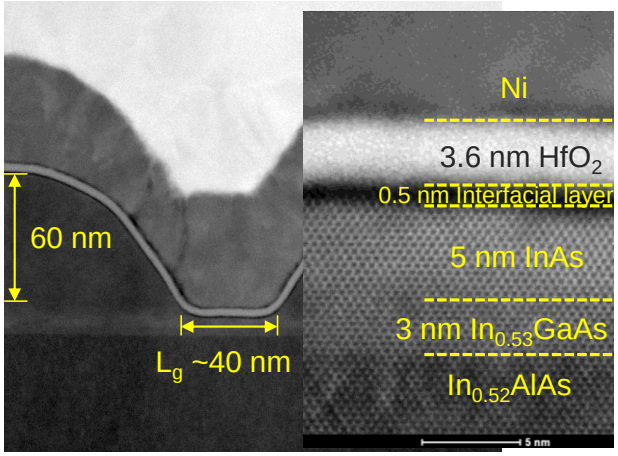




40 nm gate length, ~ 3.6 nm HfO_2 , InAs/InGaAs channel, digitally etched *







* S. Lee *et al*, VLSI 2013

High performance III-V MOS using aggressively scaled ALD dielectrics

Conclusions

65 nm gate last InGaAs MOSFET process flow using MOCVD

J_{drain} = 0.78 mA/μm at 0.5 V $V_{gs} - V_{th}$, 0.5 V V_{ds}

Peak transconductance: 1.58 mS/micron at 0.5 V V_{ds}

Self-aligned process path for sub-50 nm III-V VLSI

Continued research areas

- Thinner gate dielectrics
- Body scaling (thin planar QW and/or FinFETs)
- Improved D_{it} passivation techniques

Thanks for your time!
Questions?

contact address: adc [at] ece.ucsb.edu

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BACK UP SLIDES

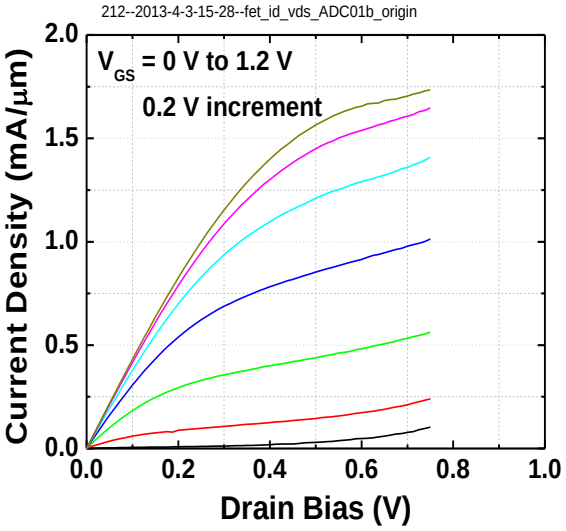
Source-Drain Regrowth Data

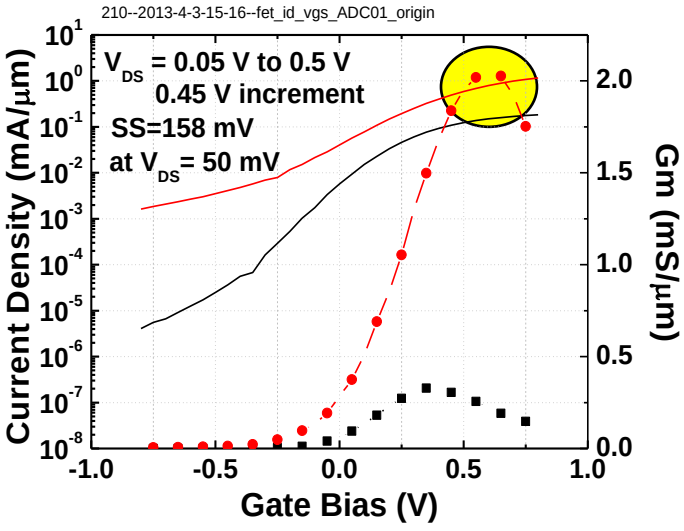
Name	Dopant (cm^{-3})	Thickness (nm)	Contact Metal	R_{sheet} ($\Omega/\square$)	R_{Access} ($\Omega \cdot \mu m$)	$\rho_{contact}$ ($\Omega \cdot \mu m^2$)	Ref.
MBE							
n-InGaAs	Si, $\sim 5\times10^{19}$	$\sim$50	Mo, *In-Situ*	29	12	5.5	[18]
n-InAs	Si, $\sim 4\times10^{19}$	$\sim$50	Mo, *In-Situ*	23	8.5	3.5	[20]
n-InAs (1)	Si, $\sim 5\times10^{19}$	$\sim$ 60	Ti/Pd/Au, *Ex-Situ*	21.4	6.5	2	[24]
n-InAs (2)	Si, $\sim 5\times10^{19}$	$\sim$ 60	Ti/Pd/Au, *Ex-Situ*	25.3	9.9	3.9	
n-InAs (1)	Si+Te, $\sim 6\times10^{19}$	$\sim$ 60	Ti/Pd/Au, *Ex-Situ*	17	4.7	1.29	
n-InAs (2)	Si+Te, $\sim 6\times10^{19}$	$\sim$ 60	Ti/Pd/Au, *Ex-Situ*	18.9	6.56	2.2	
n-InAs (3)	Si+Te, $\sim 6\times10^{19}$	$\sim$ 60	Ti/Pd/Au, *Ex-Situ*	17.8	10.6	6.32	
n-InAs	Si+Te, $\sim 6\times10^{19}$	$\sim$ 60	Ni/Pd/Au †, *Ex-Situ*	17.8	3.25	0.5	
n-InGaAs	Si+Te, $\sim 5\times10^{19}$	$\sim$ 60	Ti/Pd/Au, *Ex-Situ*	43.3	17.7	7.22	
MOCVD							
n-InGaAs (1)	Si, $\sim 4.5\times10^{19}$	$\sim$ 30	Ti/Pd/Au, *Ex-Situ*	41.8	32.44	25.2	
n-InGaAs (2)	Si, $\sim 4.5\times10^{19}$	$\sim$ 30	Ti/Pd/Au, *Ex-Situ*	39.4	16.97	7.29	
n-InGaAs (3)	Si, $\sim 4.5\times10^{19}$	$\sim$ 30	Ti/Pd/Au, *Ex-Situ*	46	19.8	8.5	
n-InGaAs	Si, $\sim 4.5\times10^{19}$	$\sim$ 60	Ti/Pd/Au, *Ex-Situ*	23.5	13.02	7.2	

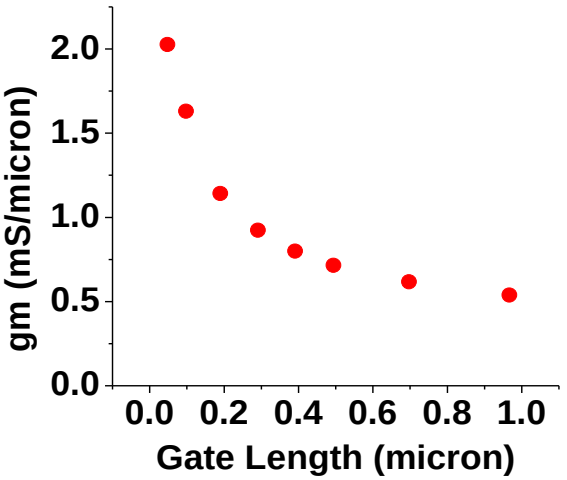
Table 4.1: Summary of MBE and MOCVD regrowth data. Dopant concentration is active carrier concentration. Electron beam evaporation for metal contacts, unless otherwise noted. † : thermal metal evaporation.

MOCVD RG: Recent Results

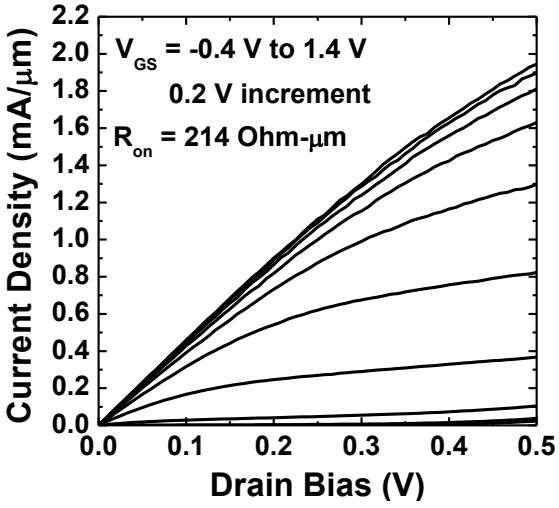
48 nm gate length, ~ 3.8 nm HfO_2, InGaAs with 2 cycle digital etching, p-doped back barrier

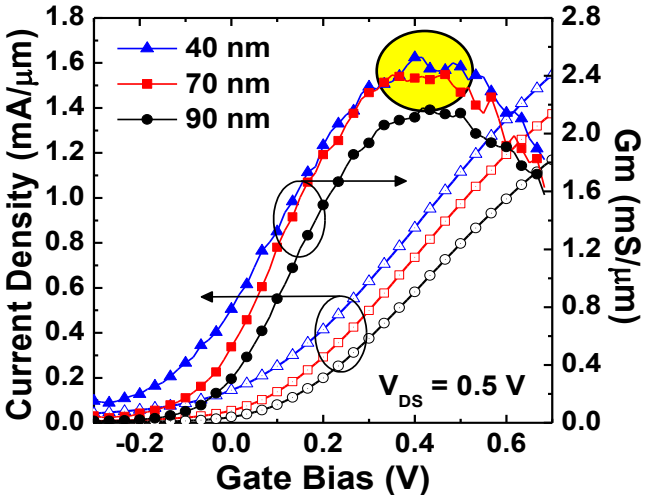


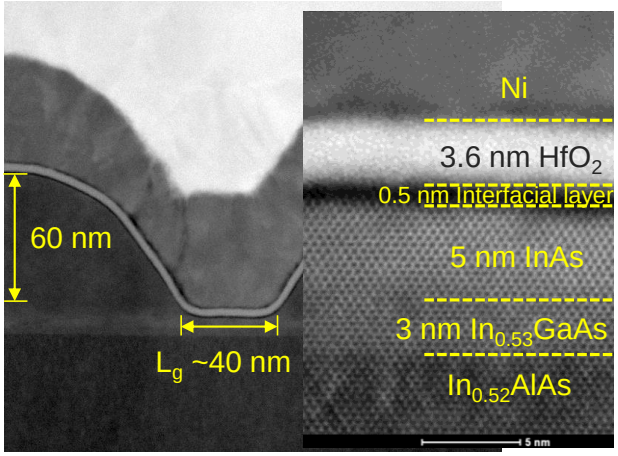




40 nm gate length, ~ 3.6 nm HfO_2 , InAs/InGaAs channel, digitally etched *







* S. Lee *et al*, VLSI 2013

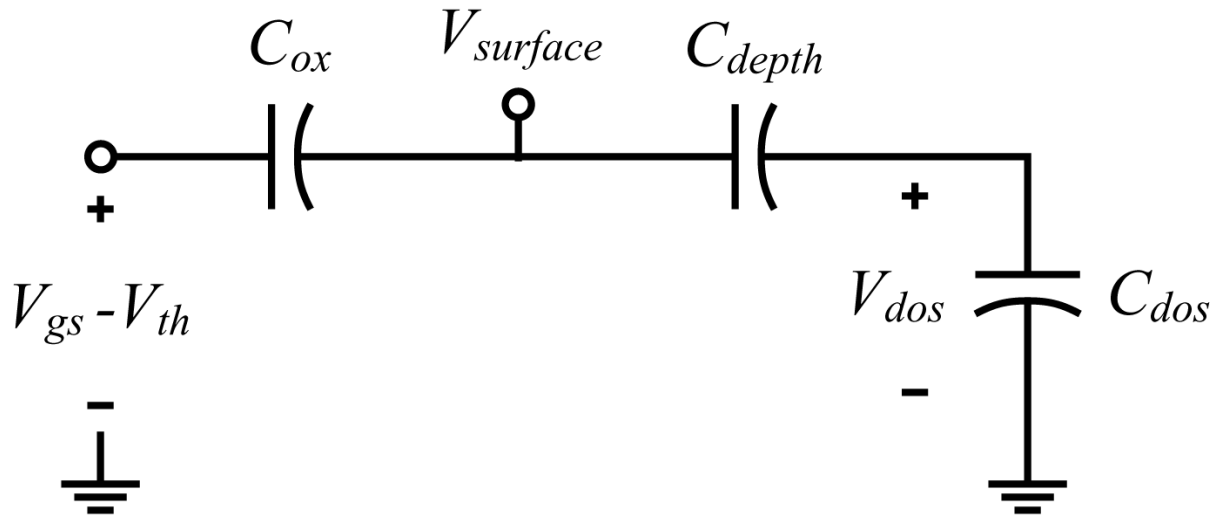
High performance III-V MOS using aggressively scaled ALD dielectrics

FET Device Physics

$$C_{ox} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}}$$

$$C_{depth} \approx \frac{\varepsilon_o \varepsilon_{channel}}{t_{channel}/2}$$

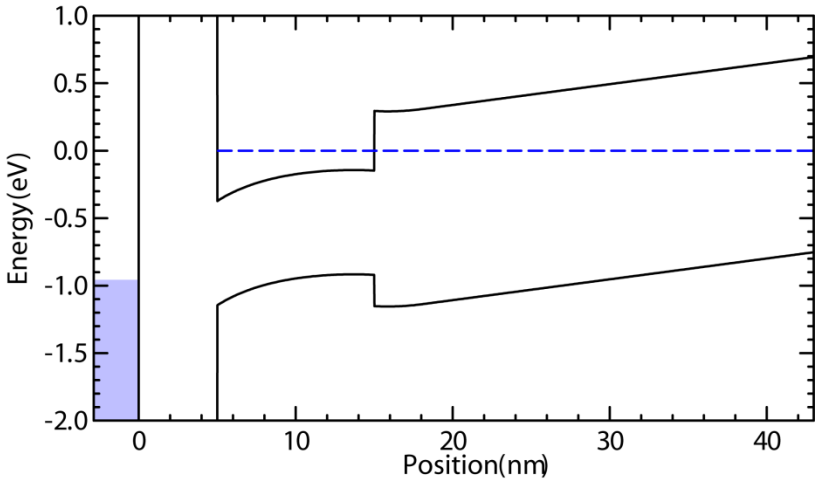
$$C_{dos,2D} = \frac{q^2 g m^*}{\pi \hbar^2}$$



$$n_{channel} = \frac{C_{dos}}{q}(V_{dos})$$

$$J_{drain} = q \cdot n_{s,channel} \cdot v_{sat}$$

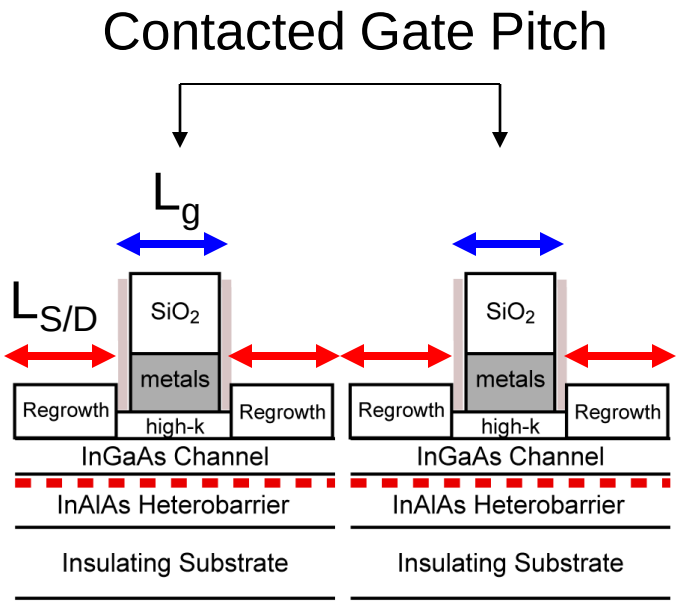
$$g_m = C_{effective} \cdot v_{sat}$$

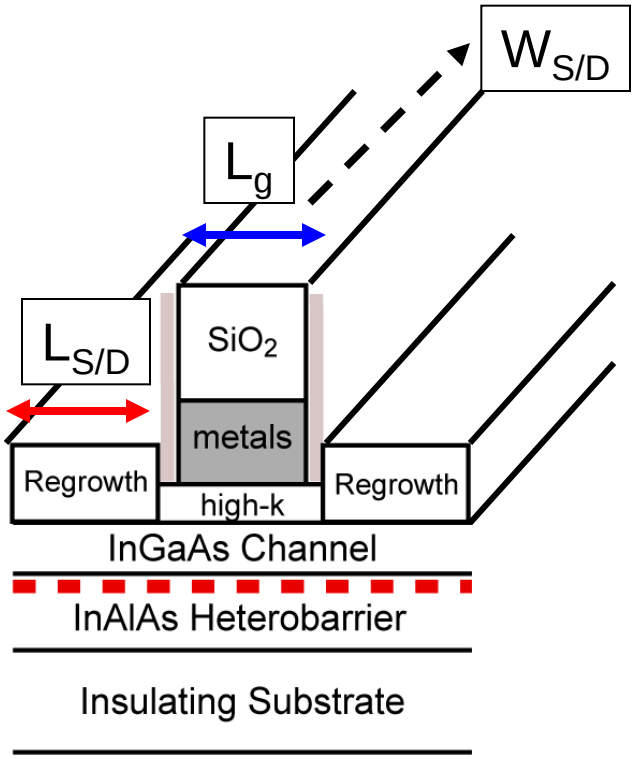


Electron band diagram of a quantum well FET

*$C_{effective}$ includes C_{ox}, C_{depth}, C_{dos}

FET Device Scaling





Si CMOS scaling: Contacted gate pitch 4x the gate length[1)]

4:1 reduction of contact area[2)] → 4:1 reduction of $\rho_{contact}$

22 nm node → 33 nm $L_{S/D}$ → For $L_{S/D} = L_T$, requires 5×10^{-9} ohm-cm^2 $\rho_{contact}$

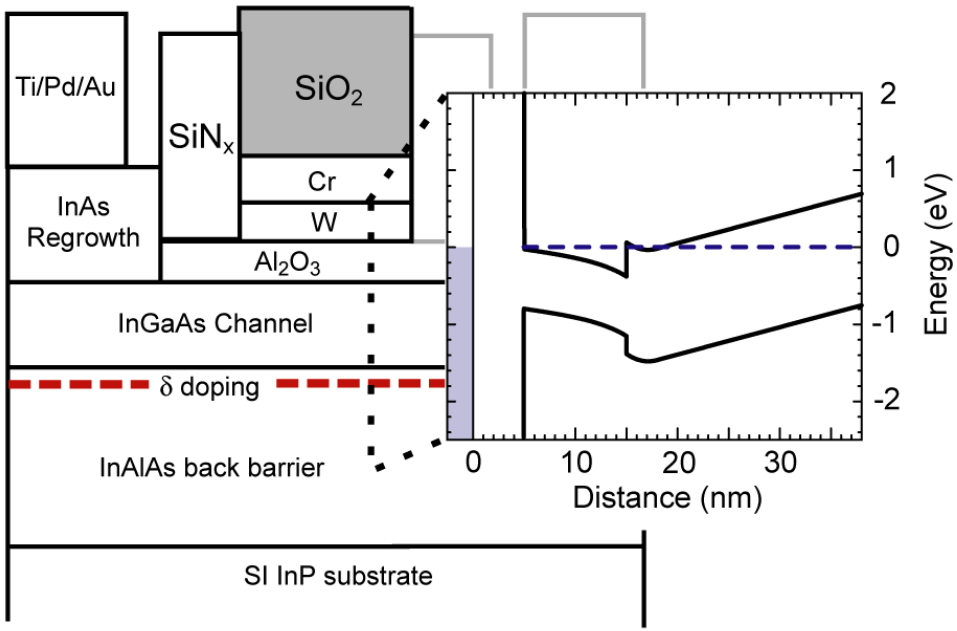
$$\text{Contact Transfer Length} = L_T = \sqrt{\frac{\rho_c}{R_{sh}}}$$

1) S. Natarajan, *et al*, IEDM 2008.

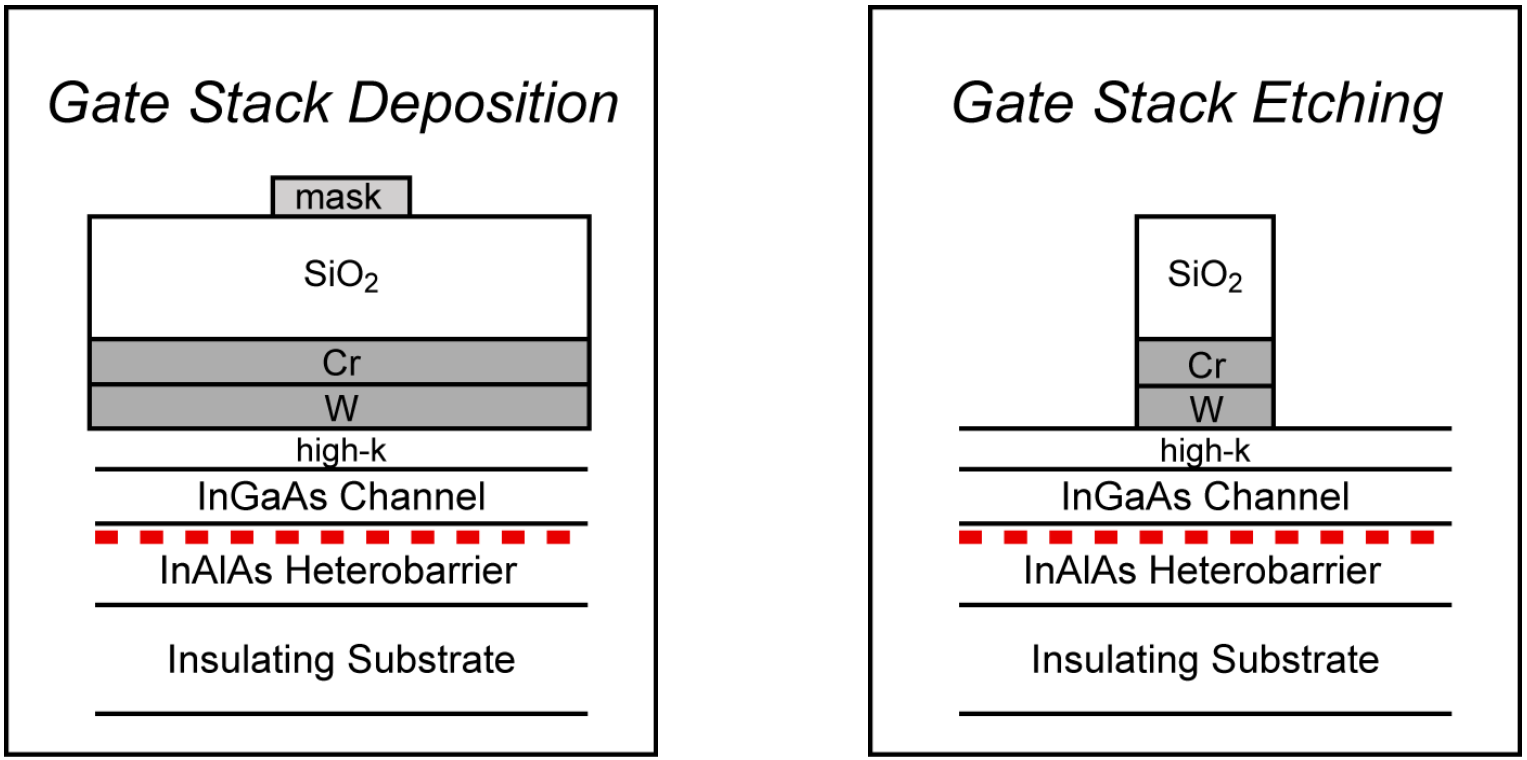
2) M.J.W. Rodwell, *et al*, IPRM 2010.

Gate First FET Process Flow

- Thick (10 nm) channel
  - Process damage mitigation
- Heavy (~ $9x10^{12}$ cm^{-2}) δ doping
  - Prevents ungated sidewall current choke
- $In_{0.52}Al_{0.48}As$ heterobarrier
  - Carrier confinement
- Semi-insulating InP
  - Device isolation



Gate First FET Process Flow



Front End: Gate Stack Definition

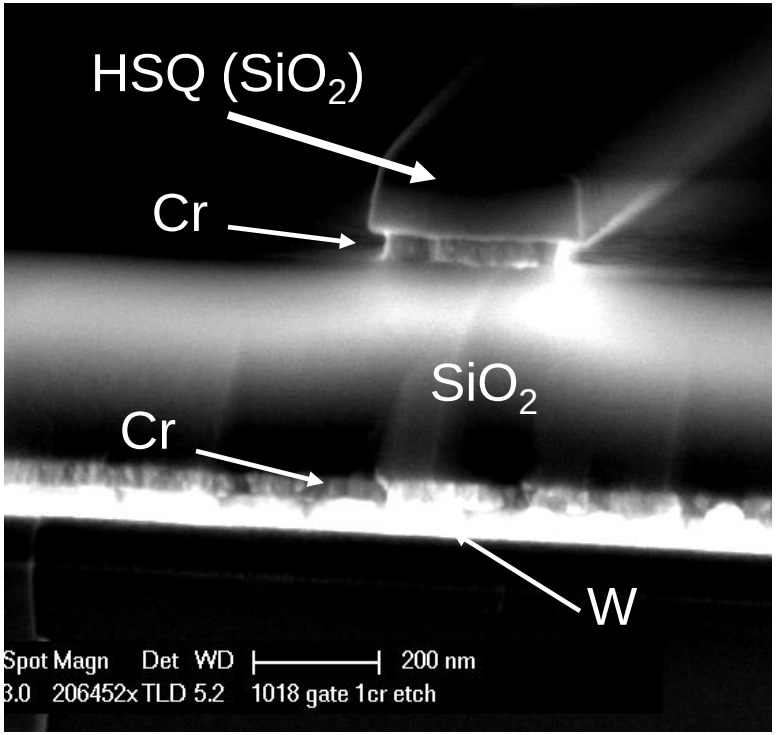
- *In-situ* hydrogen plasma / TMA treatment before Al_2O_3 growth
- Mixed e-beam / optical lithography
- Bi-layer gate (Sputtered W + e-beam evaporated Cr)
  - High selectivity, low power dry etch

FET Process Development

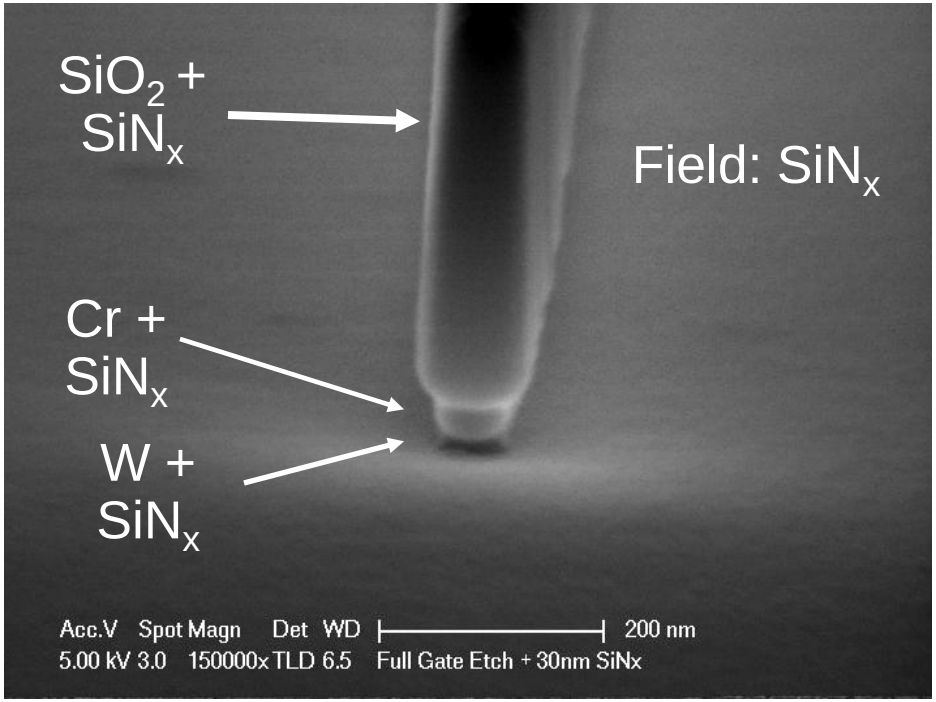
Use optical lithography to produce >0.5um gates

Use electron beam lithography to produce sub-100nm gates

Need to investigate possible e-beam damage to oxides



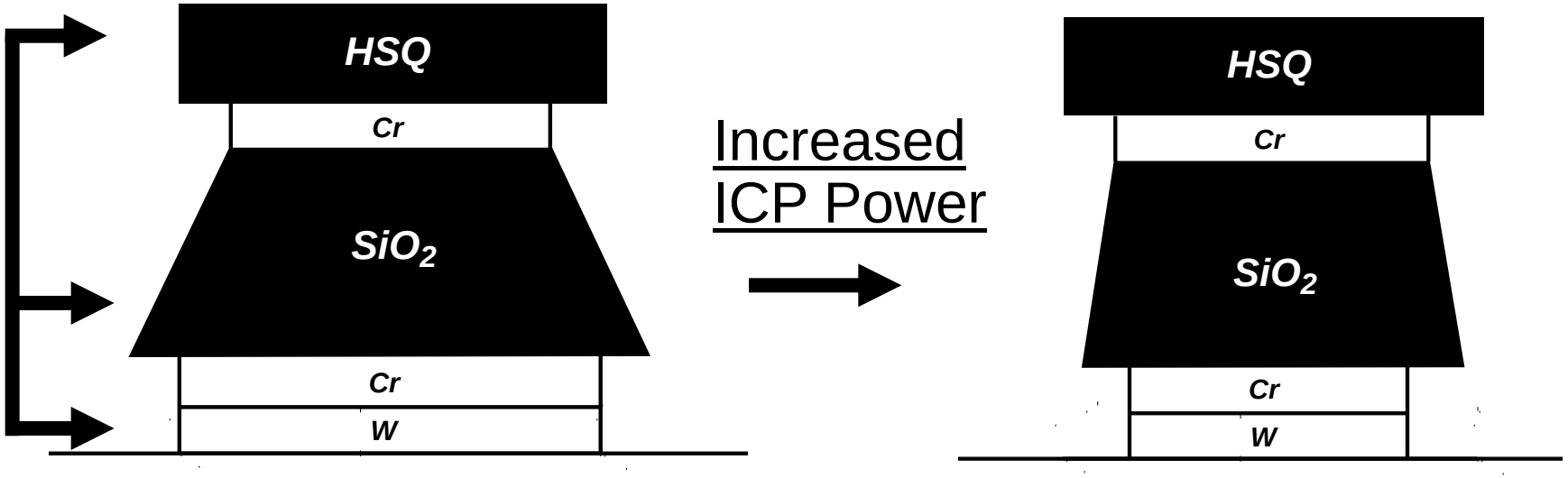
EBL Tests



Finished Gate Etch + Sidewall Deposition

FET Process Development

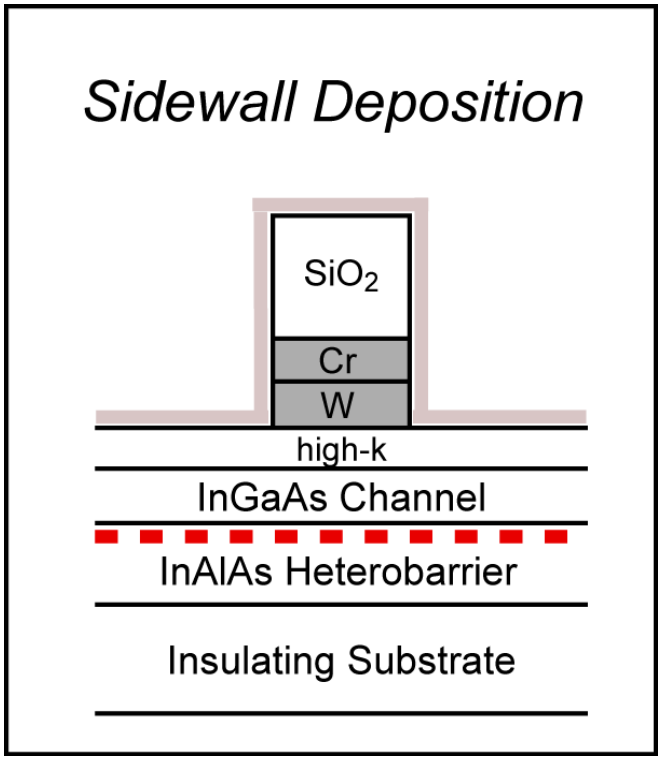
ICP dry etches calibrated to perform at sub-100nm scale

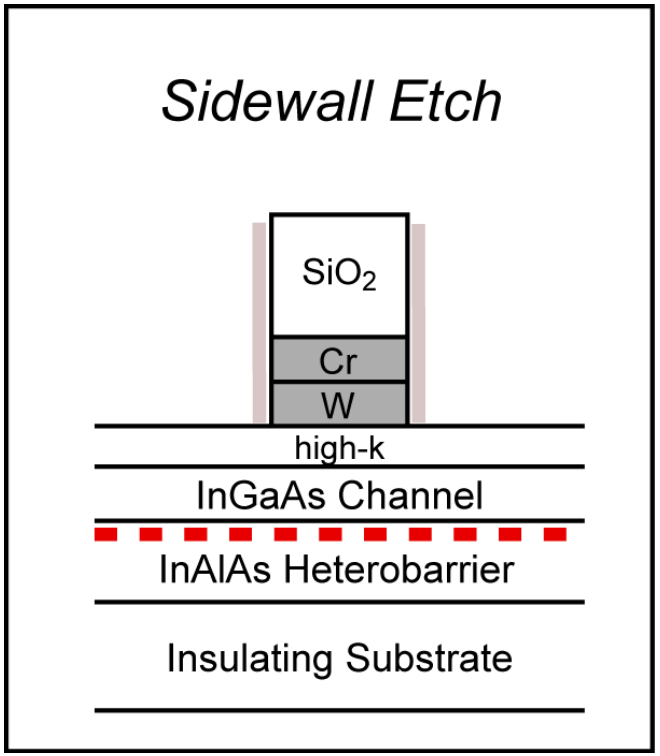


Higher power dry etch → vertical gate stack

Undercutting leads to fallen gates, ungated access regions
→ Minimize Cr undercut by reducing thickness

Gate First FET Process Flow



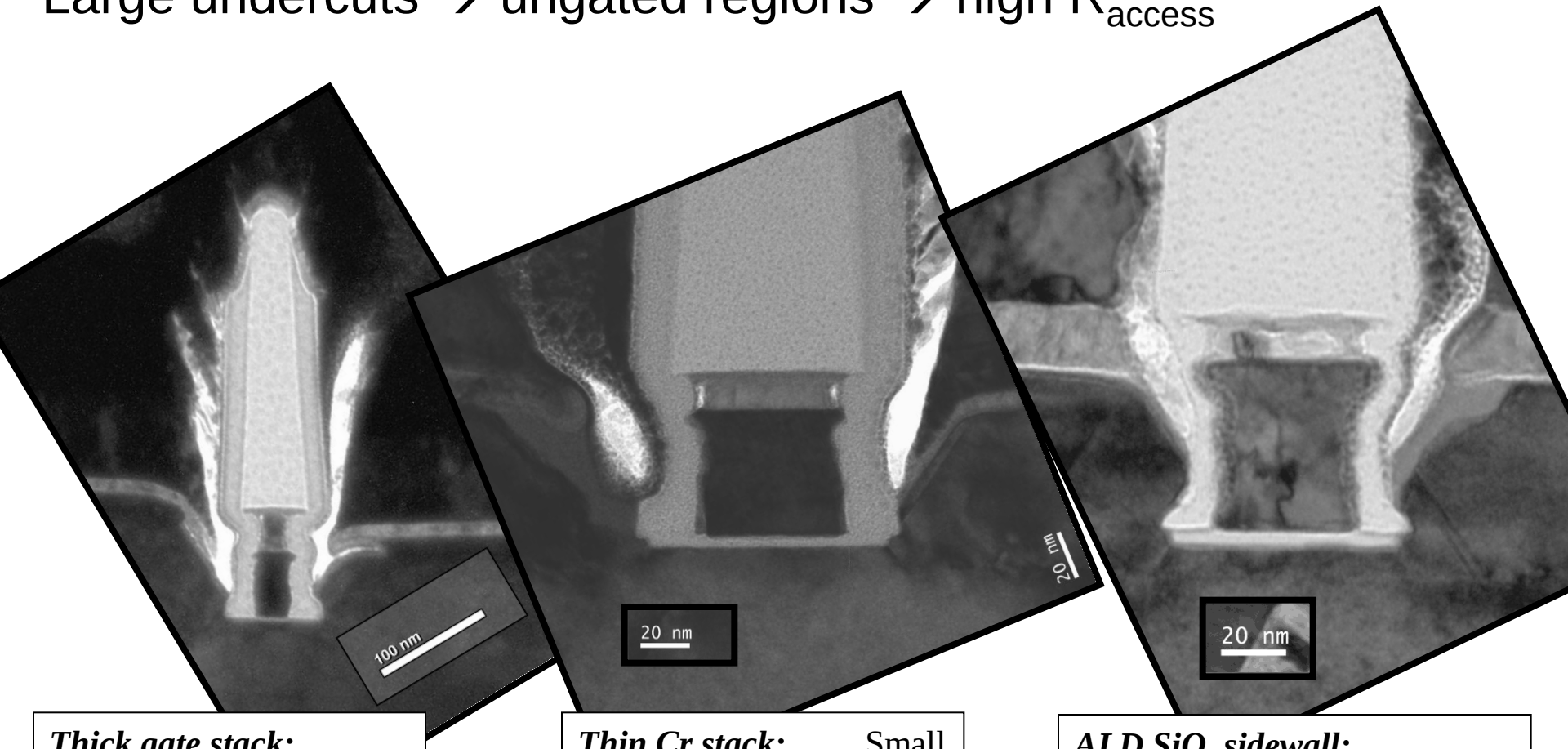


Front End: Gate Stack Definition

- Sidewall Deposition
  - Conformal, protects S/D short circuit to gate
- Sidewall etch
  - Vertical gate stack → self aligned sidewall

FET Process Development

Low power etch → Isotropic etching + undercut → fallen gates
Large undercuts → ungated regions → high R_{access}

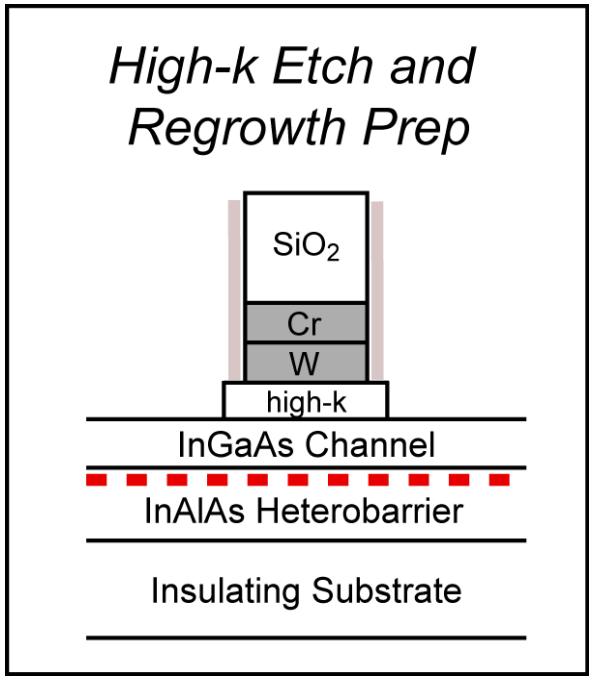


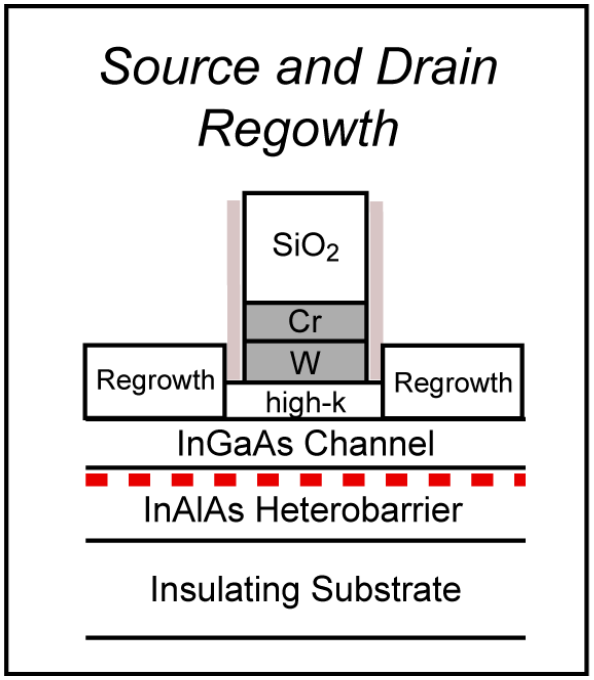
Thick gate stack:
Small L_g ☺
Large sidewall foot ☹
Unreliable gates ☹

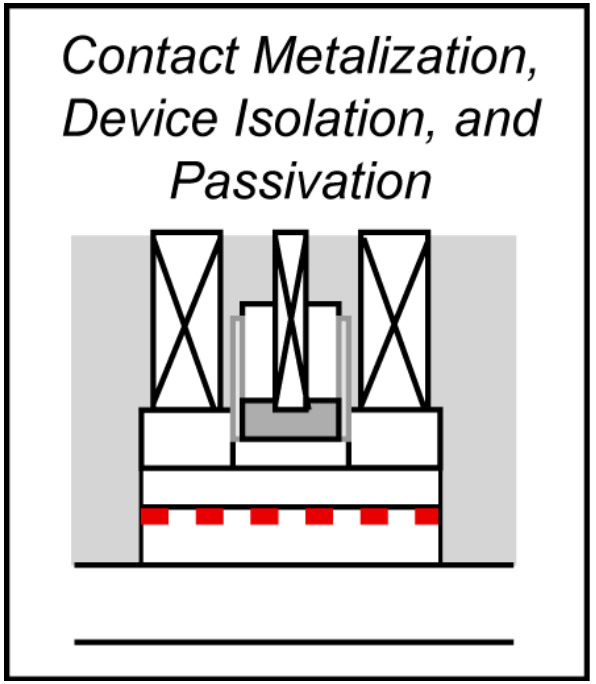
Thin Cr stack: Small L_g ☺ Large sidewall foot ☹
Repeatable gate etch?

ALD SiO_2 sidewall:
Small L_g ☺
Still sidewall foot! ☹
Unrepeatable gate undercut ☹

Gate First FET Process Flow



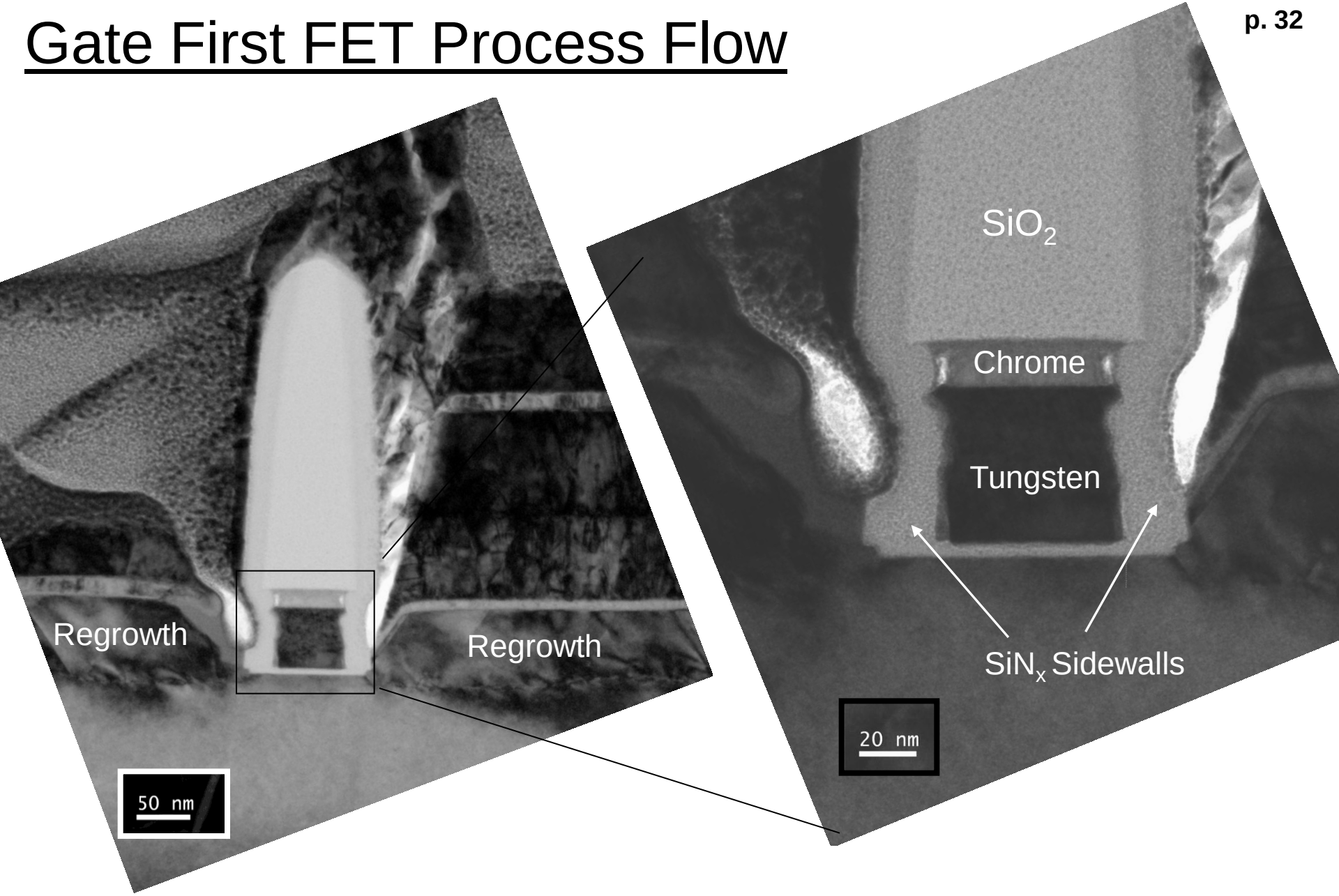




Regrowth and Back End

- Surface preparation
  - UV O_3 exposure to clean the source/drain, removed *ex-situ* before MBE load
- MBE InAs Regrowth
  - Low arsenic flux, high temperature → near gate fill in
- Metallization and Mesa Isolation
  - *In-situ* Mo in MBE optional for lower ρ_c
  - Ti/Pd/Au liftoff
  - Wet etch for mesa isolation

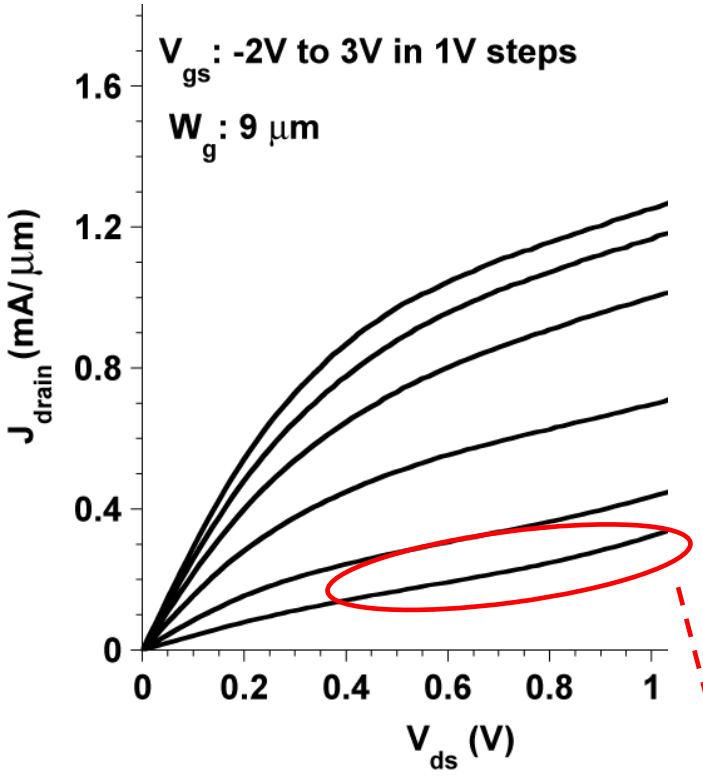
Gate First FET Process Flow



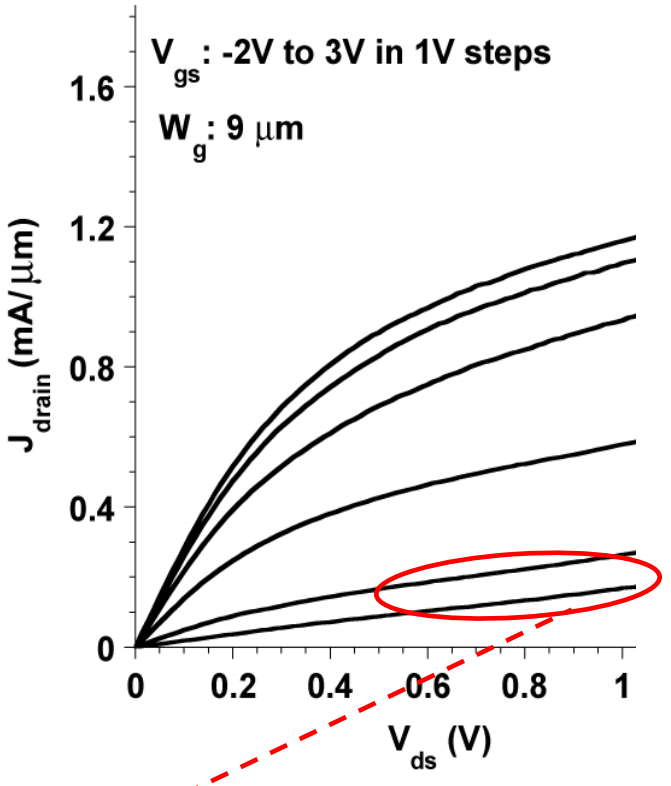
TEM micrographs of 60 nm L_g device

Gate First FET Results

60 nm L_g



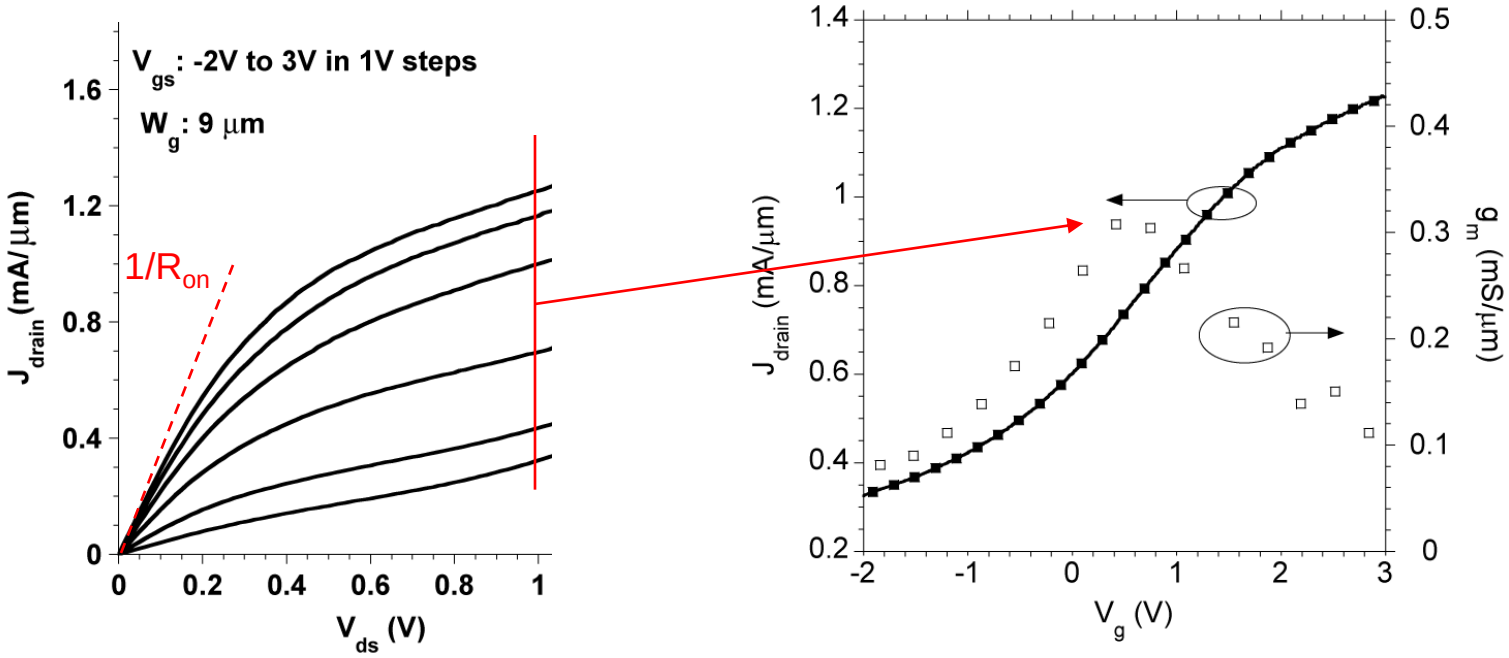
115 nm L_g



Increased leakage current:
Heavy δ doping leakage path
Drain induced barrier lowering

Gate First FET Results

60 nm L_g



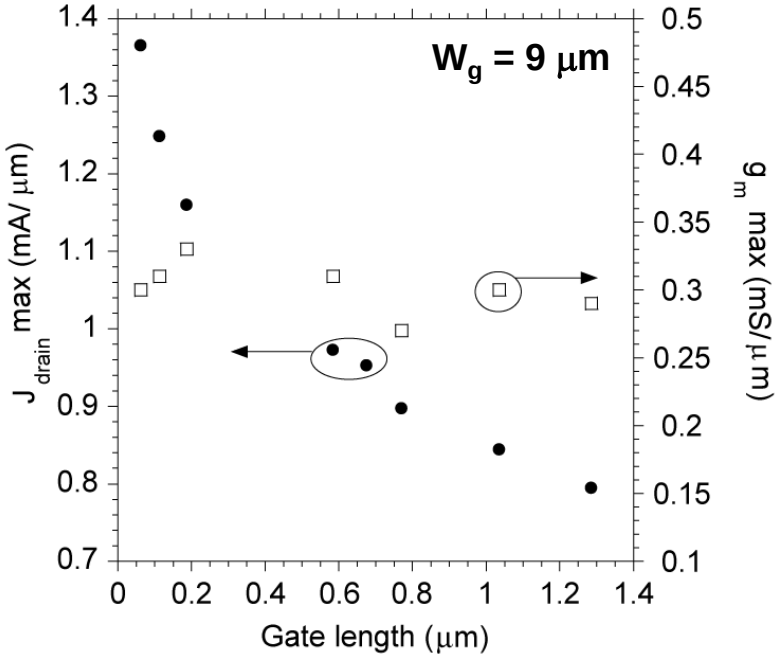
High J_{drain} but depletion mode

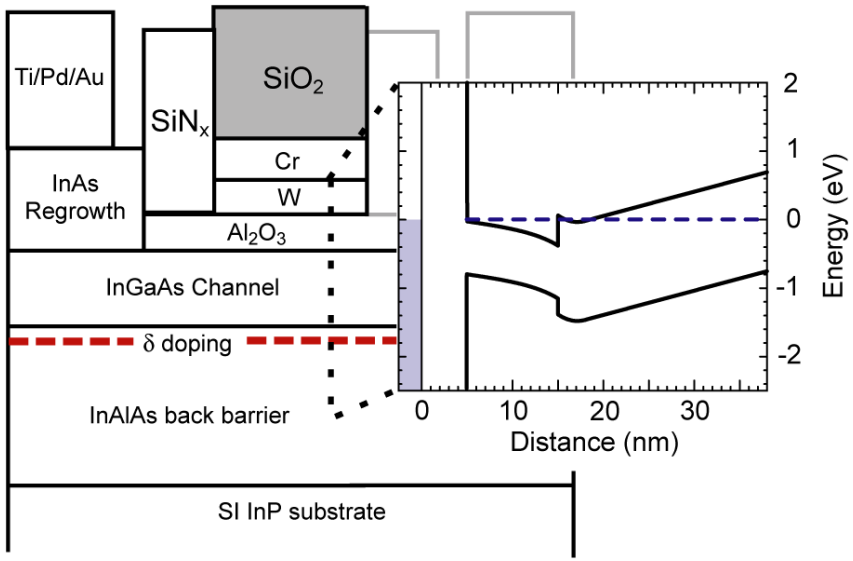
Transconductance: Similar to previous results* (~0.3mS/μm)

Low R_{on} (371 ohm-μm) for InGaAs MOSFETs

*) U. Singisetti *et al, IEEE EDL Nov. 2009.*

Gate First FET Results



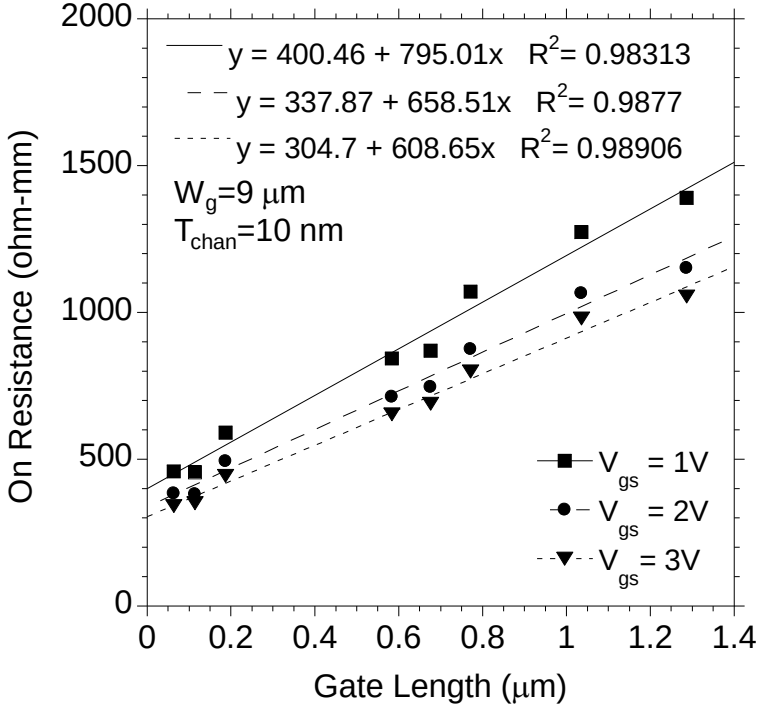


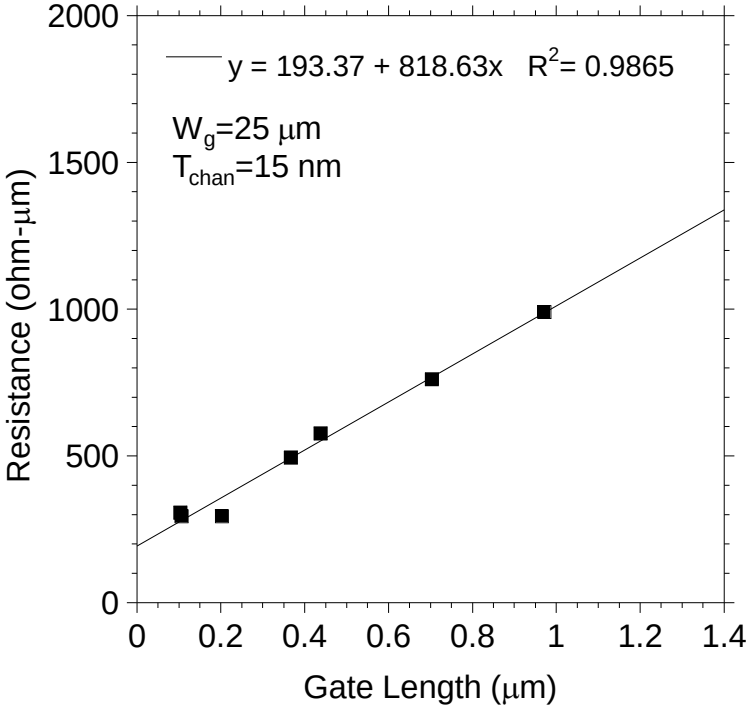
J_{drain} increases rapidly with gate length scaling

Transconductance: Relatively flat with gate length scaling

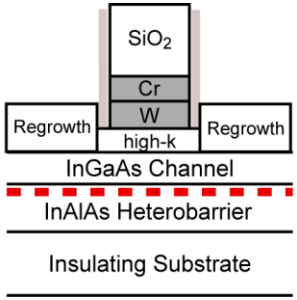
*) U. Singisetti *et al, IEEE EDL Nov. 2009.*

FET: Access Resistance

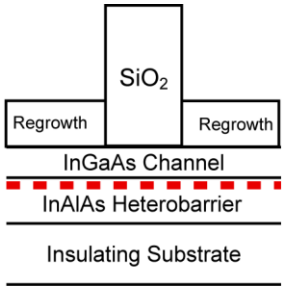




R_{access}: 200 ohm-μm



$$R_{measured} = \frac{R_{sh} L_{gap}}{W} + 2R_{access}$$



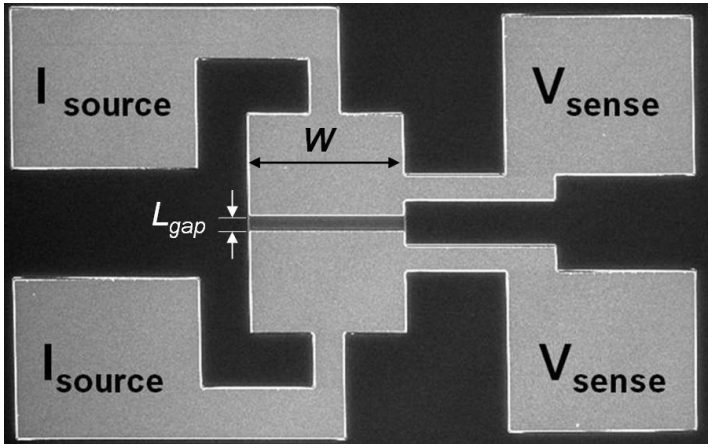
R_{access}: 100 ohm-μm

MOSFET On Resistance

Gateless Transistor Resistance

Gateless transistor effective diagnostic of regrowth

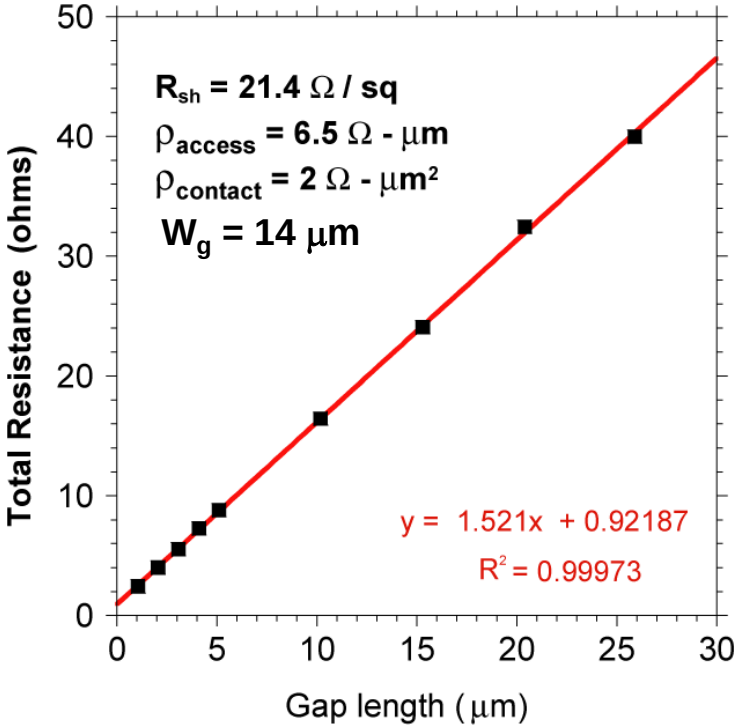
Gate First FET: Metal-Regrowth TLM



$$R_{measured} = \frac{R_{sh} L_{gap}}{W} + 2R_c$$

$$R_c \approx \frac{\rho_c}{L_T W} \text{ for } L > 1.5 L_T$$

$$L_T = \sqrt{\frac{\rho_c}{R_{sh}}}$$



Metal-Regrowth access resistance is not a limiting factor in J_{drain}

Ex-situ Ti/Pd/Au / n-type InAs contacts: $\rho_c = 2 \times 10^{-8}$ ohm-cm^2

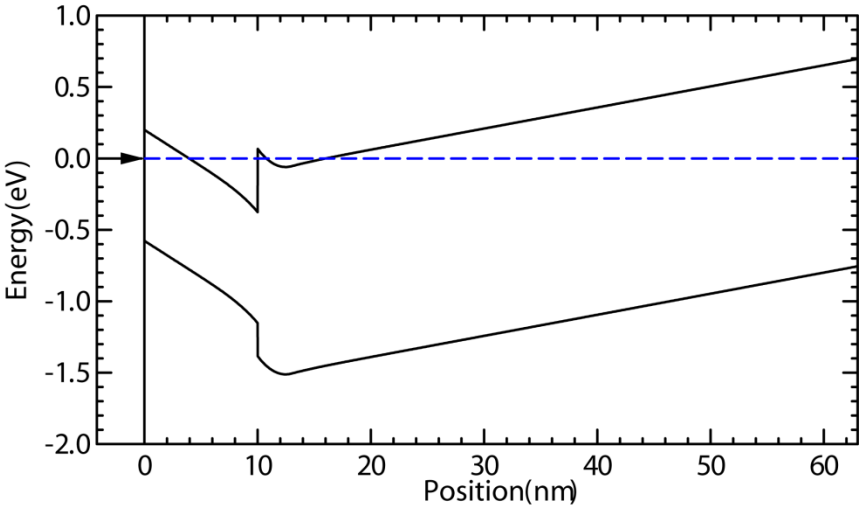
In-situ Mo / n-type InAs contacts have shown $\rho_c = 6 \times 10^{-9}$ ohm-cm^2 *

*) M.J.W. Rodwell, *et al*, IPRM 2010.

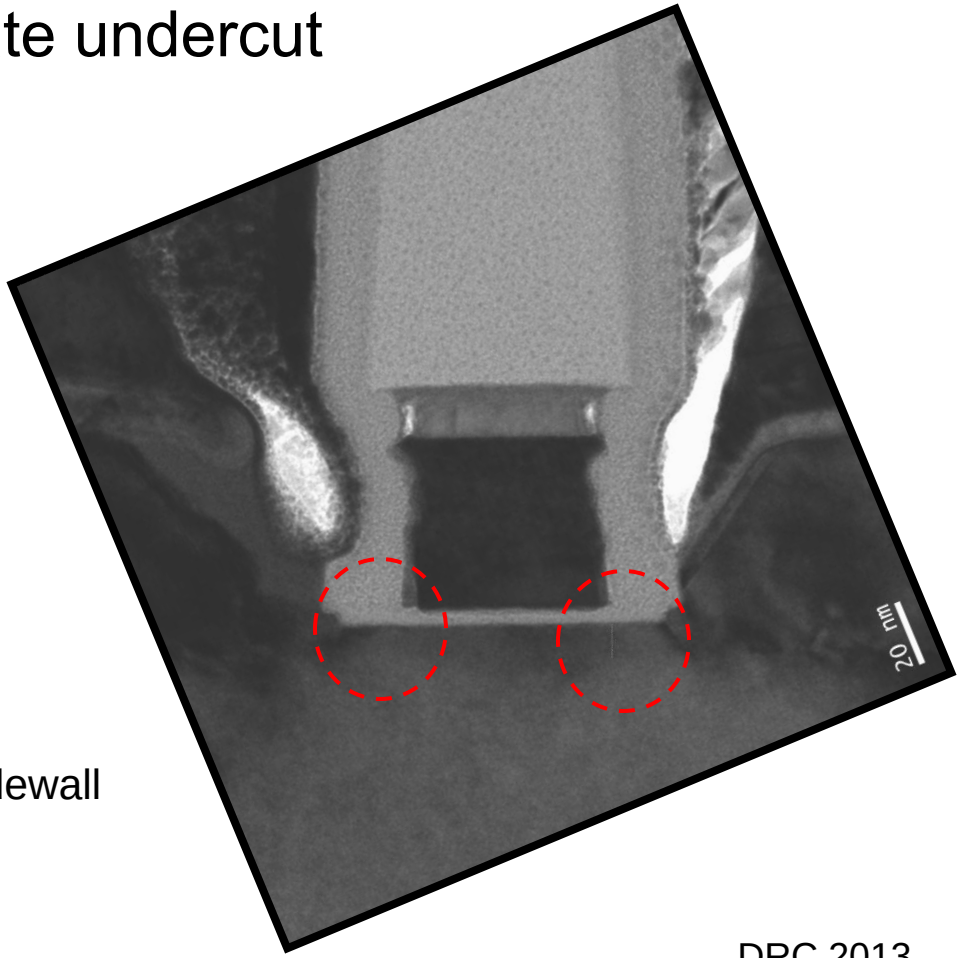
Gate First FET: Issues

Ungated region → potential current choke

- Thinner sidewall can help…
- … but hard to control with gate undercut



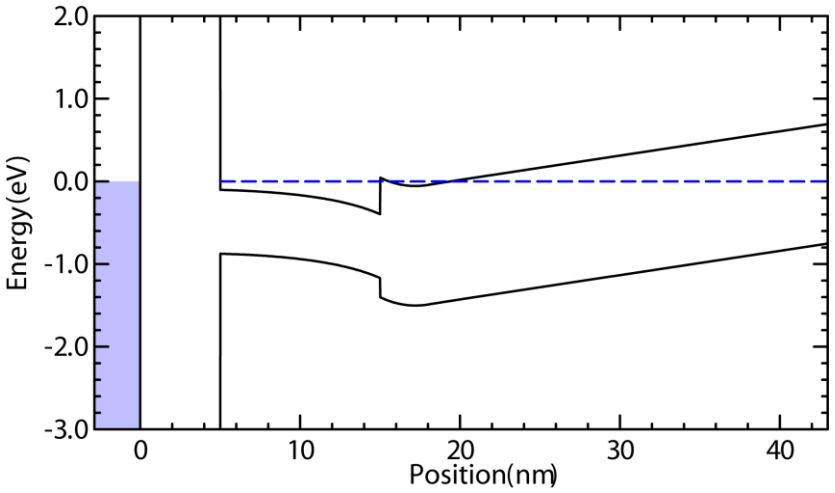
Electron band diagram of channel underneath sidewall



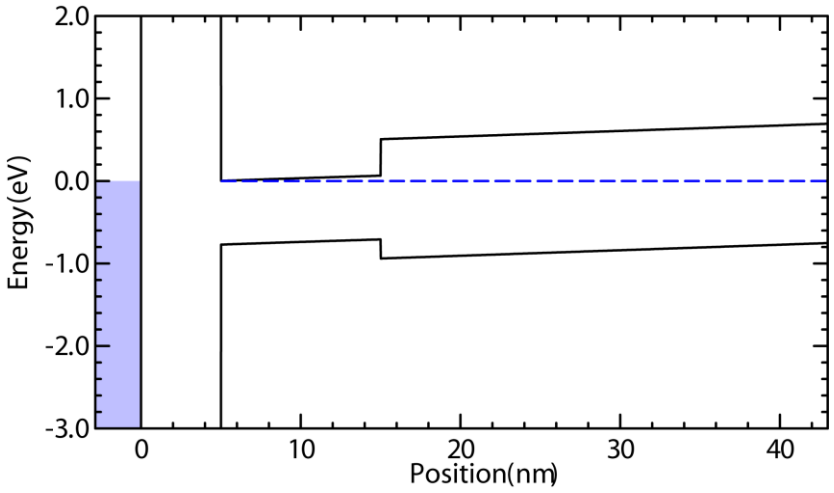
Gate First FET: Issues

Heavy δ doping → parallel conduction, poor g_m

- Large leakage current in device
- Decreases C_{depth} → limits g_m



$9 \cdot 10^{12} cm^{-2}$ δ doping



no δ doping

Must reduce δ doping while maintaining low R_{access}

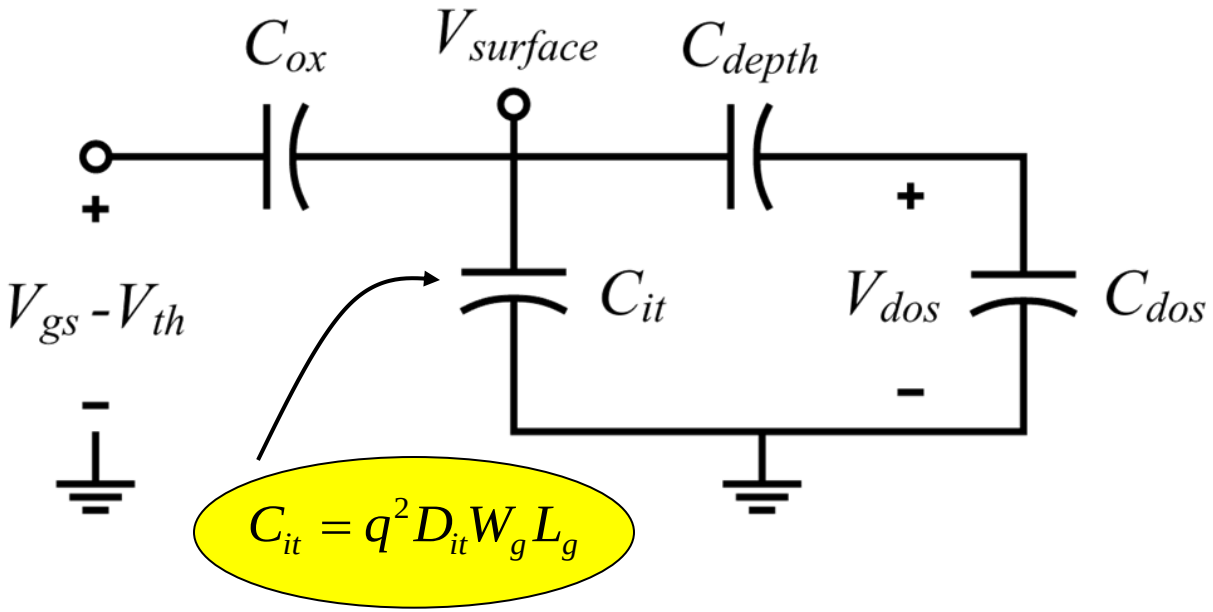
FET Device Physics

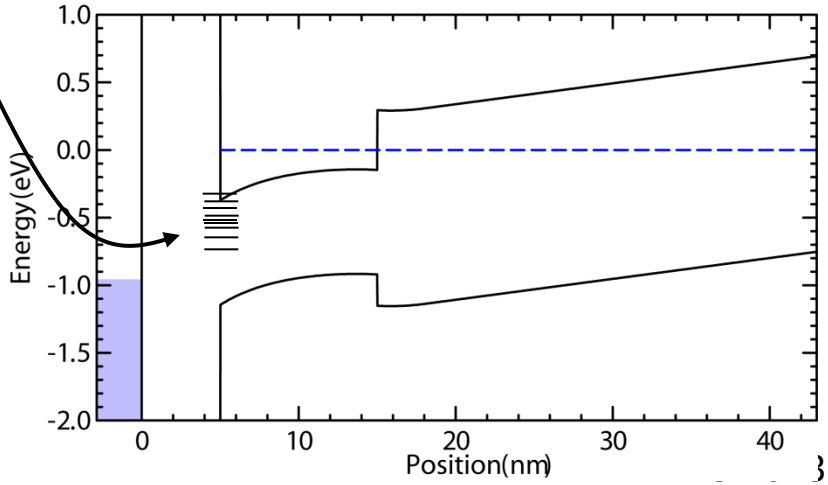
$$C_{ox} = \frac{\varepsilon_o \varepsilon_r L_g W_g}{t_{ox}}$$

$$C_{depth} \approx \frac{\varepsilon_o \varepsilon_{channel} L_g W_g}{t_{channel}/2}$$

$$C_{dos} = \frac{q^2 gm^*}{\pi \hbar^2} L_g W_g$$

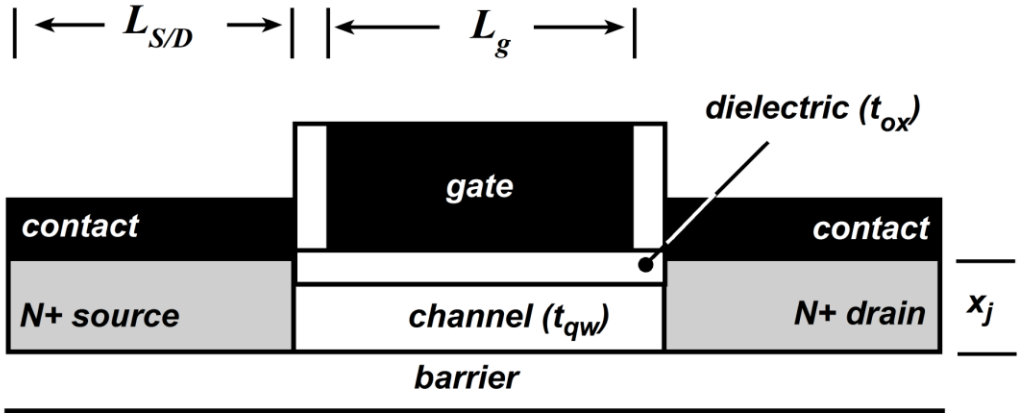
$$n_{channel} = \frac{C_{dos}}{q}(V_{dos})$$





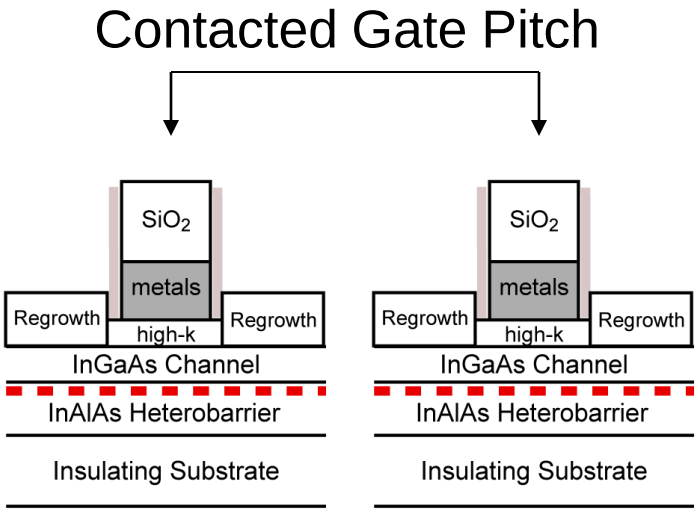
- *Dit* problem
  - ↑*Cit* , ↓ *Vsurface*
  - *Vsurface* also supplies *Cdos*
  - ↓ *Vsurface* =↓ *ndos* in *Cdos*

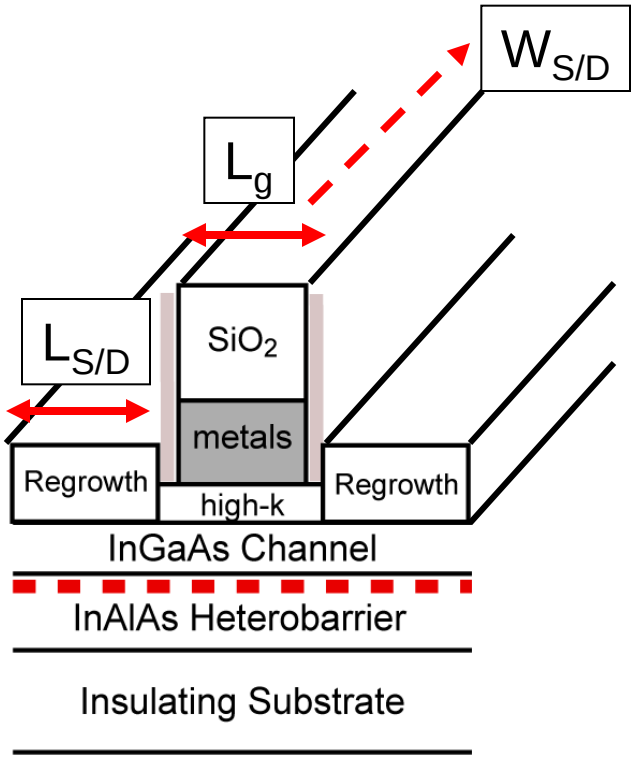
FET Device Scaling



FET parameters	*Scaling Rule*	*How?*
Current Density $(mA/\mu m)$, g_m $(mS/\mu m)$	increase 2:1	
Gate Length and Contact Spacing (L_g,$L_{S/D}$)	decrease 2:1	Lithographic Scaling
Channel Electron Density	increase 2:1	Channel Material and Orientation
Electron Transport Mass ($m^*_{transverse}$)	constant	Channel Material and Orientation
Gate Capacitance	increase 2:1	
Channel Density of States	increase 2:1	Channel Material and Orientation
Channel Thickness (T_{inv})	decrease 2:1	Materials Engineering
Effective Oxide Thickness (T_{ox})	decrease 2:1	Materials Engineering
Source/Drain Contact Resistivity	decrease 4:1	Materials Engineering

FET Device Scaling





- 5 nm channel, 500 $cm^2/(V*s)$ mobility, 5E19 cm^{-3} carriers = 500 ohm/sq
- 5E-9 ohm cm^2 contact resistance
- $L_{transfer}$ ~ 31 nm

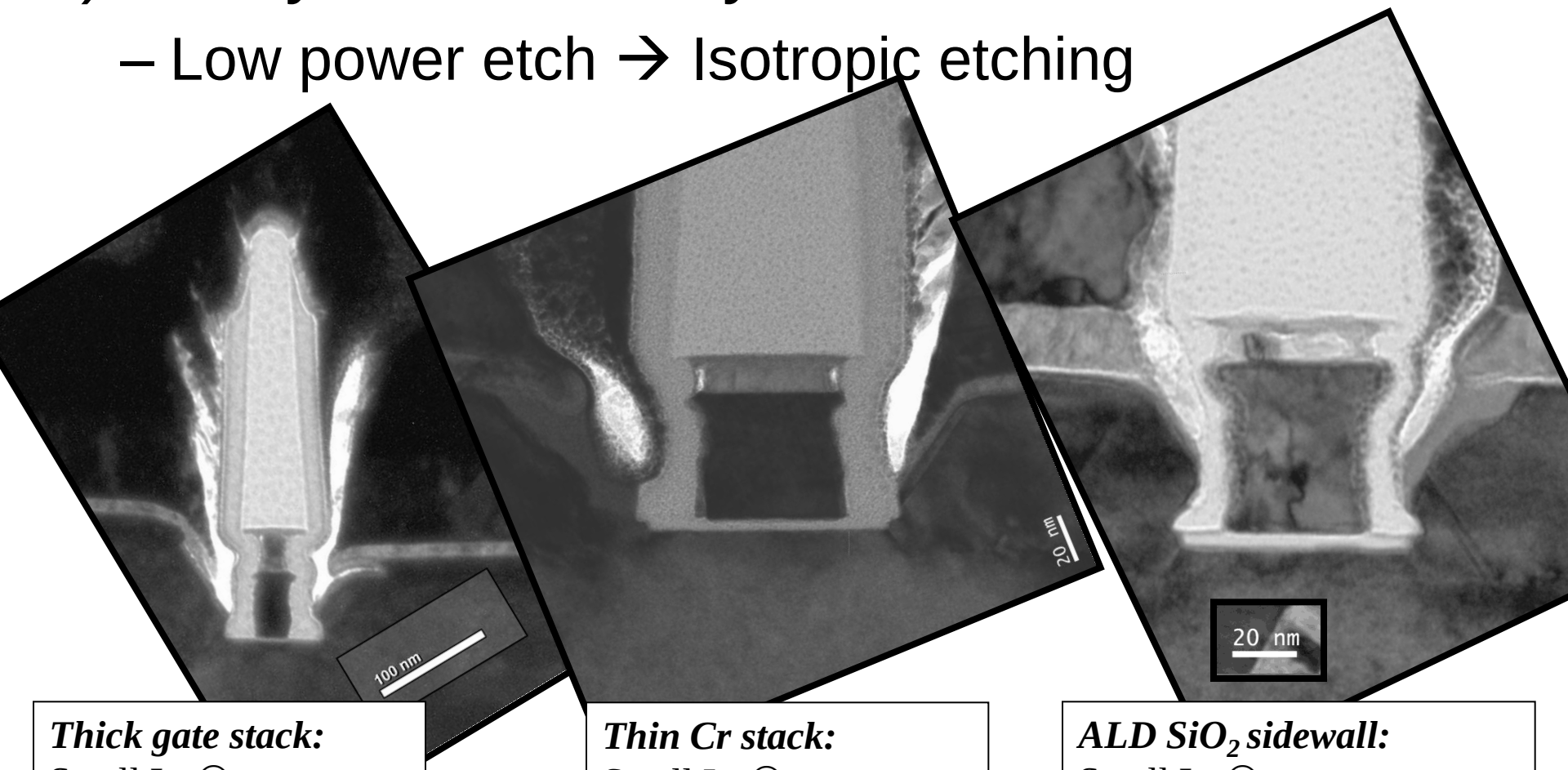
$$\text{Contact Transfer Length} = L_T = \sqrt{\frac{\rho_c}{R_{sh}}}$$

1) S. Natarajan, *et al*, IEDM 2008.
2) M.J.W. Rodwell, *et al*, IPRM 2010.

FET Process Development

1) Poorly controlled dry etch undercut

– Low power etch → Isotropic etching



Thick gate stack:
Small L_g ☺
Large sidewall foot ☹
unreliable gates ☹

Thin Cr stack:
Small L_g ☺
Large sidewall foot ☹
Reliable gate etch?

ALD SiO_2 sidewall:
Small L_g ☺
Still sidewall foot! ☹
Unreliable gate undercut ☹