Record Extrinsic Transconductance (2.45 mS/μm at V_{DS} = 0.5 V) InAs/$In_{0.53}Ga_{0.47}As$ Channel MOSFETs Using MOCVD Source-Drain Regrowth

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Outline

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- Process Flow
- Key Process Developments
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  - I-V Characteristics
  - Gate leakage & TLM measurement
  - Peak g_m and R_{on} VS L_g (Benchmarking)
- Conclusion

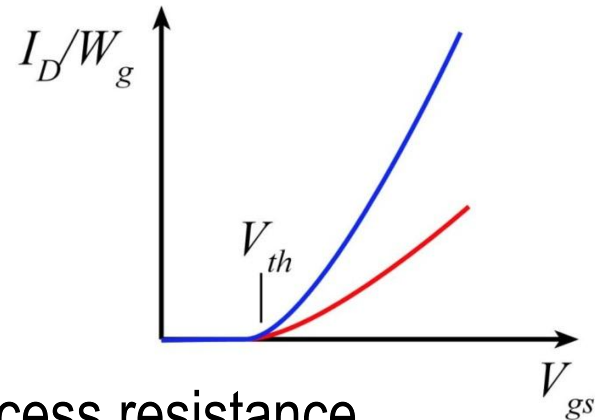
Why III-V MOSFETs in VLSI ?

more transconductance per gate width

more current (at a fixed V_{dd})⟶ IC speed

or reduced V_{dd} (at a constant I_{on})⟶ reduced power

or reduced FET widths⟶ reduced IC size



increased transconductance from:

low mass⟶ high injection velocities

lower density of states⟶ less scattering

higher mobility in N+ regions ⟶ lower access resistance

Other advantages

heterojunctions⟶ strong carrier confinement

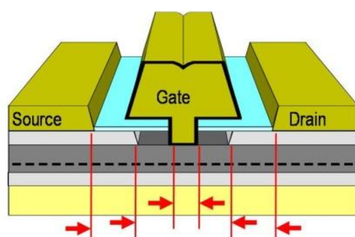
wide range of available materials

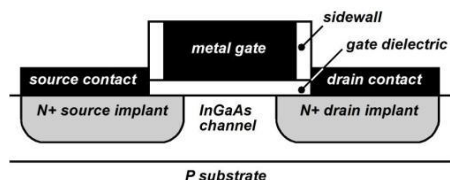
epitaxial growth⟶ atomic layer control

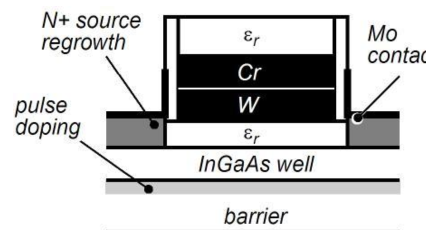
Key Design Considerations

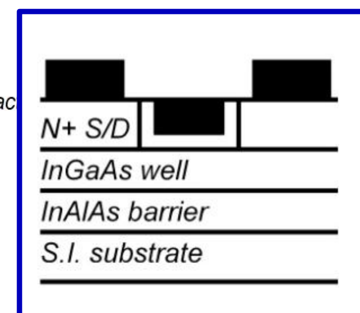
Device structure:

Scalability (sub 20 nm-L_g ,<30 nm contact pitch) : self-aligned S/D, very low ρ_c
Carrier supply: heavily doped N+ source region
Shallow junction: regrown S/D or Trench-gate









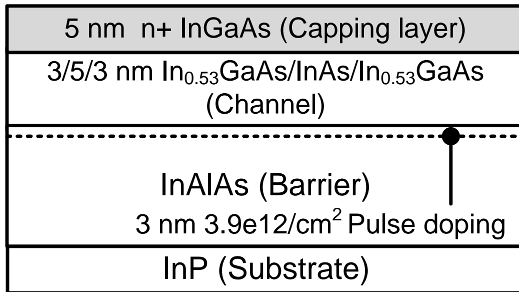
Channel Design:

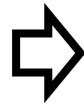
Thinner wavefunction depth: Thin channel
More injection velocity: higher In-content channel

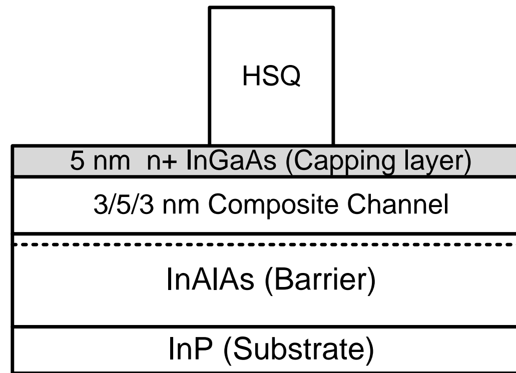
Gate Dielectric:

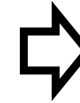
Thinner EOT : scaled high-k dielectric
Low D_{it} : surface passivation, minimized process damage

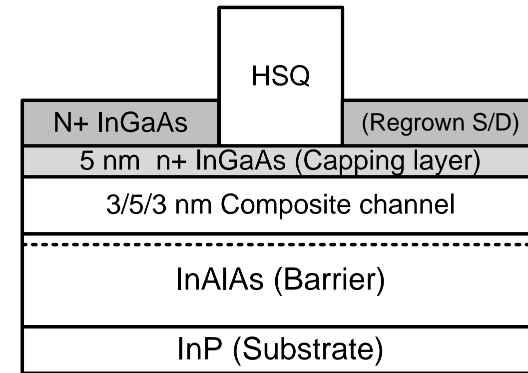
Process Flow



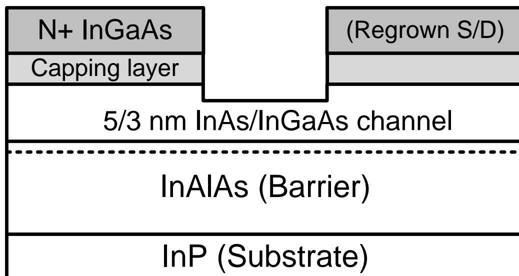


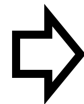


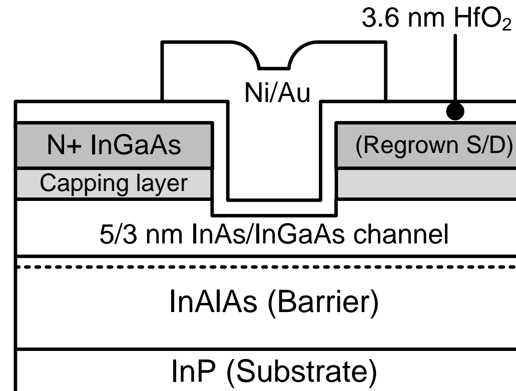


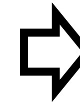


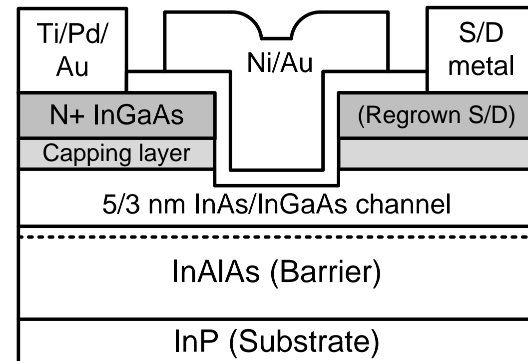
- Epitaxial layer growth using MBE
- Dummy gate definition using e-beam lithography
- N+ InGaAs S/D regrowth using MOCVD











- Dummy gate removal
- Capping layer digital etching

- High-k deposition
- Post Deposition Annealing
- Gate metal deposition

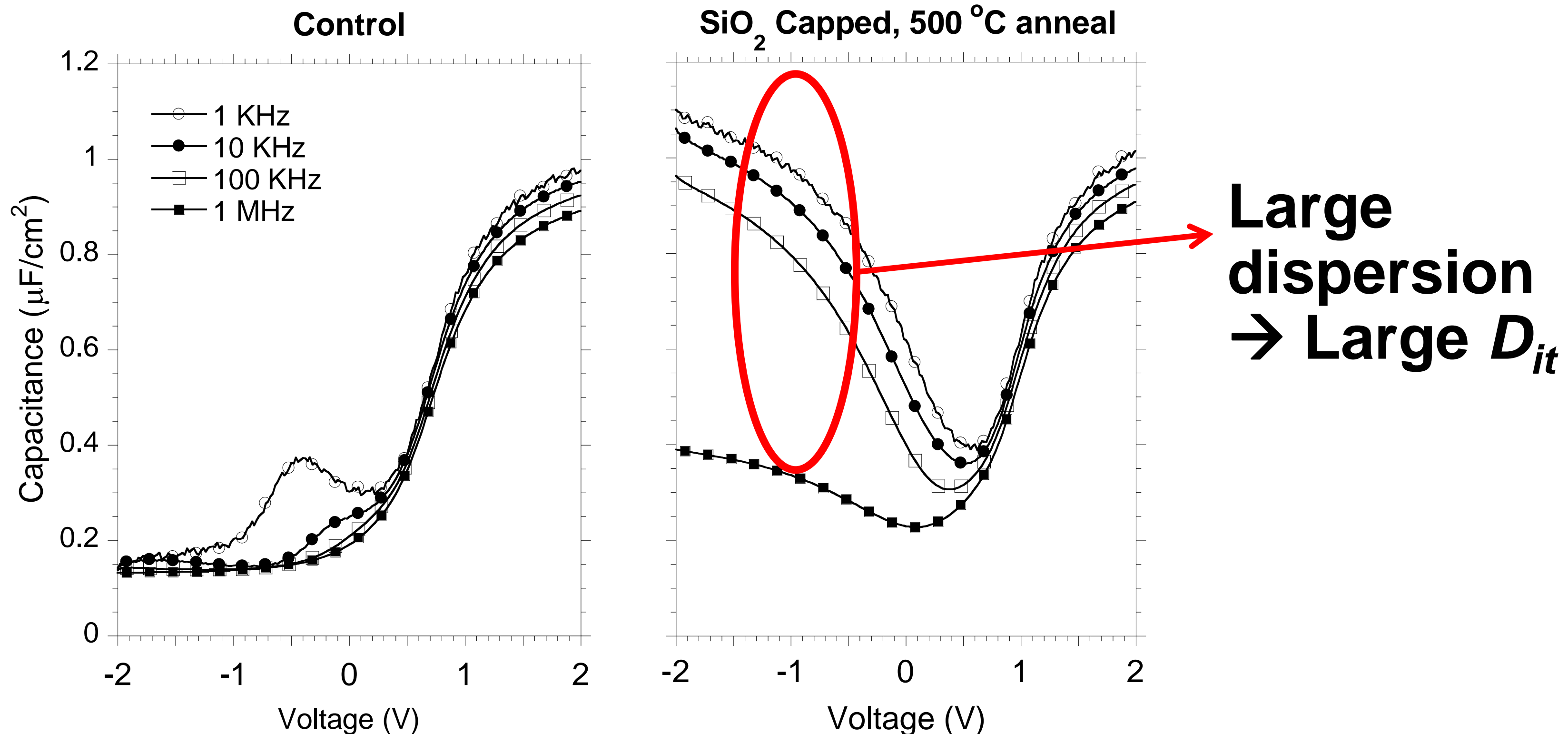
- S/D metal deposition

Evidence of Surface Damage During Regrowth

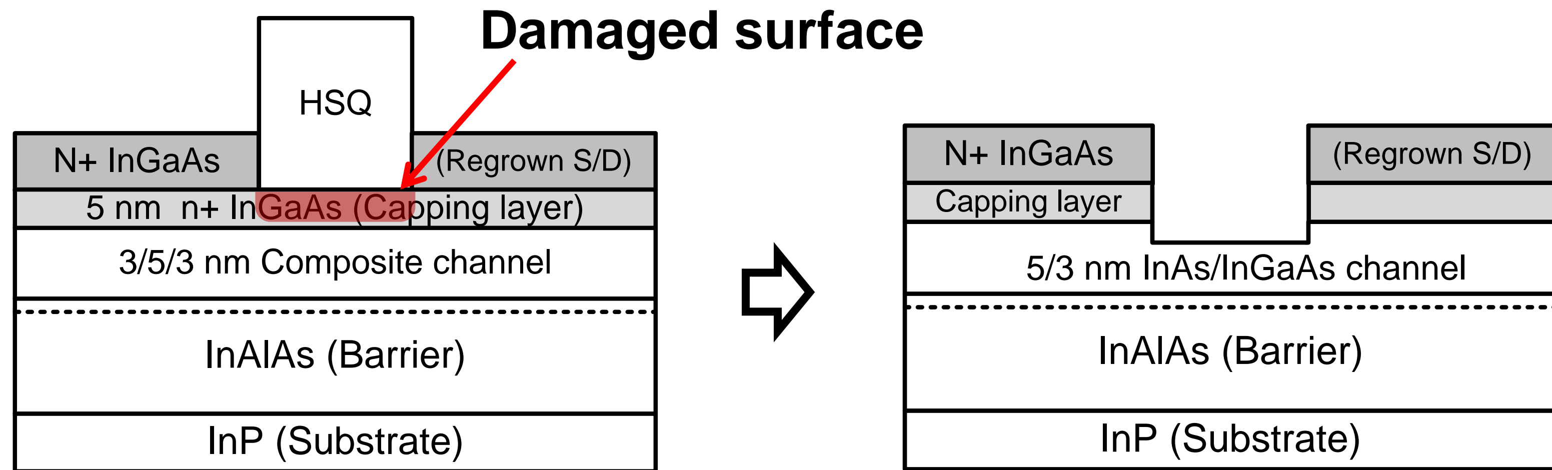
Long-channel FETs: consistently show >100 mV/dec. subthreshold swing
Indicates high D_{it} despite good MOSCAP data. Suggests process damage.

Experiment: SiO_2 capping + high temp anneal + strip → MOSCAP Process

Finding: large degradation in MOSCAP dispersion.
Confirms process damage hypothesis.



Post-Regrowth Surface Digital Etching for Damage Removal



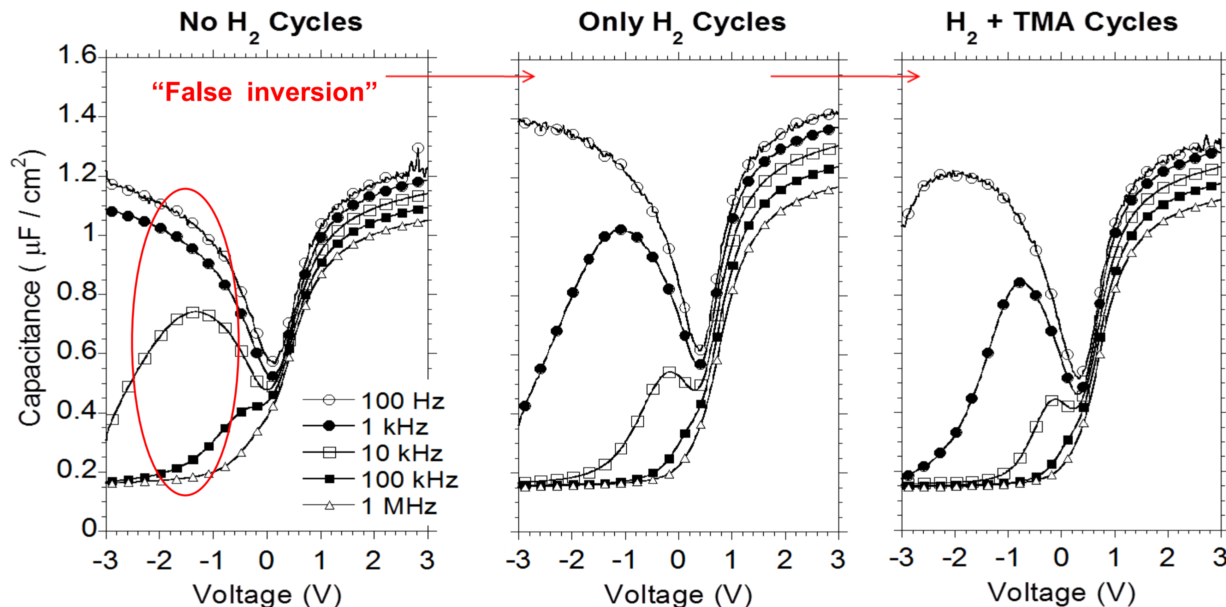
- **Surface removed by digital etch process**

  # cycles: 15' UV ozone (surface oxidation)
  1' dilute HCl (native oxide removal)
  ➔ 13 - 15 Å/cycle, ~0.16 nm RMS roughness

- **Etch significantly improves swing and transconductance**

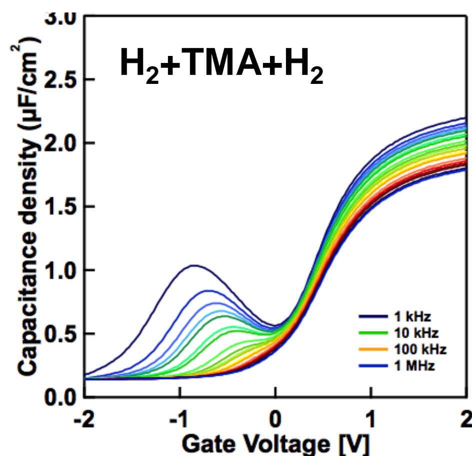
- **Using this technique, the upper cladding of the composite channel is removed**

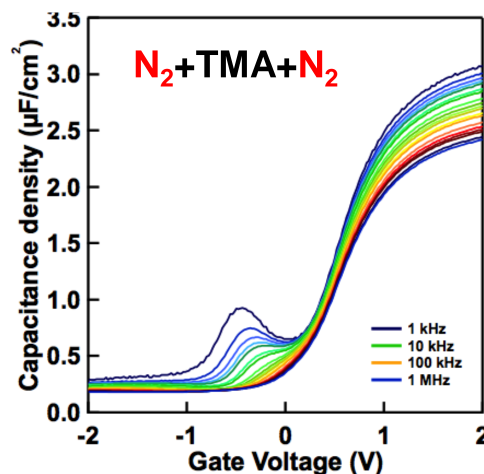
D_{it} Passivation : In-situ N_2 plasma and TMA pretreatment



- Cyclic H_2 plasma and TMA treatment ➔ D_{it} passivated

(A. Carter et al., APEX 2012)



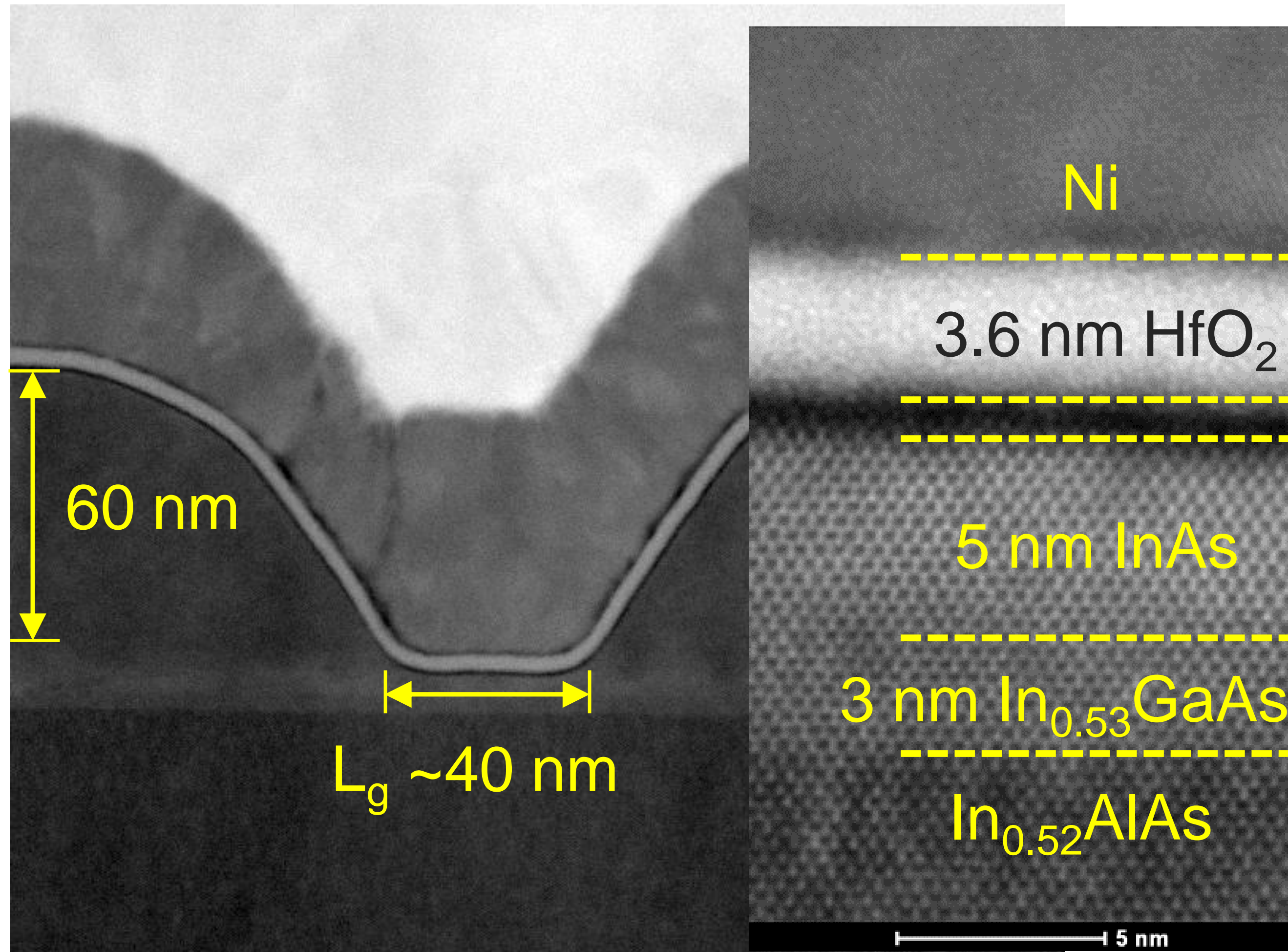


- Lower Midgap D_{it} for N_2 plasma pretreatment

- Al_2O_3 interfacial layer is not needed

(V. Chobpattana, et al. APL 2013)

Cross-sectional STEM image

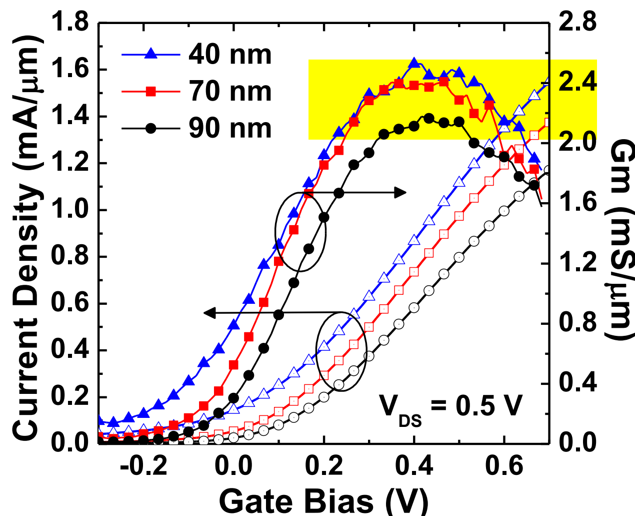


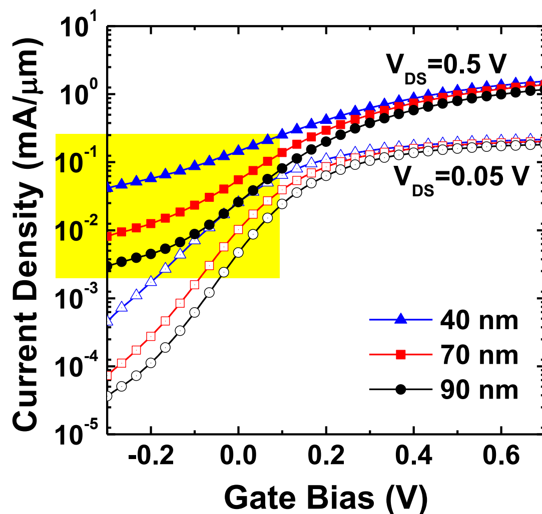
8 nm channel (5 nm/3 nm InAs/$In_{0.53}GaAs$) ; The InAs channel is not relaxed

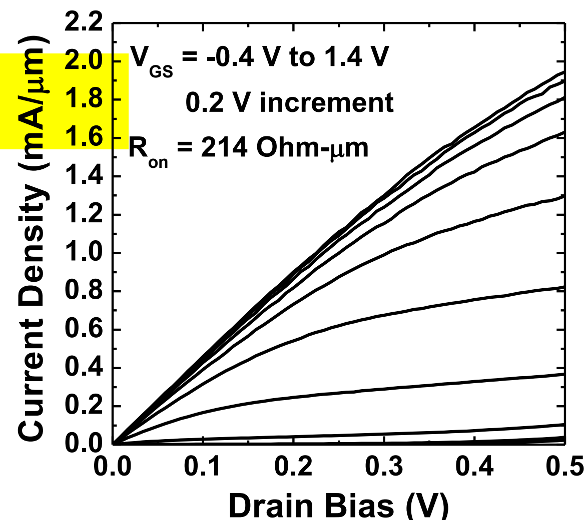
~ 3.5 nm HfO_2 and ~0.5 nm interfacial layer formed by cyclic N_2 and TMA treatment

I-V characteristics for short and long channel devices

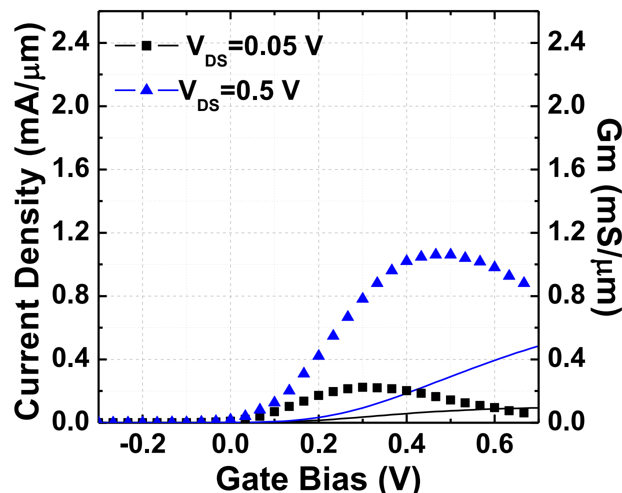
W = 10.1 µm , L = 40 nm / 70 nm / 90 nm

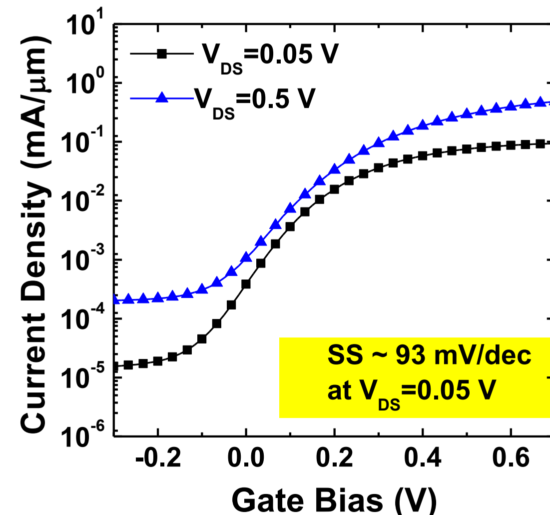


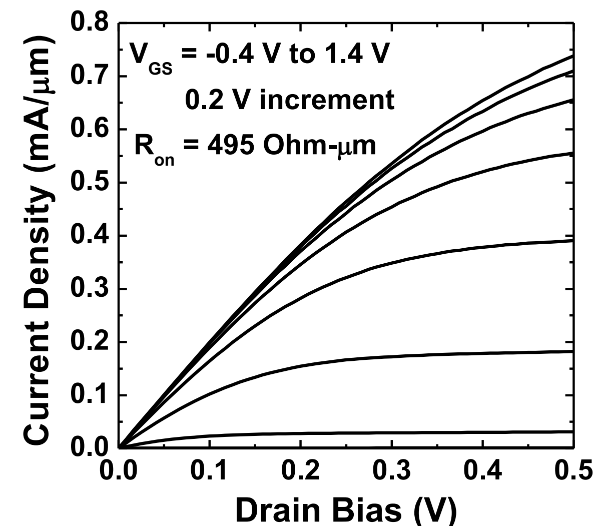




W = 10.1 µm , L = 510 nm

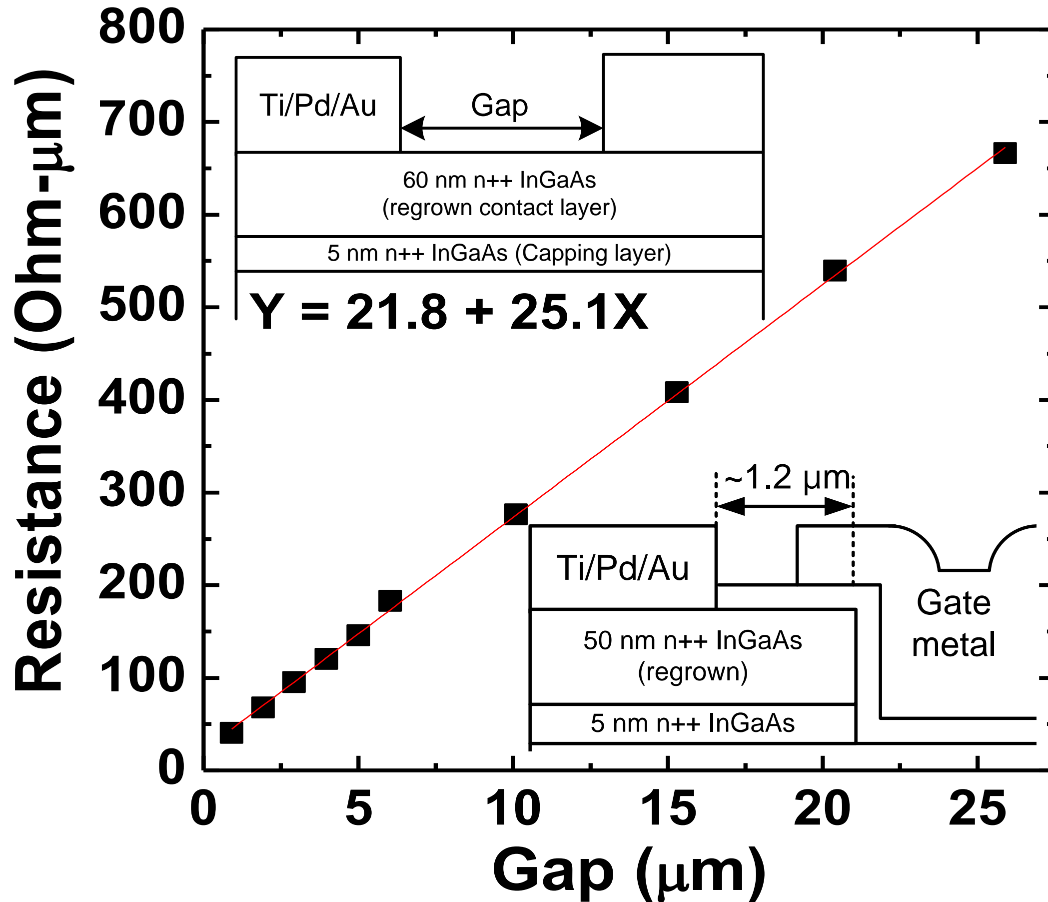


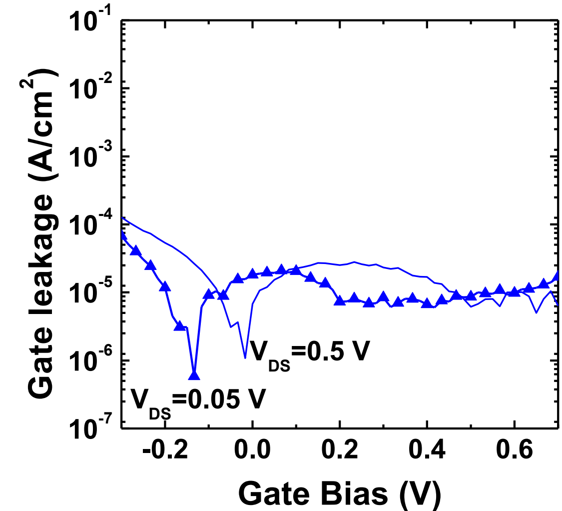




~2.45 mS/µm Peak Gm at V_{DS}=0.5 V , 93 mV/dec long-channel SS

Gate leakage, access resistance, g_m uniformity





A	mS/um	At Vgs=0.5V		2.3	X	2.1
B			2.25	2.2	X	2.3
C		2.2	2.2	2.15	2.3	2.3
D	2.3	2.2	2.2	X	2.3	2.3
E	2.2	2.2	2.25	2.2	2.3	2.4
F	X	2.2	2.2	2.3	2.3	2.4
	1	2	3	4	5	6

R_{sheet} = 25 ohm/sq ρ_c= ~4.7 ohm-µm^2 ; ~82 Ohm-µm R_{SD} : ~8% degradation

gate leakage <10^{-4} A/cm^2 at all bias conditions

Peak g_m and R_{on} vs. L_g (Benchmarking)

at V_{ds}=0.5V

G_{m_max} (mS/μm)

2.8
2.4
2.0
1.6
1.2
0.8
0.4

D.-H. Kim
2011 IEDM
(HEMT)

D.-H. Kim
2012 IEDM

T.-W. Kim
2012 VLSI

This work

Intel
2009 IEDM

J.J. Gu
2012 IEDM

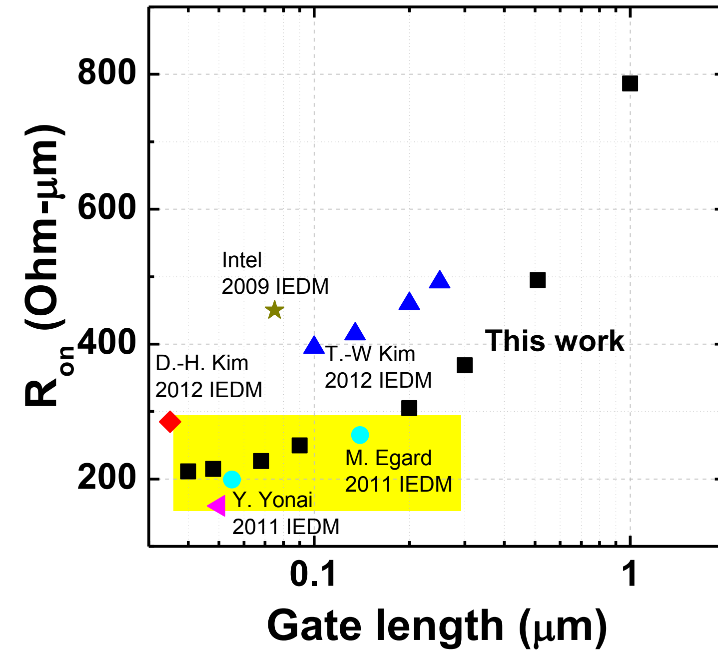
M. Egard
2011 IEDM

Y. Yonai
2011 IEDM

D.-H. Kim
2012 IEDM
(V_{DS}=1V)

0.01
0.1
1

Gate length (μm)



Record G_m over all the gate lengths

Very Low R_{on} when considering not fully self-aligned S/D contact

Conclusion

- Using digital etching, damaged surface during S/D regrowth can be effectively removed and the channel thinned in a nanometer precision without etch-stop.
- Employing N_2 plasma and TMA in-situ treatment, thin HfO_2 (3.5 nm) gate dielectric can be incorporated with low D_{it}.
- Peak g_m = 2.45 mS/μm at V_{ds}=0.5 V for a 40 nm-L_g device
- Regrown S/D provides very low access resistance (~ 200 ohm-μm) even with non-self aligned S/D metal contact.

Acknowledgment

Thanks for your attention!
Questions?

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A portion of this work was done in the UCSB nanofabrication facility, part of NSF funded NNIN network and MRL Central Facilities supported by the MRSEC Program of the NSF under award No. MR05-20415.

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