An Integrated 40 Gbit/s Optical Costas Receiver

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***Abstract*—In this paper, a highly-integrated widely-tunable optical homodyne receiver is reported with 40 Gbaud/s data rate. By using photonic and electronic integration, the receiver is realized within a size of $10 \times 10\ \mathrm{mm}^2$, and the system is very robust and resistive to environmental changes. An integrated photonic coherent receiver circuit is demonstrated with 35 GHz photodetector bandwidth, and the integrated local oscillator (LO) laser covers a 40 nm range. The electronic IC (EIC) has a working frequency up to 50 GHz. The feedback loop is carefully analyzed and designed, and the experimental results show $> 1.1\ \mathrm{GHz}$ loop bandwidth, which matches the design. The hold-in range is measured to be $> 15\ \mathrm{GHz}$. The phase noise of the transmitting laser has been cloned to the LO laser quite well, and both the linewidth measurement and phase noise measurement show no observable cross talk between binary phase shift keying (BPSK) data and the optical phase-locked loop (OPLL). Error free ($\mathrm{bit\ error\ rate} < 10^{-12}$) is achieved up to 35 Gbit/s. The system consumes 3 Watts of power.**

***Index Terms*—Coherent receiver, Costas loop, homodyne detection, optical phase-locked loops, optical receivers.**

I. Introduction

RECENTLY, a resurgence of effort is being devoted to the research of coherent optic fiber communications, because of the advantages of higher sensitivity, better noise tolerance, and, more importantly, its compatibility with complex modulation format, such as QPSK, 16 QAM, which leads to higher spectrum efficiency [1]–[5].

In order to demodulate phase shift keying (PSK) signals, coherent detection is needed. There are generally two ways to achieve coherent detection for the optical phase shift keying (PSK) signals – homodyne detection and intradyne detection [4], [5]. The homodyne detection relies on the fixed phase relation between the transmitting laser and the local oscillator (LO) laser, which can be achieved by injection locking [6] or optical phase-locked loops (OPLLs) [7]–[12]. On the other hand, intradyne detection is depended on digital signal processor (DSP) to correct the frequency and phase difference between the transmitting laser and the LO [5].

Research on the coherent receiver started in the early 1980s, and most of the early efforts focused on homodyne technologies. Homodyne receivers have been well studied both theoretically and experimentally [7]–[9], [12]–[15]. The main driving force of the homodyne receiver research was its highest sensitivity – 10^{-9} bit error rate (BER) can be achieved with only 9 photons per bit. However, one of the biggest problems that researchers were facing was the insufficient phase locking bandwidth relative to the LO laser linewidth. In other words, a very narrow linewidth laser was required to achieve a stable phase locking with respect to the limited loop bandwidth at that time. The limited speed of photodetectors and electronics components also limited the data rate, which gave rise to an even higher requirement on LO laser linewidth [9]. Therefore, external cavity lasers were normally used, which made the system bulky and expensive. As for an OPLL with absolute stability, the loop natural frequency ω_n and the loop delay τ should satisfy a relation of $\omega_n \cdot \tau < 0.736$ [16], which means that in order to achieve $> 100\ \mathrm{MHz}$ loop bandwidth, $< 1.2\ \mathrm{ns}$ loop delay is required. By using external cavity laser, bulk optics and discrete component electronics, this was very difficult at that time [17]. In order to increase the loop bandwidth and therefore make the loop more stable, photonic and electronic integration becomes necessary.

Later on, in the 1990s, with the invention of the Erbium-doped fiber amplifier (EDFA) and the wide application of wavelength division multiplexing (WDM), the interest in homodyne coherent receivers and PSK modulation dropped greatly. Many optical channels could be multiplexed into one fiber and get amplified together. Long-haul communication, and high-capacity network became more cost effective. At around year 2008, the focus on coherent communication returned, with most of the efforts focused on the intradyne receiver. The architecture of an intradyne coherent receiver normally consists of an LO laser, an optical I/Q receiver, high speed analogue-to-digital converters (ADC), and a digital signal processor (DSP). The I/Q receiver is normally built with a 90-degree hybrid and four balanced photodectors. Complicated DSP algorithms are used to recover the data. For under-sea and long haul communications, the DSP algorithms normally include, but may not limit to, chromatic dispersion (CD) compensation, clock recovery and timing adjusting, polarization de-multiplexing and polarization mode dispersion (PMD) compensation, frequency offset estimation, phase recovery, soft forward error correction (FEC), and decision [5].

The DSP-based intradyne receiver is powerful, but the high-speed sophisticated DSP not only increases the cost of coherent

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receiver tremendously, but also suffers from high power consumption. For shorter distance, where dispersion effects are not severe, the application of DSP may be overkill, even though only part of the algorithm steps are necessary for short distance.

In order to solve the high-cost and high power consumption problems that intradyne receivers have, OPLL-based homodyne receivers become an alternative. Regarding the technical problems that researchers had in the 1980s, most of them can be solved by advanced integration technologies. Integration makes the system smaller and more stable. The smaller size also leads to a shorter loop delay for the OPLL, and therefore a much wider loop bandwidth [16]–[21]. Wide loop bandwidth contributes to the better system reliability, and better laser phase noise suppression. Since there is no high-speed DSP involved, the OPLL-based receiver can be much cheaper, and has significantly lower power consumption, compared to DSP-based intradyne receivers.

The first highly integrated homodyne BPSK optical coherent receiver was proposed, and a part of the measurement results were demonstrated in our recent publications [11], [22]–[25]. In this paper, more detailed and comprehensive system design, analysis, implementation, device fabrication, and measurement results are described systematically. By photonic and electronic integration, the whole receiver system is realized within a size of $10 \times 10\ \mathrm{mm}^2$. The loop bandwidth is measured to be $> 1.1\ \mathrm{GHz}$, which is the highest to the best of our knowledge. 40 Gbit/s real-time BPSK data demodulation has been achieved. The system also shows very good stability and reliability in terms of temperature fluctuation. The power consumption is below 3 Watts, 0.5 Watts from the PIC and $< 2.5\ \mathrm{Watts}$ from the EIC, negligible ($\sim 0.07\ \mathrm{Watts}$) from the loop filter. The thermoelectric controller power consumption is no included.

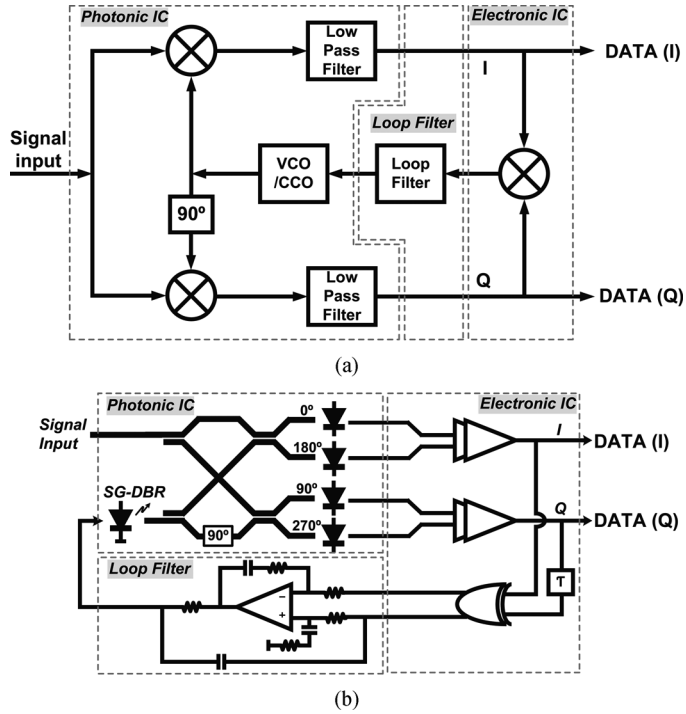

Fig. 1. (a) The classic model of a Costas loop. (b) shows the detailed architecture of the Costas loop based OPLL. The PIC, EIC and loop filter are labeled in both (a) and (b).

II. Costas Loop and System Analysis

A. Optical Costas Loop and its Components

Among all homodyne coherent receiver architectures, Costas loop is one of the most robust and commonly used. The electrical Costas loop has been applied to many applications, such as GPS receivers and orthogonal frequency-division multiplexing (OFDM). Sharing a similar architecture, optical Costas loops have also been well studied, such as decision-driven Costas loop [7]. The general architecture of the Costas loops are shown in Fig. 1(a). By phase shifting one branch of the LO by 90°, and beating with the incoming signal, in-phase (I) and quadrature (Q) signals are generated and mixed at a mixer. The mixer output feeds back to the LO, which can either be a voltage-controlled oscillator (VCO) or a current-controlled oscillator (CCO). A loop filter is built in the loop to realize the desired loop characteristics, such as loop order, bandwidth, phase margin and gain margin.

The optical Costas loop shares the same architecture [8]. A more detailed schematic of this optical Costas-loop-based coherent receiver is shown in Fig. 1(b). A widely-tunable sampled-grating DBR (SG-DBR) laser acts as the CCO, and the quadrature signals are generated in an optical 90-degree hybrid, where the 90° phase shift is introduced by an optical phase shifter, based on current injection. The I/Q signals are detected by four high speed photodetectors, which not only convert the optical signal to electrical signal, they also act as low pass filters. The mixer is realized by a delay line and an XOR gate, which act together as a quadri-correlator phase/frequency detector (PFD) [26]. The error signal from the PFD feeds back to the laser tuning section through the loop filter.

By photonic and electronic integration, the system has been realized within a size of $10 \times 10\ \mathrm{mm}^2$, and the total loop delay is as small as approximately 120 ps, where 40 ps is from the photonic IC (PIC), 50 ps is from the electronic IC and 30 ps is from the loop filter. On the photonic integrated circuit (PIC), a widely-tunable SG-DBR, an optical 90-degree hybrid, four photodetectors and RF transmission lines are integrated monolithically [22]. The Electronic IC (EIC) integrates four limiting amplifier (LIA) chains, a 10 ps delay line and an XOR gate. The input signals from the photodetectors on PIC are hard limited by the LIAs and therefore small optical power fluctuations will not influence the system performance. The delay lines and the XOR gate together act as a phase and frequency detector, which can also been understood as a quadri-correlator [25], [26]. The frequency error response is linear, and the frequency detection sensitivity is 0.3 V/25 GHz, which is determined by the delay time and EIC output maximum voltage. The XOR gate itself also acts as a nonlinear phase detector, which can be analyzed by the equivalent linear gain for simplicity [11].

The third part of this Costas loop is an active loop filter (LF), where a novel two-path loop structure has been applied [11], including an active slow path and a passive feed-forward fast path. The feed-forward path includes no active components and provides the shortest delay possible for high frequency signals, while the active path is composed of an operational amplifier (Op-amp) based active filter, which gives more gain at lower frequency, and also makes sure the loop type (type II) does not

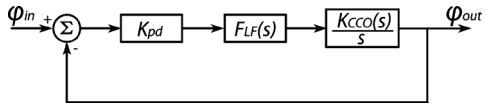

Fig. 2. Basic PLL model.

get jeopardized [27]. The structure of this loop filter is also shown in Fig. 1(b).

B. Loop Analysis

As for the loop analysis, both analytical and numerical methods are used to characterize this Costas OPLL, as well as the frequency-locked loop. Based on the loop model as shown in Fig. 2, the open loop transfer function of this OPLL is

$$G(s) = K_{PD} \cdot \frac{K_{CCO}(s)}{s} \cdot F_{LF}(s) \cdot e^{-s\tau}, \tag{1}$$

where K_{PD} is the phase detector sensitivity [*V/rad*], $F_{LF}(s)$ is the loop filter response [*A/V*], $K_{CCO}(s)$ is the CCO (LO laser) sensitivity [*rad/Hz/A*], and $e^{-s\tau}$ represents the loop delay effect. As mentioned before, the phase detector sensitivity K_{PD} is defined by the EIC gain and its output peak-to-peak voltage. Since the signal is digitized in the LIAs, the phase detector becomes a bang-bang type. To simplify the analysis, linear equivalent sensitivity is estimated and used in the loop analysis [11]. $K_{PD} = 0.2 - 0.4$ V/rad.

The CCO sensitivity $K_{CCO}(s)$ is a function of frequency, and can be expanded as

$$\frac{K_{CCO}(s)}{s} = \Re_{CCO} \cdot \frac{1}{1 + s\tau_{laser}} \cdot \frac{1}{s}, \tag{2}$$

where $\Re_{CCO}$ is the laser phase section tuning responsivity in unit of [*Hz/A*], τ_{laser} is time constant from the minority carrier lifetime, and the pole at zero frequency shows the frequency to phase conversion integral.

In order to obtain wider loop bandwidth, enough phase margin and gain margin for loop stability, the loop filter response $F_{LF}(s)$ need to be carefully designed. It is a two-path loop filter design, and the expression of $F_{LF}(s)$ can be written as

$$F_{LF}(s) = A \cdot \frac{1 + s\tau_2}{s(1 + s\tau_1)} \cdot \frac{1}{R_1 + R_{ph}} \cdot e^{-s\tau_{OP}} + \frac{1}{2} \cdot sC_{FF}. \tag{3}$$

The first term on the right hand side of this equation represents the Op-amp path, and the second term is the feed-forward path. τ_1 is the parasitic parameter from the commercial Op-amp, and τ_2 is a RC time constant introduced to avoid 180° phase difference when the responses of the two paths cross each other in frequency domain. A is the gain constant of the first path of the loop filter. R_{ph} represents the laser phase section diode I-V curve slope at the biased current (normally $\sim$ 2 mA for this Costas receiver). τ_{OP} is the extra delay introduced by Op-amp, which can be around or even larger than several ns.

The total closed-loop response is

$$H(s) = \frac{G(s)}{1 + G(s)}. \tag{4}$$

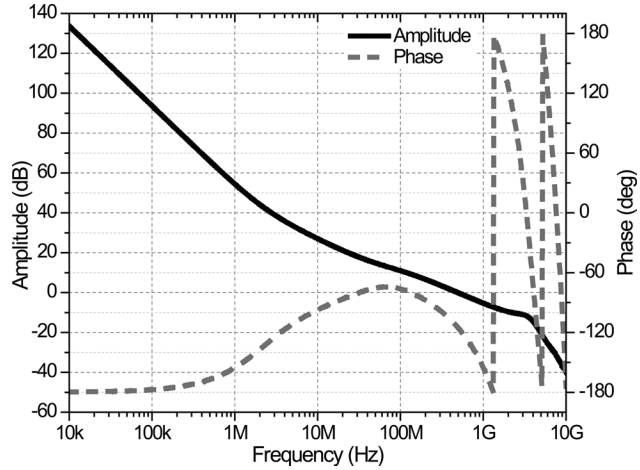

Fig. 3. Bode plot of the open loop response $G(s)$.

TABLE I
DESIGNED LOOP PARAMETERS

Parameters	Values	Descriptions
K_{PD}	0.2 - 0.4 V/rad	Phase detector sensitivity
τ	120 ps	Loop delay with feed-forward path
$\Re_{CCO}$	8 GHz/mA	CCO laser tuning responsivity
τ_{laser}	1.6×10^{-9} sec	Time constant for laser tuning
A	1×10^{6} sec^{1}	LF constant
τ_1	8.0×10^{-10} sec	Parasitic time constant from Op-amp
τ_2	7.2×10^{-8} sec	RC Time constant of LF
R_1	500 Ω	Series resistor value at LF output
R_{ph}	100 Ω	Phase tuning section AC resistance
C_{FF}	1.0 pF	Feed-forward capacitor value

The loop parameters are listed in Table I. The simulated loop response is plotted in Fig. 3. As we can see, a 550 MHz open-loop bandwidth has been achieved with 65 degree phase margin, and 7.4 dB gain margin at 1.35 GHz, where the phase response is π.

III. LOOP COMPONENTS – PIC, EIC AND LOOP FILTER

In order to design a robust synchronized homodyne coherent receiver, one of the most important considerations is the loop delay, and photonic and electronic integration becomes a perfect solution. Integration not only decreases the size of the device, which leads to shorter loop delay, but also makes the coherent system more stable and more resistive to environment changes [28]. In this section, the design details about the PIC, the EIC and the loop filter will be explained respectively.

A. PIC Design and Fabrication

As mentioned in the previous sections, the PIC includes an SG-DBR laser as the LO laser, an optical 90-degree hybrid to mix the signal and the LO, four high-speed uni-traveling-carrier (UTC) photodetectors, and microstrip transmission lines. The PIC is designed and fabricated based on semi-insulating (SI) InGaAsP/InP material. The architecture of the PIC is shown in Fig. 4 as well as a microscope picture.

The SG-DBR laser has a super-mode spacing of 7 nm, and is designed to cover 40 nm range. The phase tuning pad of the SG-DBR laser is used for the current feedback. Compared to other tuning mechanisms, such as temperature tuning or quantum stark effect, the current injection to a phase diode with a wider bandgap can change the laser frequency fast

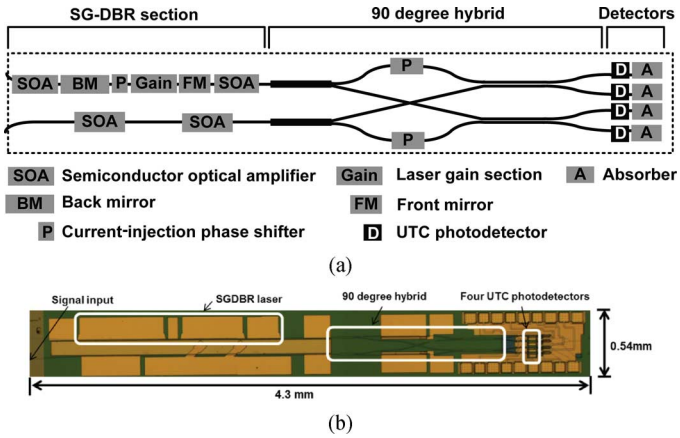

Fig. 4. (a) shows the schematic of the PIC, including three sections: an SG-DBR laser, a 90-degree hybrid and four uni-travelling carrier (UTC) photodetectors. (b) shows a microscope picture of the PIC. The different integrated components are labeled in both (a) and (b).

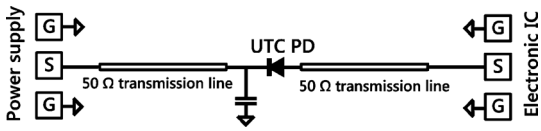

Fig. 5. Circuit schematic of the photodetector bias circuit on PIC.

and efficient, which leads to wider loop bandwidth and larger pull-in range. It also does not have the 180 ° phase transition at low frequency (normally < 1 MHz) as single-electrode lasers have [29].

The 90-degree coupler design is also shown in Fig. 1(b). It uses a 1-by-2 multi-mode interference (MMI) couplers as the first stage, which split the LO and the incoming signal into two paths, respectively. The symmetry of 1-by-2 MMI coupler ensures equal splitting. Directional couplers are used as the second stage couplers in the 90-degree hybrid, because a) directional couplers have the minimum reflection among all couplers, which is very important to avoid injection locking since there is no isolator on PIC; b) it acts as a perfect 180 degree hybrid and the phase relationship is always correct, regardless of splitting ratio.

Four UTC photodetectors are also integrated on this PIC as well as transmission lines. Because the EIC can only provide a voltage between -1.5 and -2 V, it is designed so that the UTC photodetectors can have positive voltage supplies to the N-contact in order to deplete the collector. The circuit model is shown in Fig. 5. Both P and N contacts are led to the GSG pads on the edges of the PIC by transmission lines, and a capacitor is also integrated to provide a high frequency ground on the PIC. The photodetector has a size of 3×20 μm. The designed quantum efficiency is above 95%, and with a 50 Ω load the 3-dB bandwidth can be above 50 GHz depending on the contact resistance. [23]

B. Electronic IC and Loop Filter

The electronics part of this Costas receiver includes an EIC and a loop filter. The BPSK receiver EIC is designed to work with the PIC having a 4-phase (I/Q) optical interferometer. With measurement of the I and Q signals, a signal proportional to optical frequency difference is formed by amplifying the I and

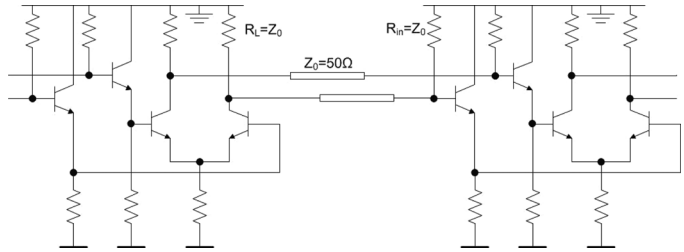

Fig. 6. Schematics of the limiting ECL gates merged in a 50 Ω transmission lines environment.

Q signals, providing a relative delay, and mixing. Under zero offset frequency, the IC output is proportional to the optical phase difference; in the presence of an optical frequency difference, the IC output is proportional to this frequency difference. The phase/frequency difference function is provided to enable PLL locking even with initial frequency offsets as large as $+/-50$ GHz, although in real case the LO laser cavity mode spacing sets a limit to the largest possible initial offset frequency range.

Fig. 1(b) shows a block diagram of the full BPSK receiver. The BPSK phase-frequency detector, denoted by the grey frame, receives its input from the optical interferometer. Assuming the LO laser electrical field is $E_{LO} = A_{LO}\cos(\omega t + \Delta\theta)$ and the carrier laser electrical field is $E_c = A_c\cos(\omega t + \Delta\theta)$, the optical interferometer provides the in-phase beat note $I = B\cos(\Delta\omega t + \Delta\theta)$ and the quadrature-phase beat note $Q = B\sin(\Delta\omega t + \Delta\theta)$, thus carrying an information on both phase and frequency offset magnitude and sign. The core of the phase-frequency detector (PFD) [25] consists of a delay line in the Q arm and a XOR gate, which is based on a Gilbert multiplier topology. To reduce the dependency on the LO and reference lasers photocurrent, The PFD is preceded by a high gain emitter coupled logic (ECL) limiting amplifier chain in order to convert the signals into a rail to rail square wave – Fig. 6. All the ECL gates are biased by a tail current of 12 mA, hence providing a differential signal of 600 mV at a full swing mode, large enough to provide a full limiting ($\gg kT/q$) as more is explained in [25].

In case of frequency detection, the Q signal is delayed by τ and then mixed with I. A linear, small signal analysis of the PFD, (5), suggests that the output signal consists of two components: a high frequency component with a double frequency but zero average and a DC component with magnitude proportional to the offset frequency Δf . Since the PFD output is integrated by a low frequency hybrid loop filter, the low frequency component is the one to consider.

$$\begin{aligned} &I'(t) \oplus Q'(t-\tau) \\ &\quad = \cos(\Delta\omega t + \Delta\theta) \cdot \sin(\Delta\omega(t-\tau) + \Delta\theta) \\ &\quad = 0.5\sin(2\Delta\omega t - \Delta\omega\tau + 2\Delta\theta) + 0.5\sin(\Delta\omega\tau) \end{aligned} \quad (5)$$

By setting $\tau = 10$ ps, the DC term of (5), provides an unambiguous frequency detection characteristics of $\Delta f = \pm 50$ GHz.

Due to the limiting amplifiers, the I/Q signals result in a hard limited square waves. In this case, the PFD output will provide a double frequency square wave with varying duty-cycle that depends on the frequency offset, resulting in the same frequency detection characteristics. Measurement data of the PFD in frequency detection mode is presented in then next section.

At phase detection mode, when $\Delta f = 0$, the PFD output is $\sin(2\Delta\theta)$. The periodic phase detection characteristic, with a factor of 2 in the sin argument makes the loop stable for both 0 and 180 degrees offset. This particular property allows the loop to lock on a BPSK modulated carrier.

This EIC is fabricated using Teledyne's 500 nm HBT process, and each transistor has 300 GHz f_t and $f_{\max}$.

The output of the EIC goes into a loop filter. It contains a short passive path and an active path with longer delay [11]. A commercial Op-amp is used as the active component, and it provides 200 MHz unity-gain bandwidth. The loop filter is built on an AlN carrier with chip resistors and capacitors with a size of 0201.

C. PIC to EIC Interconnections

Since the output of the UTC photodetectors are directly connected to the EIC input and the signal frequencies can be as high as 40 – 50 GHz, signal integrity may be a serious issue if the interconnection is not well designed. Both RF pads on PIC and EIC have a pitch size of 100 μm. In order to partially compensate the inductance introduced by wirebonds, the ground-signal-ground (GSG) pads on PIC are carefully designed to be a little capacitive. The finite-element full-wave simulation shows that as long as the wirebonding is shorter than 200 μm ($\sim$ 60 μm between the edges of the two GSG pads), 100 GHz interconnection between can be achieved between PIC and EIC with less than 1 dB loss. The simulated S-parameters are shown in Fig. 7(a) as well as a picture of the simulation model. Another situation is also simulated, where the PIC and EIC are wirebonded to the AlN carrier separately, and they are connected through the co-planar waveguide on the carrier. The distance between the two chips are 0.85 mm, and wire length is 380 μm from PIC to carrier, and 500 μm from EIC to carrier. The simulation shows that the 3-dB bandwidth is more than 40 GHz (Fig. 7(b)). The latter case is used for this Costas receiver packaging.

The two pictures in Fig. 7(a) and (b) are plotted in different scales, and the real device sizes are the same. As mentioned above, the GSG pads have a 100 μm pitch size, the signal pad on the PIC is 75-by-75 μm, and the signal pad on EIC is 75 μm wide and 100 μm long. The InP substrate thicknesses of both PIC and EIC are 6 mil.

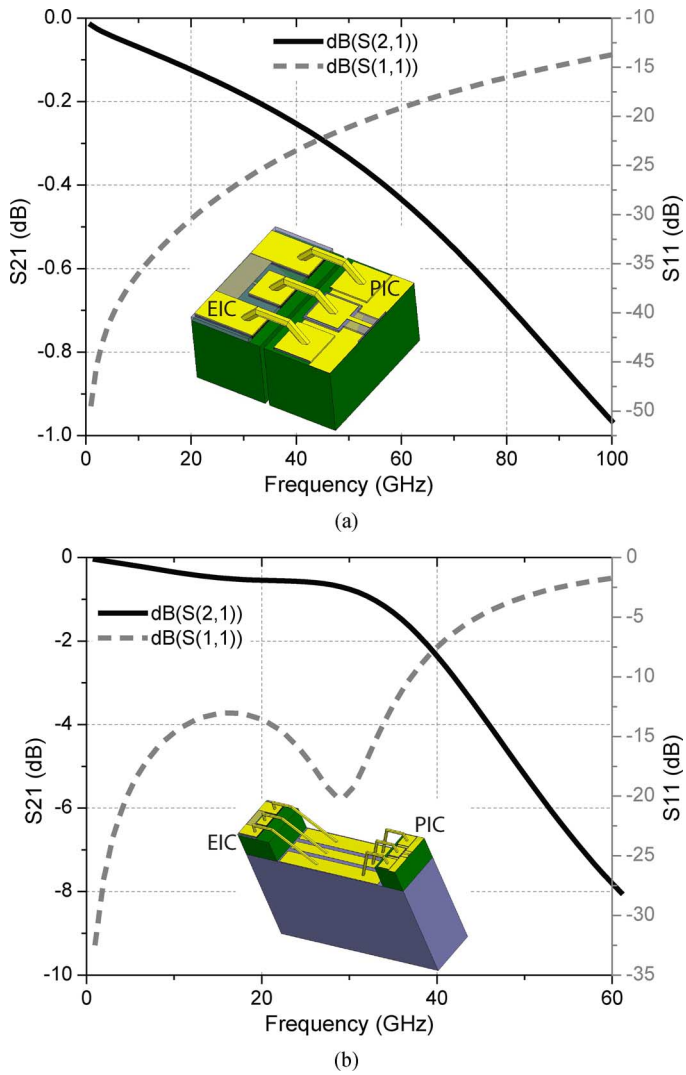

Fig. 7. Full-wave simulation results of the GSG pads for interconnections. The golden color represents gold, green color represents InP, and gray box represents AlN. (a) The wirebond is directly from one chip to the other. (b) The PIC and EIC are wirebonded to the carrier separately, and they are connected through the co-planar waveguide on the carrier.

IV. Device Characterization and System Measurement

A. Device Characterization

The PIC and EIC are characterized separately before they are used to build the Costas receiver.

The on-PIC SG-DBR laser shows a tuning range from 1541 to 1583 nm. For the L-I-V measurement, only the gain section of the laser is biased, and the boosting semiconductor optical amplifier (SOA) next to the front mirror is reversed biased as an absorber to measure the output optical power. The threshold current of the SG-DBR laser is 25 mA, and with 180 mA bias, output power can almost reach 20 mW without the boosting SOA [23]. Since the whole circuit is built on surface ridge waveguide structure, which provides small on-chip reflection, there is no injection locking has been observed.

The phase tuning section of the SG-DBR laser shows around $\Re_{CCO} = 5 - 10$ GHz/mA tuning sensitivity. Because the mirror reflectivity of the SG-DBR is not necessarily flat, the lasing wavelength change leads to the change of mirror reflectivity, which therefore changes the threshold current and the carrier density in the gain section. If the reflectivity slope is negative versus wavelength, the carrier density change in the laser gain section will increase with the current injection into the phase tuning section, which favors the frequency tuning sensitivity. Otherwise, if the reflectivity slope is positive, the tuning sensitivity is lower. The measurement shows that $\Re_{CCO}$ can vary roughly by a factor of 2, depending on how the lasing peak is aligned to the mirror reflection peak.

The RF response of the phase section is also measured. By injecting AC current into the phase diode, the laser is modulated. The injected AC current generates two modulation side lobes, which indicates the frequency response of the laser phase section. The measurement result is shown in Fig. 8. Curve fitting confirms a pole at 100 MHz, which means the time constant τ_{laser} equals 1.59 ns. This also presents the carrier life time in

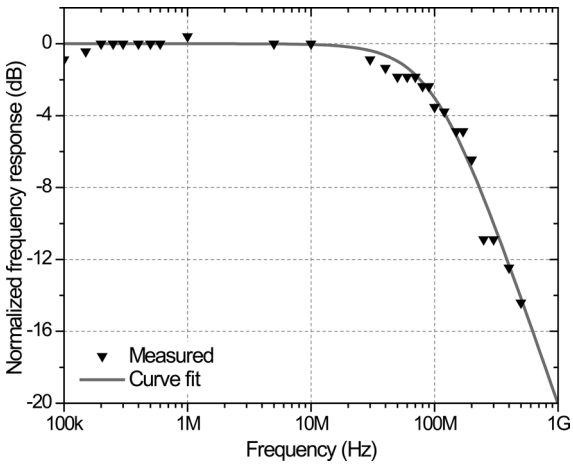

Fig. 8. Relative frequency response of the phase section diode in the SG-DBR laser.

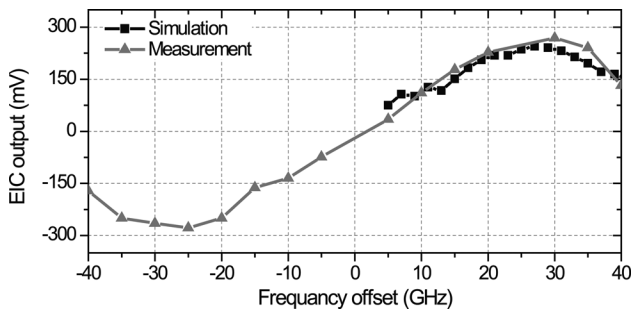

Fig. 9. PFD standalone frequency detection response, measurements versus simulation [25].

the waveguide passive section of this integration form. The mismatch between experimental result and fitted curve at low frequency is due to the cut-off frequency of the bias-Tee used in the measurement.

The 90-degree hybrid is also characterized. The power imbalance in the four photodetectors are within 5%, and the phase can be exact, since there is a tunable phase shifter in the hybrid, and the directional coupler always acts as an 180 degree hybrid, regardless of coupling ratio.

The UTC photodetector characterization is carried out by using a lightwave component analyzer (LCA). The UTC photodetector is wirebonded to the AlN carrier before testing, since in the following system testing they have to be wirebonded. Amplitude modulated laser signal is coupled into the waveguide and detected by the UTC photodetector, and the RF response is then measured by the LCA. All the cable and probe losses are de-embedded. The measurement is based on the 50 Ω load. The 3-dB bandwidth is measured to be around 35 GHz with -2 V bias [22], [23]. The major limit of the bandwidth is from the contact resistance. The measured contact resistance of this PIC is around 7000 $\Omega \cdot \mu\mathrm{m}^2$, which leads to around 100 Ω contact resistance for each UTC photodetector. The saturation current is 18 mA with -5 V bias.

As for the EIC, the electrical testing shows it fully functional. By adjusting the input frequency, the output voltage of the EIC is measured. As shown in Fig. 9, the measured result matches with simulation quite well.

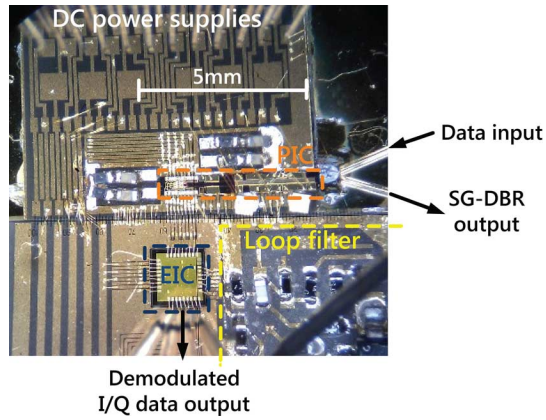

Fig. 10. Microscope picture of the Costas receiver on the test stage. The DC probe card provide DC supplies to the device from the top side of the image. The optical input and output are from the right hand side of the picture, and a four-signal-line RF probe is used to measure the demodulated I/Q output.

The more detailed testing results of this EIC is discussed in [25], and the design, fabrication and measurement result of the PIC can also be found in [22], [23].

B. OPLL Testing

The PIC, EIC and loop filter are then mounted on AlN carriers and wirebonded together. The size of the system is around 10×10 mm^2. The incoming signal is coupled into the PIC through a lensed fiber, and the SG-DBR power is coupled out to another lensed fiber through the back mirror for monitoring purpose. All the DC power supplies are connected through a DC probe card. The demodulated signal is obtained from the EIC output ports. A microscope picture of the Costas receiver is shown in Fig. 10, and PIC, EIC and loop filter are also labeled in the picture.

The Costas receiver is first tested as an OPLL. A tunable external cavity laser (ECL) is used as a reference laser with a linewidth of 80 kHz. The power of the reference laser is first coupled into the Costas receiver directly without any modulation, and the optical power of the SG-DBR laser is coupled out from the PIC and beat with the reference on an external high speed photodetector. An acousto-optic modulator (AOM) is applied to introduce a 100 MHz frequency offset. The beating spectrum between the reference laser and phase-locked SG-DBR laser is observed on an electrical spectrum analyzer (ESA). The test setup is shown in Fig. 11(a), and the beating spectrum on ESA is shown in Fig. 11(b) [18]. In Fig. 11(b), the 100 MHz peak is the beating between the SG-DBR laser and the reference ECL when they are phase locked. The 1.2 GHz peak is because of the damping of the OPLL, which indicates the loop bandwidth, and the 1 GHz peak is the 'folded' peak from the lower sideband. Therefore, the frequency difference between the main peak and the sidelobes is 1.1 GHz. Since the sidelobes are caused by the damping of the loop, the actually loop bandwidth is wider than the damping peaks [27]. The sidelobes set a lower limit for the actual closed-loop bandwidth, and the actual loop bandwidth is larger than 1.1 GHz. To the best of our knowledge, it is the widest OPLL bandwidth that has ever been reported.

Loop bandwidth measurement is also done by introducing a phase error signal in the loop. A $\mathrm{LiNbO_3}$ phase modulator has

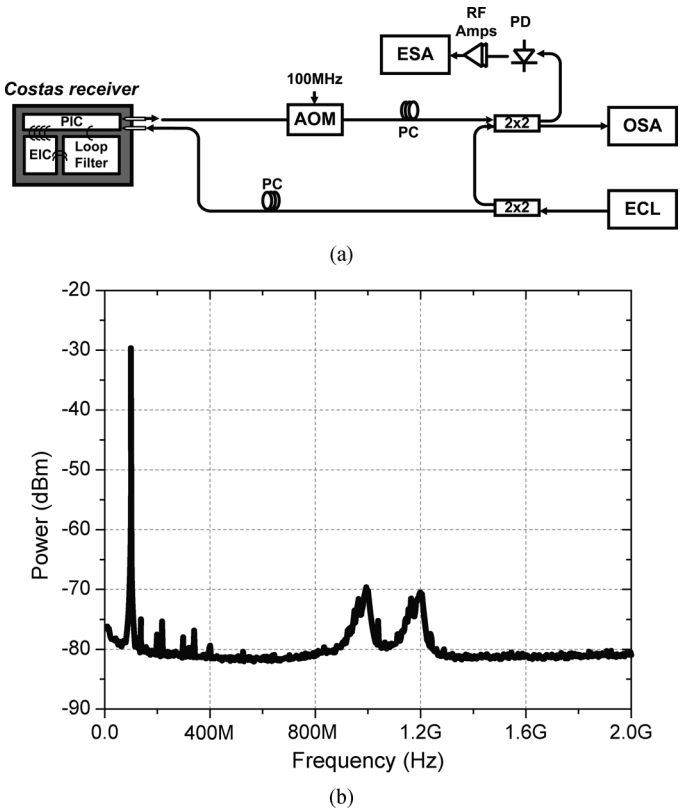

Fig. 11. (a) The test setup for the OPLL. (b) The beating spectrum of the two lasers when they are phase locked. The resolution bandwidth is 100 kHz.

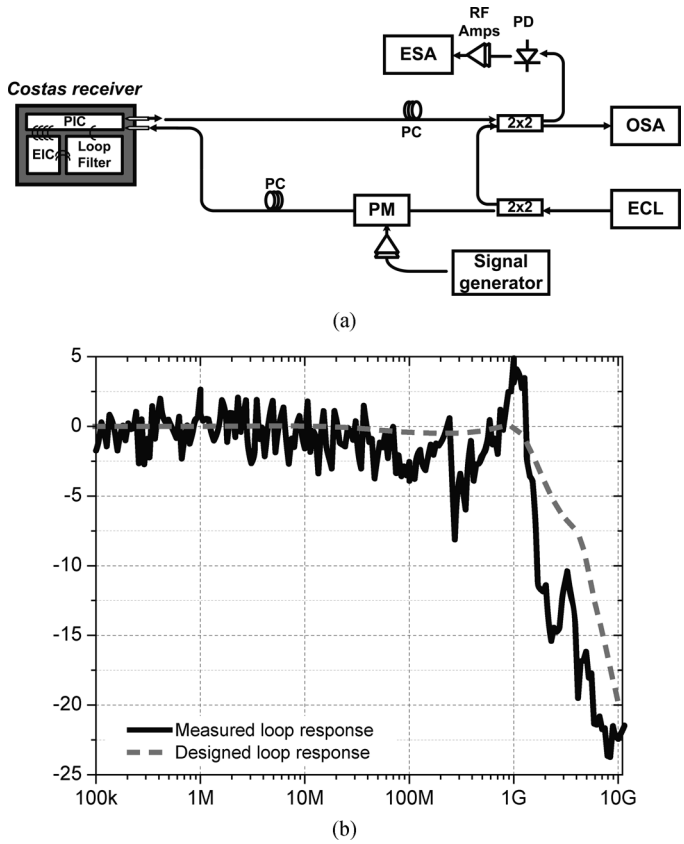

Fig. 12. (a) The test setup for loop bandwidth measurement. (b) shows the measured loop bandwidth (solid line) and the simulation result (dash line) as a comparison.

been included in the loop and relative loop response is measured on the ESA [27]. The test setup is shown in Fig. 12(a). The phase error $\Delta\varphi_{e,in}(s)$ is generated at the phase modulator, and the SG-DBR laser phase response to this phase error can be written as

$$\Delta\varphi_{e,out}(s) = \Delta\varphi_{e,in}(s) \cdot H(s) \tag{6}$$

according to (4). Since the ESA measures the residual phase noise spectrum between the SG-DBR laser and the unmodulated reference, the spectrum peak power, introduced by the modulated reference, is proportional to the square of the closed-loop transfer function.

$$P_{ESA}^{peak}(f_s) \propto \left| \frac{\varphi_{e,out}(j2\pi f_s)}{\varphi_{e,in}(j2\pi f)} \right|^2 = |H(j2\pi f_s)|^2, \tag{7}$$

where $P_{ESA}^{peak}(f_s)$ is the measured peak intensity on ESA, f_s is the signal generator frequency and also the peak frequency on ESA, and $j2\pi f \equiv s$. The normalized measurement result is shown in Fig. 12(b) as well as the simulated closed-loop function. The peaking at 1 GHz is probably because of the parasitic inductance in PIC and loop filter interconnection.

Furthermore, frequency pull-in and phase-locking is observed. By simply tuning on the loop, the two lasers are phase locked automatically. Even under the condition that the original frequency offset between two lasers is as large as 17.5 GHz, success frequency pull-in and phase locking has been observed after tuning on the loop. The pull-in range is dependent on the working conditions of the OPLL, especially on the LO laser. Frequency pull-in can only happen within one laser cavity mode.

By turning on the feedback loop, the SG-DBR laser frequency will be automatically pulled towards the reference laser frequency, and the phase lock loop starts to function when the frequency difference is within around 1 GHz. It is worth mentioning that it is the frequency locked-loop (FLL) that decides the pull-in range rather than the phase-locked loop, and FLL pull-in range is decided by the delay line in the EIC and the laser cavity mode spacing. In other words, it is not limited by the OPLL bandwidth any more. The whole pull-in and locking process takes hundreds of nanoseconds. The relatively slow frequency pull in is because of the bandwidth of the FLL bandwidth. As a first order loop, the FLL only has a designed bandwidth of 178 kHz. The frequency/phase pull-in curve is shown in Fig. 13. It is measured by applying an on-off keying modulation on the incoming signal. The OPLL will have frequency/phase pull in and lock when the incoming signal is *ON*, and lose lock when it is *OFF*. The in-phase output of the EIC is monitored on a real-time oscilloscope. As we can see, the SG-DBR laser is locked and unlocked periodically. The frequency pull-in speed is still relatively slow in the range of hundreds of nano-second. However, by redesign the loop characteristics, the pull-in speed can be possibly decreased by roughly two orders.

In addition, more than 30 GHz (> 15 GHz single-sideband) hold-in range has been observed. Within a $2.6°\mathrm{C}$ temperature fluctuation, the OPLL stays locked.

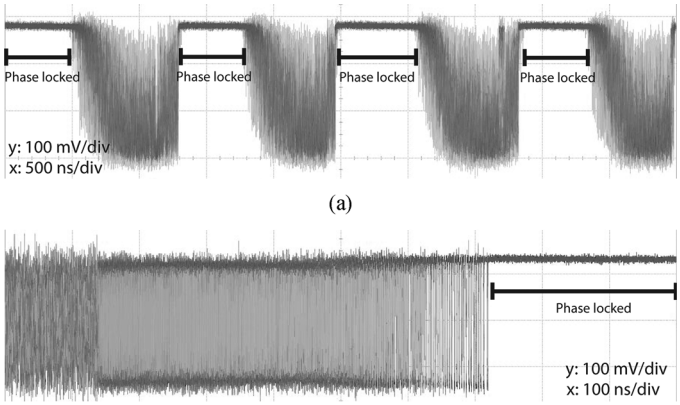

Fig. 13. The real-time oscilloscope result of the OPLL frequency pull-in and phase locking. Four periods are shown in (a), and (b) shows another set of time domain data with a smaller span.

C. Linewidth and Phase Noise Measurement

As for the linewidth measurement, self-heterodyne method is used. The laser under testing is split into two branches, a 25-km fiber delay is in one branch to get rid of the coherence and an acousto-optic modulator (AOM) is in the other branch to introduce the 100-MHz offset frequency. The linewidth of the reference laser is first measured, and 80 kHz full width at half maximum (FWHM) linewidth is obtained. The free-running SG-DBR (LO) laser linewidth has also been measured using the same method, and the FWHM linewidth is roughly 10 MHz.

The SG-DBR laser is then phase locked to the reference laser, and the linewidth of the phase-locked SG-DBR laser is measured. After applying the BPSK-modulated signal on the reference laser, the linewidth of the SG-DBR laser has been measured again. The test setup is shown in Fig. 14(a), and the results can be found in Fig. 14(b). As we can see, the locked SG-DBR laser has the same linewidth as the reference, even when the reference is modulated by a BPSK signal. The data rate is 25 Gbit/s, and $2^{31}-1$ pseudo-random binary sequence (PRBS) data is used.

The phase noise of this OPLL system is also measured on the ESA, and the test setup is shown in Fig. 15(a). In order to cancel out the reference laser noise, the fiber length is well matched with a length error smaller than 1 meter. As indicated in Fig. 15(b), the phase noise curves with and without data modulation match very well, which confirms that there is no observable data-OPLL cross talk in this Costas receiver, and also verifies the good matching in the linewidth measurement. The phase noise of the RF source that is used to drive the AOM is also measured for comparison. For all four sets of measurement, the signal power is always kept at -30 dBm, and the background noise is taken based on the assumption of the same signal power.

Comparing the OPLL phase noise with the signal generator phase noise, both of them reach the ESA noise floor at the frequency above 50 kHz, and the 1.1 GHz peak indicates the closed-loop bandwidth. However, at frequencies below 50 kHz, the OPLL present more noise compared to the RF source. This low frequency noise component is believed to be introduced by the test setup rather than OPLL itself. The fiber vibration can be one of the possible justifications. It causes phase fluctuation

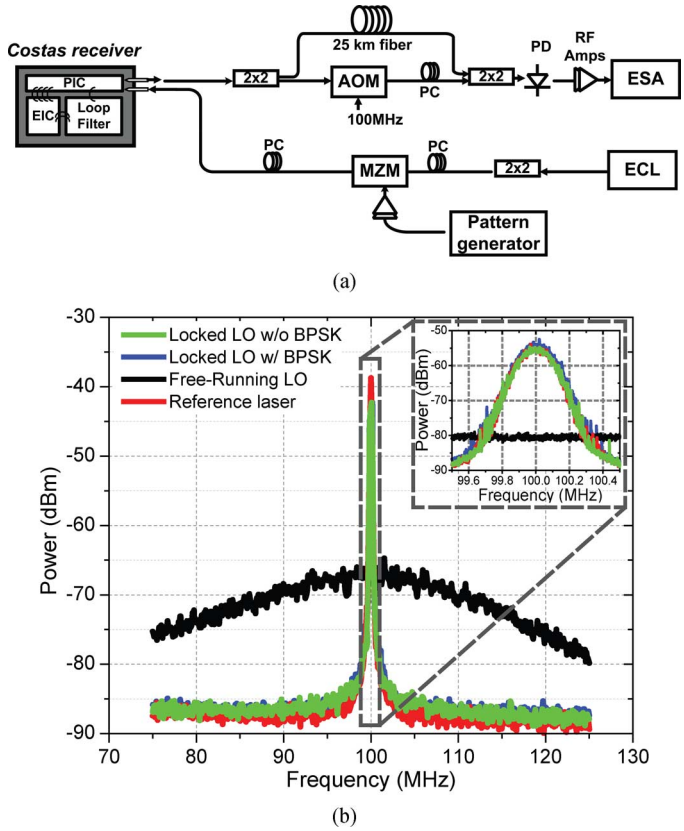

Fig. 14. (a) The test setup for linewidth measurement. (b) shows the measured linewidth of the reference laser (red), the free running SG-DBR (LO) laser (black), the phase-locked SG-DBR laser without modulated signal input (green), and the phase-locked SG-DBR with BPSK modulated signal input (blue). A zoomed-in plot is shown in the upper right corner. The resolution bandwidths are 50 kHz and 3 kHz, respectively.

in the Mach-Zehnder Interfermeter formed by two 2-by-2 fiber couplers, which may lead to higher low-frequency residual phase noise. Another possible cause is the fiber mismatch. If the fiber path length matching is not perfect, the laser phase noise will not be totally canceled out, and consequently shown on the OPLL phase noise.

D. Bit Error Rate Measurement

As for data reception of a Costas loop, the same as DSP-based intradyne systems, phase ambiguity needs to be taken into consideration. The incoming signal phase will be doubled in the quadri-correlator PFD, by which the 0 and π signal phase will be erased. However, the carrier phase will also be doubled at the same time, which means that the carrier phase of π and 2π become identical and indistinguishable to the OPLL. One way to solve this phase ambiguity problem is using differential encoding and decoding.

In the experiment, since PRBS data is used (the differential sequence of a PRBS is itself), no encoder is needed at the transmitter side. On the receiver output, the output data sequence needs to be decoded. One bit delay is introduced to the $\bar{I}$ output, and an XOR operation is carried out on the I and delayed $\bar{I}$ signals, and resulting output of the XOR gate is the inverse of the original PRBS sequence. The output of the XOR gate is connected to a bit error rate tester (BERT), and BER is then obtained. The eye diagram is measured at the EIC output directly

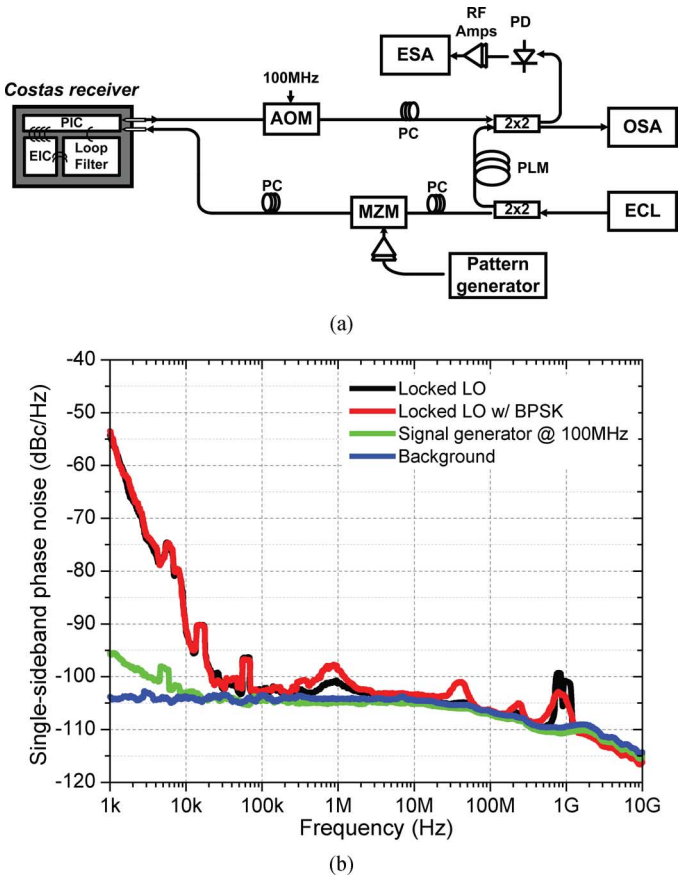

Fig. 15. (a) The test setup for phase noise measurement. (PLM: path length matching.) (b) shows the measured phase noise of the beating between the phase-locked SG-DBR laser and the reference laser with (red) and without (black) data modulation. The ESA background noise (blue), and the 100-MHz RF signal phase noise (green) are also plotted.

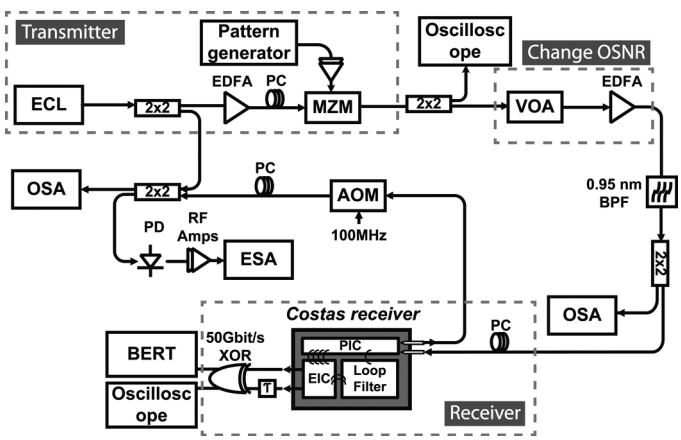

Fig. 16. Test setup for the BER measurement. The three dashed boxes indicate the transmitter, the receiver and the section that is used to vary the OSNR. The rest parts of the test setup are for monitoring purpose.

without the decoding circuit, and a 70 GHz sampled oscilloscope with a remote sampling head is used. Since the application of limiting amplifiers in EIC, BER cannot be estimated from the eye diagrams.

The test setup is shown in Fig. 16. The transmitter part is the same as the previous experiments, and $2^{31} - 1$ PRBS pattern is used. A variable optical attenuator (VOA) and an EDFA are

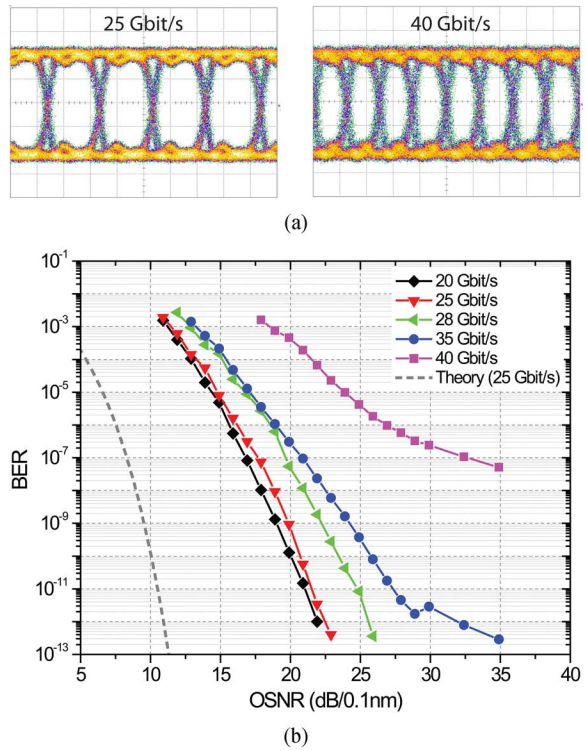

Fig. 17. (a) The eye diagrams of received data at 25 Gbit/s and 40 Gbit/s. (b) The bit error rate measurement results of the coherent receiver. The BER vs OSNR curves were measured at the data rate of 20, 25, 28, 35, 40 Gbit/s. The theoretical curve is also plotted at 25 Gbit/s data rate for an ideal receiver.

used to change the optical signal-to-noise ratio (OSNR). An optical filter with an FWHM bandwidth of 0.95 nm is used to filter out the amplified spontaneous emission (ASE) noise from the EDFA. The incoming signal is coupled to the receiver through a lensed fiber, and demodulated signal is detected by a 50 Gbit/s BERT through the decoding circuit. The BER is measured by the BERT. The RF cable is kept as short as possible to avoid excessive loss from the receiver to the measurement equipment. The measured eye diagrams at 25 and 40 Gbit/s are shown in Fig. 17(a), from which we can see the eyes are fairly open even at 40 Gbit/s. The BER measurement are carried out at the bit rates of 20, 25, 28, 35, and 40 Gbit/s. By varying the VOA, the OSNR from the EDFA output changes, and therefore the BERs are measured at different OSNR. The results are shown in Fig. 17(b). The theoretical BER for an ideal receiver is also calculated at 25 Gbit/s data rate. Comparing the measured BER and the theoretical BER, there is a 6–10 dB OSNR penalty. There are several potential factors that may introduce this difference. First, the residual LO laser phase noise may have influence on the receiver power penalty. Since the free running LO has a linewidth of 10 MHz, even with a 1 GHz OPLL loop bandwidth, the residual phase noise can be more than 10 degrees, which will cause a higher BER for the receiver performance, especially when OSNR is high. Second, since the device is not packaged, mechanical vibration can possibly cause worse BER. More specifically, the vibration of the fiber coupling can introduce optical amplitude noise on the photodetector, and the amplitude noise will pass through OPLL and change the LO laser phase and introduce phase error in consequence. The phase error variance of the OPLL directly influences the BER.

As shown in Fig. 17(b), error free ($\mathrm{BER} < 10^{-12}$) is achieved at the data rate up to 35 Gbit/s. At 40 Gbit/s, it is believed that the phase shifter, which is used to introduce a 1 bit delay in the differential decoding circuit, reaches its bandwidth. However, the differential decoding circuit can be potentially integrated in the EIC, and therefore it will not limit the receiver performance.

V. Conclusions

In this paper, an optical Costas receiver is demonstrated, and real-time 40 Gbit/s coherent communication is achieved without any DSP. We achieve error free up to 35 Gbit/s BPSK signal. By recovering the phase of the carrier, the LO laser 'clones' the linewidth of the transmitting laser. The OPLL closed-loop bandwidth is 1.1 GHz. With 2.6°C temperature change, the OPLL still stays locked, which indicates more than 30 GHz hold-in range (> 15 GHz for single sideband). The power consumption is < 3 Watt without taking thermoelectric cooler power consumption into account.

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