Journal of Crystal Growth 378 (2013) 92–95

Contents lists available at SciVerse ScienceDirect

Journal of Crystal Growth

journal homepage: www.elsevier.com/locate/jcrysgro

Co-doping of $In_xGa_{1-x}As$ with silicon and tellurium for improved ultra-low contact resistance

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ARTICLE INFO

Available online 10 January 2013

Keywords:
A1. Doping
A1. Contact resistivity
A3. Molecular beam epitaxy
B2. Semiconducting indium gallium arsenide

ABSTRACT

We report Te doping of bulk $In_{0.53}Ga_{0.47}As$ up to $2.6\times10^{19}\,cm^{-3}$ without saturation effects, and structural characterization and contact resistances between metal and epitaxial regrowth for four structures: Si doped and Si and Te co-doped n^+ InAs regrowth on a 10 nm $In_{0.53}Ga_{0.47}As$ channel, Si doped and Si and Te co-doped n^+ $In_{0.53}Ga_{0.47}As$ regrowth on a 7 nm $In_{0.53}Ga_{0.47}As$ channel. We observe that the contact resistance for the Si doped and Si and Te co-doped n^+ InAs regrowth on the 10 nm $In_{0.53}Ga_{0.47}As$ channel is 9.9 Ω μm (3.9 Ω μm^2) and 6.6 Ω μm (2.3 Ω μm^2), and the contact resistance for the Si doped and Si and Te co-doped n^+ $In_{0.53}Ga_{0.47}As$ regrowth on the 7 nm $In_{0.53}Ga_{0.47}As$ channel is 8.5 Ω μm (2.3 Ω μm^2) and 6.8 Ω μm (1.9 Ω μm^2). The improvement in contact resistance comes from improvements in electron mobility consistent with Te improving material quality as a surfactant.

1. Introduction

With each technology node, field-effect-transistor source and drain contact lengths in VLSI decrease by approximately 1:$\sqrt{2}$ [1]. Given adequately low access resistance, and a 1:$\sqrt{2}$ reduction in dielectric equivalent thickness, on-state current per unit gate width would also increase by $\sqrt{2}$:1 [2]. To permit this increase in on-state current, FET contact resistivities must decrease by 1:2 [2]. For MOSFETs at ~20 nm gate and contact lengths, access and contact resistivities of less than 10 Ω μm and 0.2 Ω μm^2 would be needed for <10% degradation in the transistor on-state current [2]. The high dopant concentrations achievable by MBE provide a method for creating low-resistance ohmic contacts: increased doping decreases the depletion depth due to surface Fermi level pinning or due to the work function difference between the semiconductor and the metal, and increases tunneling probability through any barrier [3]. Co-doping of the InAs (and thus $In_xGa_{1-x}As$) system with a group IV (Sn) and a group VI (Te) is possible and can provide high doping densities ($2.9\times10^{19}\,cm^{-3}$ in InAs) [4]. Te has a lower diffusivity than Si (in GaAs), which will prevent unwanted movement of dopant atoms during thermal cycling [5]. We show that Te can dope $In_{0.53}Ga_{0.47}As$ up to $2.6\times10^{19}\,cm^{-3}$, and that the contact resistivity between an ex-situ deposited metal and Si and Te co-doped InAs and $In_{0.53}Ga_{0.47}As$ is lower than that of InAs and $In_{0.53}Ga_{0.47}As$ doped only by Si.

Specifically, we present room temperature Hall measurement of the Te doped $In_{0.53}Ga_{0.47}As$ Hall samples using a standard Van der Pauw technique showing electrically active carrier concentrations of up to $2.6\times10^{19}\,cm^{-3}$ (with mobility of 1466 cm^2/V s) without saturation effects. Co-doping of $In_{0.53}Ga_{0.47}As$ by Si and Te lowered overall sheet resistance, but did so by improving mobility and not increasing total electrically active impurity incorporation (which has been previously demonstrated to lower contact resistivity [3]). Si, Te, and Si+Te doped $In_{0.53}Ga_{0.47}As$ has a sheet resistance of 3.65, 3.62, and 2.95 Ω, respectively. Simultaneously, the active carrier concentrations for Si, Te, and Si+Te doped $In_{0.53}Ga_{0.47}As$ were 4.39, 2.16, and $3.81\cdot10^{19}\,cm^{-3}$ while the mobilities were 780, 1601, and 1111 cm^2/V s. The use of GaTe as an intentionally incorporated impurity improved the mobility of carriers in the $In_{0.53}Ga_{0.47}As$ by acting as a surfactant that improved material quality [6,7]. 50 nm of Si and Te co-doped InAs grown at 500 and 450 °C showed active carrier concentrations of 5.99 and $7.05\times10^{19}\,cm^{-3}$, respectively. Finally, the incorporation of Te during the growth of n^+ $In_{0.53}Ga_{0.47}As$ and n^+ InAs layers lowers ex-situ ohmic contact resistance to these same layers as compared to doping with only Si. Specifically, the contact resistivity (as measured by transmission line model/measurement (TLM) test structures) to 60 nm of Si and Te co-doped InAs (sheet resistance of 18.9 Ω) was 6.6 Ω μm (2.3 Ω μm^2) while the contact resistivity to 60 nm of Si doped InAs (sheet resistance of 25.3 Ω) was 9.9 Ω μm (3.9 Ω μm^2). The contact resistivity to 60 nm of Si

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http://dx.doi.org/10.1016/j.jcrysgro.2012.12.122

and Te co-doped $In_{0.53}Ga_{0.47}As$ (sheet resistance of 24 Ω) was 6.8 Ω μm (1.9 Ω μm^2) while the contact resistivity to 60 nm of Si doped $In_{0.53}Ga_{0.47}As$ (sheet resistance of 31 Ω) was 8.5 Ω μm (2.3 Ω μm^2). These results suggest that co-doping of $In_xGa_{1-x}As$ by Si and Te is an effective way to lower the metal–semiconductor contact resistance and resistivity.

2. Experiment

Semiconductor epitaxial layer structures were prepared in a Varian (Veeco) Gen II solid source MBE system. All samples were grown on (100) semi-insulating InP substrates and were nominally lattice matched (to within 0.5% alloy concentration) to InP with V:III BEP ratios during growth of ~30 unless otherwise specified. Samples for Hall measurement had the following layer structure: 150 nm $In_{0.52}Al_{0.48}As$ (125.0 nm of which were grown at 490 °C while the remaining 25.0 nm were grown while the sample was cooling to 400 °C), 500 nm Te doped $In_{0.53}Ga_{0.47}As$ (grown at 400 °C) with Te (GaTe source material) cell temperatures of 475, 487, 500, 520, 525, 550, 562, 582, and 625 °C; 150 nm $In_{0.52}Al_{0.48}As$ (125.0 nm of which were grown at 490 °C while the remaining 25.0 nm were grown while the sample was cooling to 400 °C), 500 nm Si doped $In_{0.53}Ga_{0.47}As$ (grown at 400 °C) with Si cell temperature of 1392 °C; and 150 nm $In_{0.52}Al_{0.48}As$ (125.0 nm of which were grown at 490 °C while the remaining 25.0 nm were grown while the sample was cooling to 400 °C), 500 nm Si and Te co-doped $In_{0.53}Ga_{0.47}As$ (grown at 400 °C) with Si cell temperature of 1392 °C and Te cell temperature of 625 °C. Contact resistance measurement structures had the following form: Samples A and B: 400 nm $In_{0.52}Al_{0.48}As$ (375.0 nm of which were grown at 490 °C while the remaining 25.0 nm were grown while the sample was cooling to 460 °C), 3 nm of Si-doped 1×10^{19} cm^{-3} $In_{0.52}Al_{0.48}As$ (grown at 460 °C), 7 nm of $In_{0.53}Ga_{0.47}As$ (grown at 460 °C), 60 nm (Si (A) or Si and Te doped (B)) $In_{0.53}Ga_{0.47}As$ (growth conditions discussed below). Samples C and D: 400 nm $In_{0.52}Al_{0.48}As$ (375.0 nm of which were grown at 490 °C while the remaining 25.0 nm were grown while the sample was cooling to 460 °C), 3 nm of Si-doped 1.3×10^{19} cm^{-3} $In_{0.52}Al_{0.48}As$ (grown at 460 °C), 10 nm of $In_{0.53}Ga_{0.47}As$, (grown at 460 °C) and 60 nm (Si (C) or Si and Te doped (D)) InAs (growth conditions discussed below). Samples A–D were removed from vacuum prior to growth of the top n^+ layer. To clean the surface prior to reloading to vacuum, samples were oxidized with UV ozone [8] and those oxides were removed by a 1 min. dip in $10H_2O$:1 HCL [9–12]. At a base pressure of approximately 1×10^{-9} Torr, samples were heated to 420 °C and treated with thermally cracked hydrogen ($\approx 1\times10^{-6}$ Torr partial pressure) for 40 min prior to regrowth. The cracking filament was operated at 8 A yielding a filament temperature of ~2200 °C and a cracking efficiency of ~10%. After regrowth Samples A–D were metalized with lifted-off e-beam evaporated Ti/Pd/Au and mesa isolated (by wet chemical etching) by standard photolithographic techniques.

The top n^+ layers of Samples A–D were regrown at 500 °C with V:III beam equivalent pressure ratios of ~5.0 and employed quasi-migration enhanced epitaxy (MEE); which can provide smooth, facet-free surfaces and good fill-in of regrowth near the edges of the dielectric masks [13,14]; however, as there were no dielectric masks on any of the samples, these processes were undertaken in order to be congruent with processing steps in the fabrication of MOSFETs in a gate-last process flow [15–17]. Quasi-MEE growth or, in this case, regrowth is performed in a series of cycles consisting of a growth phase wherein group III and group V fluxes are first impinging on the sample surface simultaneously, followed by a growth interruption where only the group V flux is supplied. This group III flux interruption permits further migration of the group III species on the surface [18]. During regrowth one MEE growth period consisted of a growth phase in which ~0.5 nm of InAs or $In_{0.53}Ga_{0.47}As$ is deposited followed by a 15 s growth interruption under exposure to the As_2 flux.

Hall measurements were carried out by placing indium contacts on ~1 cm^2 pieces which were cleaved from the original growths; however, these were not the same pieces that were used for contact resistance extraction, which may introduce unintended error. TLM structures were used to extract resistance as a function of gap spacing, and contact resistance and resistivity were derived from the TLM method [19]. An Agilent 4155C semiconductor parameter analyzer with a four-point (Kelvin) probe technique was used to measure resistance of a TLM structure optimized to reduce errors in contact resistance extraction [20]. Contact separations were varied from ~1.0 μm to 25 μm on devices with 15 μm width. Device dimensions were all measured by scanning electron microscope (SEM) after electrical measurement. The n^+ layers were kept less than 75 nm to mitigate two-dimensional current flow within layers which would invalidate the TLM extraction.

3. Results and discussion

Fig. 1 shows an Arrhenius plot of inverse GaTe cell temperature (abscissa) versus active carrier concentration (ordinate). The plot shows no saturation of active carrier concentration with increasing GaTe cell temperature up to a GaTe cell temperature of 625 °C (a corresponding active carrier concentration of 2.6×10^{19} cm^{-3}), i.e. the trend shows linear behavior on a log plot over a wide range of dopant cell temperatures. In general, the doping of $In_{0.53}Ga_{0.47}As$ by Te ranges from 2.1×10^{17} to 2.6×10^{19} cm^{-3} indicating that Te is an effective dopant over a wide range of active carrier concentrations. Pushing the GaTe cell temperature higher may increase active carrier concentrations. When saturation of active carriers with increasing metallurgical doping occurs, optimization of growth conditions may

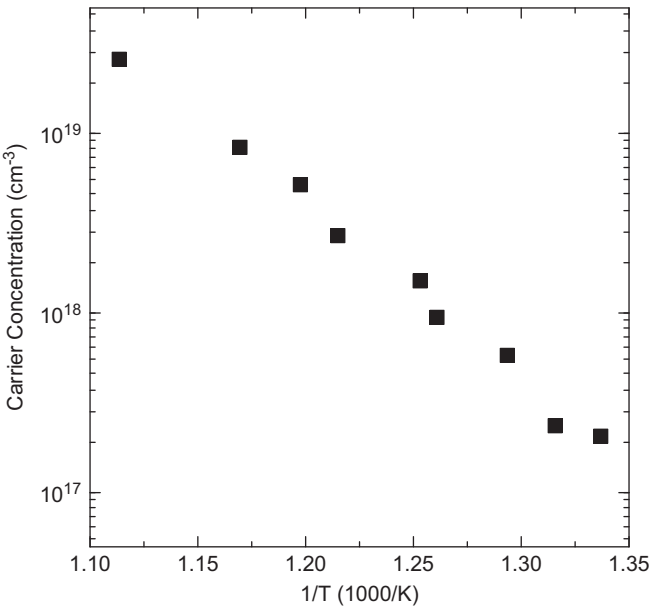

Fig. 1. Arrhenius plot of inverse GaTe cell temperature (abscissa) versus active carrier concentration (ordinate).

help push this maximum active carrier concentration yet higher. Three samples were prepared to compare the Hall measurement of Si only, Te only, and Si and Te co-doped $In_{0.53}Ga_{0.47}As$. Table 1 summarizes the results of the Hall measurement. Specifically, Table 1 shows that Si, Te, and Si+Te doped $In_{0.53}Ga_{0.47}As$ had a sheet resistance of 3.65, 3.62, and 2.95 Ω, respectively. Simultaneously, the active carrier concentrations for Si, Te, and Si+Te doped $In_{0.53}Ga_{0.47}As$ were 4.39, 2.16, and 3.81×10^{19} cm^{-3} while the mobilities were 780, 1601, and 1111 $cm^2/V\,s$, indicating that Te improves the mobility of carriers in the $In_{0.53}Ga_{0.47}As$. It is known that Te acts as a surfactant, and can improve the material quality of heavily lattice mismatched alloys, thus Te is likely acting as a surfactant that helps improve the incorporation of Si and thus improves material quality [6,7].

Fig. 2 shows atomic force microscopy (AFM) images of the surfaces of the Si, Fig. 2(a), and Si+Te, Fig. 2(b), doped $In_{0.53}Ga_{0.47}As$ growths. There is a reduction of the number of surface defects, in particular, the cat-eye-like defects, from 1.10×10^7 cm^{-2} in the Si doped sample (Fig. 2(a)) to 4.75×10^6 cm^{-2} in the Si+Te co-doped sample (Fig. 2(b)). This reduction corroborates the improvement in material quality evidenced in the improved Hall mobility via the introduction of Te.

Table 1
Summary of Hall data for Si, Te, and Si+Te co-doped $In_{0.53}Ga_{0.47}As$.

	Si doped $In_{0.53}Ga_{0.47}As$	Te doped $In_{0.53}Ga_{0.47}As$	Te and Si co-doped $In_{0.53}Ga_{0.47}As$
R_{SH} (Ω)	3.65	3.62	2.95
μ ($cm^2/V\,s$)	780	1601	1111
n_d (cm^{-3})	4.39×10^{19}	2.16×10^{19}	3.81×10^{19}

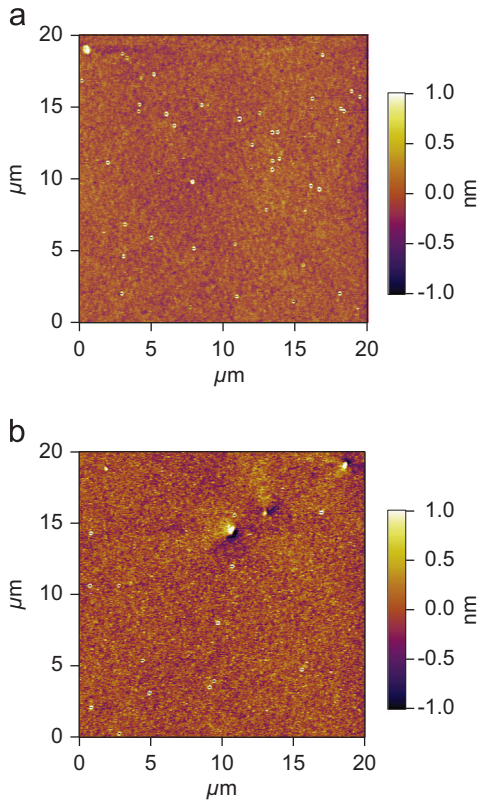

Fig. 2. AFM images of (a) Si doped n^+ InGaAs and (b) Si+Te co-doped n^+ InGaAs surfaces.

The reduction of the number of surface-terminated defects gives the wafer surface a more optically specular reflection.

Fig. 3 shows plots of measured resistance versus gap spacing (standard TLM measurement technique) for the various samples, and Table 2 summarizes the measurement results. Fig. 3(a) shows the variation of TLM structure resistance versus contact spacing for Si doped and Si and Te co-doped $In_{0.53}Ga_{0.47}As$ while Fig. 3(b) shows the same data for the Si doped and Si and Te co-doped InAs. The contact resistivity to the Si and Te co-doped $In_{0.53}Ga_{0.47}As$ (sheet resistance of 24 Ω) was 6.8 Ω μm (1.9 Ω μm^2) while the contact resistivity to the Si doped $In_{0.53}Ga_{0.47}As$ (sheet resistance of 31 Ω) was 8.5 Ω μm (2.3 Ω μm^2). The contact resistivity to the Si and Te co-doped InAs (sheet resistance of 18.9 Ω) was 6.6 Ω μm (2.3 Ω μm^2) while the contact resistivity to the Si doped InAs (sheet resistance of 25.3 Ω) was 9.9 Ω μm (3.9 Ω μm^2). The introduction of Te as a second dopant decreases sheet resistance in the TLM structures made of InAs and $In_{0.53}Ga_{0.47}As$ and also decreases the sheet resistance in the $In_{0.53}Ga_{0.47}As$ Hall structure. Contact resistance (Ω μm) and contact resistivity (Ω μm^2) are decreased by the intentional incorporation of Te along with Si. These results suggest that co-doping of $In_xGa_{1-x}GaA$ by Si and Te is an effective way to lower the metal–semiconductor contact resistance and resistivity. The Hall (Table 1) and AFM (Fig. 2) results suggest that the lowered contact resistance is

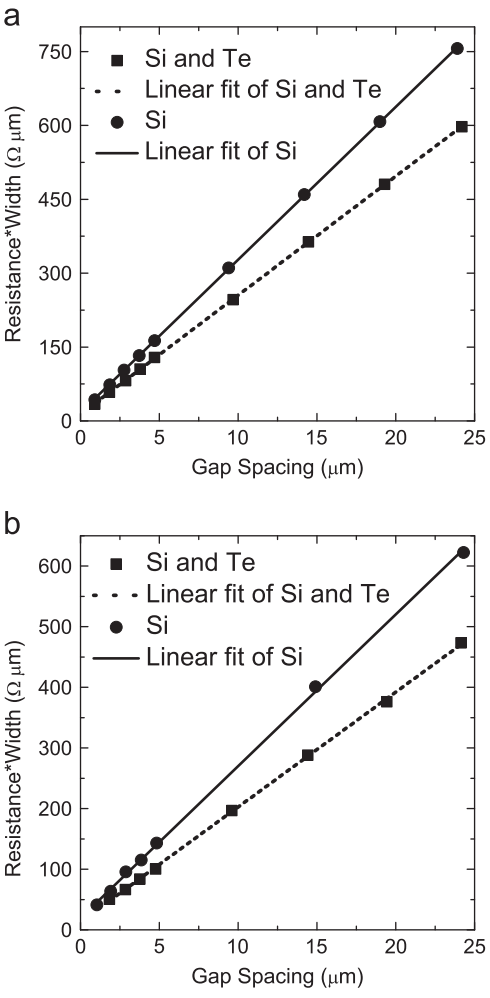

Fig. 3. Plot of variation of TLM structure resistance (normalized to device width) versus contact separation (symbols) and linear fit (lines) for (a) $In_{0.53}Ga_{0.47}As$ doped with Si and Si+Te and (b) InAs doped with Si and Si+Te.

Table 2
Summary of contact resistance data extracted by the TLM model for Si and Si+Te doped InAs and $In_{0.53}Ga_{0.47}As$.

	Si doped InAs	Si+Te doped InAs	Si doped $In_{0.53}Ga_{0.47}As$	Si+Te doped $In_{0.53}Ga_{0.47}As$
R_{SH} (Ω)	25.3	18.9	31.0	24.0
R_C ($\Omega\,\mu m$)	9.9	6.6	8.5	6.8
ρ_C ($\Omega\,\mu m^2$)	3.9	2.3	2.3	1.9

not a property of increased active carrier concentration, which is the typical mode of improving contact resistance [3]. But, rather, the improved contact resistivity is likely a consequence of improved material quality and improved interface quality, which has been shown to improve contact resistivity [21], as evidenced by the improved Hall mobility (Table 1) and lower density of surface defects (Fig. 2) for structures that incorporate Te. In addition to the lowered contact resistivity, the lowered sheet resistance of the devices that incorporated Te would reduce external parasitic resistances if these materials were incorporated as a regrown source or drain as in Lee et al. [15].

4. Conclusion

We have report lowered sheet resistance, contact resistance ($\Omega\,\mu m$), and contact resistivity ($\Omega\,\mu m^2$) to InAs and $In_{0.53}Ga_{0.47}As$ as a result of Te incorporation. Hall measurements indicate that the addition of Te as a co-dopant increases the mobility of the material, likely by acting as a surfactant during growth which improves material quality and surface morphology. This improved material quality and surface morphology lead to improved interface quality and lowered contact resistance. Specifically, with the introduction of Te as a co-dopant, contact resistances (resistivities) to InAs go from 9.9 $\Omega\,\mu m$ (3.9 $\Omega\,\mu m^2$) to 6.6 $\Omega\,\mu m$ (2.3 $\Omega\,\mu m^2$), and contact resistances (resistivities) to $In_{0.53}Ga_{0.47}As$ go from 8.5 $\Omega\,\mu m$ (2.3 $\Omega\,\mu m^2$) to 6.8 (1.9 $\Omega\,\mu m^2$).

Acknowledgments

This work was supported by the SRC Non-classical CMOS Research Center (Task 1437.006). A portion of this work was done in the UCSB Nanofabrication facility, part of the NSF funded NNIN network and MRL Central Facilities supported by the MRSEC Program of the NSF under Award no. MR05-20415.

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