Low Distortion 50 GSamples/s Track-Hold and Sample-Hold Amplifiers

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***Abstract*—We report 50 GSamples/s track-hold amplifier (THA) and sample-hold amplifier (SHA) designed and fabricated in a 250 nm InP double heterojunction bipolar transistor (DHBT) technology. Because the base-emitter junction reverse breakdown voltage is low in the process technology employed, the circuits use a base-collector junction diode as the switching element in the signal path. Operating with −5 V and −2.5 V supplies, the THA achieves >+16 dBm input-referred third-order intercept (IIP3) at signal frequencies below 22 GHz, while the SHA achieves IIP3>+17 dBm for 2–22 GHz inputs.**

***Index Terms*—Analog-to-digital converter (ADC), track-hold amplifier (THA), sample-hold amplifier (SHA), InP technology, nonlinearity analysis.**

I. Introduction

OPTICAL and microwave receivers increasingly use digital processing and consequently high speed analog-to-digital converters (ADCs) are required [1]. Overall receiver performance is strongly dependent on the ADC bandwidth, sampling rate, resolution and linearity; hence the ADC's input track-hold amplifier (THA) or sample-hold amplifier (SHA) must have wide bandwidth, low noise, and low distortion. Applications such as satellite and wireless communications [2], [3], military radar systems [4], DSP-based fiber optic equalizer [5] and instrumentation [6] also benefit from a high performance THA.

A variety of track-hold amplifiers with more than 10 GSamples/s sampling rate have been reported, including designs in SiGe heterojuction bipolar transistor (HBT) [1]–[11], CMOS [12], InP HBT [13]–[18] and InP BiCMOS [19] process technologies. These designs use either diode bridges [3], [4] or switched emitter followers (SEF) [1], [2], [5]–[19] as the sampling element.

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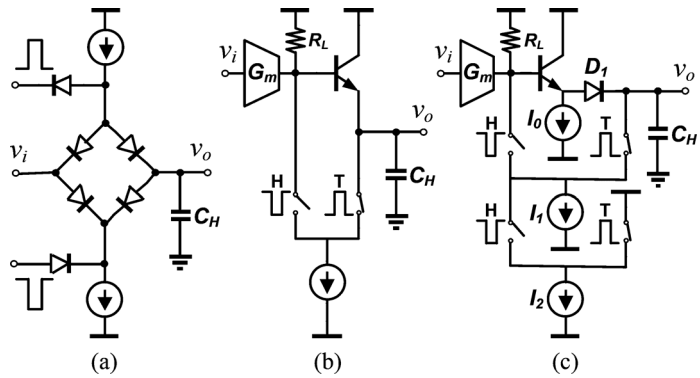


Fig. 1. Implementation of the track-hold switch using: (a) diode bridge; (b) switched emitter follower (SEF); (c) base-collector diode.

Here we report a track-hold amplifier with sampling rate up to 50 GSamples/s [20] implemented in a 250 nm InP technology. We also report a sample-hold amplifier formed from two cascaded track-hold amplifiers in a master-slave configuration. These ICs use a novel switching stage in which a DHBT base-collector diode is driven and switched by an emitter follower (Fig. 1(c)). While design of this stage is broadly similar to that of a switched emitter follower [5], the base-collector diode has smaller RC junction parasitics, and much larger reverse breakdown, than the DHBT emitter-base junction, factors which provide shorter sampling capacitor charging times, larger off-state isolation, and smaller off-state leakage currents than those of a switched emitter follower.

Because the input and output buffers were designed for low third-order distortion, the reported sample-hold amplifier has >17 dBm input-referred third order intercept point (IIP3) for 2–22 GHz input frequencies, and >55 dB spurious-free dynamic range SFDR for 2–18 GHz input frequencies. We will present design of these ICs, and will compare their performance to similar designs fabricated in a 500 nm InP technology. Hand analysis of circuit distortion by direct solution of the circuit nonlinear relationships becomes intractable as the number of nonlinear elements increases, and we therefore present analysis of the buffer stage third-order distortion using a more concise perturbation technique.

In this paper, Section II will describe the 250 nm and 500 nm InP technologies used in this work. Section III will review the THA switching techniques and will describe in detail the base-collector diode characteristics. Section IV will explain the SHA architecture and describe nonlinearity analysis of the buffers. Measurement results will be presented in Section V. The paper concludes in Section VI.

II. 250 NM AND 500 NM INP DHBT PROCESS

The first iteration of THA and SHA ICs were designed using a 250 nm InP DHBT process. When biased at an emitter current density of $J_E = 8$ mA/μm^2, transistors in this technology having a 250 nm by 4μ m emitter-base junction, exhibit a current-gain cutoff frequency of $f_\tau = 370$ GHz, a power-gain cutoff frequency of $f_{\max} = 650$ GHz, and a current gain of $\beta = 25$.

Subsequent to characterization of these ICs, a second set of THA and SHA ICs were fabricated in a 500 nm InP DHBT process. In these designs, IC performance was characterized as a function of key circuit variables, in particular the area of the base-collector sampling diode. When biased at $J_E = 4$ mA/μm^2, transistors in this technology having a 500 nm by 4 μm emitter-base junction, exhibit a current-gain cutoff frequency of $f_\tau = 290$ GHz, a power-gain cutoff frequency of $f_{\max} = 300$ GHz, and a current gain of $\beta = 40$. For both processes, there are four Au interconnect planes, M_1, M_2, M_3 and M_4 (top) of 1 μm, 1 μm, 1 μm, and 3 μm thicknesses. A 3 μm thick Benzocyclobutene (BCB) ($\epsilon_r = 2.7$) dielectric separates M_4 from M_3, while 1 μm of BCB separates M_3 from M_2, and M_2 from M_1. The process provides 0.3 fF/μm^2 MIM capacitors and 50 $\Omega/\square$ thin-film-resistors (TFR).

III. BASE-COLLECTOR DIODE AS A SWITCH

Fig. 1 shows three different implementations of a track-hold switch. The topology shown in Fig. 1(a) is an idealized diode sampling bridge [3], [21]–[24]. If fast Schottky diodes are used [21], the diode bridge can have wide bandwidth, but there are design challenges in matching the positive and negative current sources and in matching the timing of the positive and negative pulse drivers. The switched emitter follower (SEF) topology, Fig. 1(b), first proposed in [25], does not require complementary positive and negative DC current sources and complementary positive and negative pulse drivers, and has been reported extensively in the literature [1], [2], [5]–[16]. The SEF has better linearity and dynamic range compared to the diode bridge. However, the emitter follower can show ringing or oscillation given the large capacitive load.

To enable $f_{\max}$ above 500 GHz, the InP DHBTs used in this work have extremely high emitter and base doping, and extremely narrow (10–20 nm) emitter-base depletion widths [26]. As a consequence, the emitter-base junction reverse breakdown voltage is low, and the junctions show substantial reverse leakage currents and even weak Esaki-diode characteristics [27], [28] in reverse bias. This large leakage current would significantly discharge the hold capacitor during the signal hold period.

An alternative track-hold switch (Fig. 1(c)) adds a series sampling diode D_1 and current source I_0 to the switched emitter follower of Fig. 1(b). In this configuration, during the signal hold period the bias source I_0 provides bias current to the emitter follower, and the emitter follower remains on at all times. It is the diode D_1 alone which switches, with an on-state bias current I_1 and (in the absence of an RF input) an off-state reverse bias voltage $R_L(I_1 + I_2)$.

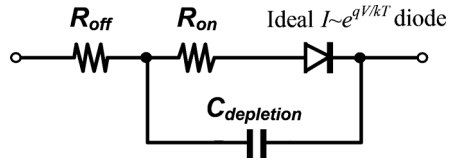


Fig. 2. Circuit model of the base-collector sampling diode with off-state series resistance R_{off}, on-state series resistance R_{on}, and depletion capacitance $C_{depletion}$.

Physics of the sampling diode is critical to the design. In a forward-biased PN junction, such as the base-collector junction of a GaAs/AlGaAs or Si/SiGe heterojunction bipolar transistor (HBT), substantial minority carriers are stored in both the N and P regions. Removal of this stored minority charge results in a significant reverse recovery time [29]. Note that in a bipolar transistor, the N+ subcollector is much thicker than the P+ base, and the total hole minority charge stored in the subcollector is much greater than the electron minority charge stored in the base. To avoid such charge storage, sample-hold ICs can use Schottky diodes [22] with their negligible minority carrier storage, although additional IC process steps are necessary to fabricate these.

Unlike the base-collector junctions of GaAs/AlGaAs and SiGe/Si HBTs, the IC technology here employed provides *double* heterojunction bipolar transistors (DHBTs), wherein the base-collector junction contains a grade from a $\sim$0.7 eV bandgap InGaAs base to a $\sim$1.4 eV bandgap collector and subcollector [30]. The base-collector heterojunction presents a large energy barrier to holes, preventing significant hole injection under forward junction bias from the base into the collector. Hole minority carrier storage is thereby eliminated. Although electron minority carrier storage in the base remains present in forward-biased DHBT base-collector junctions, the minority carrier storage time is small. In the case of an ungraded base, the electron minority carrier storage time in the base under forward-biased base-collector bias would be equal to the (electron) base transit time under normal transistor bias. Given that the DHBTs used here employ a graded base to *accelerate* electron transport from emitter to collector, under forward-biased base-collector junction bias the same grade *retards* the electron transport from the collector to the base contact. Under base-collector junction forward bias the electron minority carrier storage time is then $\sim$5:1 larger than the base transit time, i.e., $\sim$0.4 ps. This time has minimal impact upon the performance of the ICs reported in this work.

Fig. 2 shows an approximate equivalent circuit for the base-collector junction. In addition to the normal junction depletion capacitance $C_{depletion}$, and the normal parasitic series resistance R_{off} associated with Ohmic contacts and N+ and P+ semiconductor layer resistivities, the diode also has a significant on-state series resistance $R_{\mathrm{on}} \sim T_c^2/2\epsilon v_{th}$ associated with the electron space-charge within the depletion region, where T_c is the collector depletion thickness, ϵ the semiconductor permeability, and v_{th} the carrier thermal velocity. For a 4 μm^2 base-collector diode in the 250 nm InP DHBT technology, $R_{\mathrm{on}} = 26\ \Omega$, $R_{\mathrm{off}} = 2\ \Omega$, and $C_{depletion} = 8$ fF; $C_{depletion}$ varies in proportion to the diode junction area while R_{on} and R_{off} vary as its inverse.

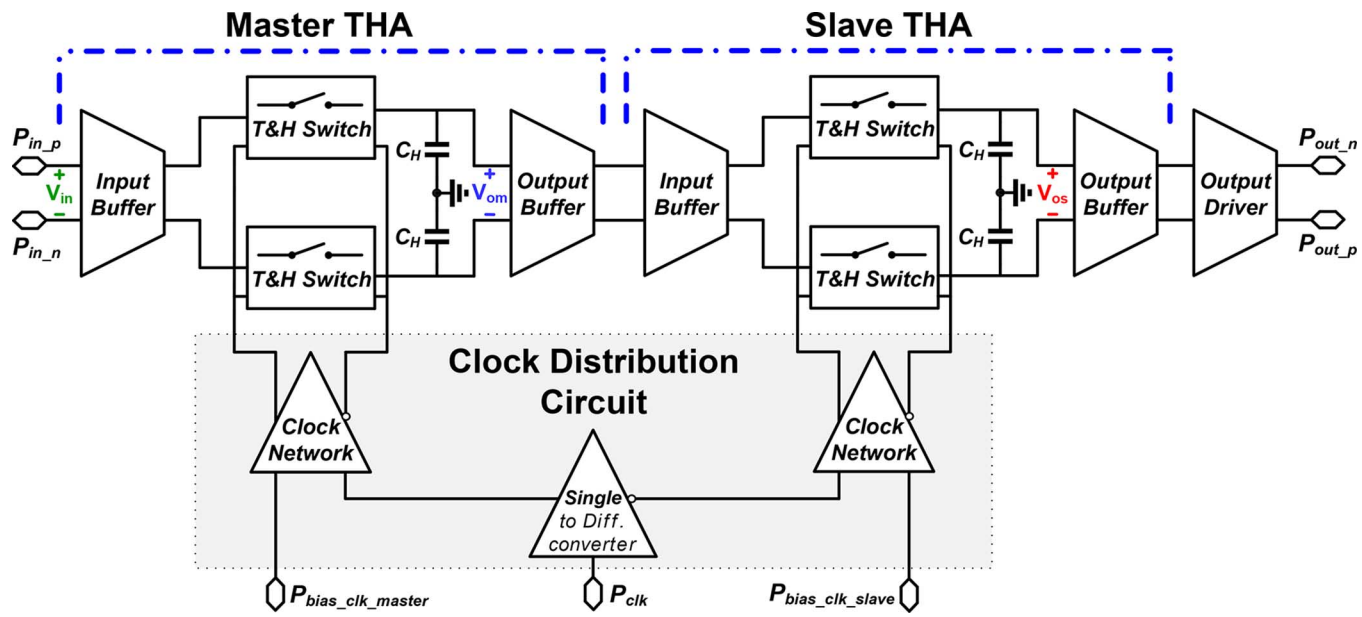


Fig. 3. Sample-hold amplifier block diagram.

In a track-hold switch (Fig. 1(c)) with hold capacitance $C_{\rm hold}$, absent additional circuit charging resistances, the track-mode charging time is $\tau_{\rm track} \sim (R_{\rm off} + R_{\rm on})C_{hold}$, while the hold mode isolation is $\sim C_{depletion}/C_{hold}$. The diode time constant $R_{\rm on}C_{depletion}$ is therefore a key device figure of merit. Note that in the 250 nm InP DHBT technology, $R_{\rm on}C_{depletion}$ is small, approximately 200 fs, which is a key advantage of the DHBT base-collector sampling diode.

IV. Sample-Hold Amplifier Design

Track-hold amplifiers are key components supporting analog-to-digital converters (ADCs). A THA is composed of a sampling switch with a hold capacitance; in track mode the THA output follows the input signal, holding the output constant when the sampling switch is open. To accurately digitize the signal, most ADCs must have an input signal with minimal time variation during the conversion period. This is the function of a THA or SHA at the ADC input. While the THA output varies whenever the circuit is in track mode, for a sample-hold circuit the output is stable except during switching transitions. This provides greater timing margins in ADC design.

A sample-hold amplifier (SHA), as shown in Fig. 3, is composed of cascaded master and slave THAs while a distribution network provides two sets of clocks, at $\sim$180° phase separation, to the master and slave THAs. When its clock is high, the master THA tracks the input signal, while the slave THA is in hold mode, holding its output signal from the previous acquisition cycle. Upon a clock transition, the master THA holds its output and the slave THA switches to track mode. The slave THA output is then equal to its input, i.e., the master THA output. Fig. 4 shows simulated waveforms within the reported 250 nm SHA with a 20 GHz clock signal, where $V_{\rm in}$ is the input signal and $V_{\rm om}$ and $V_{\rm os}$ are the output signals of the master and slave THAs, respectively. Note that the outputs of the slave THA are stable with time in both track and hold modes, with the outputs changing only at the sampling transition times.

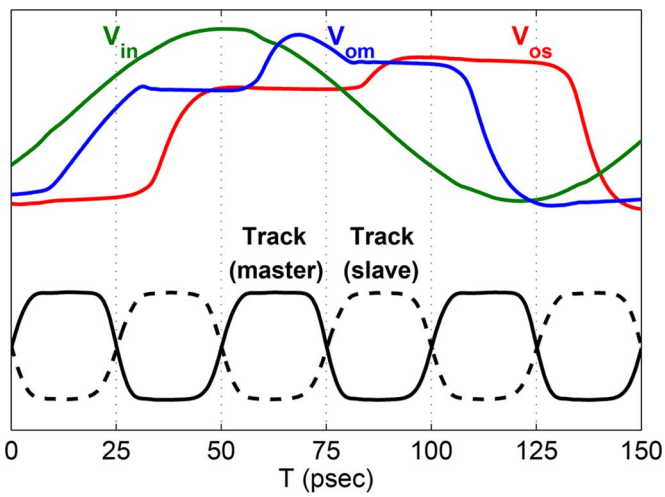


Fig. 4. Simulated output waveforms of the proposed SHA in Fig. 3 with a 20 GHz clock signal.

A. Track-Hold Switch

The THA architecture of Fig. 3 is based on that proposed in [25] where a high linearity input buffer precedes differential track-hold switches. Fig. 5 presents the transistor-level schematic diagram of the input buffer and track-hold switches for the designs reported here. The core of the input buffer is a differential pair with emitter degeneration (Q_3, Q_6, R_{EE3}, R_L), to which a compensation stage (Q_1, Q_4, R_{EE1}) is added to cancel the cubic distortion arising from nonlinear variation with collector currents of transistor base-emitter voltages [24].

The differential output of input buffer is connected to two track-hold switches which consist of a sampling base-collector diode, a hold capacitance and a control circuit. Although the two track-hold switches always operate at the same mode (track or hold), to distinguish the track mode operation from the hold mode, the left side of the Fig. 5 indicates bias conditions when

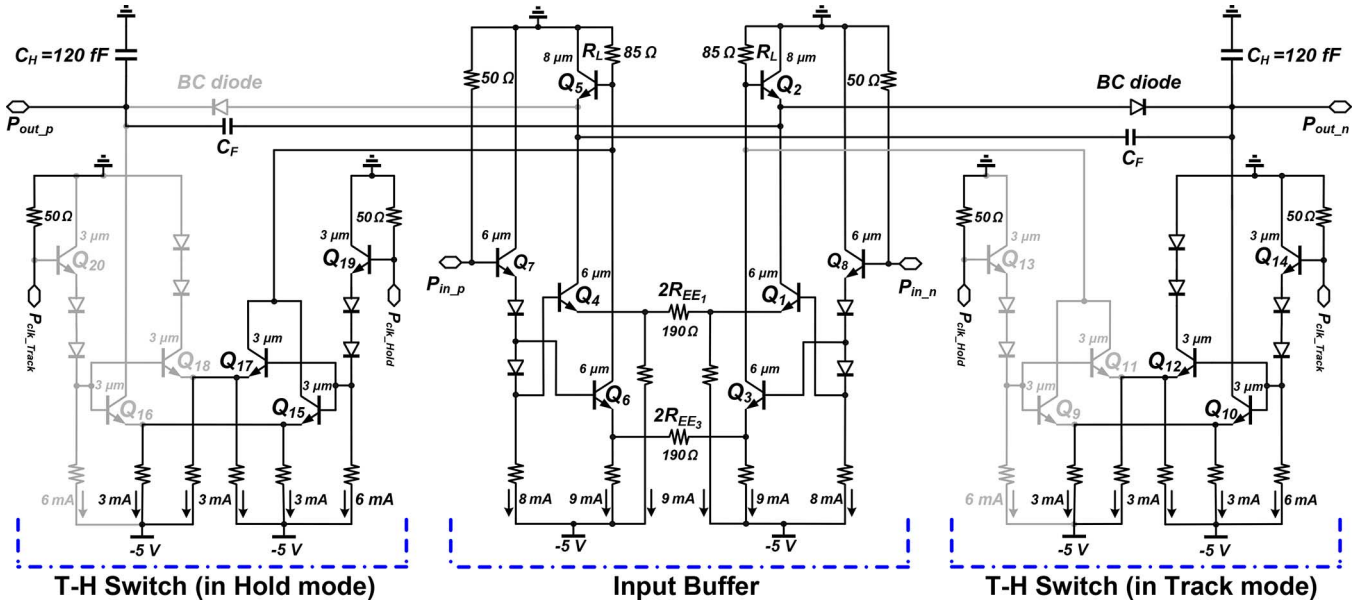


Fig. 5. Schematic diagram of the input buffer preceding the differential T&H switches of the THAs of Fig. 3. All HBTs have 250 nm emitter width. Emitter junction lengths are indicated in the figure.

operating in the hold mode, while the right side of the figure indicates bias conditions when operating in the track mode; with inactive circuit connections indicated by gray shading. The operation of the track-hold switches can be explained as follows:

- In track mode operation (shown in the right side of Fig. 5), transistors $Q_{10,16}$ are conducting and each is drawing a 6 mA current from $Q_{2,5}$ which consequently turns on the base-collector diodes. $Q_{9,11,15,17}$ are off in this mode.
- The clock signal in hold mode operation (shown in the left side of Fig. 5) turns on $Q_{9,11,15,17}$ and switches off $Q_{10,12,16,18}$. Therefore, a 12 mA current is drawn from R_L and produces a voltage drop of $\sim$1 V across that which completely turns off the sampling diode. Note that in order to have high linearity not only at DC, but also at Nyquist rate, this voltage drop across R_L must be at least twice the largest input peak RF signal amplitude. This requirement makes high sampling rates more difficult to obtain.

Two feedthrough cancellation capacitors (C_F) equal to the capacitance of the base-collector diodes are also added to completely eliminate the hold mode signal feedthrough. Explicit design methodology of THA circuit is described in [5], [16], [25], and [31].

B. Nonlinearity Analysis of the Input Buffer

Fig. 6(a) shows the simplified half circuit of the input buffer in track mode, and its corresponding ac small-signal model is shown in Fig. 6(b). In track mode, the primary sources of signal distortion are the modulation of the base-emitter voltages $(\delta v_{be1}, \delta v_{be2}, \text{ and } \delta v_{be3})$ of transistors Q_1, Q_2, and Q_3, and the modulation of the forward voltage of the switching diode (δv_D). These distortion voltages are induced by the currents $(i_{c1}, i_{c2}, i_{c3}, i_D)$ passing through these junctions. Circuit distortion is minimized by selecting the circuit topology and design such that contributions of these distortion generators sum to zero at the buffer output.

In the circuit, the target signal frequencies are typically less than 10% of f_τ, hence within the transistor stages themselves, we will neglect the effect of transistor junction capacitances, and hence will neglect the effect of frequency-dependent current amplitudes upon the circuit distortion. The hold capacitance must however be large to maintain adequately low droop rates, hence the signal current in the sampling diode and the resulting distortion voltage (δv_D), both vary strongly with frequency, and their effect on the distortion of the circuit needs to be considered.

The input/output characteristics of a weakly nonlinear, frequency-independent amplifier can be modeled by a Taylor series truncated at the third order

$$v_o(t) \approx \alpha_0 + \alpha_1 v_i(t) + \alpha_2 v_i^2(t) + \alpha_3 v_i^3(t). \tag{1}$$

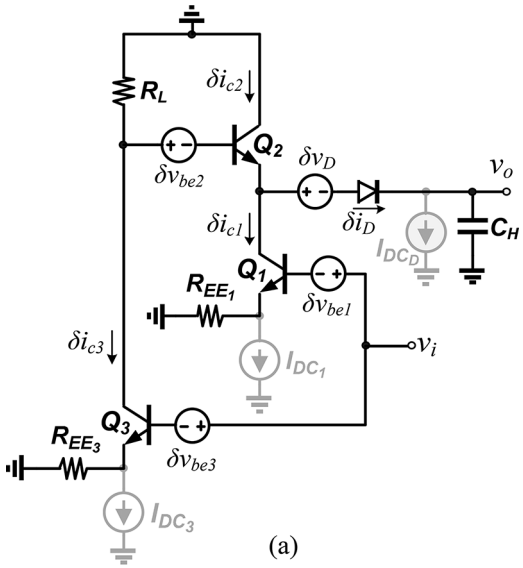
With a two-tone input of the form $v_i(t) = V_p(\sin\omega_1 t + \sin\omega_2 t)$, the cubic term will generate two-tone intermodulation distortion products at frequencies $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$, whose amplitude relative to that of the linear output responses at ω_1 and ω_2 is [32]

$$IM_3 = \frac{3}{4}\frac{\alpha_3}{\alpha_1}V_P^2. \tag{2}$$

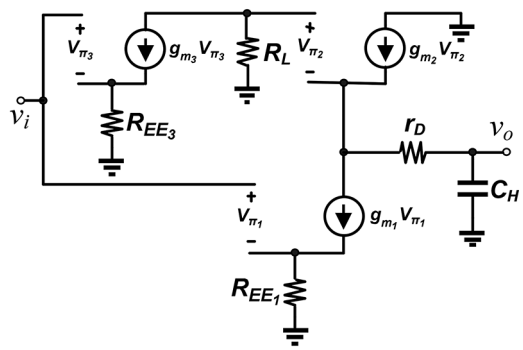
We show below a simple procedure to determine the coefficients α_1 and α_3, from which the IM_3 distortion can be calculated [33]. We use the simplified model for the transistors assuming $\beta \to \infty$, in order to find meaningful expressions in the simplest possible form to describe distortion coefficients associated with (2).

The coefficient α_1, i.e., the small-signal gain of the circuit of Fig. 6(a), is

$$\alpha_1 = \frac{v_o}{v_i} = \frac{-X_C}{Z_L + 1/g_{m_2}} \times \left[\frac{1/g_{m_2}}{R_{EE_1} + 1/g_{m_1}} + \frac{R_L}{R_{EE_3} + 1/g_{m_3}}\right] \tag{3}$$



(a)



(b)

Fig. 6. (a) Simplified half circuit model of the input buffer and (b) its corresponding ac small-signal model.

where $X_C = 1/j\omega C_H$, $Z_L = r_D + X_C$ and r_D is the small-signal resistance of the sampling diode. To find the coefficient α_3, we take the following steps: First using a simplified *linear* equivalent circuit model (Fig. 6(b)), the transistor small-signal collector currents and the diode small-signal current are computed as a function of the input signal variation (δv_i), from which we find

$$\begin{cases} \delta i_{c1} = \dfrac{1}{R_{EE_1} + 1/g_{m_1}} \delta v_i \\ \delta i_{c3} = \dfrac{1}{R_{EE_3} + 1/g_{m_3}} \delta v_i \\ \delta i_D = \dfrac{-1}{Z_L + 1/g_{m_2}} \left[\dfrac{1/g_{m_2}}{R_{EE_1} + 1/g_{m_1}} + \dfrac{R_L}{R_{EE_3} + 1/g_{m_3}} \right] \delta v_i \\ \delta i_{c2} = \delta i_{c1} + \delta i_D. \end{cases} \tag{4}$$

In the second step, using a perturbation technique, we assign a small-signal voltage source to each base-emitter (δv_{be_n}) and the base-collector (δv_D) junctions. This voltage source represents the *nonlinear* modulation of the junction voltage arising from the corresponding small-signal variation in the junction current. By superposition, the resulting change in the circuit output voltage is determined by separately computing the change in output voltage as each voltage source in Fig. 6(a) is separately applied, from which we find

$$\begin{cases} \delta v_o = \dfrac{X_C}{Z_L + 1/g_{m_2}} \times \dfrac{1/g_{m_2}}{R_{EE_1} + 1/g_{m_1}} \delta v_{be_1} \\ \delta v_o = \dfrac{-X_C}{Z_L + 1/g_{m_2}} \delta v_{be_2} \\ \delta v_o = \dfrac{X_C}{Z_L + 1/g_{m_2}} \times \dfrac{R_L}{R_{EE_3} + 1/g_{m_3}} \delta v_{be_3} \\ \delta v_o = -\dfrac{X_C}{Z_L} \delta v_D. \end{cases} \tag{5}$$

Consequently, the total effect of the perturbation signals due to the modulation of base-emitter voltages on the output voltage of the circuit is found by adding the expressions in (5) as follows:

$$\delta v_o = -\frac{X_C}{Z_L} \delta v_D + \frac{Z_L}{Z_L + 1/g_{m_2}} \times \left[\frac{1/g_{m_2}}{R_{EE_1} + 1/g_{m_1}} \delta v_{be_1} - \delta v_{be_2} + \frac{R_L}{R_{EE_3} + 1/g_{m_3}} \delta v_{be_3} \right]. \tag{6}$$

Next, the magnitudes of the small-signal perturbation voltage sources associated with the diode junctions in Fig. 6(a) are computed with respect to the small-signal junction currents using a Taylor series expansion as

$$\begin{cases} \delta v_{be_1} = \left(\dfrac{V_T}{I_{DC_1}}\right) \delta i_{C1} - \left(\dfrac{V_T}{2I_{DC_1}^2}\right) \delta i_{C1}{}^2 + \boxed{\left(\dfrac{V_T}{6I_{DC_1}^3}\right) \delta i_{C1}{}^3} \\ \delta v_{be_2} = \left(\dfrac{V_T}{I_{DC_2}}\right) \delta i_{C2} - \left(\dfrac{V_T}{2I_{DC_2}^2}\right) \delta i_{C2}{}^2 + \boxed{\left(\dfrac{V_T}{6I_{DC_2}^3}\right) \delta i_{C2}{}^3} \\ \delta v_{be_3} = \left(\dfrac{V_T}{I_{DC_3}}\right) \delta i_{C3} - \left(\dfrac{V_T}{2I_{DC_3}^2}\right) \delta i_{C3}{}^2 + \boxed{\left(\dfrac{V_T}{6I_{DC_3}^3}\right) \delta i_{C3}{}^3} \\ \delta v_D = \left(\dfrac{V_T}{I_{DC_D}}\right) \delta i_D - \left(\dfrac{V_T}{2I_{DC_D}^2}\right) \delta i_D{}^2 + \boxed{\left(\dfrac{V_T}{6I_{DC_D}^3}\right) \delta i_D{}^3} \end{cases} \tag{7}$$

cubic terms $(\delta v_{be_③}, \delta v_{D_③})$

where $V_T = KT/q$ and $I_{DC_1}, I_{DC_2}, I_{DC_3}, I_{DC_D}$ are the DC bias currents of the transistors Q_1, Q_2, Q_3 and sampling diode in track mode, respectively. Note that the linear terms in the Taylor series are now omitted, as the linear components of the voltage generators δv_{be1}, δv_{be2}, δv_{be3} and δv_D represent the linear modulation of base-emitter and base-collector junction voltages with changes in their corresponding output currents. The linear modulation of these junction voltages is of course already modeled in the analysis by the associated small-signal transconductances $g_m = I_{DC}/V_T$. Further note that the circuit is differential, hence the second order terms in (7) are suppressed. The distortion perturbation generators consequently contain only the cubic distortion terms. Substituting the currents in these cubic terms with the currents in (4), they can be represented as shown in (8), at the bottom of the next page.

Finally, replacing $\delta v_{be_1}, \delta v_{be_2}, \delta v_{be_3}$ and δv_D in (6) with the equivalent expressions of $\delta v_{be_1③}$, $\delta v_{be_2③}$, $\delta v_{be_3③}$ and v_D in (8) respectively, the total cubic distortion in the output signal ($\delta v_{o_③}$) due to the modulation of base-emitter and base-collector voltages is derived. This will be an expression in the form of $\delta v_{o_③} = \alpha_3 \delta v_i^3$.

In order to derive a short form expression for IM_3, we consider a common case where

$$\begin{aligned} R_{EE_3} &= R_{EE_1} = R_{EE} \\ I_{DC_3} &= I_{DC_1} = I_{DC} \\ I_{DC_2} &= kI_{DC} \\ I_{DC_D} &= (k-1)I_{DC} \\ g_{m_3} &= g_{m_1} = g_m \\ g_{m2} &= kg_m. \end{aligned} \tag{9}$$

Therefore, the 3rd-order intermodulation distortion of the circuit is extracted as

$$\begin{aligned} IM_3 = &\frac{V_T V_P^2}{8I_{DC}^3 \left(R_{EE} + \dfrac{1}{g_m}\right)^2 \left(R_L + \dfrac{1}{kg_m}\right)} \\ &\times \left[\frac{(Z_L - R_L)^3}{k^3 \left(Z_L + \dfrac{1}{kg_m}\right)^3} \right. \\ &\left. - \frac{R_L + \dfrac{1}{kg_m}}{R_{EE} + \dfrac{1}{g_m}} - \frac{\left(R_L + \dfrac{1}{kg_m}\right)^3}{(k-1)^3 Z_L \left(Z_L + \dfrac{1}{kg_m}\right)^2} \right]. \end{aligned} \tag{10}$$

Fig. 7 compares the IIP3 extracted from (10) with the one extracted from CAD simulation of the circuit in Fig. 6 which verifies the frequency dependency of distortion due to the hold capacitance. Because *broadband* cancellation of the resulting frequency-dependent distortion is not trivial, the THA is designed

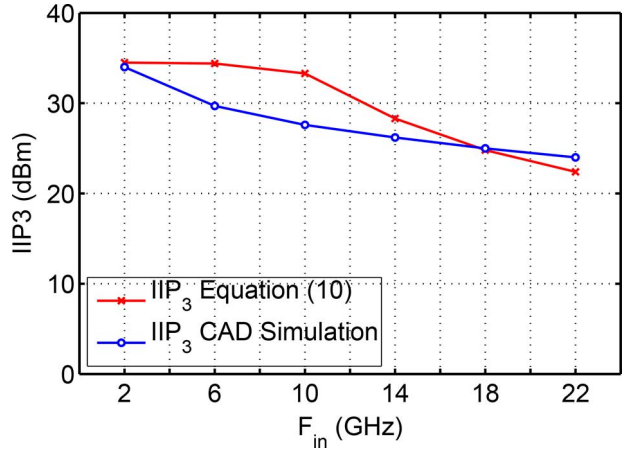


Fig. 7. Comparison of IIP3 extracted from (10) and CAD simulation of the circuit of Fig. 6 Circuit parameters are: $I_{DC_1} = I_{DC_3} = 9$ mA, $I_{DC_2} = 15$ mA, $R_{EE_1} = R_{EE_3} = 95\,\Omega$, $R_L = 85\,\Omega$, $r_D = 28\,\Omega$ and $C_H = 130$ fF.

to minimize only the frequency-independent distortion of the input buffer arising from Q_2, Q_5, Q_3, and Q_6. Equation (10) for the input buffer with no load ($r_D, C_H \to 0$ and $k = 1$) is simplified to

$$IM_3 = \frac{V_T V_P^2 (R_{EE} - R_L)}{8I_{DC}^3 \left(R_{EE} + \dfrac{1}{g_m}\right)^3 \left(R_L + \dfrac{1}{g_m}\right)} \tag{11}$$

which is driven to zero when $R_L = R_{EE}$. Note that in this case the third term inside the bracket in (10) is eliminated as the Taylor series expansion of the diode voltage source in (7) does not exist. The above perturbation method for IM_3 calculation provides insight into the circuit distortion sources and is readily extended to the hand analysis of larger circuits.

Based upon the sampling diode model and a total 130 fF hold capacitance (including 10 fF stray capacitance), circuit parameters are set from the above distortion analysis to $I_{DC_1} = I_{DC_3} = 9$ mA, $I_{DC_2} = 15$ mA, $I_{DC_D} = 6$ mA, $R_{EE1} = R_{EE3} = 95\,\Omega$, and $R_L = 85\,\Omega$.

C. Clock Distribution Circuit

The clock distribution circuit of the SHA shown in Fig. 3 is composed of a single to differential converter followed by two clock networks which provide two sets of 50 GHz clocks with 180° phase shift for the master and slave THAs. As represented in Fig. 8, the network consists of a chain of low and high power CML inverters as the clock buffers/drivers and

$$\begin{cases} \delta v_{be_1③} = \left(\dfrac{V_T}{6I_{DC_1}^3}\right) \left(\dfrac{1}{R_{EE_1} + 1/g_{m_1}}\right)^3 \delta v_i^3 \\ \delta v_{be_2③} = \left(\dfrac{V_T}{6I_{DC_2}^3}\right) \left[\dfrac{1}{R_{EE_1} + 1/g_{m_1}} - \dfrac{1}{Z_L + 1/g_{m_2}} \times \left(\dfrac{1/g_{m_2}}{R_{EE_1} + 1/g_{m_1}} + \dfrac{R_L}{R_{EE_3} + 1/g_{m_3}}\right)\right]^3 \delta v_i^3 \\ \delta v_{be_3③} = \left(\dfrac{V_T}{6I_{DC_3}^3}\right) \left(\dfrac{1}{R_{EE_3} + 1/g_{m_3}}\right)^3 \delta v_i^3 \\ v_{D③} = \left(\dfrac{V_T}{6I_{DC_D}^3}\right) \left[\dfrac{-1}{Z_L + 1/g_{m2}} \times \left(\dfrac{1/g_{m2}}{R_{EE1} + 1/g_{m1}} + \dfrac{R_L}{R_{EE3} + 1/g_{m3}}\right)\right]^3 \end{cases} \tag{8}$$

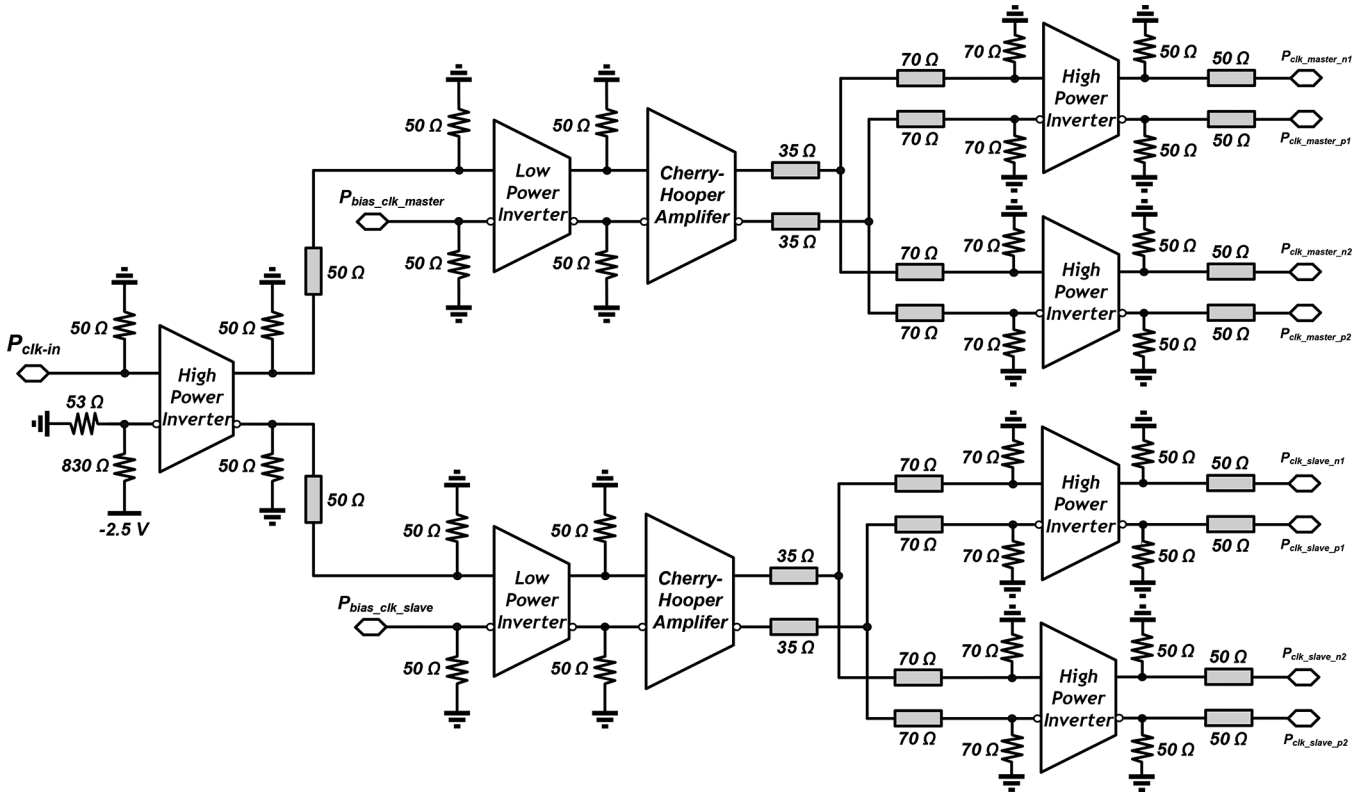


Fig. 8. Block diagram of the clock distribution circuit.

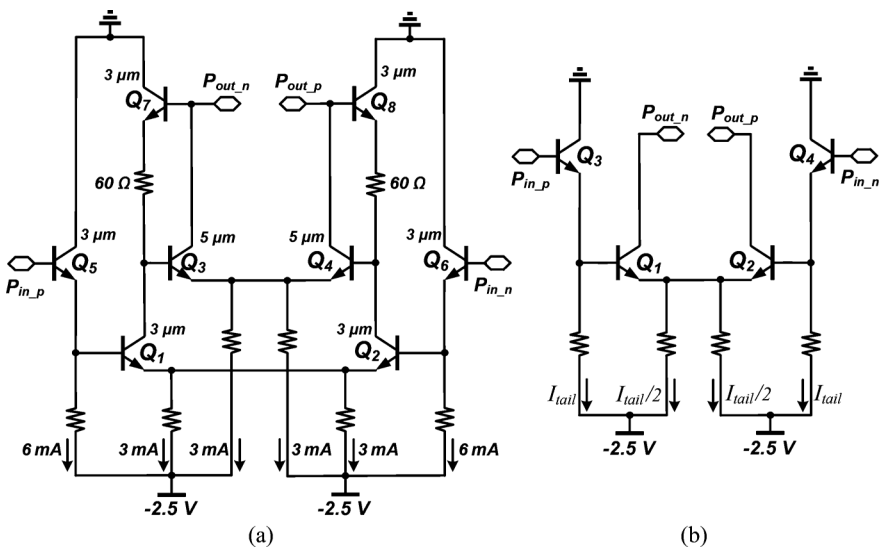


Fig. 9. Schematic of (a) Cherry-Hooper amplifier, and (b) low and high power CML inverters, used in the clock distribution circuit of Fig. 8.

a Cherry-Hooper amplifier in the middle of the chain. Low power CML clock buffers are used for short-distance clock signal transmission while long distance distribution of the signal is achieved using terminated transmission lines between the blocks followed by high power CML drivers. Wide bandwidth is accomplished by using a single-stage Cherry-Hooper amplifier as shown in Fig. 9(a). The measurement results [34] of a test chip of a similar Cherry-Hooper amplifier but having two stages verifies a bandwidth of 100 GHz. Schematics of the low-power and high-power CML inverters are shown in Fig. 9(b) where I_{tail} is 6 mA and 12 mA, respectively. Two control signals ($P_{bias\_clk\_master}$ and $P_{bias\_clk\_slave}$ in Fig. 8) determine the threshold levels for transition from low to high for each master and slave THA clock signal which consequently enable optimizing the duty cycle of track and hold clock signals applied to these THAs.

D. Output Buffer and Driver

Because the InP DHBTs have low DC current gain, turning the THA output buffers partially off during the hold mode can significantly decrease the signal droop [5], [16], [25]. However, by disabling the output buffer, the output signal is not available

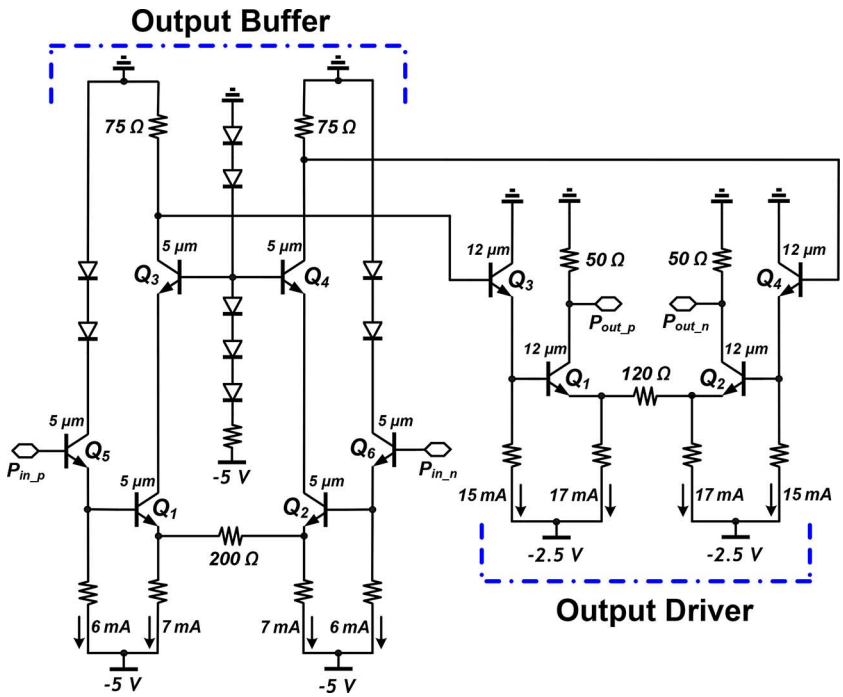


Fig. 10. Schematic of the output buffers and the output driver in the SHA of Fig. 3.

to subsequent stages until the buffer is again turned on. This would complicate the timing design of sampled systems, and in particular would render more difficult interface between an SHA and an ADC. Therefore, the output buffer of THA is designed to be always in the on state and hence its input DC bias current causes signal droop during the hold mode.

To drive long transmission-line interfaces, a 50 Ω output driver is also included in the output of SHA. The schematic of the output buffer preceding the output driver is shown in Fig. 10. Unlike the input buffer, these stages do not use cubic distortion compensation; instead, cubic distortion is kept small by using large emitter bias currents and large emitter degeneration resistances. In simulations, IM_3 arising in the output buffer and driver has smaller magnitude than that generated by the track-hold switch.

E. Fabrication and Layout Techniques

The ICs designed using inverted thin-film microstrip wiring (M_4 ground plane) [35] to permit a continuous ground plane without breaks, maintaining ground integrity and avoiding ground bounce. The characteristics of all IC interconnects were simulated using a 2.5-D CAD tool (Agilent Momentum). In order to have a symmetric layout, the resistor in the emitter of each differential pair has been laid out using two parallel resistors.

The first iteration of THA and SHA ICs whose die photos are shown in Fig. 11, were designed and fabricated in a 250 nm InP DHBT technology with a single-finger base-collector diode as the switch. Then, in order to investigate the effect of switch size and type on the linearity, similar designs were fabricated in 500 nm InP DHBT technology with three different choices of diode switches: (a) a one-finger base-collector diode, (b) a two-finger base collector diode, and (c) a DHBT transistor in a diode-connected configuration. Note that SEF configuration could not be included in this set of designs due to the large value of V_{CE} imposed by the DC level shifting of transistors $Q_{3,6}$ in Fig. 5. Table I shows the list of fabricated THA and SHA ICs in this work.

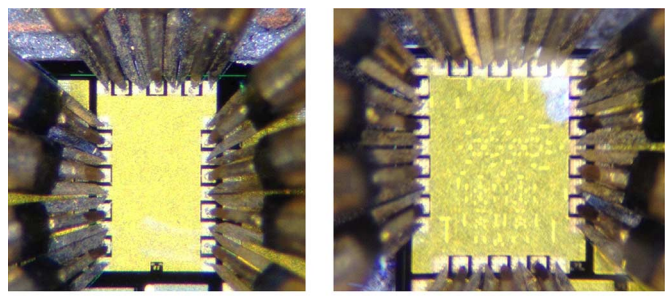


Fig. 11. Die photos of (a) THA_1 (0.675×1.075 mm^2) and (b) SHA_1 (0.875×1.075 mm^2) ICs.

V. Measurement Results

A. DC Bias and Power Consumption

The clock distribution circuit and the output driver block in Fig. 3 are designed to operate with a -2.5 V supply while the remaining blocks operate from a -5 V supply. The THA_1 chip consumes 130 mA and 220 mA from -5 and -2.5 V supplies, respectively (a total power consumption of 1.2 W) while the SHA_1 draws 260 mA and 320 mA from -5 and -2.5 V supplies, respectively (a total power consumption of 2.1 W).

B. S-Parameters

S-parameters (small-signal parameters) of a clocked system such as THA is defined when the system is in a stable mode,

TABLE I
LIST OF FABRICATED THA AND SHA ICS

ICs	Switch Type	Switch Size	Switch resistance*	InP DHBT Process
THA_1, SHA_1	1 finger base-collector diode	$Area_{base} = 6\,\mu m^2$	$28\,\Omega$	250 nm
THA_2, SHA_2	1 finger base-collector diode	$Area_{base} = 6\,\mu m^2$	$28\,\Omega$	500 nm
THA_3, SHA_3	2 finger base-collector diode	$Area_{base} = 12\,\mu m^2$	$14\,\Omega$	500 nm
THA_4, SHA_4	diode-connected transistor	$Area_{emitter} = 0.5 \times 5\,\mu m^2$	$9\,\Omega$	500 nm

* Small-signal AC resistance of the diode at a 6 mA bias current.

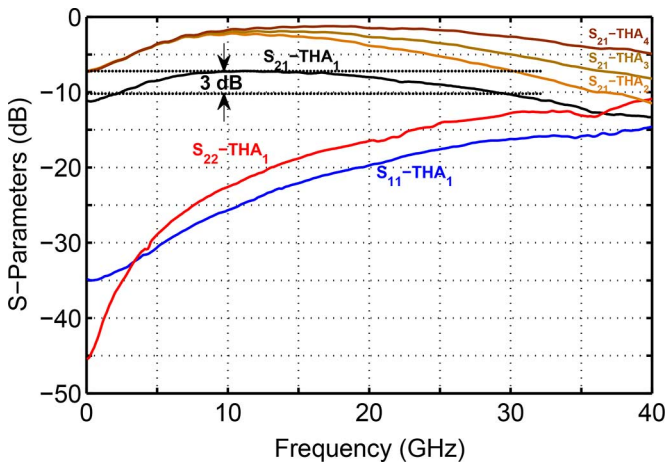


Fig. 12. Measured single-ended S-parameters of the THA ICs in track mode.

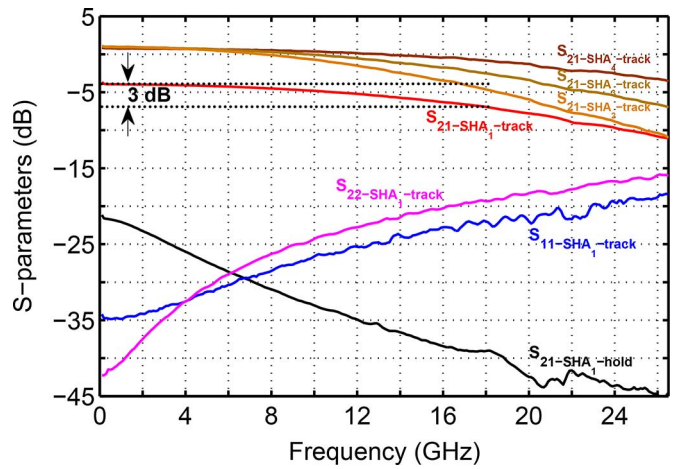


Fig. 13. Measured single-ended S-parameters of the SHA ICs with both master and slave THAs at track mode.

either track or hold mode where the track-hold switch is either conducting or turned off. We have measured the S-parameters of THAs by forcing them to track mode using the control signals of the clock distribution circuit and disconnecting the RF input clock signal. Fig. 12 shows the single-ended measured S-parameters of all THAs. The widest bandwidth is achieved by THA_4, where the switch resistance is the smallest among the designs. The THA_1 has a 3-dB bandwidth of greater than 27 GHz. The input and output return losses are better than 15 dB and 13 dB over the 3-dB bandwidth.

In the case of SHA, as we mentioned earlier, in transient operation where a clock signal is applied to the circuit, two master and slave THAs are in 180° phase shift with respect to each other and at each instant of time, one of them is always in hold mode. However, to perform the S-parameters measurement, we have set the two control signals of clock circuit to a DC level of high which consequently forces both master and slave THAs to track mode. The single-ended measured S-parameters of all SHAs are shown in Fig. 13 where the SHA_1 shows a flat S_{21} gain of -4 dB and a 3-dB bandwidth of 18 GHz. The input and output return losses are better than 15 dB and 19 dB over the 3-dB bandwidth. Note the absence of significant S_{21} gain ripple in the designs. Moreover, the bandwidth variation of S_{21} in Figs. 12 and 13 is due to the variation in the small-signal resistance of the switch used in THA and SHA ICs which are listed in Table I.

C. Linearity Measurements

The measured single-ended input compression point (P1dB) of the THA_1 at 50 GSamples/s is compared to P1dB of the SHA_1 at 30, 40, and 50 GSamples/s sampling rates in Fig. 14 where THA_1 and SHA_1 have P1dB more than $+6$ and $+8$ dBm, respectively over an input frequency range of 2 to 22 GHz.

IIP3 measurements have been performed by separately applying two signals with 100 MHz separation to the circuit input ports, then capturing the fundamental signal powers and their corresponding third-order intermodulation products using a Rohde&Schwarz FSU 20 Hz–46 GHz spectrum analyzer. The extrapolated IIP3 for SHA_1 at sampling rates of 30, 40, and 50 GSamples/s is compared to the IIP3 of SHA_{2-4} at 30 GSamples/s in Fig. 15. The SHA_1 has IIP3 more than $+17$ dBm over the input frequency range of 2 to 22 GHz. Note that the designs using diode-connected transistors show poorer IIP3 than those using base-collector diodes as a result of the large and bias-dependent emitter-base junction capacitance, and of the low reverse breakdown, of the diode-connected transistor.

HD_3 which is the difference between the fundamental signal power and the third harmonic, is measured for a single-ended output at two input power levels: (a) P1dB input compression point corresponding to a large signal excitation and (b) 10 dB below P1dB corresponding to a small-signal excitation. The values are shown in Fig. 16 where the SHA_1 shows HD_3 values

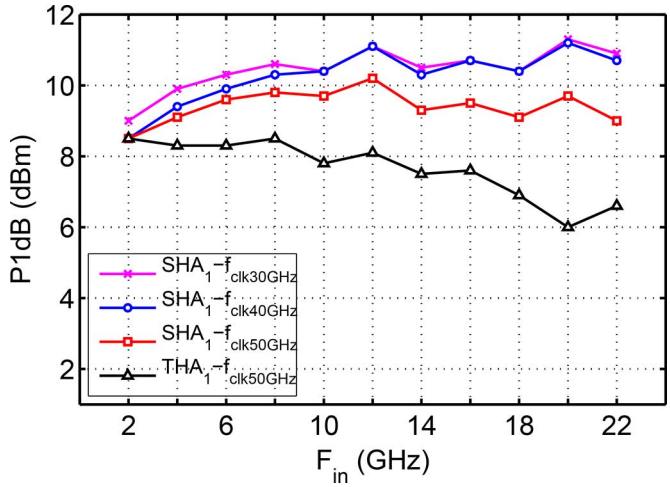


Fig. 14. Measured single-ended 1 dB input compression point (P1dB) of SHA_1 at clock frequencies of 30, 40, and 50 GHz, compared to the measured single-ended P1dB of THA_1 at a clock frequency of 50 GHz.

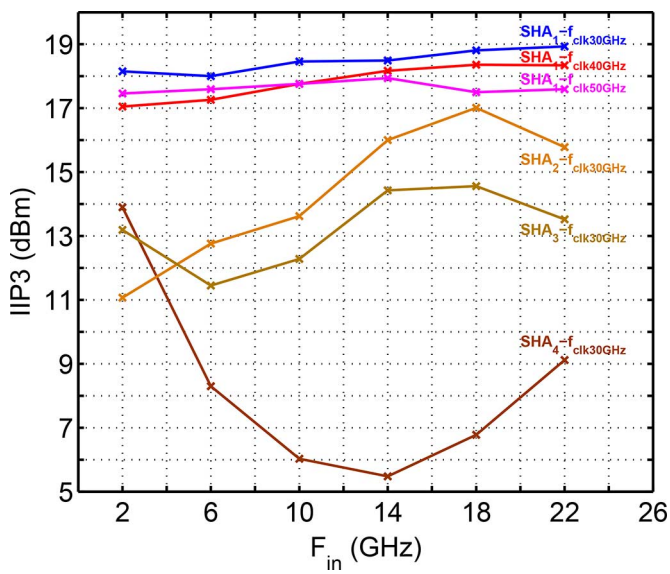


Fig. 15. Measured input-referred third order intercept (IIP3) of SHA_1 at clock frequencies of 30, 40, and 50 GHz, compared to the measured IIP3 of SHA_{2-4} at a clock frequency of 30 GHz.

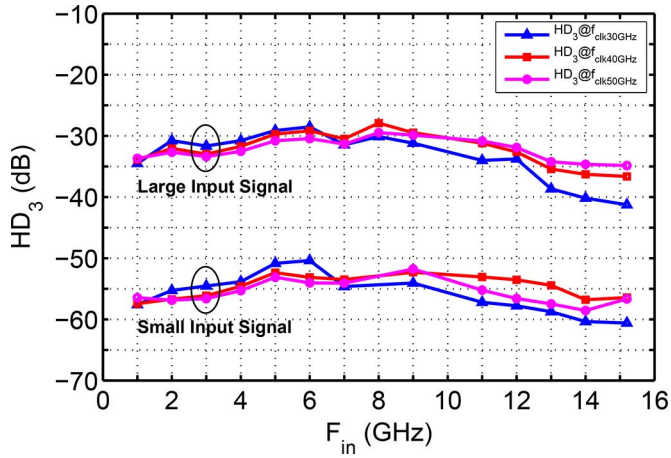


Fig. 16. Measured HD_3 of SHA_1 at input powers corresponding to P1dB (large input signal), and 10 dB below P1dB (small input signal), at clock frequencies of 30, 40, and 50 GHz.

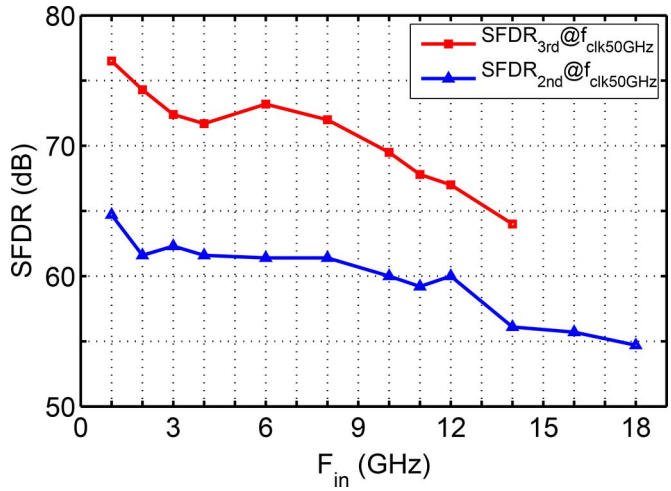


Fig. 17. Measured 2nd and 3rd harmonic SFDR of SHA_1 at a clock frequency of 50 GHz.

below −28 dB for large signal excitation and below −50 dB for small-signal excitation, over the input signal frequency range of 1 to 15.2 GHz for all measured sampling rates.

Based on the definition of SFDR in [5], the $SFDR_{2nd}$ and $SFDR_{3rd}$ are measured as the difference between the fundamental signal power and its corresponding second-order $(SFDR_{2nd})$ or third-order harmonic $(SFDR_{3rd})$, at the input power where the corresponding harmonic power exceeds the noise floor of the amplifier. The integrated noise floor level of SHA_1 is measured approximately −100 dBm. Based on this noise floor level, $SFDR_{2nd}$ and $SFDR_{3rd}$ are measured and shown in Fig. 17 where $SFDR_{2nd}$ is more than 55 dB and $SFDR_{3rd}$ is more than 64 dB over the measured input frequency range at 50 GSamples/s. Therefore, the effective number of bits (ENOB) is estimated as 8 bits based on minimum value of $SFDR_{2nd}$. Note that in the operation of SHA, the output is corresponding to a sampled signal in contrast to the operation of THA where the output is in track in the half clock cycle and not in hold mode. Therefore, analog measurement of SHA constitutes a more representative of a sampling circuit measurement. We, therefore, base our statement of circuit ENOB on SHA measured data.

Beat frequency tests were performed at the P1dB input power level and at an input frequency of 20 GHz which is close to the 3-dB bandwidth of the SHA. Fig. 18 shows the measured single-ended spectral characteristics of the beat frequency test with $f_{in} = f_s + \Delta f$ where $f_s = 20$ GHz and $\Delta f = 2$ MHz. The difference between the fundamental and 2nd harmonic is more than 40 dB. Linearity measurement results of THA_1 have also been reported in [20].

D. Time-Domain Measurement

Time-domain measurements were conducted using Rohde&Schwarz SMF 100 A signal generator for the input signal and Agilent E8257D-M50 50 GHz signal generator for the clock source. Fig. 19 captured by an Agilent 86100A wide-band sampling oscilloscope, shows a differential output

TABLE II
PERFORMANCE COMPARISON OF SAMPLING AMPLIFIERS

	Sample Rate (GS/s)	BW (GHz)	Input Range (V_{pp})	THD@f_{in}/f_s (dBm@GHz/GHz)	IIP3@f_{in}/f_s (dBm@GHz/GHz)	Power (mW)	V_{Supply} (V)	Die-Size (mm^2)	Process
[1]	50	42	0 dBm	–	21@30/50	640	4, 3.3	1.28 × 1.15	SiGe BiCMOS
[5]	40	43	−8 dBm	−29@10/40 −27@19/40	8@6/40 0@19/40	540	3.6	1.0× 1.1	SiGe HBT f_τ=160 GHz
[6]	18	7	1	−32.3@2/18	–	128	3.5	1.58× 1.7	SiGe HBT f_τ=120 GHz
[8]	40	43	−8 dBm	−29@10/40 −27@19/40	6@8/40 2.5@12/40	540	3.6	1.1× 1.0	SiGe BiCMOS f_τ=160 GHz
[11]	40	16	1	−32.4@10/40 −44.2@3/18 −50.5@2/12	15.6@10/40	560	5.5	1.8× 1.0	SiGe HBT f_τ=200 GHz
[12]	30	7	−12 dBm	−30@1/30 −29@13/30 −29@7/30	1@5/30 0@9/30	270	1.8	1.0	0.13 μm CMOS Technology
[13]	20	20	0.5	−38.8@6/20 −38@9/20	16@2/20	1990	−6	1.6× 1.4	InP HBT f_τ=210 GHz
[14]	20	–	0.5	−45@0.9/20 −18@9.9/20	–	735	−5.2	2.0× 2.0	SiGe BiCMOS f_τ=200 GHz
[15]	40	27	0.5	−48@2/40	–	1900	−6	1.4× 1.6	InP HBT f_τ=210 GHz
[17]	50	50	1	−56.3@3/50 −36.5@25/50	–	1850	−6.2	1.5× 1.2	InP DHBT f_τ=320 GHz
[18]	70	51	1	−52@2/60 −37@15/60	22@5/60	–	–	1.5× 1.2	InP DHBT f_τ=320 GHz
[19]	30	–	0.6	−59@1/30 −50.5@31/30	19@1/30	420	5.5	1.1× 0.7	InP BiCMOS f_τ=300 GHz
This work THA_1	50	27	9 dBm	−29.5@15/50	20.7@6/50 17.4@18/50 16.7@22/50	1200	−5, −2.5	0.675× 1.075	250 nm InP DHBT f_τ=370 GHz
This work SHA_1	50	18	9 dBm	−33.6@4/50 −31.6@9/50 −38.5@15.2/50	17.5@6/50 17.5@18/50 17.6@22/50	2100	−5, −2.5	0.875× 1.075	250 nm InP DHBT f_τ=370 GHz

signal with frequency of 10 GHz which is being sampled by 50 GSamples/s sampling rate.

Table II compares the performance of THA_1 and SHA_1 with the state of the art THAs reported in the literature. Note that although the differential operation will partially suppress the even harmonics, the values of THD for THA_1 and SHA_1 ICs in this table are calculated based on single-ended measurement results under large-signal excitation and using only the second and third harmonics since the higher harmonics had much lower amplitudes.

VI. CONCLUSION

THA and SHA ICs were designed and fabricated in a 250 nm InP DHBT technology. A high sampling rate of 50 GSamples/s has been achieved due to using (a) high speed base-collector diodes as the switching element and (b) a wideband clock

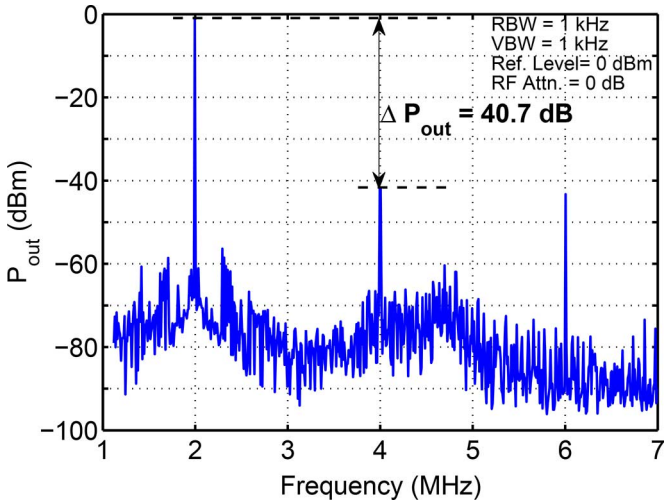


Fig. 18. Beat frequency test of SHA_1, where a 20.002 GHz input signal is sampled at 20 GSamples/s.

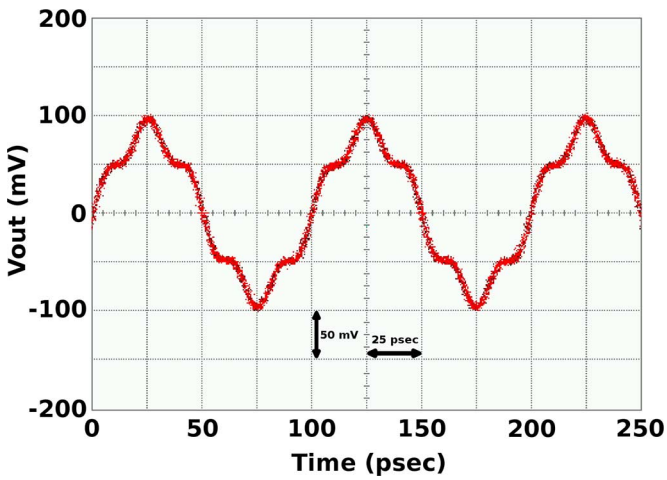


Fig. 19. Measured differential output signal of the SHA_1, where a 10 GHz RF input signal is sampled at 50 GSamples/s.

distribution circuit. A low-distortion input buffer architecture has been used in the design of the amplifiers where the SHA achieves an IIP3 more than 17 dBm for the input frequency range up to 22 GHz, a THD below −28 dB for the input frequency range up to 15 GHz and a SFDR better than 55 dB for the input frequency range up to 18 GHz.

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