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Optimization of direct current performance in terahertz InGaAs/InP double-heterojunction bipolar transistors

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As the dimensions of $In_{0.53}Ga_{0.47}As$/InP double-heterojunction bipolar transistors (DHBTs) scale for terahertz applications, the DC current (β) decreases. To improve the DC performance in such scaled devices, we analyze three modified HBT geometries: a HBT with a surface pulse-doped layer in the base, a HBT having this pulse-doped layer under the emitter junction and under the base contact, but with it removed by etching in the region between the base and emitter contacts, and a device, necessarily fabricated by regrowth, in which the pulsed doped layer is present under only the base contacts. Based on a drift-diffusion/recombination model, carrier transport in the DHBT base is simulated and the corresponding β is computed using TCAD software. The structures with a pulse doped layer can attain $\beta = 31 \sim 39$ at 100 nm emitter width. The structures with a trench between the base contact and emitter show $\beta = 39 \sim 54$ at 100 nm emitter width. Finally, the structure with recessed base-emitter junction and regrown emitter demonstrate $\beta = 62$–119 at 100 nm emitter width. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4899197]

I. INTRODUCTION

NPN-DHBTs based on the $In_{0.53}Ga_{0.47}As$/InP materials systems have wide RF bandwidth and high breakdown voltages and are suitable for application in mixed-signal ICs, high speed digital logic, millimeter-wave communications, and imaging and sensing at far-infrared wavelengths.[1] State of the art DHBTs simultaneously demonstrating record current gain/power gain cutoff frequencies (f_τ/f_{max}) of ~0.5/1.1 THz and common emitter breakdown voltage (BV_{CEO}) of 3.5 V have been reported by Urteaga *et al.*[2] The high cutoff frequencies of these devices is the result of scaling to reduce carrier transit times and parasitic *RC* delays, which have been achieved by small epitaxial and lateral dimensions as well as high doping concentrations at the Ohmic contacts.[1] However, when the device is scaled, the DC current gain ($\beta = I_C/I_B$) decreases.[3,4] As shown in Fig. 1, experimental devices with base-emitter junction widths (W_E) of 200 and 75 nm exhibit β of approximately 20 and 8, respectively. Low β increases noise in HBT RF amplifiers and reduces DC gain and precision in analog ICs. Therefore, mitigating the reduction of β with scaling is important in the design of future scaling generations of terahertz (THz) HBTs.

To increase β, the base current must be reduced. In HBTs, the base current (I_B) consists of bulk ($I_{B,Bulk}$) and edge ($I_{B,Edge}$) components. $I_{B,Bulk}$ arises from recombination mechanisms in the bulk base semiconductor and is dominated in THz HBTs by Auger recombination due to the high doping concentration.[3] In THz HBTs, $I_{B,Bulk}$ is proportional to the emitter current and hence at a fixed current density scales in proportion to the base-emitter junction area, $A_{je} = W_E L_E$, where L_E is the length of the emitter stripe. $I_{B,Edge}$ originates from surface recombination and from lateral diffusion of the injected electrons to the base contact via the bulk base region and through the surface depletion layer of the base semiconductor induced by surface defect states.[3–5] Since this current emanates from the edge of the base-emitter junction, it scales in proportional to the junction periphery, $P_{je} = 2(W_E + L_E)$. The DC current gain in HBTs can be written as

$$\frac{1}{\beta} = \frac{I_{B,Bulk} + I_{B,Edge}}{I_C} = \frac{1}{\beta_{Bulk}} + \frac{P_{je} K_{B,Edge}}{A_{je} J_C} \approx \frac{1}{\beta_{Bulk}} + \frac{2K_{B,Edge}}{W_E J_C}, \quad (1)$$

where $K_{B,Edge}$ is the edge sheet current density and J_C is the collector current density. The approximation in equations holds if $L_E \gg W_E$.

Current gain in THz DHBTs is small. β of a DHBT with a very wide emitter, i.e., negligible $I_{B,Edge}$, is the ratio of the electron lifetime to the base transit time, i.e., $\beta_{Bulk} = \tau_n/\tau_B$. If the base doping concentration is increased, the Auger recombination lifetime decreases, and hence τ_n and β_{Bulk} decrease.[3,6] In a DHBT with a narrow emitter, β is also limited by the edge current, and β decreases as W_E reduces.[3,4]

We have previously modelled DC current gain using a commercial transport simulator.[3,4] From this model, β can be estimated for various HBT structural designs. In this paper, three DHBT geometries are designed for improved DC current gain.

II. SIMULATION PARAMETERS AND STRUCTURES

A cross-section of a typical experimental DHBT is shown in Fig. 2. Under bias, electrons are injected from the emitter into the base. Beneath the base-emitter junction, most injected electrons traverse to the collector and become collector current. A portion of the electrons recombine with holes, generating $I_{B,Bulk}$. At the vicinity of emitter edge, a fraction of injected electrons diffuse through the bulk base

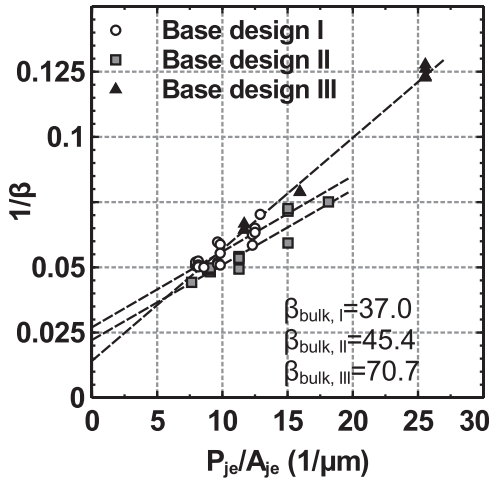

FIG. 1. Inverse DC current gain ($1/\beta$) vs. HBT emitter periphery to area ratio ($P_{je}/A_{je} \approx 2/W_E$) of experimental DHBTs with distance between base and emitter contacts (W_{gap}) ≈ 10 nm and different base designs measured at emitter current density $J_E \approx 25\,mA/\mu m^2$. Design I has a 25 nm thick base with doping varying from $9 \times 10^{19}\,cm^{-3}$ at the emitter side to $5 \times 10^{19}\,cm^{-3}$ at the collector side. Design II has a 20 nm thick base with doping varying from $1.2 \times 10^{20}\,cm^{-3}$ at the emitter side to $8 \times 10^{19}\,cm^{-3}$ at the collector side.[3] Design III has an 18 nm thick base with doping varying from $1.2 \times 10^{20}\,cm^{-3}$ at the emitter side to $8 \times 10^{19}\,cm^{-3}$ at the collector side.

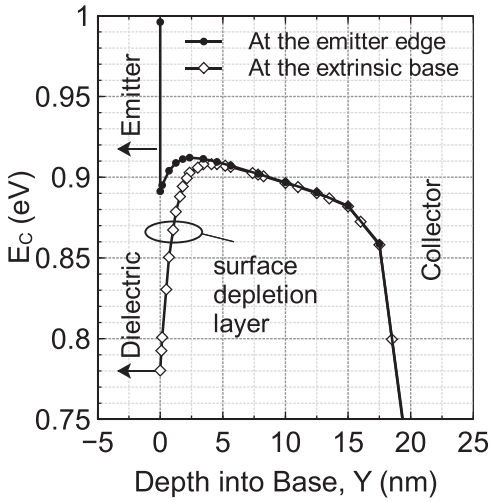

FIG. 3. Simulated conduction band energy (E_C) at $V_{BE} \approx 1.2$ V vs. depth into the base semiconductor at the edge of the emitter and in the extrinsic base. The simulation assumes a 20 nm thick base with doping varying from $1.2 \times 10^{20}\,cm^{-3}$ at the emitter side to $8 \times 10^{19}\,cm^{-3}$ at the collector side.[4] The energy is relative to the base Fermi level.

region towards the base contact. They then recombine at the contact, which leads to base current (bulk lateral diffusion). In our simulations of experimental devices,[3,4] for HBTs with a 20 nm-thick base and 10 nm base-emitter distance (W_{gap}), this current contributes approximately 30% of the edge current. For devices with a 100 nm-wide emitter, at an emitter current density $J_E \approx 25\,mA/\mu m^2$, the edge sheet current density $K_{B,Edge}$ (Ref. 3) due to lateral diffusion in the bulk is $\sim 20\,\mu A/\mu m$.

At the InGaAs/dielectric interface within the space between the base and the emitter contacts (the extrinsic base), the surface Fermi level is pinned by interface trap states, resulting in a surface depletion layer and producing the conduction-band profile shown in Fig. 3. In the base, some fraction of the injected electrons will diffuse towards this depletion layer, where they will then be trapped by the high field. The trapped electrons then diffuse laterally towards the base contact. The trapped electrons either

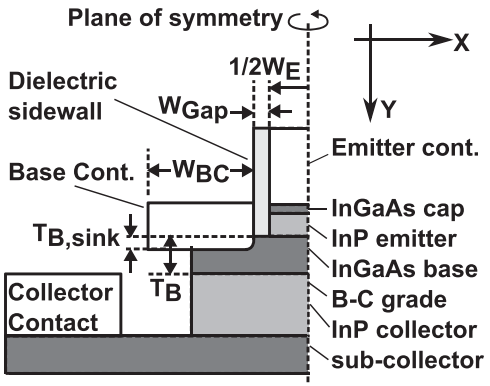

FIG. 2. A schematic cross-section (normal to the emitter stripe) of an experimental DHBT. The device is symmetric about the indicated line; hence only half the structure is shown.

recombine *en route* with interface trap states (surface recombination) or recombine after reaching the contact (surface conduction).[5] The current due to surface recombination is proportional to the surface recombination velocity (SRV), $v_{surf.Rec.}$, and the area of the extrinsic base, $2 \times W_{gap}L_E$. In scaled HBTs,[11] W_{gap} is less than 15 nm, from TEM analysis. For an InGaAs surface terminated by native oxide, $v_{surf.Rec.}$ ranges from 10^3 to 10^4 cm/s depending upon the surface trap density.[7] The resulting surface recombination current density is less than $1\,\mu A/\mu m$, which is negligible in comparison to other components of $I_{B,Edge}$. The remainder of the edge current is primarily due to surface conduction. For HBTs with a 20 nm-thick base, a 100 nm-wide emitter, and $W_{gap} = 10$ nm, the surface conduction current density is $\sim 50\ \mu A/\mu m$ at $J_E \approx 25\,mA/\mu m^2$.

The electron concentration in the surface inversion layer depends on the density of interface traps (D_{it}). With higher D_{it}, more electrons accumulate at the interface, increasing surface conduction. D_{it} on the extrinsic base is directly affected by the surface preparation prior to dielectric deposition. There is variation among HBT samples, which renders the evaluation of D_{it} challenging. Since the intent of this study is to improve β by modifying the HBT geometry, D_{it} in this work is assumed to be $5 \times 10^{13}\,cm^{-2}\ eV^{-1}$, as obtained from the model fitted to results from experimental devices with a 20 nm thick base.[4] Precise setup and details of the physical models incorporated in the simulations have been reported in Refs. 3 and 4. Key parameters used in this work are listed in Table I.

Because of its complex structure, numerical solution to the coupled continuity, drift-diffusion, and Poisson's equations at the full HBT is computationally demanding. However, the simulation seeks only to determine DC current gain. The base layer of experimental DHBTs has a setback layer composed of lightly doped n-type InGaAs below it. At current densities below the Kirk effect limit (J_{Kirk}), at which the base push-out occurs,[1] the transport boundary condition

TABLE I. Auger coefficient (C_{Auger}), SRV ($v_{surf.Rec}$), and interface trap density ($D_{it.}$) for $In_{0.53}Ga_{0.47}As$ used in the simulations and their corresponding references. We assume a Gaussian energy distribution centered at 0.2 eV below the conduction band with a variance of 0.1 eV.

	Carrier type		
Parameter	Electrons	Holes	Unit
C_{Auger} (Refs. 8–10)	2.5×10^{-29}	2.5×10^{-29}	cm^6/s
$v_{surf.Rec}$ (Ref. 7)	1.0×10^4	1.0×10^4	cm/s
$D_{it.}$ (Ref. 4)	5×10^{13}		$cm^{-2}eV^{-1}$

at the base-collector junction depends solely on the field in the setback layer, and the InP collector design has no effect on β. Therefore, single-heterojunction bipolar transistors (SHBTs), identical to double-HBTs (DHBTs) except without the InP collector and superlattice grade, were simulated. β was computed using Synopsis® Sentaurus, whereby the coupled equations were self-consistently solved.

The simulated SHBT structures have W_E varying from 75 to 250 nm and have W_{gap} of 10 nm. Starting from the emitter side, the base is composed of a thin layer of extremely heavily doped p-type $In_{0.53}Ga_{0.47}As$ (pulse doped layer), followed by a layer of doping-graded p-type $In_{0.53}Ga_{0.47}As$. Because the base contact resistivity varies exponentially with doping concentration,[12] a surface pulse doping layer serves as a contact layer to reduce the base specific contact resistivity[1] and hence increase f_{max}. The increased doping concentrations in the pulse-doped layer, compared to the doping-graded layer, induces an abrupt conduction band offset, as shown in Fig. 4. This band offset, and its associated retarding field, opposes the diffusion of electrons towards the base top surface. This partially suppresses both surface conduction and bulk lateral diffusion towards the base contacts, and hence increases β. For the graded base, two designs, which generate similar magnitudes of quasi-electric field, were studied. The layer structures are listed in Table II. For the HBT geometries, a conventional HBT structure and two new designs were examined.

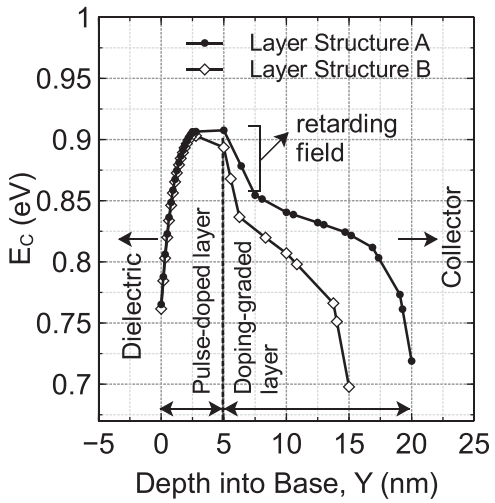

FIG. 4. Simulated conduction band energy (E_C) at $V_{BE} \approx 1.2$ V vs. depth into the base semiconductor in the extrinsic base. The simulation assumes both layer structures listed in Table II. The energy is relative to the base Fermi level.

The first structure studied was a conventional mesa DHBT. Fig. 5(a) shows the cross-section of the simulated SHBT which emulates DHBTs fabricated using the process flow of Jain *et al.*[11] The base contact is formed immediately after the emitter semiconductor wet etch. Dielectric is then deposited by atomic layer deposition (ALD) to protect the InGaAs base top surface from subsequent process damage. Unlike Ref. 11, a pulse-doped base design, as listed in Table II, is assumed.

The second structure used a trenched extrinsic base to increase β. Lateral diffusion of carriers can be suppressed if the distance between the base contact and the emitter (W_{gap}) is increased.[3] However, this also increases the base resistance[1] and decreases f_{max}. If the p+ pulse-doping layer in the space between the base contacts and the emitter (W_{gap}) is removed by a digital surface etch,[13] the electrons carried in the bulk region in this gap will encounter an opposing field as they pass vertically from the graded InGaAs base, through the pulse-doping layer, and into the base contact. This will reduce the diffusion current reaching the base contact. The cross-section of this design is shown in Fig. 5(b), where the pulse doping layer in the extrinsic base is removed prior to ALD dielectric deposition. The depth of the etch can be modulated precisely by the number of self-limiting oxidation/wet etch cycles.[13]

A third design assumes a recessed base-emitter junction, necessarily formed by a junction regrowth technique.[14–16] In THz HBTs, high base doping is required for low contact resistivity[12] and for low sheet resistance in the base-emitter gap and under the emitter.[1] In particular, base doping $> 10^{20}\,cm^{-3}$ is necessary for $<1\ \Omega{\cdot}\mu m^2$ contact resistivity,[12] but such high doping, if present over the full base thickness in the base directly under the emitter, would result in high Auger recombination.[3] This design trade-off can be avoided by using a recessed base-emitter junction (Fig. 5(c)), wherein the p+ pulse layer is present beneath the base contacts but not under the emitter. This structure requires either emitter[14,16] or base regrowth.[15] For emitter regrowth, starting with epitaxial layers without the emitter semiconductor, the p+ pulse-doped layer in the active base region would be first

TABLE II. Two sets of the SHBT layer structures simulated.

Layer	Material	Thickness (Å)	Doping (cm^{-3})
Layer structure A: 46 meV, 15 nm grade			
Emitter	InP	150	5×10^{19}:n
Emitter	InP	150	2×10^{18}:n
Pulse-doping	$In_{0.53}Ga_{0.47}As$	50	1.2×10^{20}:p
Graded base	$In_{0.53}Ga_{0.47}As$	150	$7–4 \times 10^{19}$:p
Collector	$In_{0.53}Ga_{0.47}As$	200	5×10^{16}:n
Sub-collector	$In_{0.53}Ga_{0.47}As$	200	2×10^{19}:n
Layer structure B: 35 meV, 10 nm grade			
Emitter	InP	150	5×10^{19}:n
Emitter	InP	150	2×10^{18}:n
Pulse-doping	$In_{0.53}Ga_{0.47}As$	50	1.2×10^{20}:p
Graded base	$In_{0.53}Ga_{0.47}As$	100	$5–3 \times 10^{19}$:p
Collector	$In_{0.53}Ga_{0.47}As$	200	5×10^{16}:n
Sub-collector	$In_{0.53}Ga_{0.47}As$	200	2×10^{19}:n

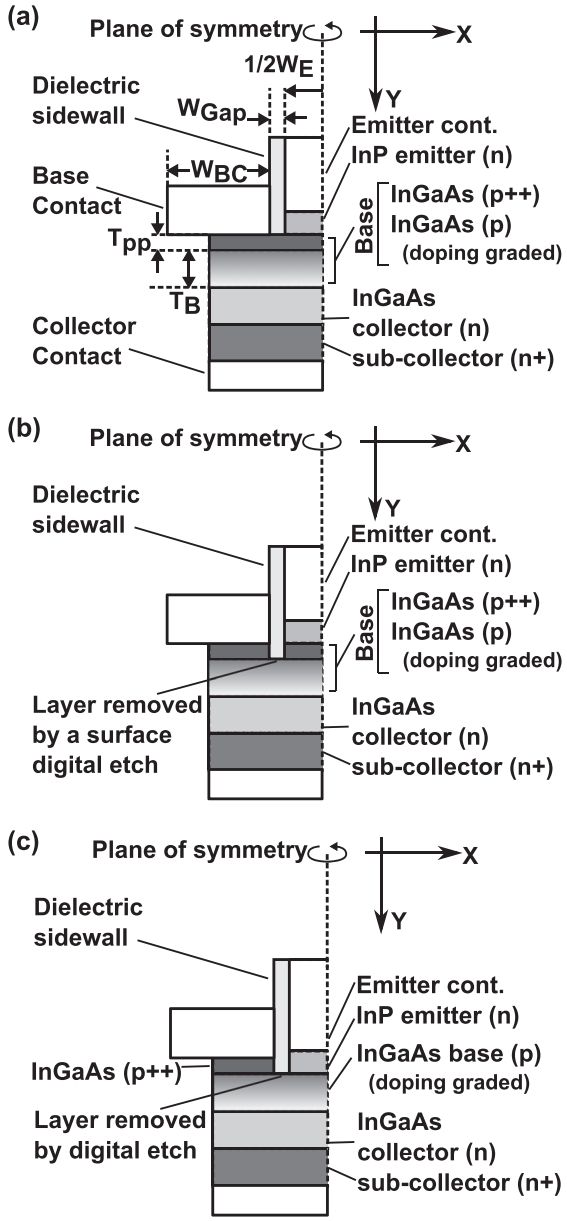

FIG. 5. Schematic cross sections (normal to the emitter stripe) of different HBT geometries: (a) conventional design, (b) trenched extrinsic base, and (c) recessed base-emitter junction. The device is symmetric about the indicated line; hence only half the structures is shown.

removed by a digital etch, and the emitter semiconductor is then regrown by either metalorganic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE)[14,16] within this region.

III. RESULT AND DISCUSSION

We first consider the conventional structure. Fig. 6 shows $1/\beta$ as a function of $1/W_E$, computed for the three HBT geometries and two base designs at $J_C \approx 25\,\text{mA}/\mu\text{m}^2$. The current gains of HBTs with very wide emitters, i.e., when the effect of edge current is insignificant, are extrapolated from the reciprocals of the y-axis intercepts, and are listed as β_{Bulk}, the bulk DC current gain. The slope of the curves is $2K_{\text{B,Edge}}/J_C$, from which the edge sheet current density ($K_{\text{B,Edge}}$) is extracted.

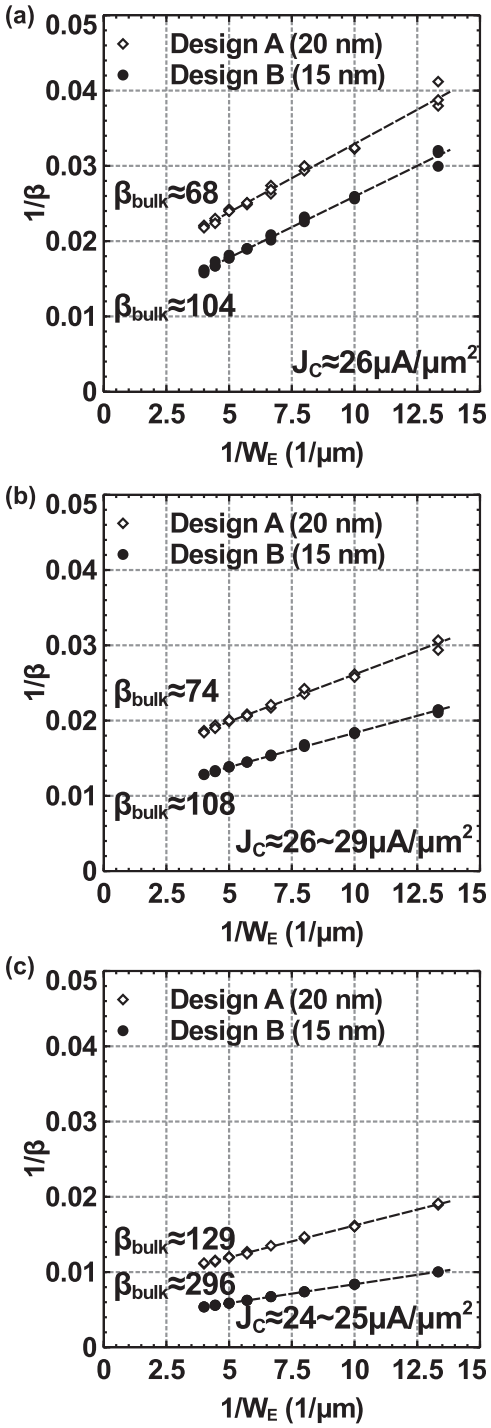

FIG. 6. Inverse DC current gain ($1/\beta$) vs. inverse emitter width ($1/W_E$) for 10 nm and 15 nm base design and different HBT geometries: (a) conventional design, (b) trenched extrinsic base, and (c) recessed Base-emitter junction. Current gain was simulated for base contact widths of $1.2W_E$, $1.4W_E$, and $1.6W_E$.

The inverse current gain vs. inverse emitter width for the conventional designs is shown in Fig. 6(a). For layer structure A, which employs a 15 nm base grade, β_{Bulk} and $K_{\text{B,Edge}}$ are 68 and 23.6 μA/μm, respectively. Devices with 100 nm W_E exhibit β of 31. This implies that approximately 28% of the base current is due to the edge current at this W_E. If the base grade is thinned to 10 nm (i.e., layer structure B), β_{Bulk} increases to 104 and $K_{\text{B,Edge}}$ decreases to 21.2 μA/μm.

At $W_E = 100$ nm, $\beta \approx 39$ and ~32% of the base current originates from the edge. The edge current from both designs[3] is comparable to experimental values (20 μA/μm) in the devices without pulse doping. This implies that the opposing field (barrier) induced between the base pulse doping and the base graded layer does not adequately suppress the lateral diffusion current.

Fig. 6(b) shows $1/\beta$ vs. $1/W_E$ for HBTs with the pulse-doped (p++) layer removed from the extrinsic base region, i.e., the trench-etched design. β_{Bulk} in this geometry is similar to the values composed for the conventional design, since their active base regions are identical. With the extended effective W_{gap} and with the barrier to the electrons in the bulk region, lateral diffusion is suppressed, causing $K_{B,Edge}$ for both layer structure A and B to drop to 18.2 and 11.8 μA/μm, respectively. The corresponding β at 100 nm W_E has been increased to 39 and 54, for layer structures A and B. The edge current contributes approximately 25% of the base current in both layer structures.

The trenched structure thus shows its potential to improve β. The trench etch process using a digital etch appears to be compatible with current HBT fabrication process,[11] and the trench depth can be well controlled.[13,17] However, there are two disadvantages to this structure. The sheet resistance of the base increases in the region where the pulse-doped layer is removed. This increases the base access resistance (R_{bb}) and somewhat decreases f_{max}. Furthermore, since β_{Bulk} remains that of the conventional design, the improvement in β is still ultimately limited by Auger recombination. If these HBTs are to be scaled to $W_E = 50$ nm, β will decrease to 25–40 because a larger ratio of edge current to emitter current.

We now consider the recessed base-emitter junction. In this structure, it is possible to reduce both the edge current and the Auger recombination, by reducing the doping concentration in the active base region, increasing β_{Bulk}, while increasing the doping concentration under the base contacts, reducing the contact resistance. Simulated results for this geometry are plotted in Fig. 6(c). In the absence of the pulse-doped layer, the active base region is thin and lightly doped. Thus, the Auger recombination rate decreases, and β_{Bulk} is greatly increased to 129 and 296 for layer structures A and B, respectively. Furthermore, lateral diffusion of electrons is reduced by the retarding field at the interface to the pulse-doped layer, and hence edge currents are further suppressed. $K_{B,Edge}$ is 10.6 and 6.3 μA/μm for layer structures A and B, respectively. The corresponding β at 100 nm W_E increases to 62 and 119 in the structures, as a result of high β_{Bulk} and low $K_{B,Edge}$.

Among the three HBT geometries, the design with the recessed base-emitter junction demonstrates the best DC performance. To simultaneously achieve $\beta > 50$ and low base access resistance in HBTs with sub-100 nm emitter width, the recessed structure is desirable. A process flow involving both a digital etch of the p+ pulse-doped layer and emitter regrowths must be developed and integrated into the present HBT process flow in order to fabricate this structure. Fig. 7 shows a possible process flow which could be integrated.[18] Such a process would extend upon the work of Refs. 14–16.

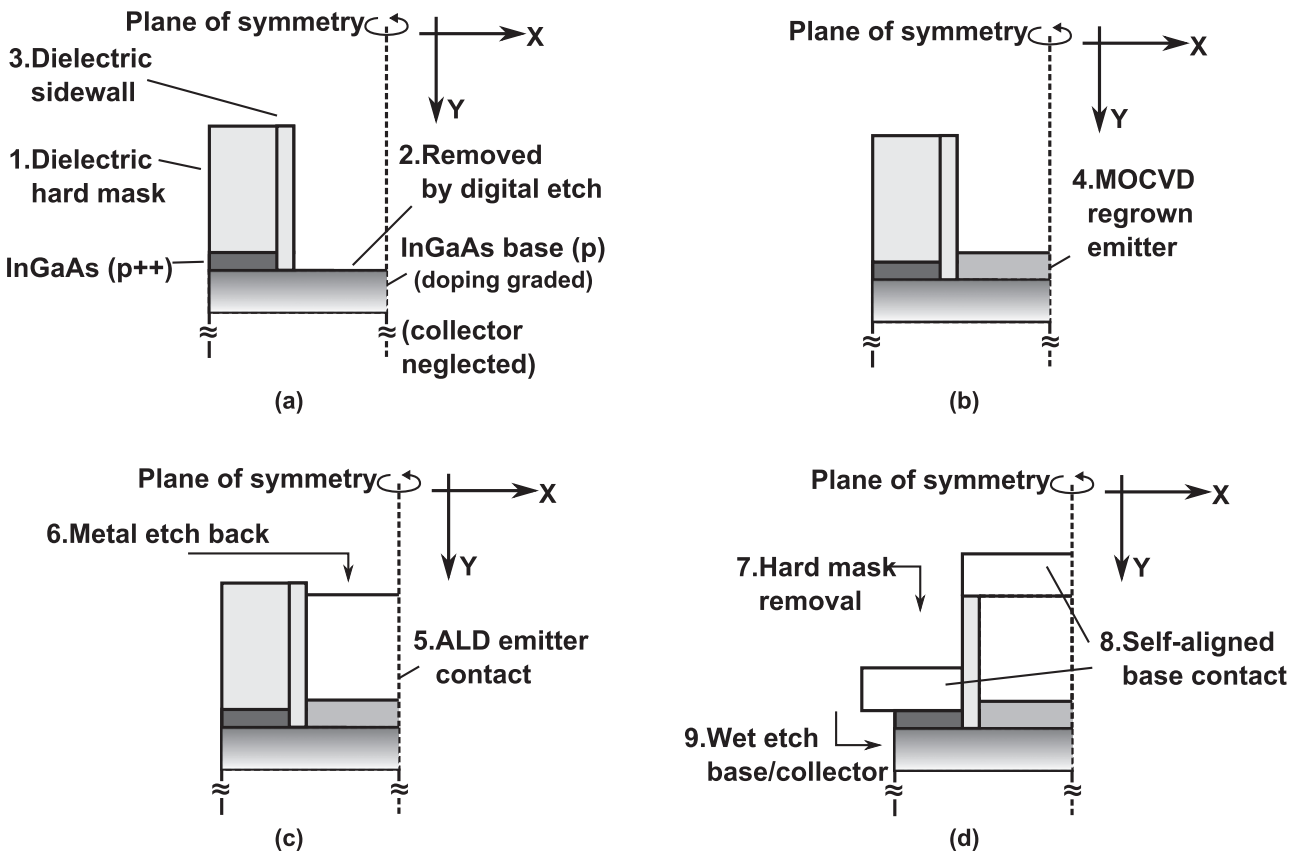

FIG. 7. A process flow for the recessed base-emitter junction.

Recombination due to the defects at the regrowth interface is a significant concern.

The above analysis focuses on the effect of HBT geometry. Base current due to surface conduction can also be reduced if fewer electrons accumulate at the InGaAs/dielectric interface. With adequate surface pretreatment prior to ALD dielectric passivation, D_{it} at the InGaAs/dielectric interface can be reduced.[19] This would weaken surface depletion, reduce surface conduction, and increase β.

IV. CONCLUSION

We have proposed three HBT geometries for increased current gain. The corresponding β was computed using TCAD simulation. A conventional structure with surface pulse-doped layer in the base does not significantly suppress edge current. A structure with a trenched extrinsic base should be relatively easy to incorporate into DHBT fabrication, but provides only a small suppression in edge current. A structure with a recessed base-emitter junction, though requiring a complex process flow, enables a lightly doped active base region and a retarding field suppressing electron diffusion to the base contacts, and thus exhibits the greatest improvement in β. If such structure can be fabricated by regrowth with adequately low defect density, $\beta > 50$ will be feasible in future scaling generations of DHBTs with sub-100 nm emitter width.

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