# Low Power III-V InGaAs MOSFETs Featuring InP Recessed Source/Drain Spacers with $I_{on}$=120 µA/µm at $I_{off}$=1 nA/µm and $V_{DS}$=0.5 V

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## Abstract

We report InGaAs-channel MOSFETs using recessed InP spacer layers in the regrown source and drain. By replacing narrow band-gap InGaAs with wide band-gap InP within the high-field region near the drain end of the channel, band-to-band tunneling (BTBT) leakage is significantly reduced. A 30 nm gate length device using InP spacers shows a minimum $I_{off}$~60 pA/µm, approximately 100:1 smaller than a similar device using InGaAs source/drain spacers. A FET using InP spacers, with 45 nm gate length, and with a 3 nm $ZrO_2$ gate oxide shows $I_{on}$=150 µA/µm at $I_{off}$=1 nA/µm and $V_{DS}$=0.5 V. The low off-state leakage current observed with InP source/drain spacers makes InGaAs MOS technology viable for low-power logic.

## Introduction

Planar ultra-thin-channel InAs III-V MOSFETs have recently shown performance (0.5 mA/µm $I_{off}$ at $V_{DS}$=0.5 V) comparable to Si 22 nm FinFETs for ITRS high performance (HP) applications [1] where the off-state leakage current $I_{off}$ is set at 100 nA/µm. Though In(Ga)As MOSFETs have high on-state transconductance ($g_m$), the small band-gap of the In(Ga)As channel gives rise to high $I_{off}$ at short gate lengths ($L_g$) through band-to-band tunneling (BTBT) [2], rendering prior reported III-V MOSFETs unsuitable for low-power (LP; $I_{off}$=30 pA/µm) and standard-performance (SP; $I_{off}$=1 nA/µm) applications [1-10]. Recently, we reported that either InP channel cap layers or recessed InP source/drain (S/D) spacers can further reduce $I_{off}$ because InP ($E_g$~1.35 eV) is less prone to BTBT [11]. Similarly, Mo *et al.* reported reduced leakage current using an asymmetric InP drain electrode [12]. In [11], placing InP in the regions of highest electric field reduced $I_{off}$ to 1 nA/µm, but thick InP spacers also increased the parasitic source/drain resistance and degraded $I_{on}$. Here we report low-leakage InGaAs MOSFETs with gate lengths as small as 22~30 nm. Thinning the InGaAs channel from 4.5 nm to 3 nm allows low $I_{off}$ (1 nA/µm at $V_{DS}$=0.5 V), but degrades the transconductance and $I_{on}$. Using instead a 4.5 nm InGaAs channel with a partially recessed, doping-graded InP spacer, the minimum $I_{off}$ can be reduced to 60 pA/µm at 30 nm $L_g$. With a recessed InP spacer and thin oxide, a high 150 µA/µm on-state current $I_{on}$ at $I_{off}$=1 nA/µm can be obtained for 45 nm-$L_g$ devices. This high on-off ratio ($1.5 \cdot 10^5$) in a short $L_g$ device demonstrates the potential for III-V MOSFETs in low-power logic.

**Fig. 1** shows a progression of III-V MOSFETs designs for reduced $I_{off}$. P-doped InAlAs or wider-bandgap AlAsSb back barriers reduce back barrier leakage currents [13]. Particularly for InAs, with its small band gap, BTBT leakage arises primarily in the high field region, either at the drain end of the channel next to the gate edge or at the junction between the channel and the regrown heavily-doped drain [14]. Thinning the channel increases the quantized band-gap, reducing BTBT, and improves electrostatics, improving the subthreshold swing (S.S.). Drain vertical field spacers reduce the gate-drain field, reducing BTBT, and also improve electrostatics [1]. Unfortunately, in thin channels, electron mobility is decreased and electron effective mass increased. Here, we show that using an InP recessed spacer provides an alternative means to reduce the $I_{off}$ leakage floor without extreme thinning of the channel.

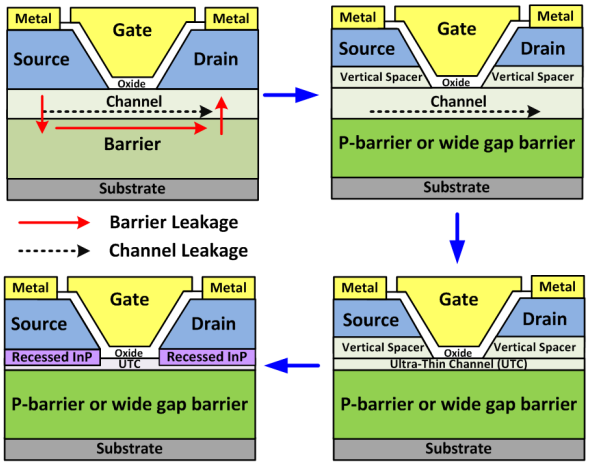
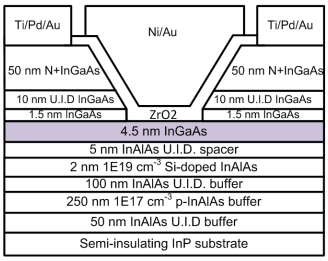



**Fig. 1: Progression of III-V MOSFET designs for reduced off-state leakage current.**

## Device Fabrication

Epitaxial layers were first grown with 6 nm InGaAs channels and P-doped InAlAs barriers (**Fig. 2**). To form dummy gates, 30 nm hydrogen silsesquioxane (HSQ) was spun and patterned by e-beam lithography. The vertical spacer and N+ source/drain contact layers, either InGaAs or InP, were selectively regrown by MOCVD. Device mesas were isolated and the dummy gates removed in buffered oxide etch. For all samples, in the gate region, the channel surface was removed (2 cycles for Sample B; 1 cycle for the others) by digital etching to remove damage and adjust the channel thickness [15]. Sample A is the control sample, with a 4.5 nm thick channel, and was reported in [11]. Sample B has a 3 nm thick channel and an InGaAs spacer, while the other samples (sample C, D, and E) have a 4.5 nm thick InGaAs channel with an InP source/drain spacer recessed ~1.5 nm into the channel. The samples were then immediately transferred into

- MBE growth: 6 nm InGaAs channel
- HSQ dummy gate patterning
- MOCVD S/D regrowth
  - 10 nm UID InGaAs spacer
  - 50 nm N+ InGaAs contact layer
- Isolation and dummy gate removal
- Digital etch
  - Sample A: 1 cycle (4.5 nm InGaAs)
  - Sample B: 2 cycle (3 nm InGaAs)
- High-k dielectric: 30Å $ZrO_2$
- Gate metal liftoff process
  - Ni/Au thermal evaporation
- S/D metal liftoff process
  - Ti/Pd/Au E-beam evaporation




| Sample | A | B |
|---|---|---|
| Channel (nm) | 4.5 | 3 |
| InGaAs spacer (nm) | 11.5 | 13 |

**Fig. 2: Gate-last process flow and device structures of samples A and B.**

the ALD reactor, and pre-cleaned and passivated by cycles of $N_2$ plasma and TMA [16]. $ZrO_2$ gate dielectric was then deposited (38 Å for sample E, 30±1 Å for all others). The samples were then annealed at 400 °C in forming gas for 15 minutes. Ni/Au was thermally deposited as the gate electrode, and Ti/Pd/Au source/drain contacts were deposited.

## Results and Discussion

**Figs. 3** and **4** show the transfer and output characteristics of samples A and B. Thinning the channel from 4.5 nm to 3 nm reduces the minimum $I_{off}$ to 3.5 nA/μm but degrades $I_{on}$ and the transconductance. **Fig. 5** compares the gate $I_G$ and drain $I_D$ leakage for sample B over a larger bias range; the minimum off-state leakage is still dominated by BTBT rather than by gate leakage. **Fig. 6** shows the computed band structures of samples A and B. Thinning the channel increases the quantized band gap, thus reducing BTBT. However, even for a 3 nm InGaAs channel, the minimum BTBT leakage floor is still ~1 nA/μm at $V_{DS}$=0.5 V. For lower-power logic applications, we seek to further reduce BTBT leakage while maintaining high on-state performance.

**Fig. 7** shows the structures of samples C, D and E. All have a 4.5 nm InGaAs channel, and have InP source/drain spacers, with the regrowth interface recessed 1.5 nm below the oxide/III-V interface. Sample C has a 5 nm undoped InP spacer. Samples D and E have a 5 nm undoped spacer, and above it an 8 nm linearly doping-graded InP spacer. Samples D and E have 30 Å and 38 Å $ZrO_2$, respectively.

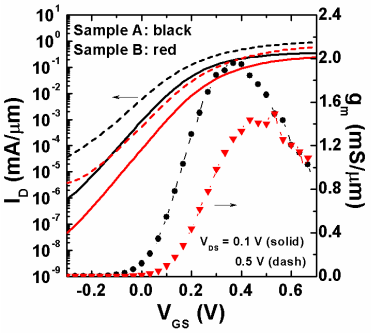



**Fig. 3: Transfer characteristics of sample A and sample B.**

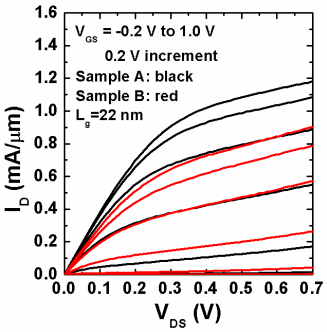



**Fig. 4: Output characteristics of sample A and sample B.**

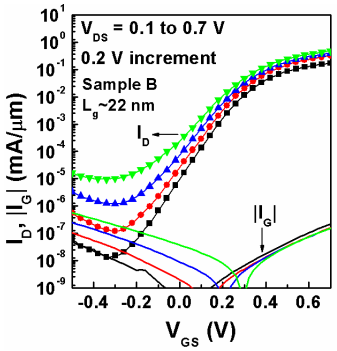



**Fig. 5: $I_G$-$V_{GS}$ and $I_D$-$V_{GS}$ characteristics of $L_g$=22 nm devices on sample B.**

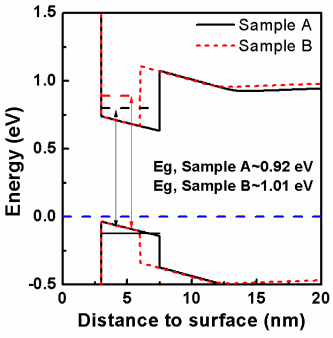



**Fig. 6: Energy band diagram in the channel for samples A and B.**

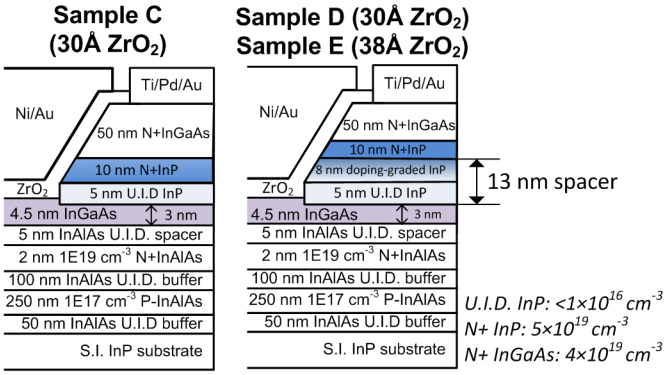



**Fig. 7: Device structures of samples C, D, and E with a recessed InP source/drain spacer. All the samples have the symmetric source/drain and only the drain side is shown here.**

**Fig. 8** and **Fig. 9** compare the transfer and output characteristics of samples A and C at $L_g$=60 nm. The off-state leakage floor of sample C is reduced 10:1 at $V_{DS}$=0.7 V and 3:1 at $V_{DS}$=0.5 V. For sample C, the minimum $I_{off}$ is limited by gate leakage $I_g$, while in sample A the minimum $I_{off}$ is limited by BTBT. All samples have a ~1 $\mu$m overlap between the gate and the source and drain, hence $I_g$ would be 10:1-50:1 smaller in a self-aligned device. As compared to FETs

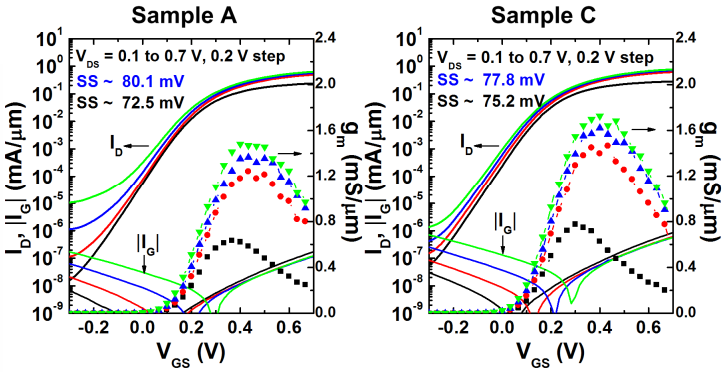



**Fig. 8: Transfer characteristics of sample A and C for 60 nm $L_g$. The minimum off-state leakage floor is dominated by BTBT for sample A and gate leakage for sample C.**

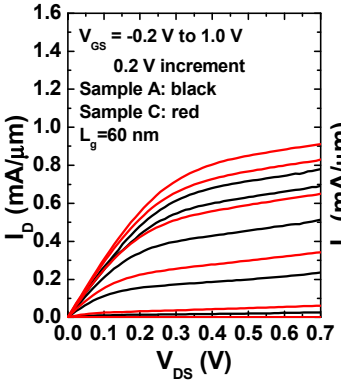



**Fig. 9: Output characteristics of samples A and C at $L_g$=60 nm.**

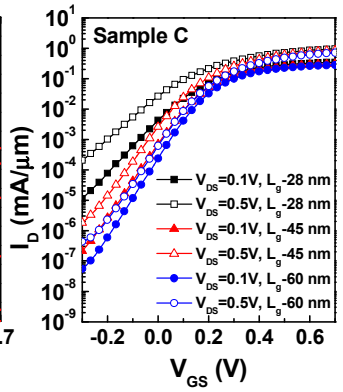



**Fig. 10: $I_D$-$V_{GS}$ characteristics vs. $L_g$ for sample C.**

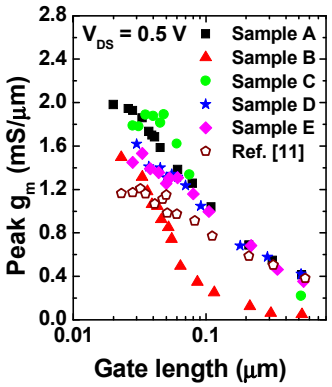



**Fig. 12: $G_m$ vs. $L_g$ for all samples.**

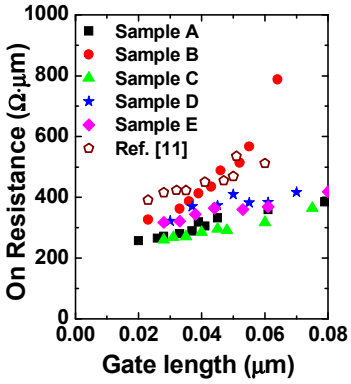



**Fig. 13: $R_{on}$ vs. $L_g$ for all samples.**

using 13 nm InP spacers [11], sample C, with 5 nm InP spacers, has smaller source/drain resistance. Higher added resistance is observed with InP than InGaAs spacers; we attribute this to the 0.2 eV InP-InGaAs band offset and the consequently smaller surface inversion sheet charge density of InP spacers. Although thinner InP spacers reduce $R_{on}$ and increase $I_{on}$, FETs with thinner InP spacers have poorer electrostatics, hence increased *S.S.*, at short gate lengths (**Fig. 10**). To maintain good electrostatics, hence low *S.S.*, the spacer must have some minimum thickness, yet for low BTBT leakage only a fraction of this at the high-field region need be InP; thick, fully-depleted InP spacers reduce the on-state transconductance. For simultaneous high $I_{on}$ and low $I_{off}$, this suggests the use of spacers alloy-graded from InP to InGaAs. Alternatively, a doping-graded InP spacer would be lightly depleted in the source, minimizing access resistance, yet heavily depleted in the drain, minimizing BTBT and *S.S.*.

**Fig. 11** shows the transfer characteristics of samples D and E. By using a 5 nm undoped recessed InP spacer in combination with an 8 nm doping-graded InP spacer, the drain electric field is further smoothed, and low BTBT leakage and high $I_{on}$ are achieved. The $L_g$=30 nm devices show 300 pA/μm minimum off-state leakage at $V_{DS}$=0.5 V, being limited by gate leakage. The peak transconductance is 1.6 mS/μm.

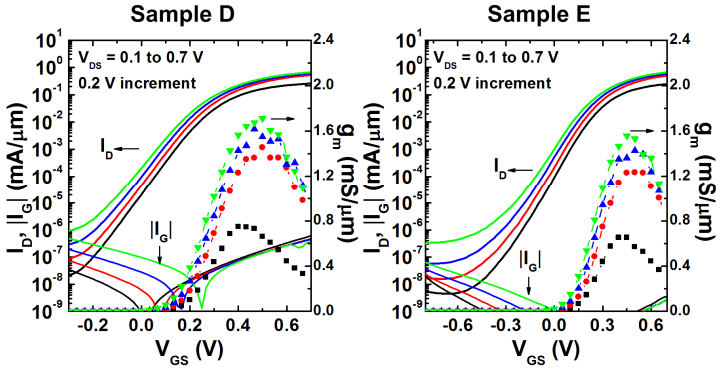



**Fig. 11: $I_G$-$V_{GS}$ and $I_D$-$V_{GS}$ characteristics of $L_g$=30 nm devices for samples D (30 Å $ZrO_2$) and E(38 Å $ZrO_2$).**

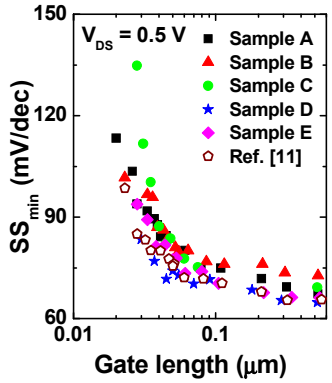



**Fig. 14: SS vs. $L_g$ for all samples.**

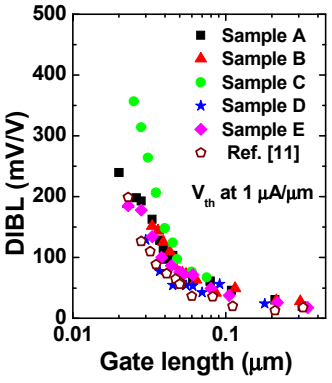



**Fig. 15: *DIBL* vs. $L_g$ for all samples.**

Further increasing the oxide thickness from 30 Å (sample D) to 38 Å(sample E) decreases the gate leakage, and the minimum $I_{off}$ is reduced to 60 pA/μm, with a 100:1 smaller BTBT leakage floor than obtained using InGaAs source/drain spacers (sample A, **Fig. 3**). To our knowledge, this is the lowest leakage current observed in an InGaAs MOSFET at a VLSI-relevant gate length.

**Fig. 12** shows the variation of $g_m$ with $L_g$. Compared to [11], the on-state performance is greatly improved by thinning the InP spacer from 13 nm to 5 nm (Sample C). Using a doping-graded InP spacer, high $g_m$ and low $I_{off}$ can be obtained, with $g_m$ reduced 10~20% compared to that with InGaAs spacers at small $L_g$. **Fig. 13** shows $R_{on}$ vs. $L_g$; reducing the InP spacer thickness reduces $R_{on}$. The $R_{on}$ extrapolated to zero $L_g$ is ~207 Ω·μm for an 11.5 nm InGaAs spacer (Sample A), ~199 Ω·μm for a 5 nm InP spacer (Sample C), and 260~280 Ω·μm for a 13 nm doping-graded spacer (Samples D, E). Compared to [11], linearly doping-graded InP spacers improve the on-resistance from 364 Ω·μm to ~270 Ω·μm, indicating significantly reduced parasitic source/drain resistance.

**Fig. 14** and **Fig. 15** show the variation of *S.S.* and DIBL with $L_g$. Increasing the spacer thickness improves DIBL through improved electrostatics, and improves *S.S.* through both

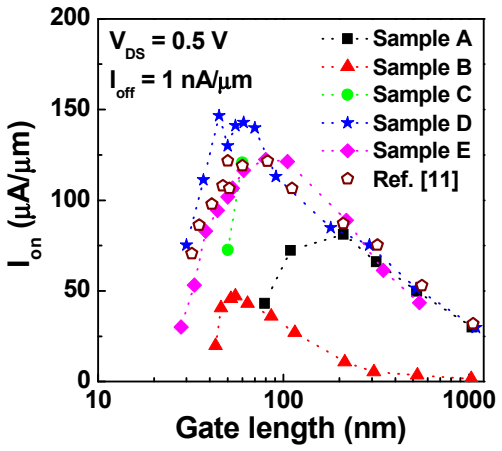



**Fig. 16: $I_{on}$ vs. $L_g$ at $I_{off}$=1 nA/μm and $V_{DS}$=0.5 V.**

improved electrostatics and reduced BTBT. Sample C shows high *S.S.* and large DIBL at small $L_g$ because of poor electrostatics from the thin spacer **(Fig. 10)**. In contrast, with a 13 nm doping-graded InP spacer (Samples D, E, also [11]), $SS_{min}$ is ~90 mV/dec at $L_g$=30 nm.

**Fig. 16** shows $I_{on}$ vs. $L_g$ at $I_{off}$=1 nA/μm and $V_{DS}$=0.5 V. Samples A and B shows low $I_{on}$ at smaller $L_g$ because the high BTBT leakage not only degrades the *S.S.*, but also increases $I_{off}$ above 1 nA/μm at small $L_g$. Instead of further thinning the channel, samples C, D and E use recessed InP spacers, and show significantly improved $I_{on}$ at small $L_g$ due to reduced BTBT leakage. Sample D shows the maximum peak $I_{on}$=150 μA/μm at $L_g$= 45 nm. Sample E shows slightly reduced $I_{on}$, due to the thicker gate dielectric, which decreases $g_m$ and increases *S.S.* For samples C, D, and E, $I_{on}$ decreases rapidly as $L_g$ is reduced below 40 nm. This is a consequence of poor electrostatics, hence large *S.S.*, at these gate lengths.

**Fig. 17** shows $I_{on}$ vs. $L_g$ at $V_{DS}$=0.5 V, but at a larger $I_{off}$=100 nA/μm, benchmarking recent III-V MOSFETs. The FETs reported here use $In_{0.53}Ga_{0.47}As$ channels and show performance comparable to leading III-V FETs. Given an $I_{off}$=100 nA/μm metric, the 2.7-nm-thick InAs channel MOSFETs of [1] show highest $I_{on}$, as a consequence of larger gate capacitance and good electrostatics. In contrast, for low-power applications, a wider band-gap $In_{0.53}Ga_{0.47}As$ channel more readily provides low leakage current. To further improve $I_{on}$ at small $L_g$, a tri-gate or nanowire structure would provide improved electrostatics and hence improved *S.S.* Combined with recessed InP source/drain spacers for low BTBT leakage, InGaAs MOSFETs would then be suitable for low-power logic.

## Conclusions

We have demonstrated that recessed InP source/drain spacers can reduce band-to-band leakage current in InGaAs-channel MOSFETs while maintaining high transconductance. The minimum $I_{off}$ for a 30 nm gate length device was 60 pA/μm,

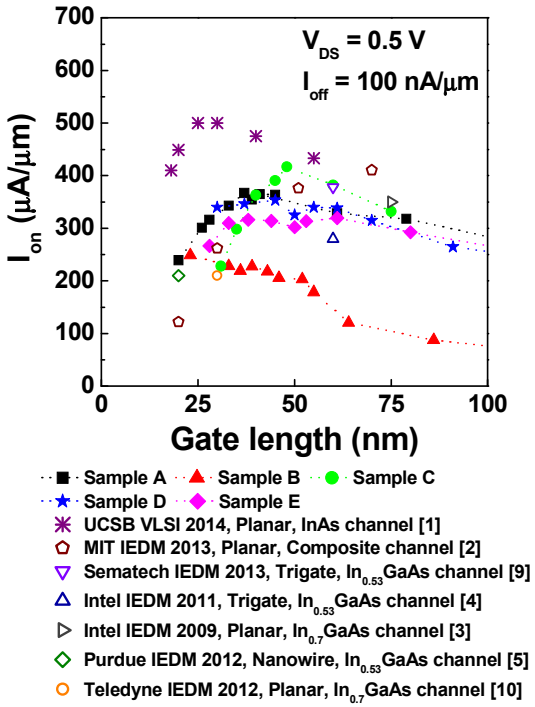



**Fig. 17: $I_{on}$ vs. $L_g$ at $I_{off}$=100 nA/μm and $V_{DS}$=0.5 V and the benchmark with recent III-V FETs.**

100:1 smaller than the leakage of a FET using InGaAs S/D spacers. The devices with thin oxide show the on-state current $I_{on}$=150 μA/μm at $I_{off}$=1 nA/μm and $V_{DS}$=0.5 V. These recessed InP source/drain spacers greatly reduces the leakage floor, making III-V InGaAs MOSFETs feasible for low-power logic.

## Acknowledgement

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