Low Power III-V InGaAs MOSFETs Featuring InP Recessed Source/Drain Spacers with I_{on}=120 μA/μm at I_{off}=1 nA/μm and V_{DS}=0.5 V

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IEDM 2014
San Francisco, CA, USA

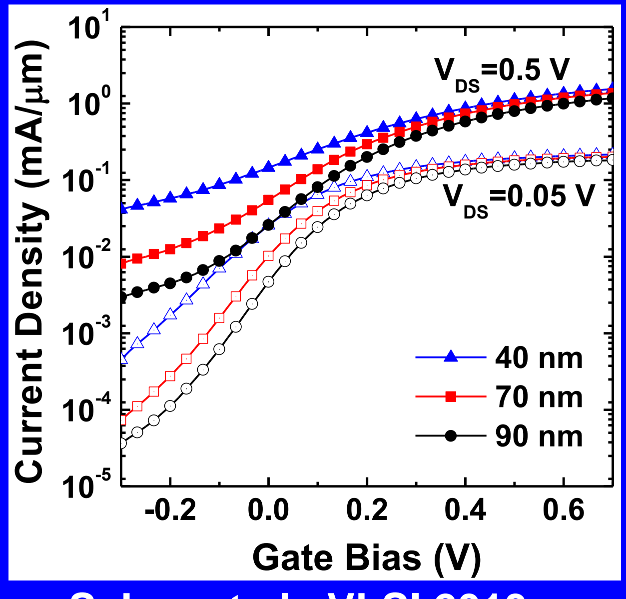
Outline

- Problem: III-V MOSFETs are very leaky
- Gate-last Process Flow
- Knob 1: Wide band-gap barrier
- Knob 2: Source/Drain vertical spacer
- Knob 3: Ultrathin channel
- Knob 4: Recessed InP S/D spacer
- Knob 5: Doping-graded InP spacer
- Summary

InGaAs/InAs FETs are leaky!

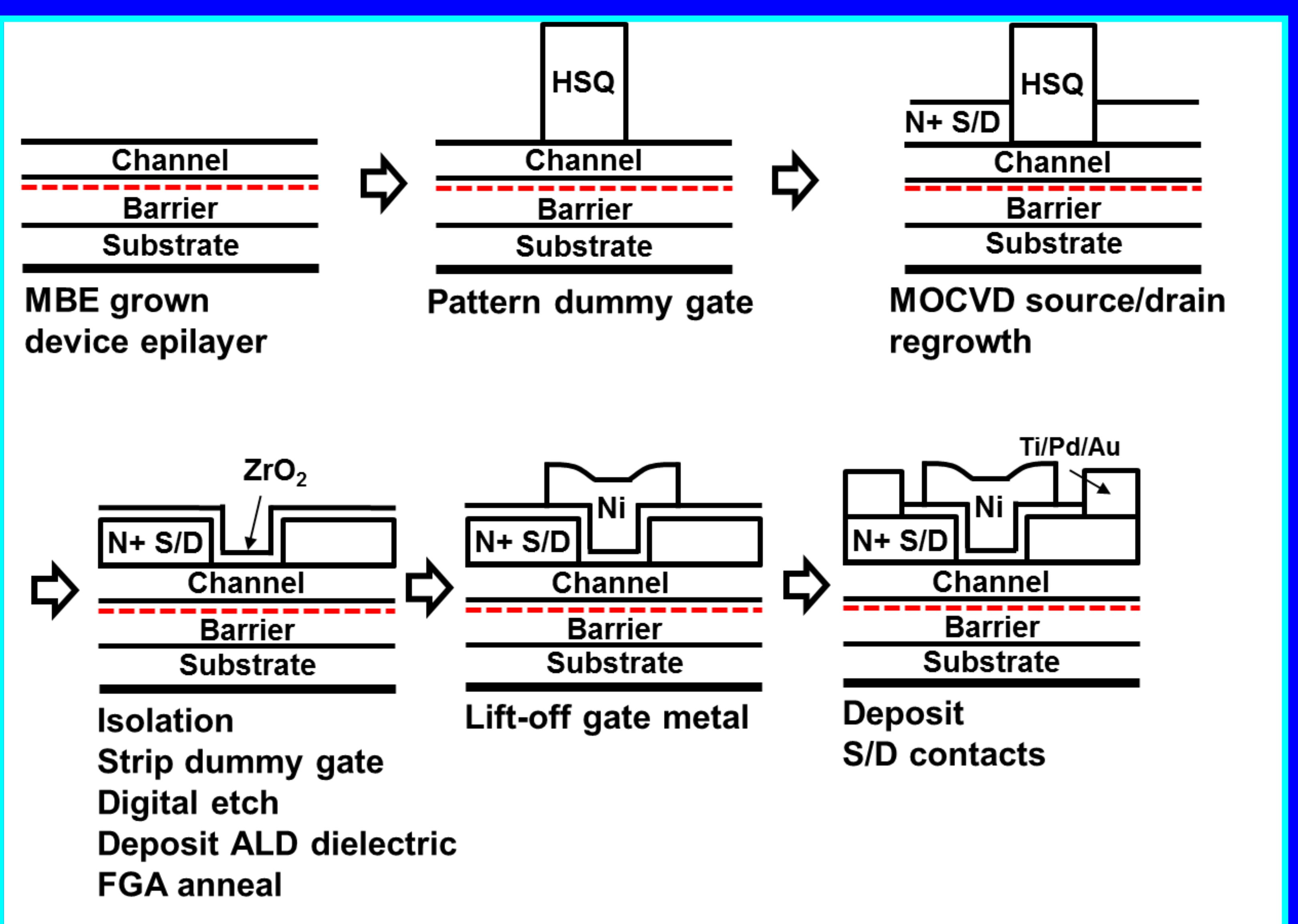
- III-V channel: low electron effective mass, high velocity, high mobility→ higher current at lower V_{DD} ☺
- Low band gap→ band-to band tunneling (BTBT) ☹
- High permittivity→ worse electrostatics, large DIBL ☹
- Goal: reduce leakage current for low power logic!

300K	Si	Ge	GaAs	InAs	$In_{0.53}Ga_{0.47}As$
m_e^*	0.19	0.08	0.063	0.023	0.041
$\mu_e(cm^2/V{\cdot}s)$	1450	3900	9200	33000	12000
$\mu_h(cm^2/V{\cdot}s)$	370	1800	400	450	<300
Eg(eV)	1.12	0.664	1.424	0.354	0.75
ε_r	11.7	16.2	12.9	15.2	13.9
a(Å)	5.43	5.66	5.65	6.06	(InP)



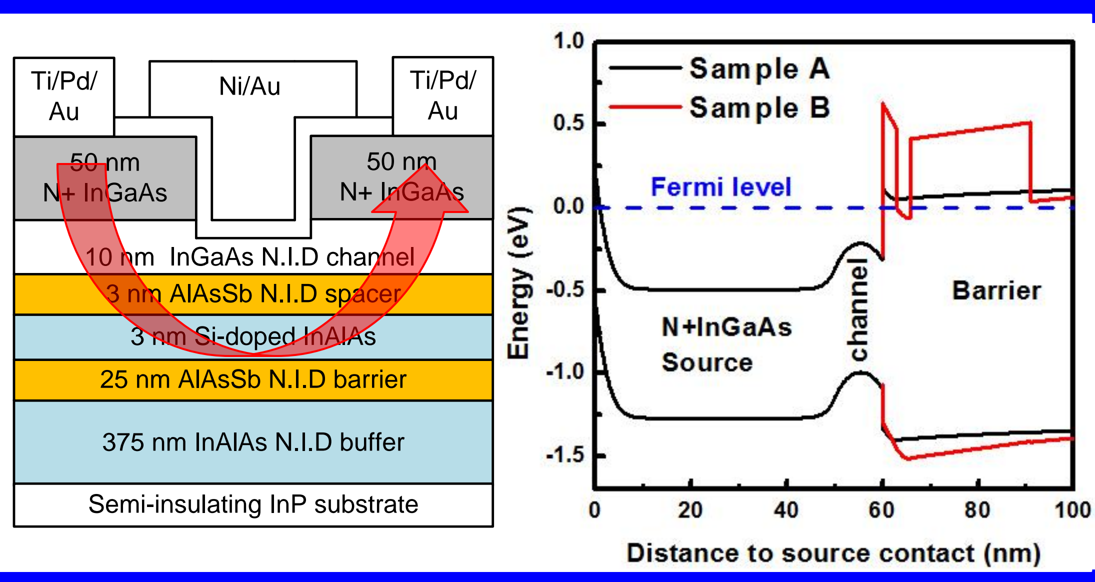
S. Lee et al., VLSI 2013

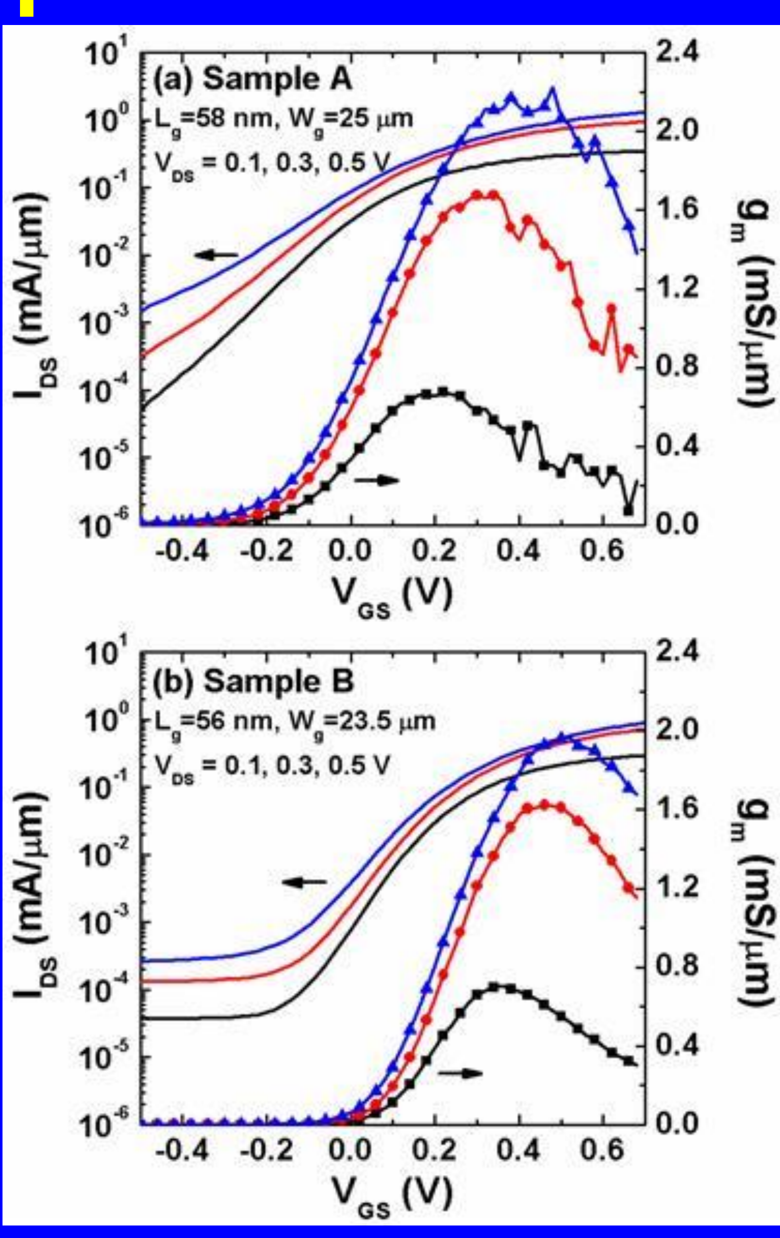
UCSB Gate Last Process Flow



Knob 1: Wide Band-gap Barrier

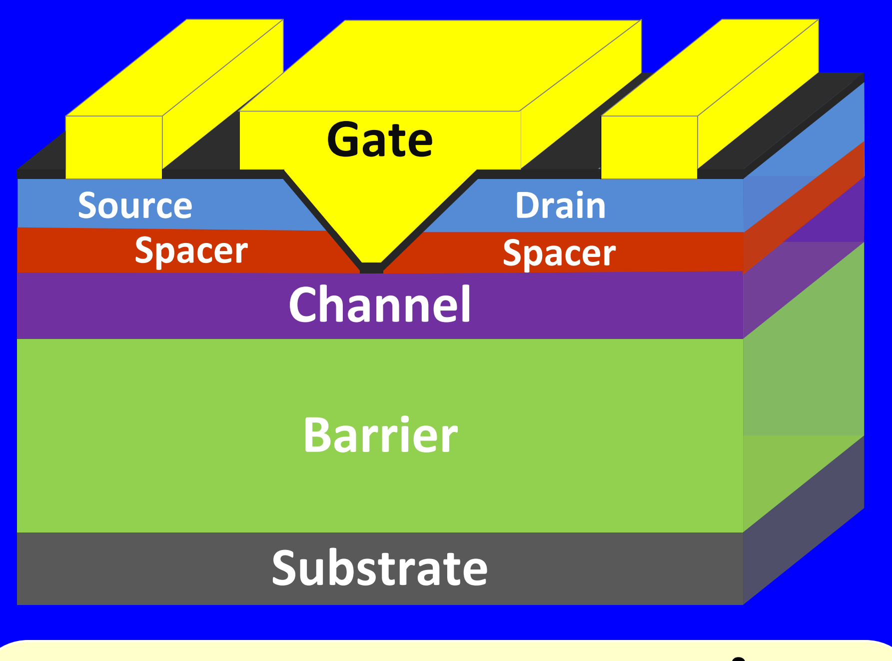
- Wide band-gap barriers or P-doped back barriers reduces bottom leakage path.
- Solution 1: AlAsSb barriers (Sample B) reduces subthreshold leakage.
- Solution 2: P-doped InAlAs barriers also work well.

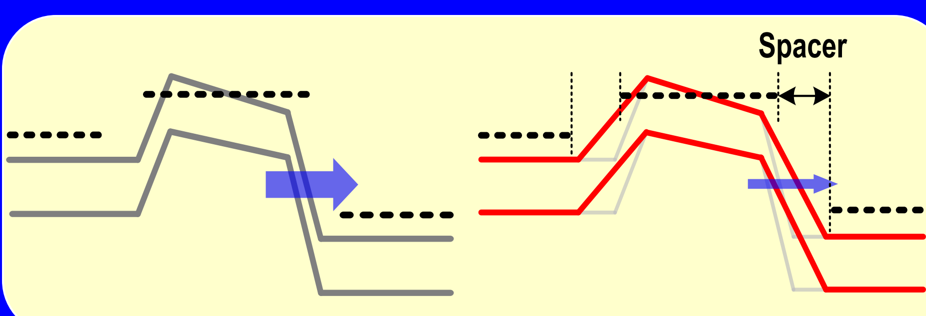


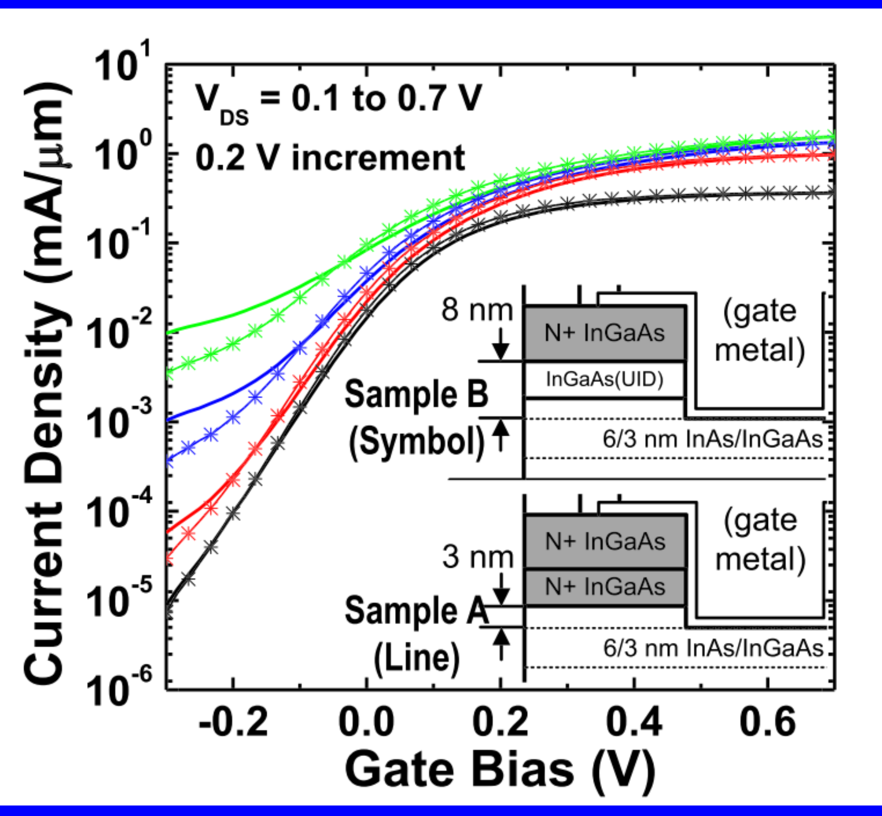


C. Y. Huang et al., APL., 103, 203502 (2013)

Knob 2: Source/Drain Vertical Spacer



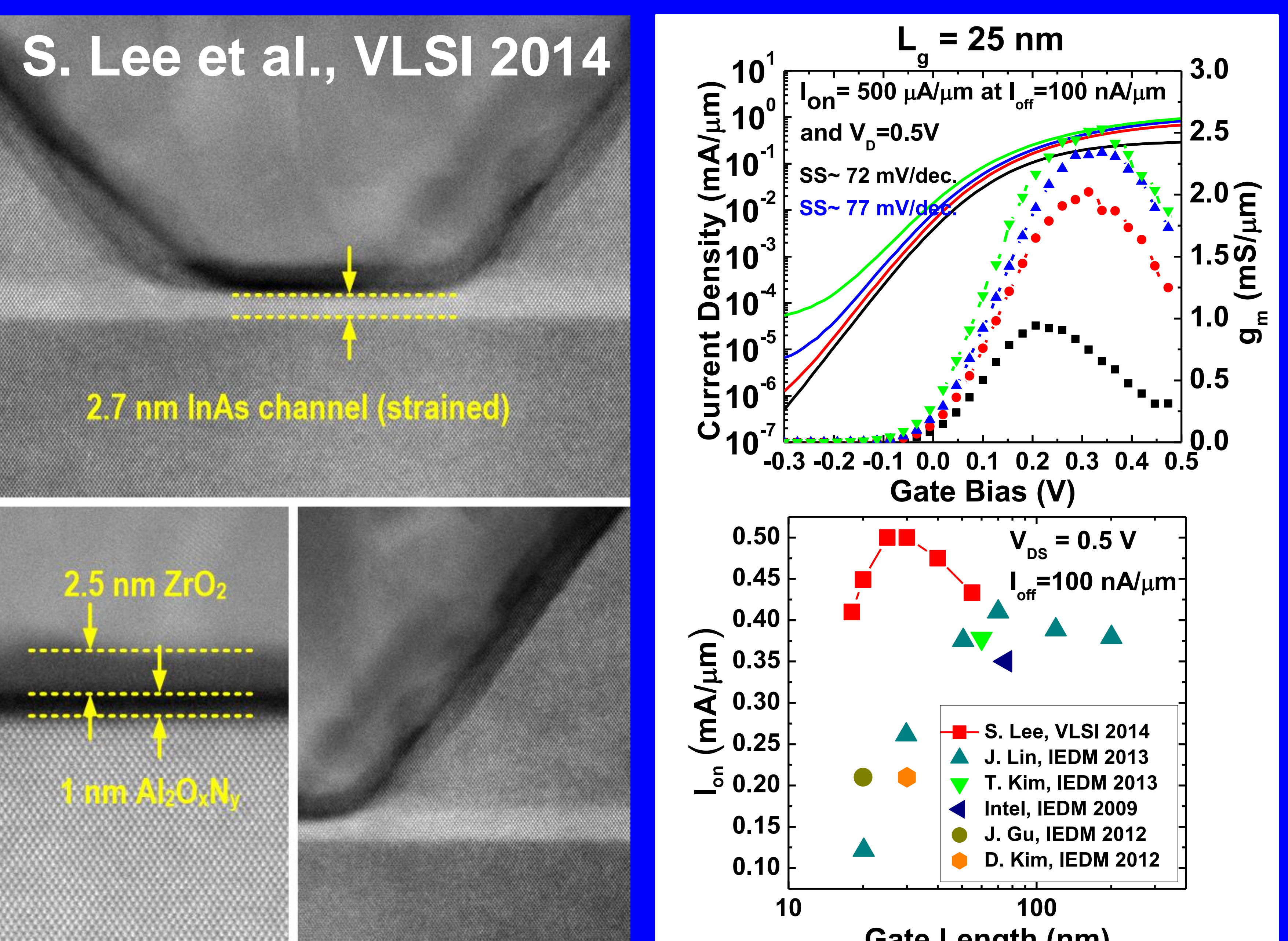




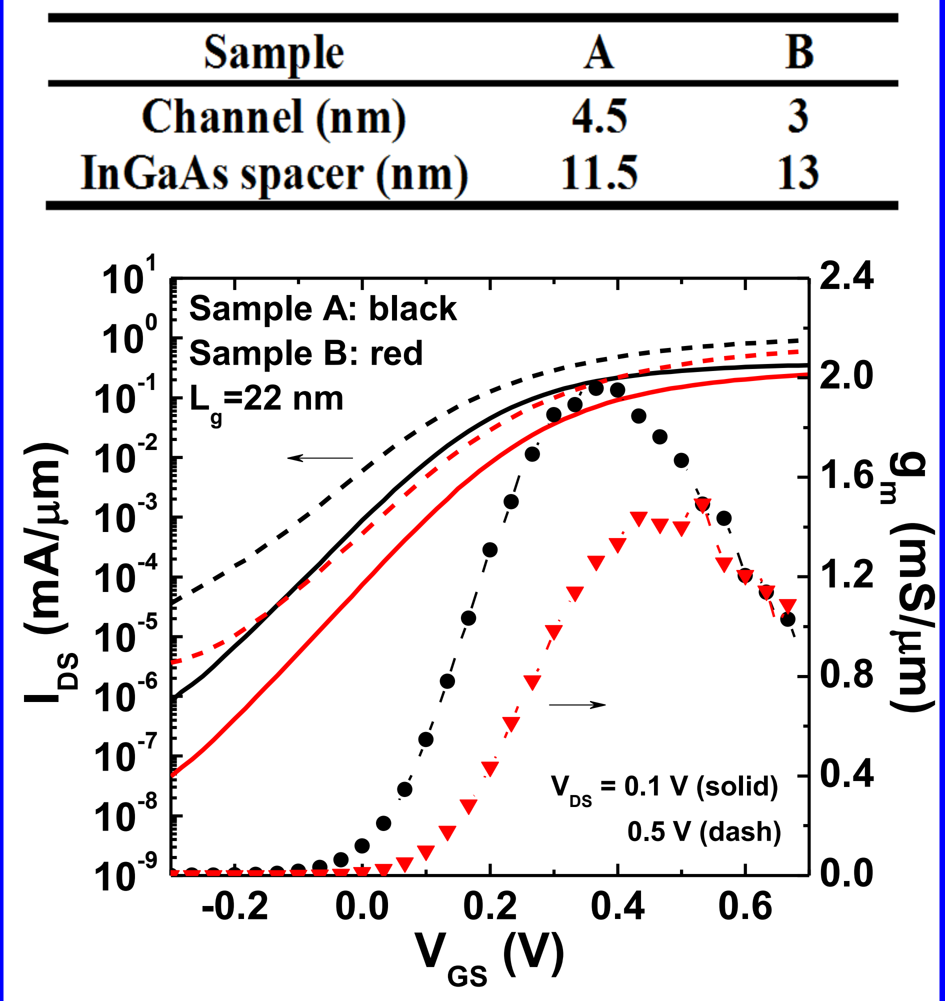
S. Lee et al., APL 103, 233503 (2013)
C. Y. Huang et al., DRC 2014.

Vertical spacers reduce the peak electric field, improve electrostatics, and reduce BTBT floor.

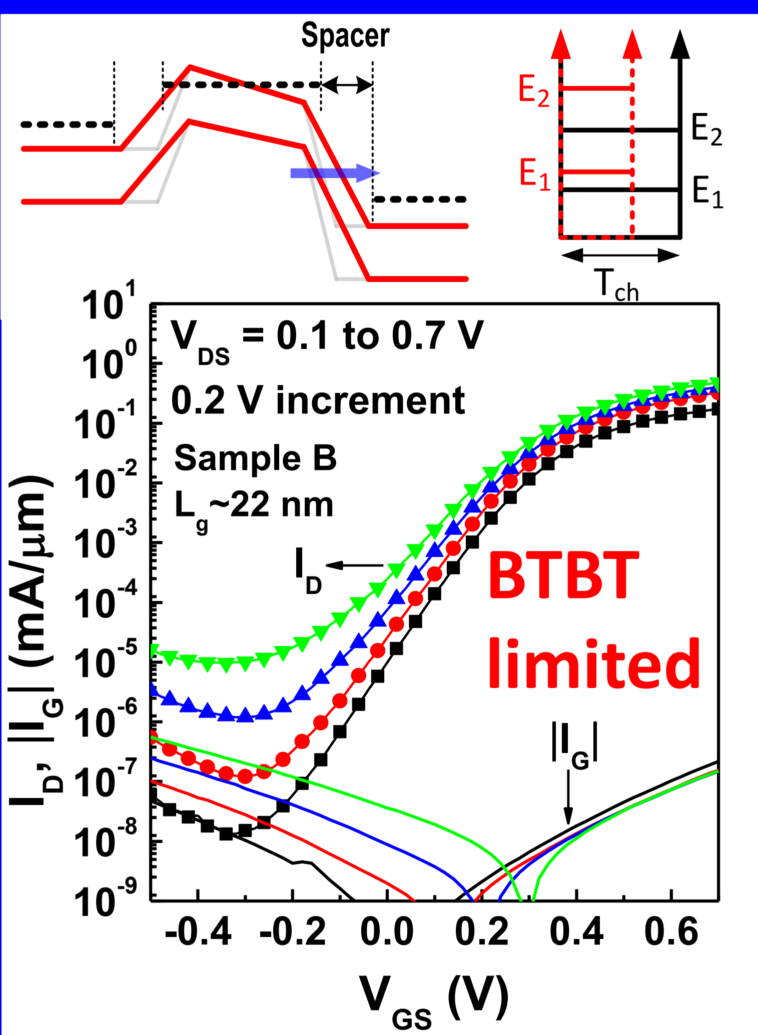
Knob 3: Ultra-thin channel



Increasing band gap: $In_{0.53}Ga_{0.47}As$ channel

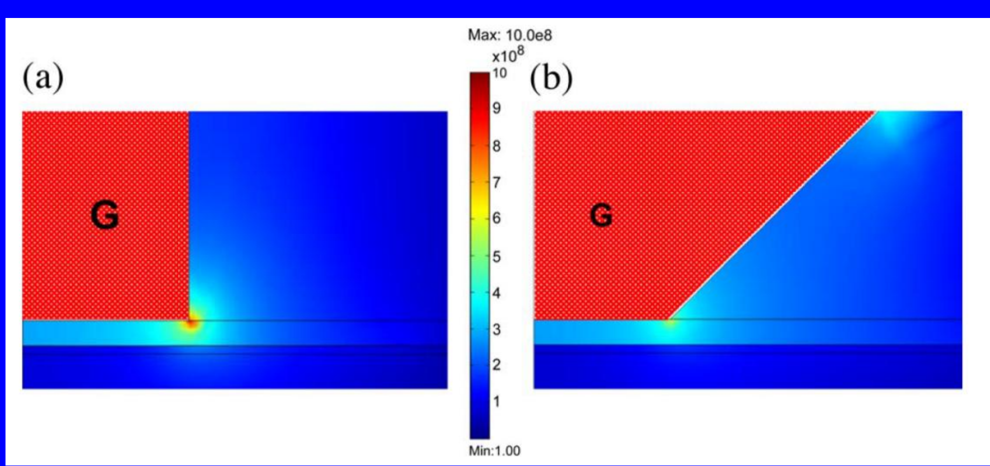


Sample	A	B
Channel (nm)	4.5	3
InGaAs spacer (nm)	11.5	13

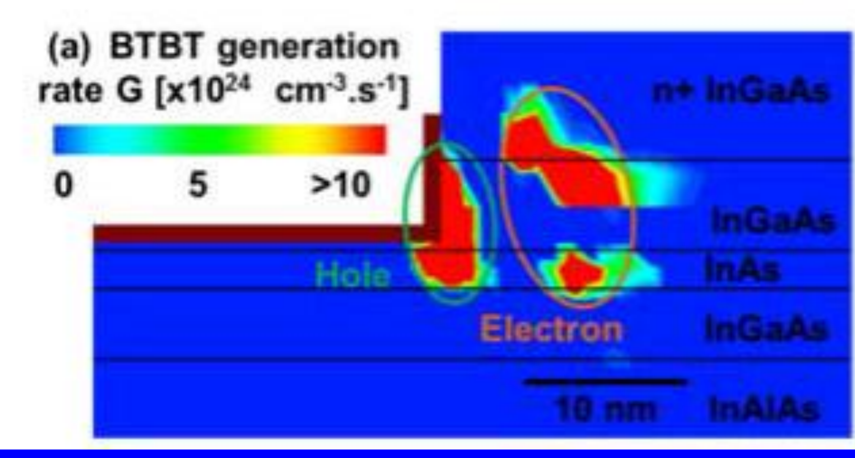


Reducing channel thickness improves electrostatics, increases confinement bandgap and reduces BTBT.

E-field and BTBT contour



R. Chu et al., EDL 29, 974 (2008)

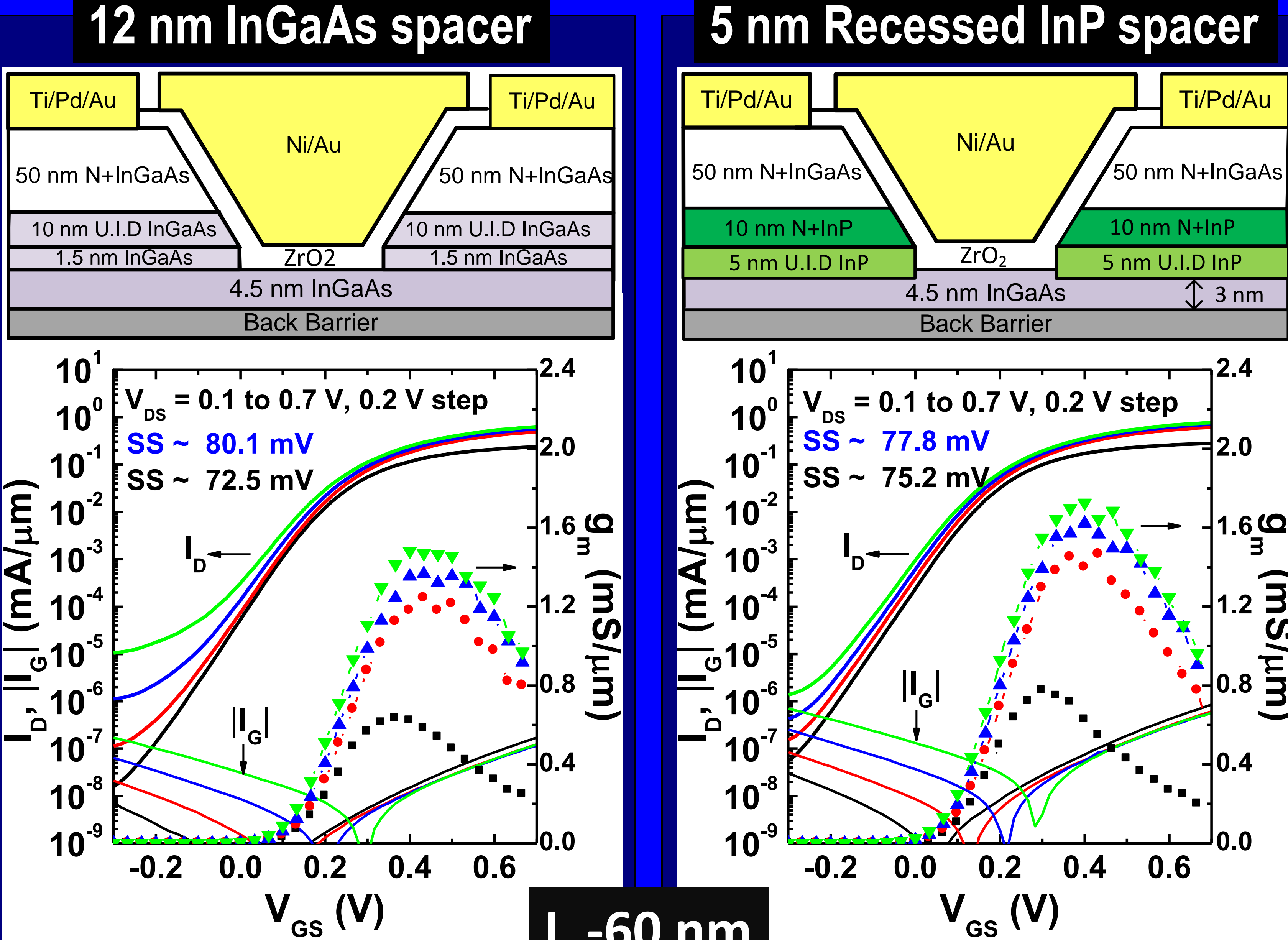


J. Lin et al., EDL 35, 1203 (2014)

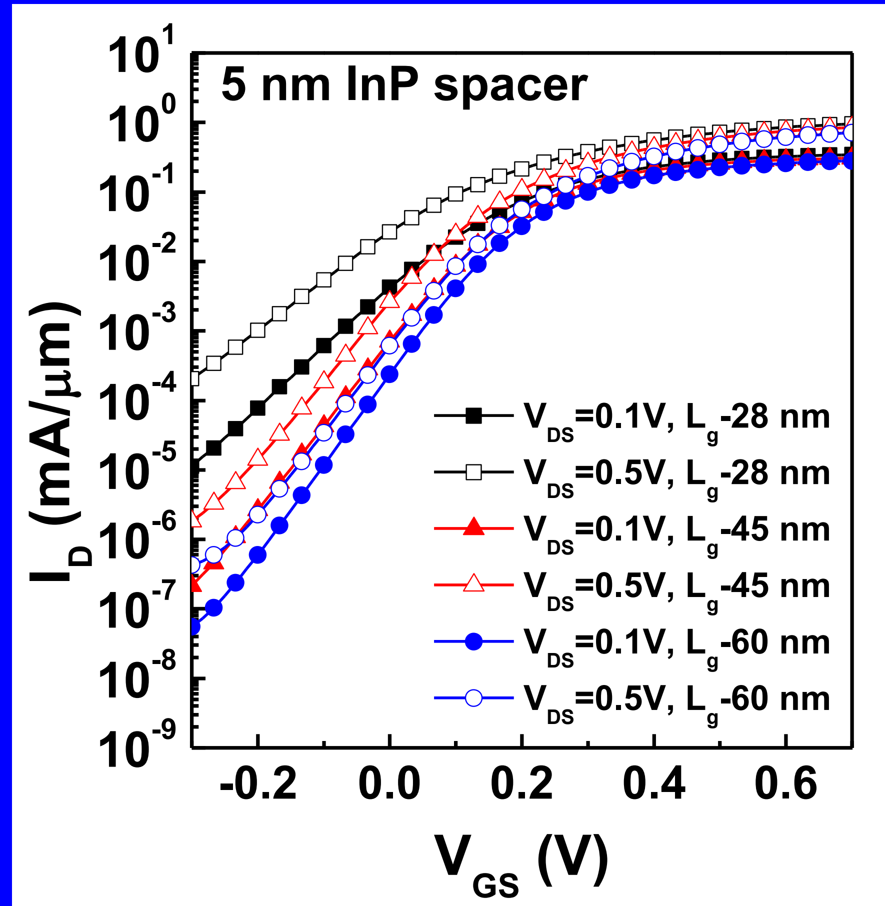
- Concentrated electric field at the drain end of the channel next to the gate edge.
- <u>Solution:</u>

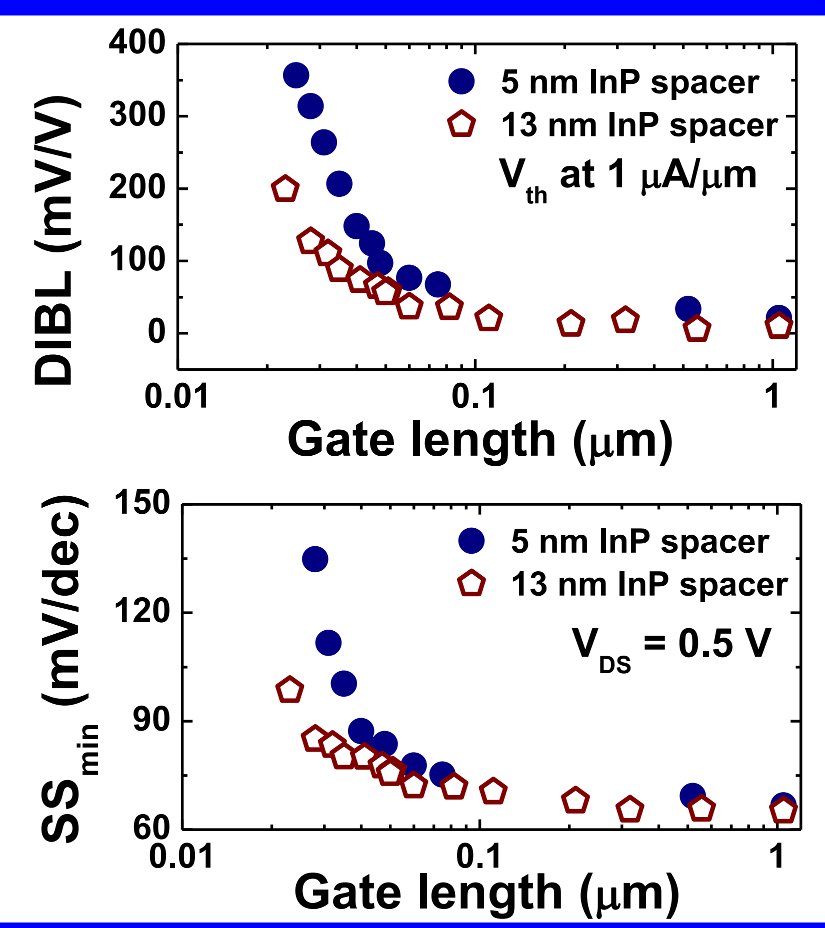
  Replace InGaAs with wide band-gap InP (E_g~1.35 eV)

Knob 4: Recessed InP S/D spacer



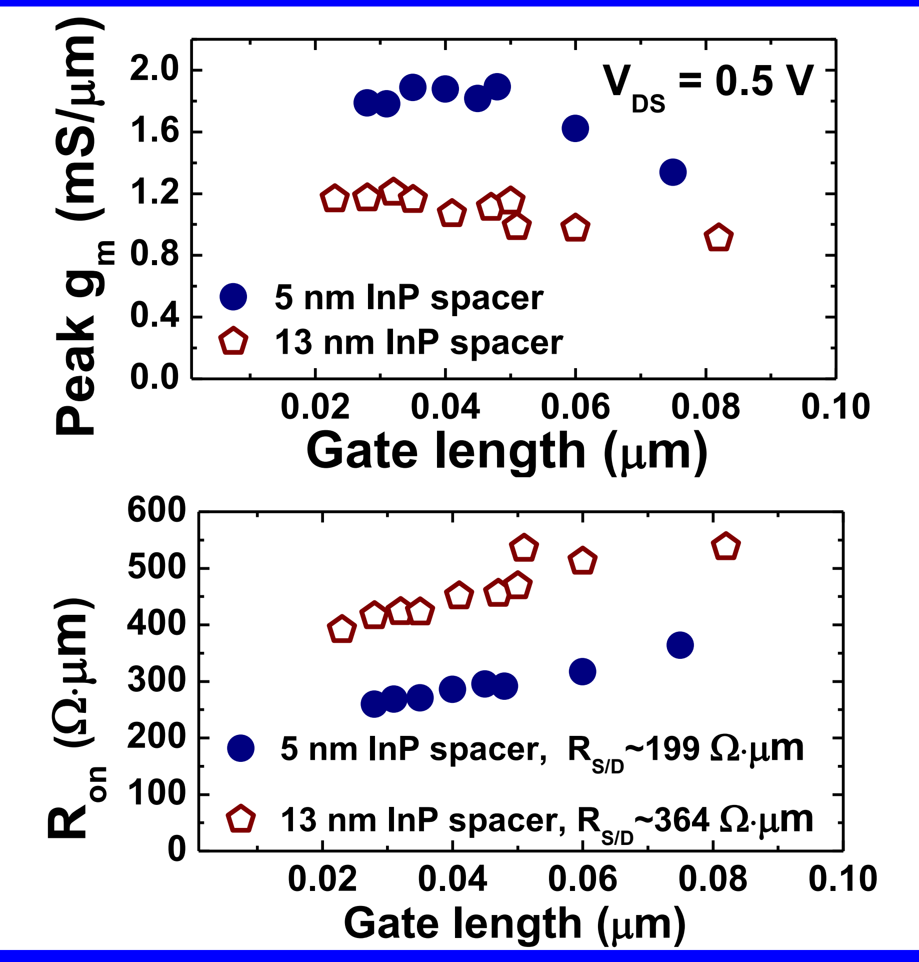
InP spacer thickness: subthreshold

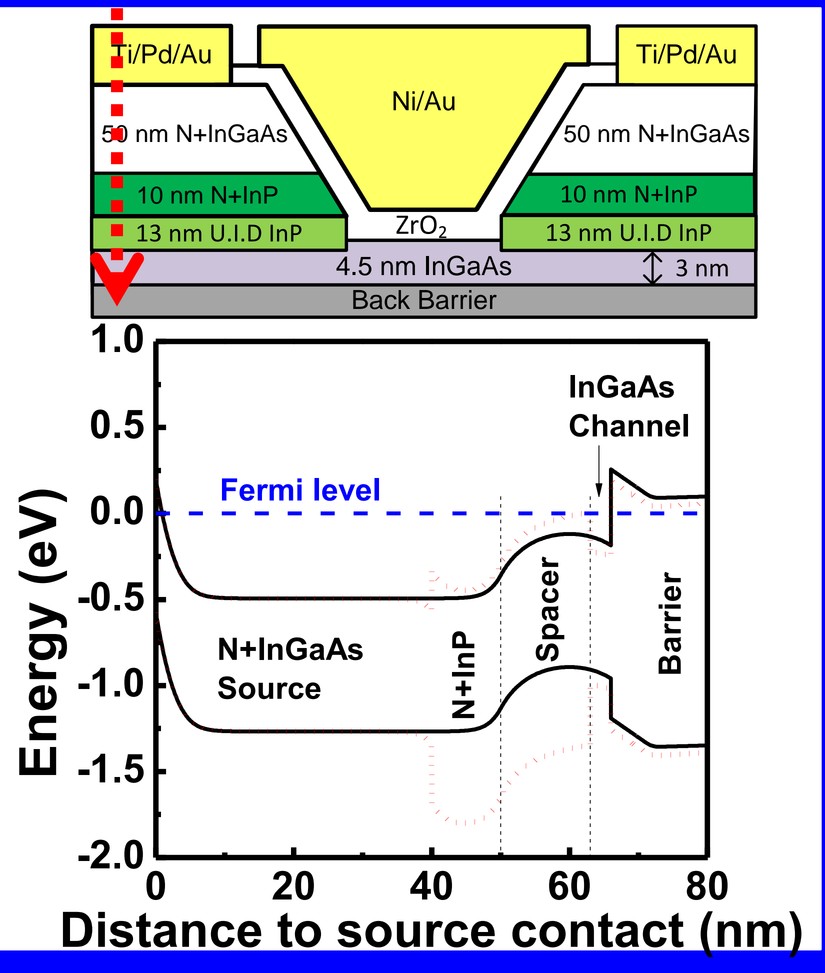




- Minimum spacer thickness is required to maintain good electrostatics.
- Thicker spacer is desired at drain to smooth electric field.

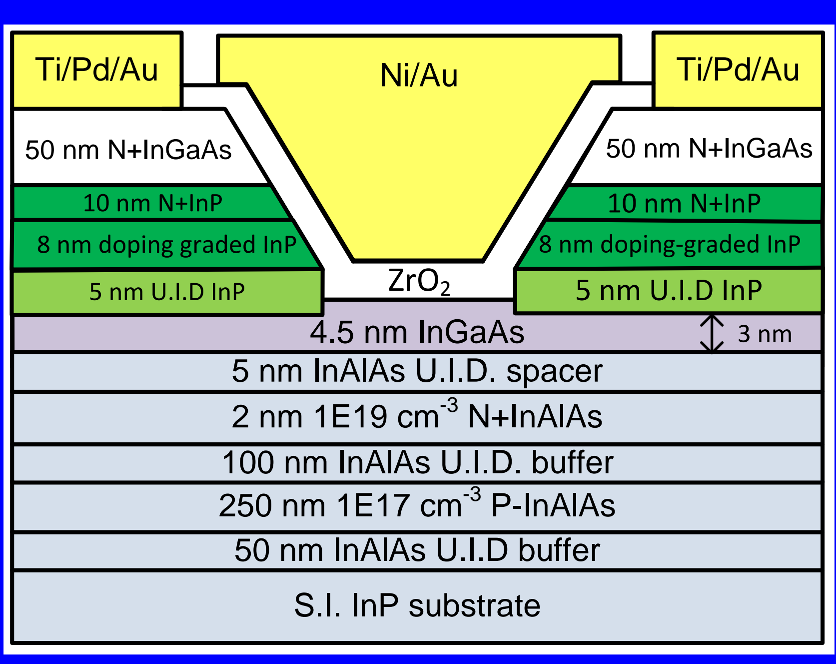
InP spacer thickness: on-state



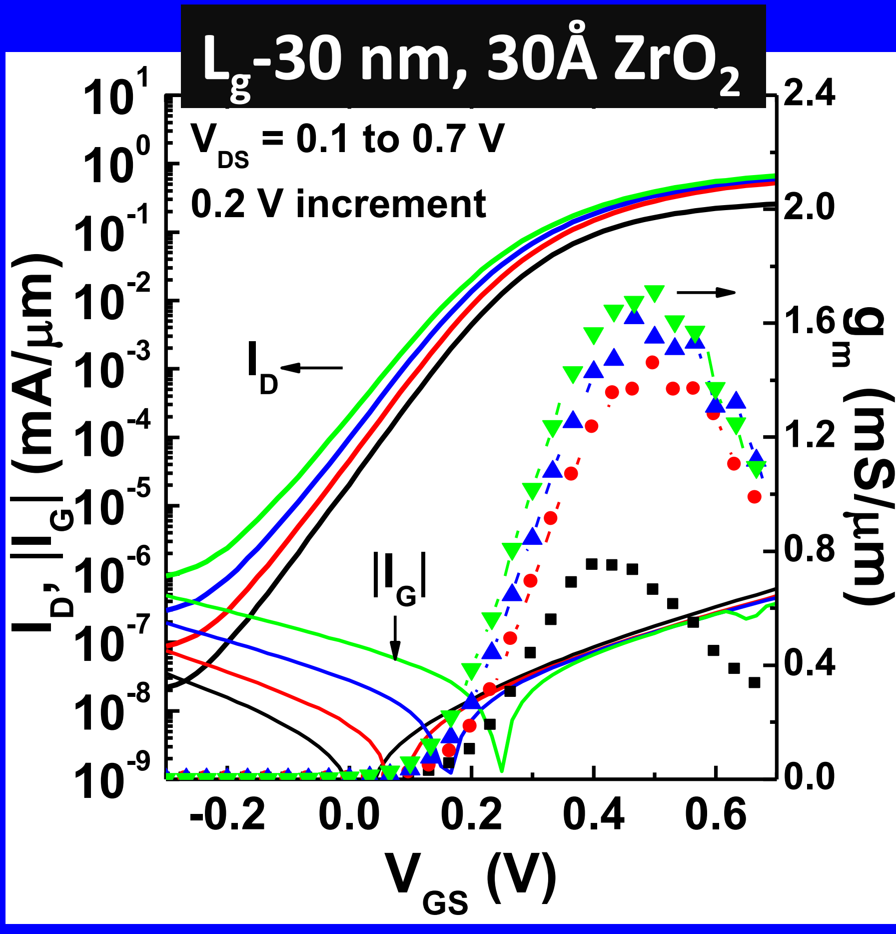


- Thicker InP spacer increases R_{on}, and degrades G_m
- Thinner spacer is desired at source to reduce $R_{S/D}$.

Knob 5: Doping-graded InP spacer

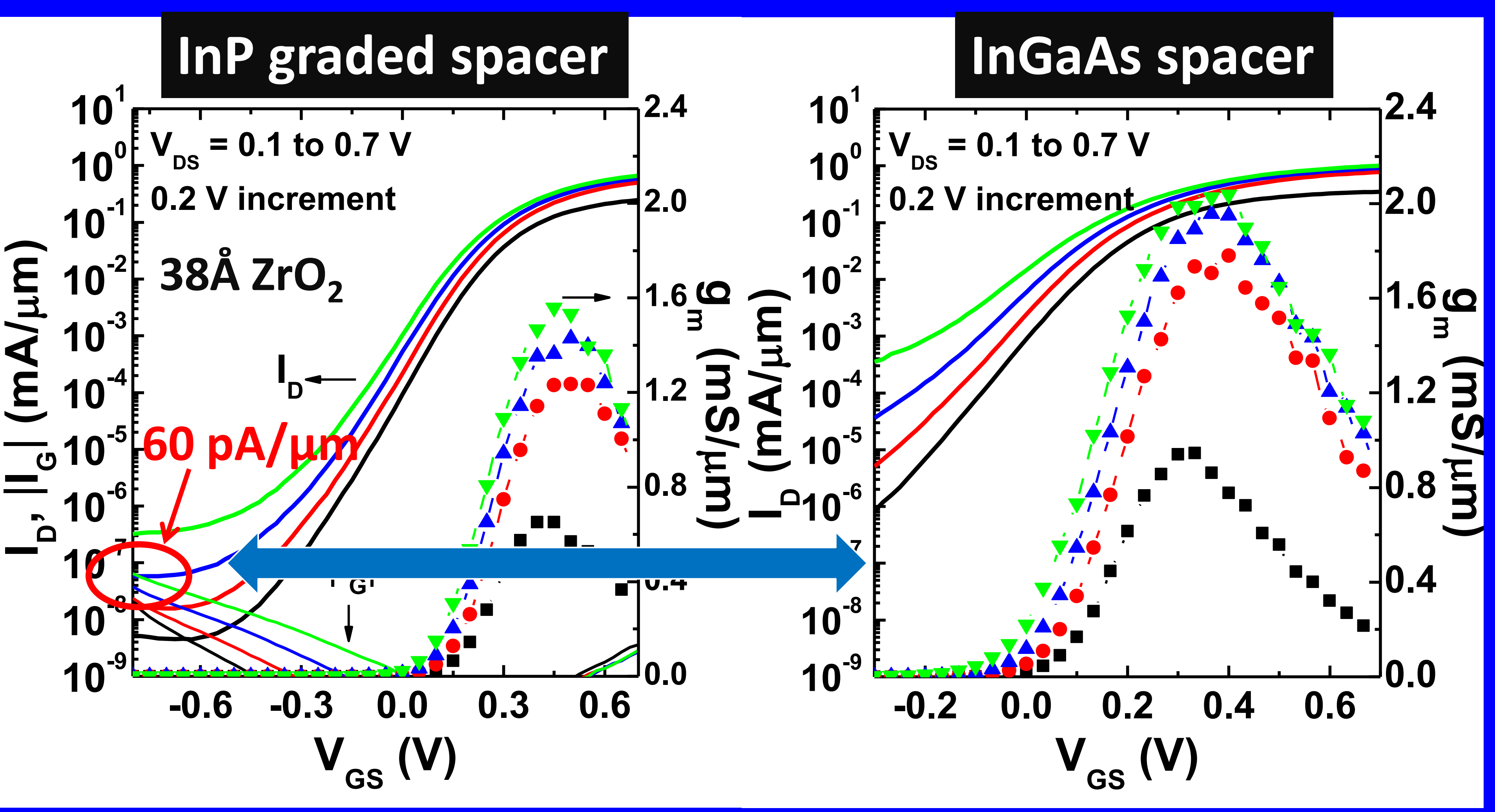


R_{on} at zero L_g (Ω·µm)	5 nm UID InP	13 nm UID InP	Doping graded InP
	~199	~364	~270



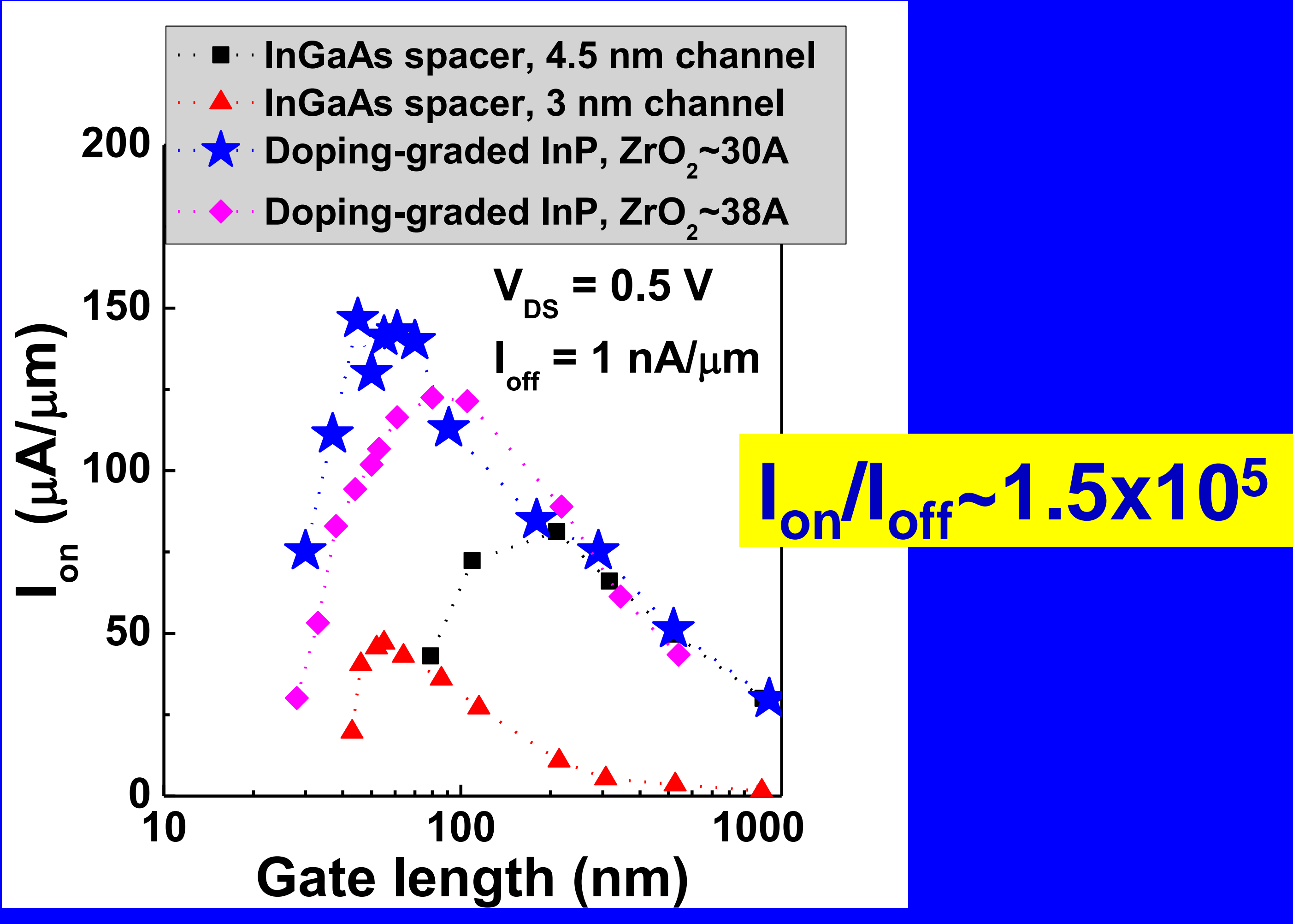
- Doping-graded InP spacer reduces parasitic source/drain resistance and improves G_m.
- Gate leakage limits I_{off}~300 pA/µm.

Doping-graded InP spacer+Thicker oxide



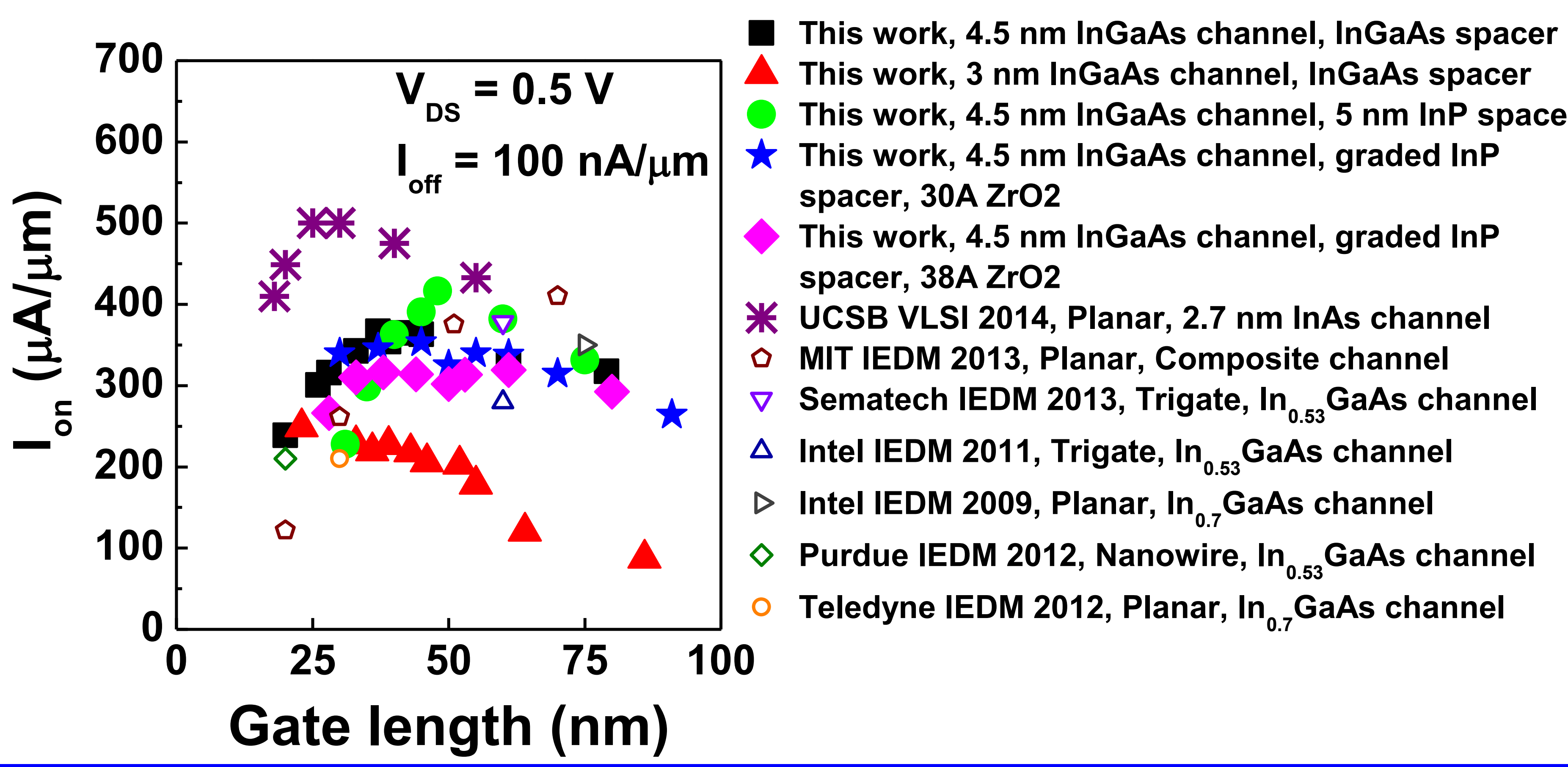
- Minimum I_{off}~ 60 pA/µm at V_D=0.5V for L_g-30 nm
- 100:1 smaller I_{off} compared to InGaAs spacer

I_{on} vs L_g at I_{off} = 1 nA/µm

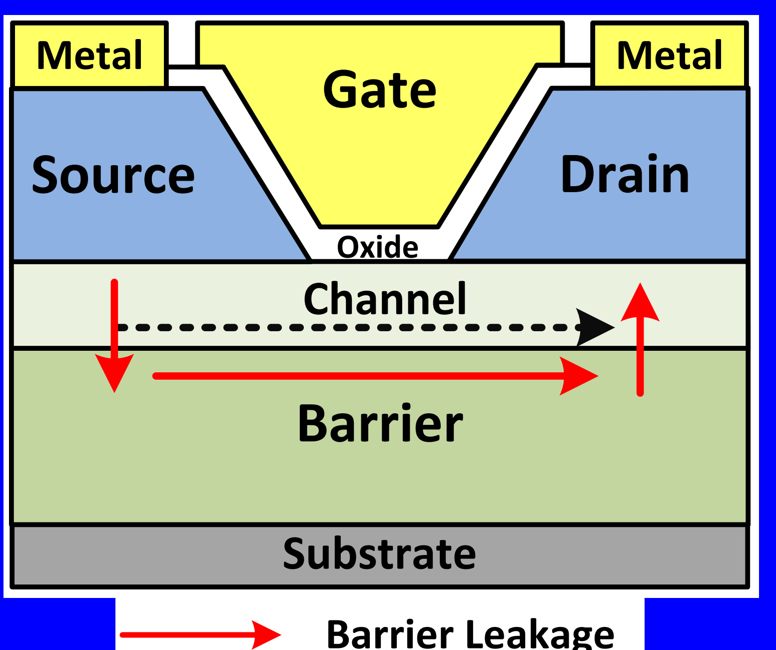


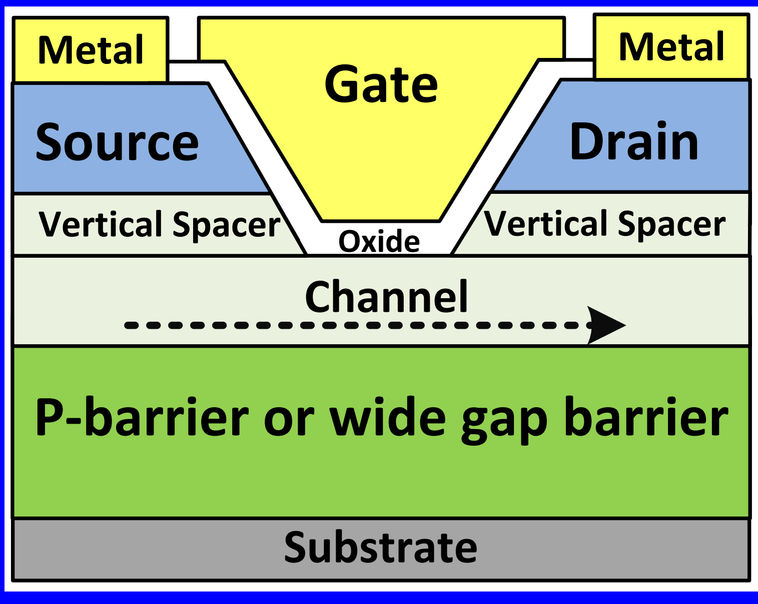
- Peak I_{on}= 150 µA/µm at V_{DS}=0.5V for L_g-45 nm devices.

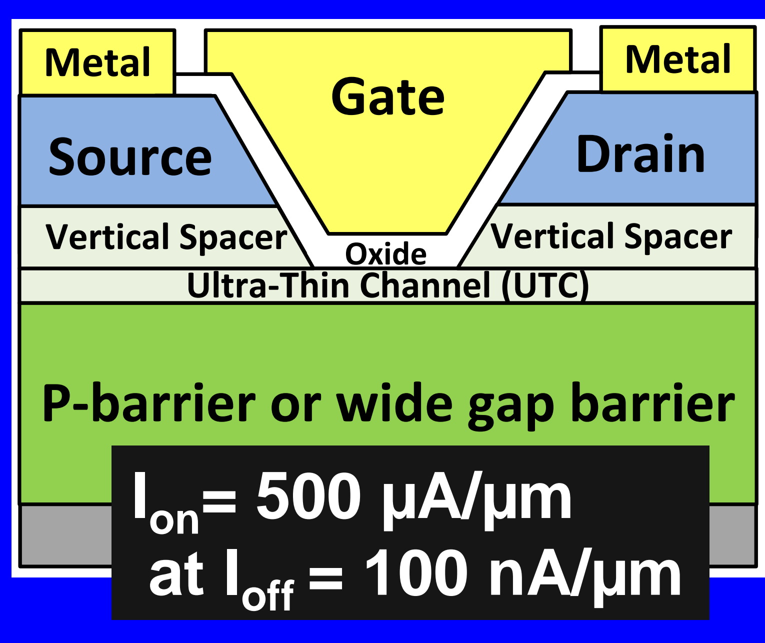
I_{on} vs L_g at I_{off} = 100 nA/µm

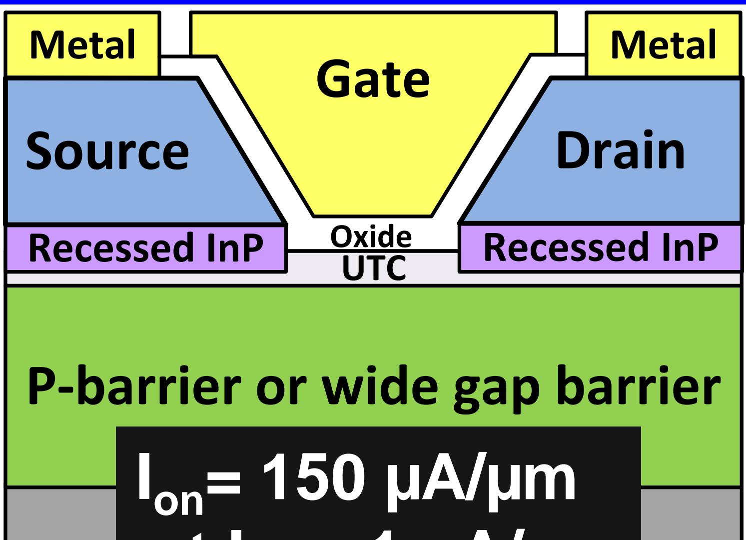


- Peak I_{on}= 415 µA/µm at V_{DS} = 0.5V for this work.
- Ultrathin InAs channel shows highest I_{on}.


Metal
Gate
Metal
Source
Drain
Oxide
Channel
Barrier
Substrate
Barrier Leakage
Channel Leakage

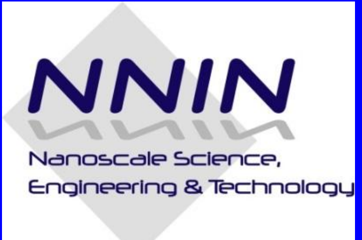

Metal
Gate
Metal
Source
Drain
Vertical Spacer
Oxide
Vertical Spacer
Channel
P-barrier or wide gap barrier
Substrate


Metal
Gate
Metal
Source
Drain
Vertical Spacer
Oxide
Vertical Spacer
Ultra-Thin Channel (UTC)
P-barrier or wide gap barrier
I_{on}= 500 μA/μm
at I_{off} = 100 nA/μm


Metal
Gate
Metal
Source
Drain
Recessed InP
Oxide
UTC
Recessed InP
P-barrier or wide gap barrier
I_{on}= 150 μA/μm
at I_{off} = 1 nA/μm

Recessed InP source/drain spacers enable III-V MOSFETs for low power logic.

Thank you!



- *This research was supported by the SRC Non-classical CMOS Research Center (Task 1437.009) and GLOBALFOUNDRIES(Task 2540.001).*
- *A portion of this work was done in the UCSB nanofabrication facility, part of NSF funded NNIN network.*
- *This work was partially supported by the MRSEC Program of the National Science Foundation under Award No. DMR 1121053.*