Phase-Locked Coherent Optical Interconnects for Data Links

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University of California, Santa Barbara

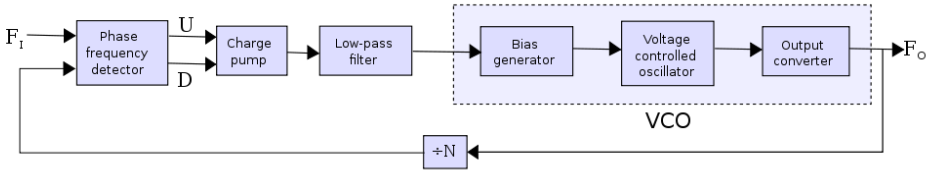
Z. Griffith, M. Urteaga
Teledyne Scientific

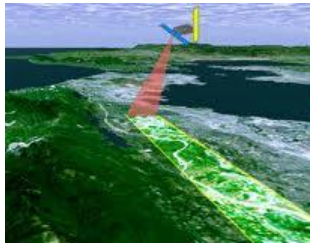
Wavelength synthesis: precise optical spectral control

1977 40-channel Citizen's band radio.

...had to purchase <u>40</u> quartz crystals

By 1980, frequency synthesis reduced this to <u>one</u>





<u>Frequency synthesis enabled modern RF systems</u> :

Precision phase/frequency control

→ efficient & controlled use of the spectrum

Today's optical systems look like a 1977 CB radio

Phase-locked coherent optical systems:

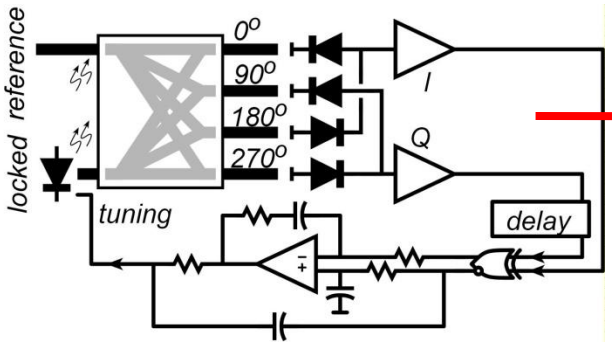
control optical channel spacings
over 100's of GHz,
with sub-Hz precision

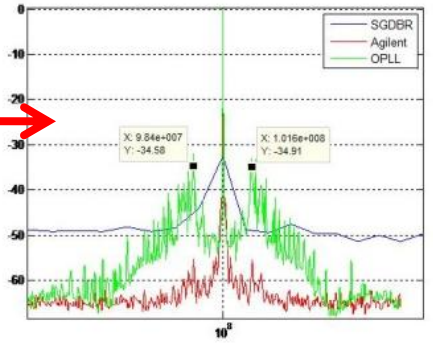
→ sensitive, compact, <u>spectrally efficient</u>,
optical communications

Optical Phase-Locked-Loops: Applications

Wideband laser locking & noise suppression.

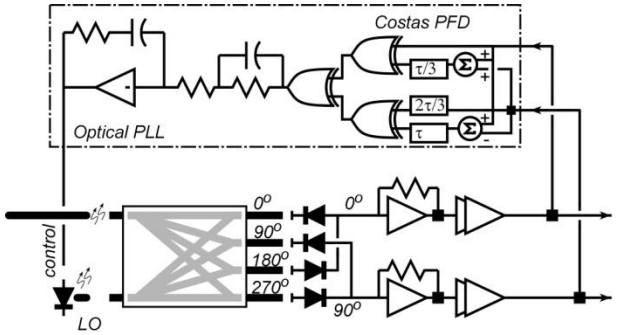
improved spectral purity without external cavities.

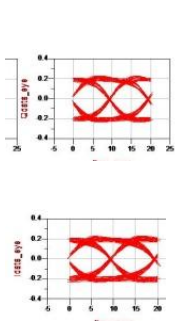


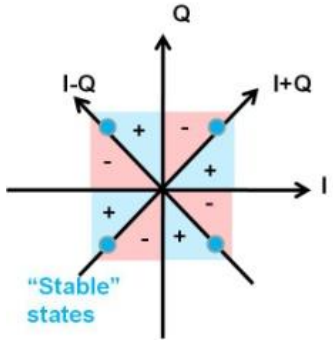


BPSK/QPSK Coherent Receivers

Short- to mid-range links, no DSP, inexpensive wide-linewidth lasers

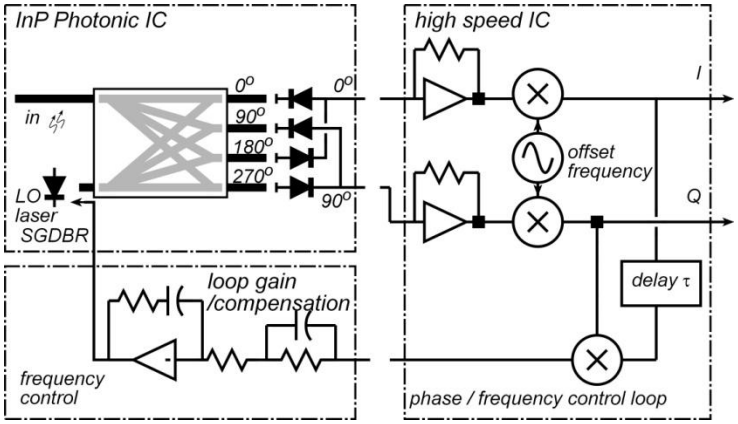


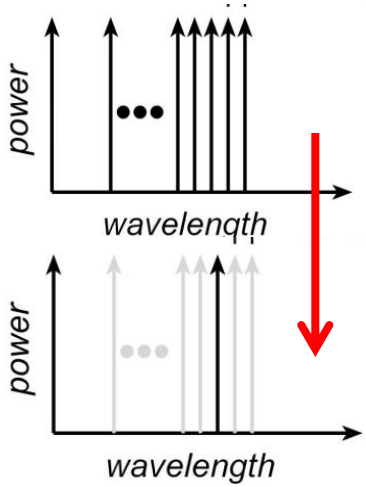




Tunable Wavelength-Selection in Receivers

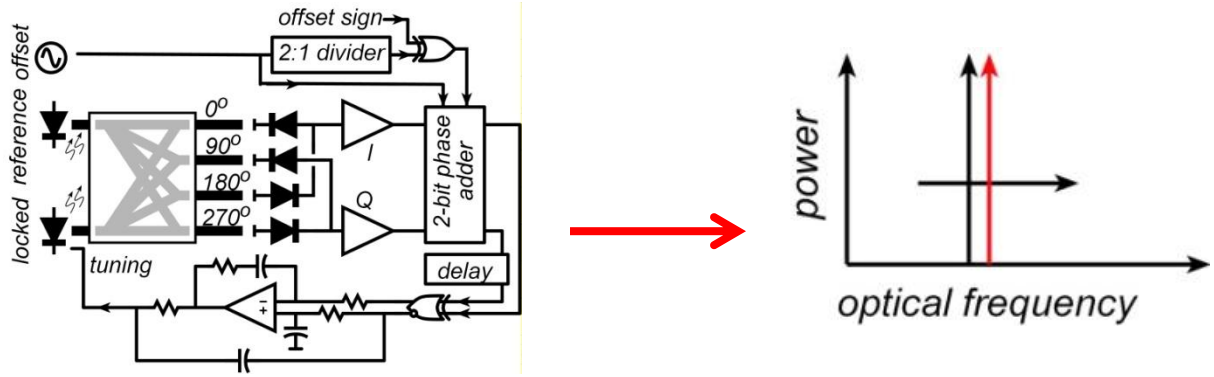
WDM: electronic channel selection.





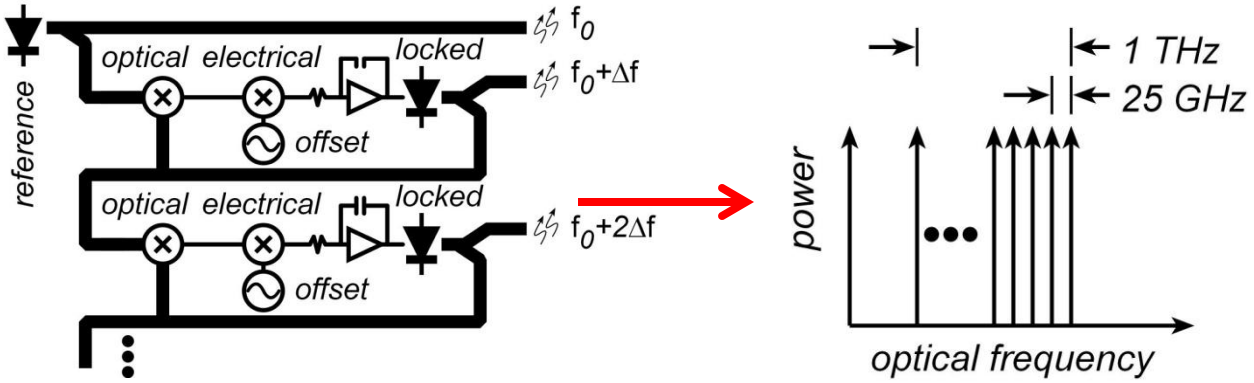
Optical Phase-Locked-Loops: Applications

Wavelength synthesis, & sweeping → digital control of wavelength spacings.



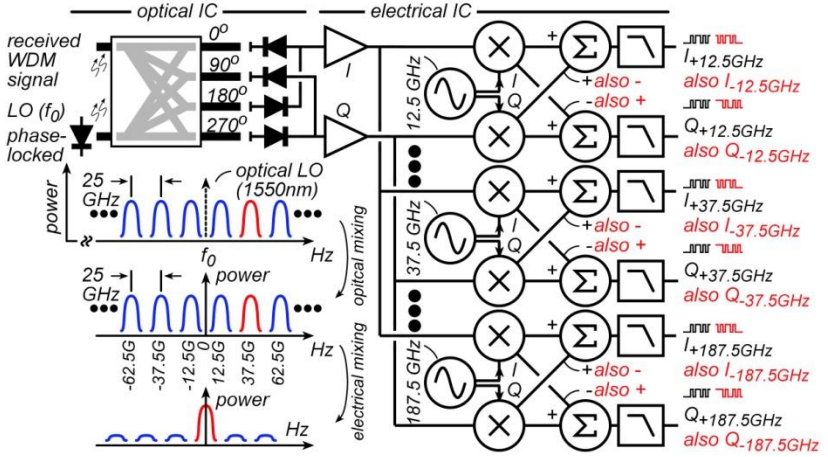
Synthesis, Sweeping of Wavelength Combs

WDM: precise channel spacing, no guard bands.

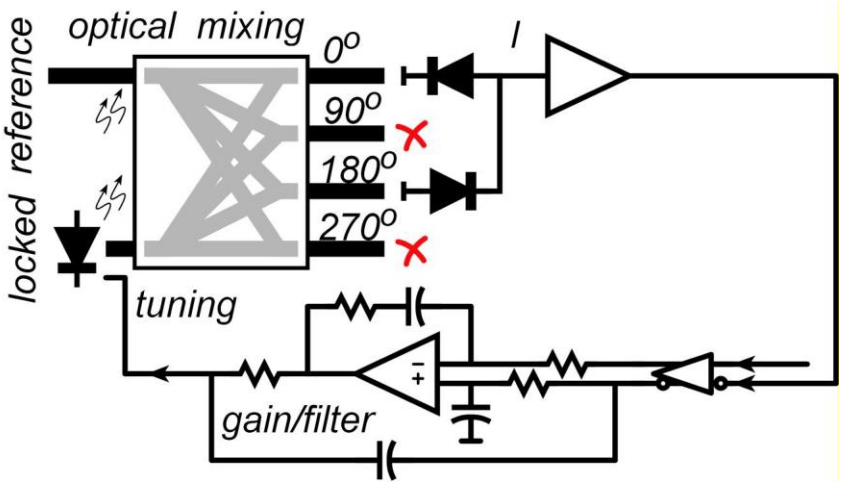


Single-Chip Multi-Wavelength Coherent Receivers

WDM



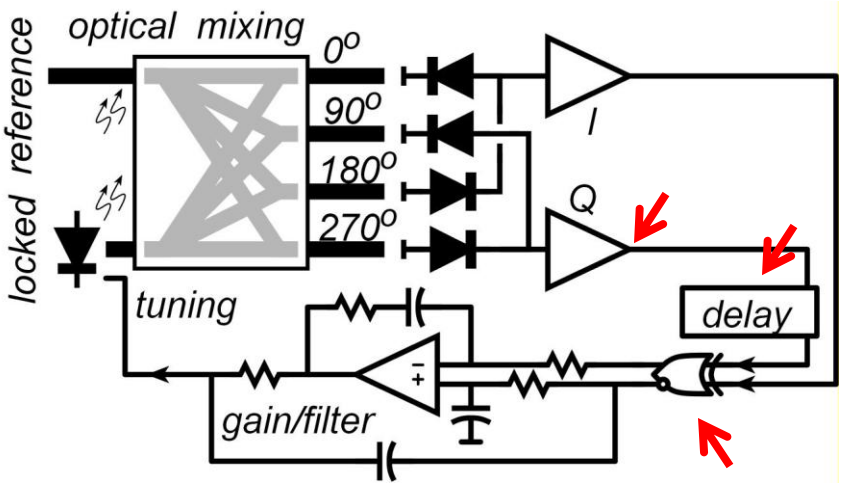
Optical PLLs: Basics



Phase-lock tunable laser to optical reference
Lock to one line + improve linewidth / SNR

Inexpensive laser with no external cavity ?
- → ***large laser linewidth***
- → ***1GHz loop bandwidth for noise suppression***
- → ***tight optical/electrical integration***

Optical PLLs: Frequency-Difference-Detector



~ 1 GHz loop bandwidth

~20 GHz initial frequency error

→ loop will not acquire lock

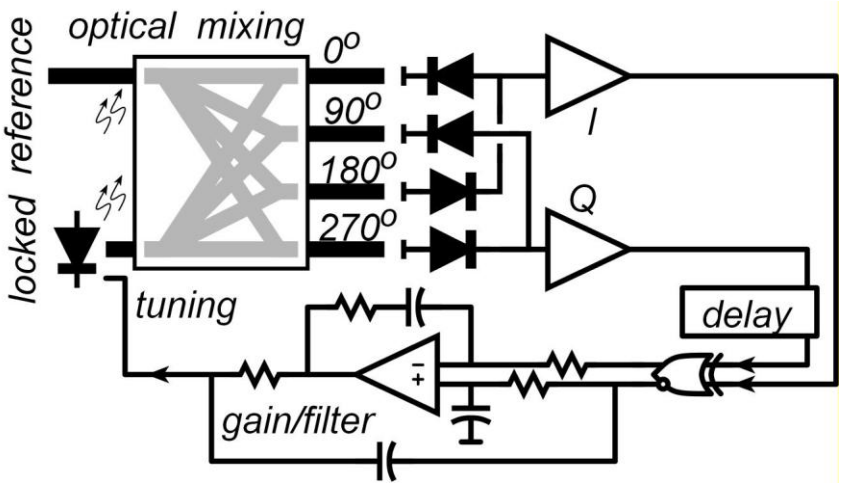
→Add frequency-difference detector

Requires I/Q (0°,90°) optical mixing

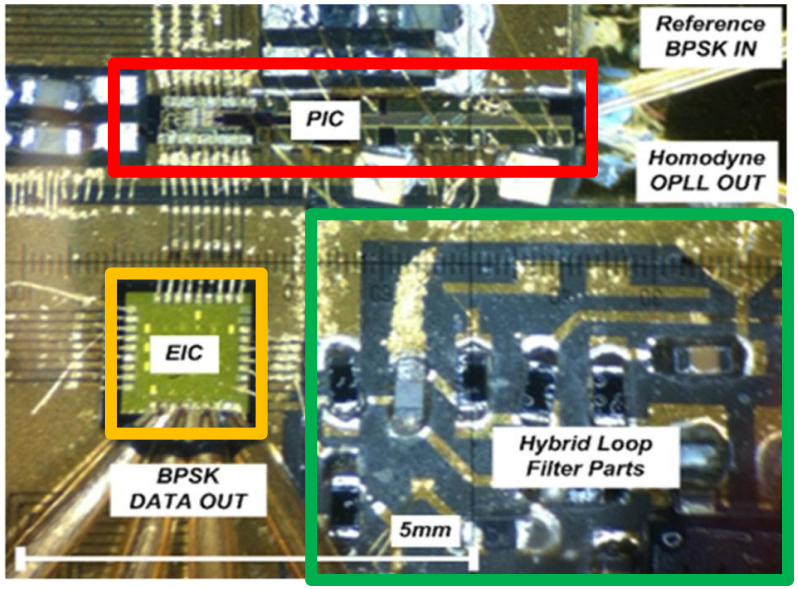
Full information of optical field is maintained

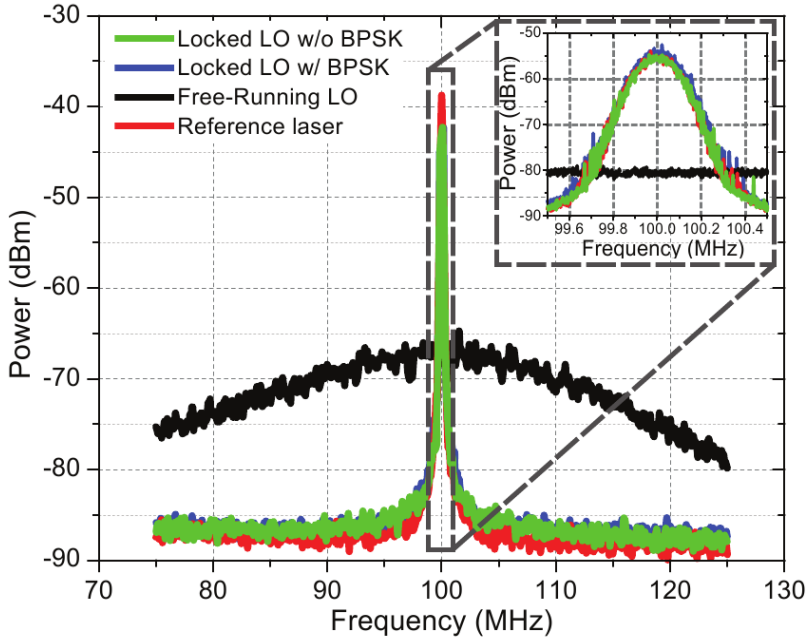
→ use later for other purposes

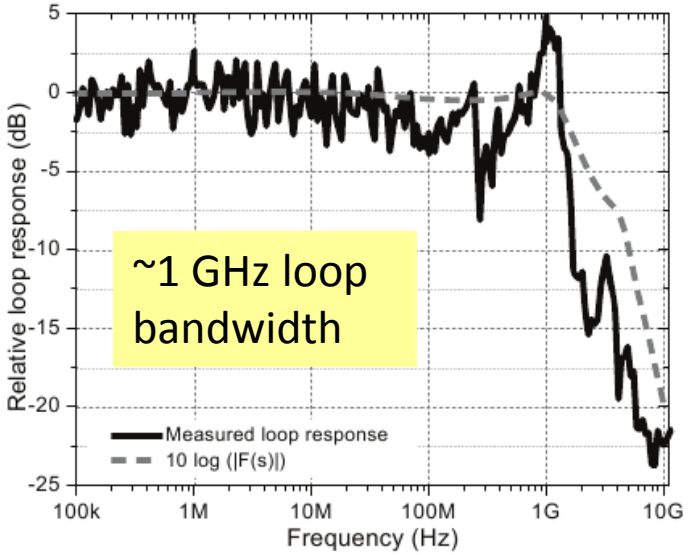
Optical PLLs: Demonstrated



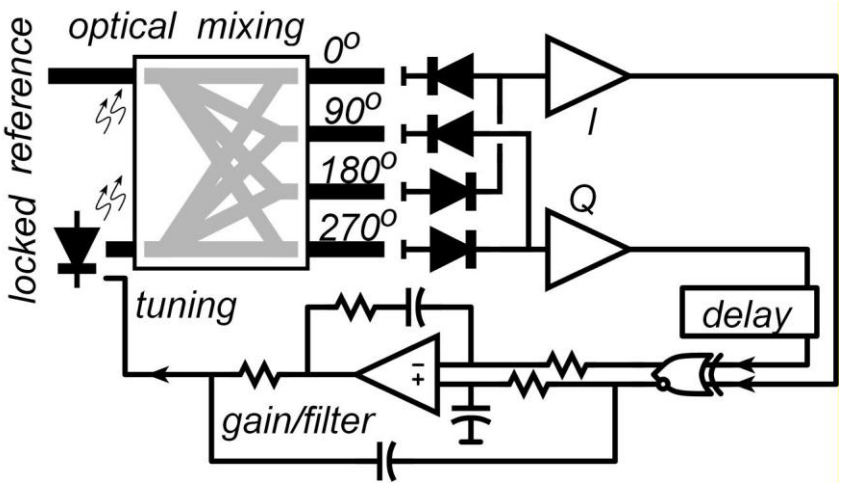
H. Park, M. Lu, et al, ECOC'12, Th3A.2 (2012)

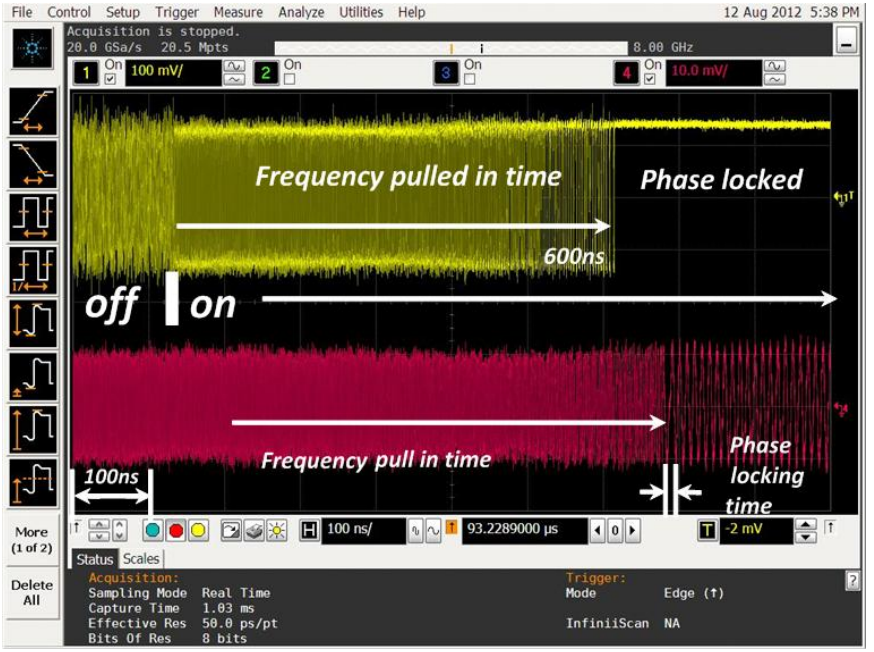






Optical PLLs: Frequency Acquisition





H. Park, M. Lu, et al, ECOC'12, Th3A.2 (2012)

High carrier frequency (200 THz) but limited OPLL bandwidth (1.1 GHz)

- ***Slow frequency capture outside OPLL bandwidth***
- ***Need Optical Frequency Phase Lock Loop***

Phase-Frequency Locking Demonstrated→ 50 GHz pull-in range

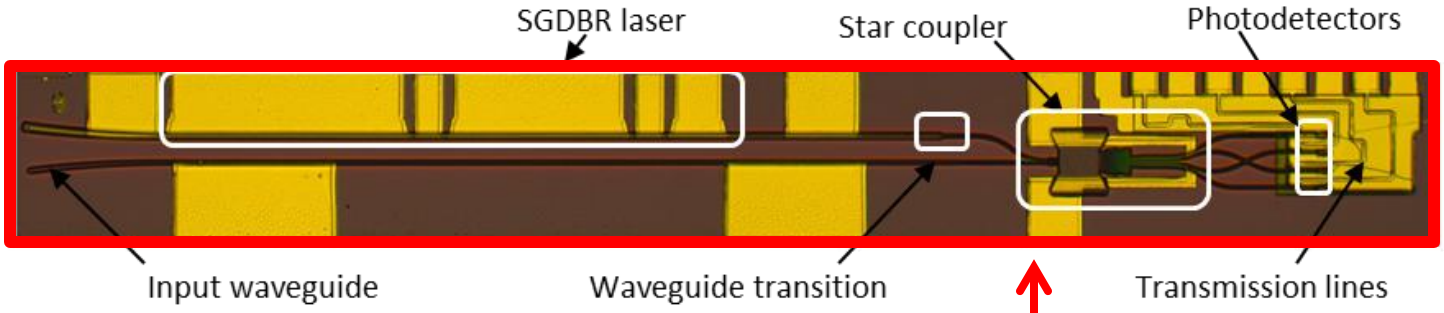
- ***600ns frequency pull-in time***
- ***<10 ns optical phase lock time***

OPLL Components

Photonic IC

Coldren group

InP integration

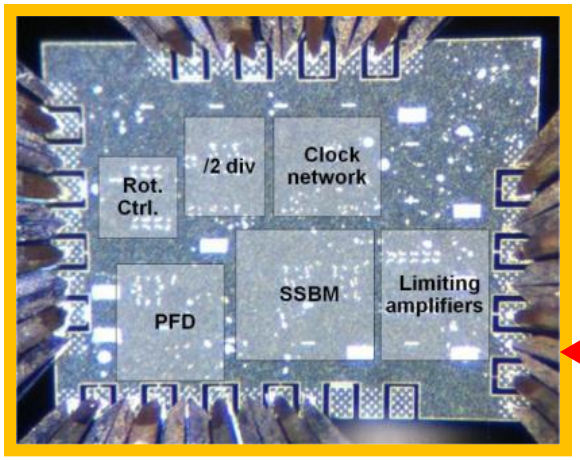


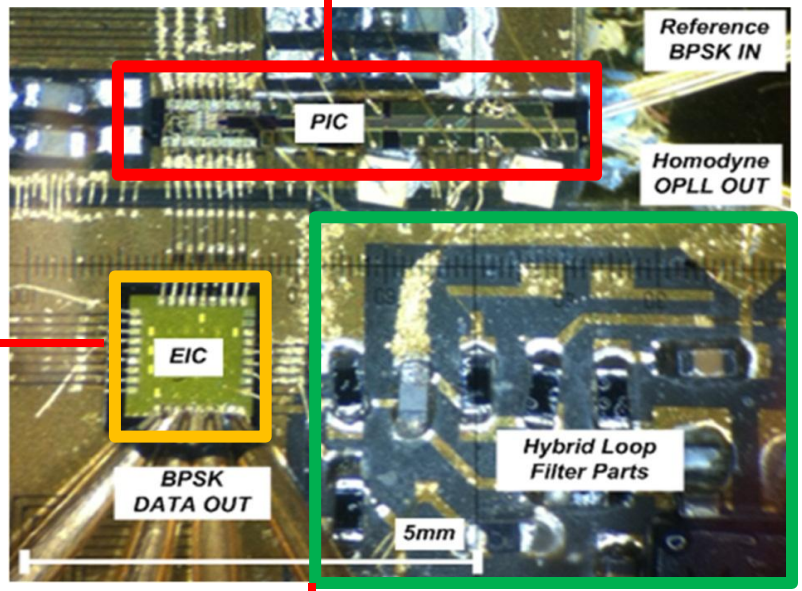
Fast electrical IC

Design: Rodwell group

Fab: Teledyne InP HBT

details to follow



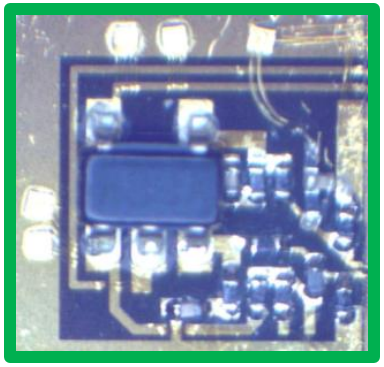


Hybrid loop filter

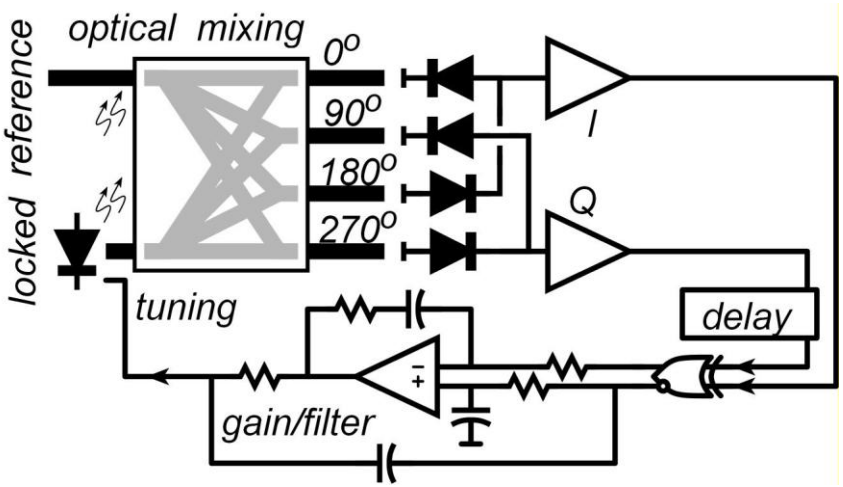
slow/fast design

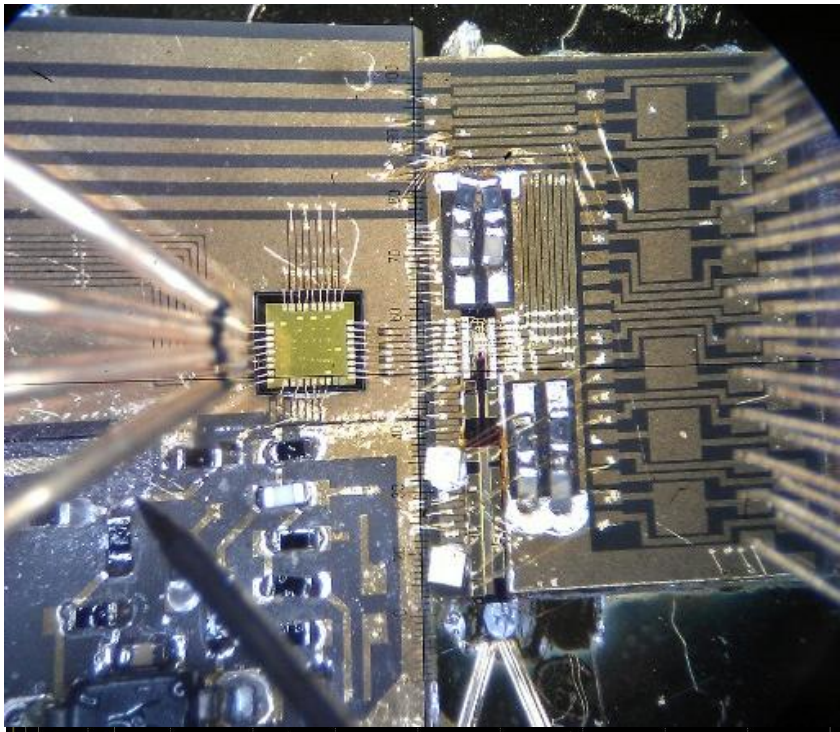
slow: op-amp integrator

fast: passive feedforward

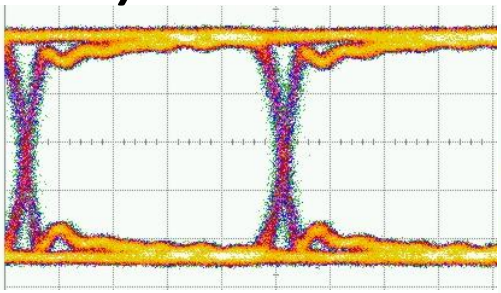


Optical PLLs: Phase-Locked BPSK Receiver

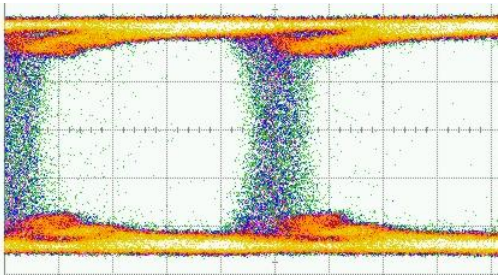




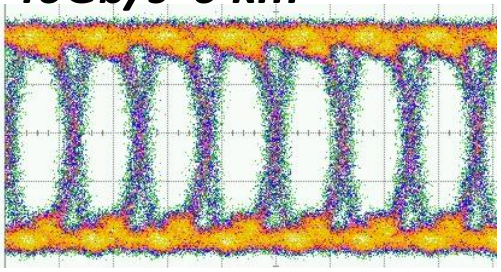
10Gb/s 0 km



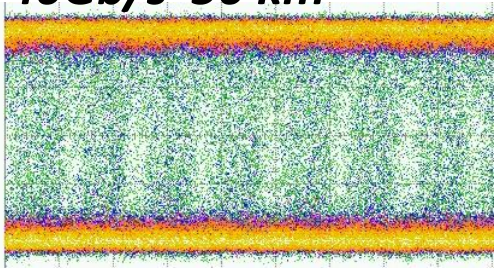
10Gb/s 75 km

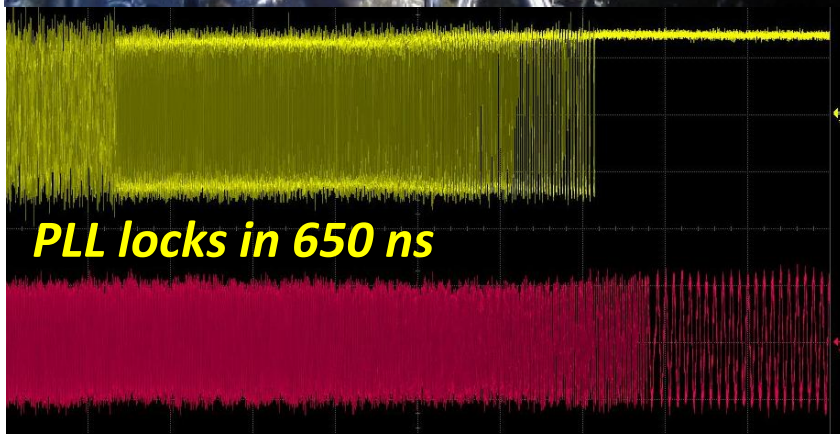


40Gb/s 0 km



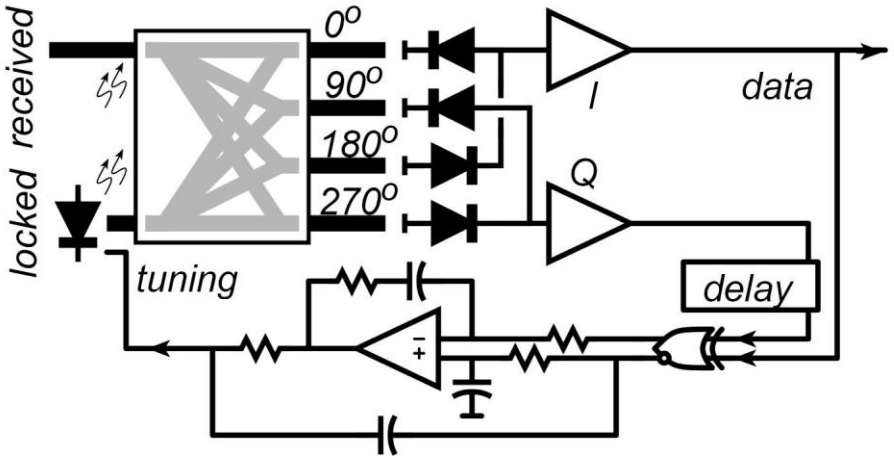
40Gb/s 50 km

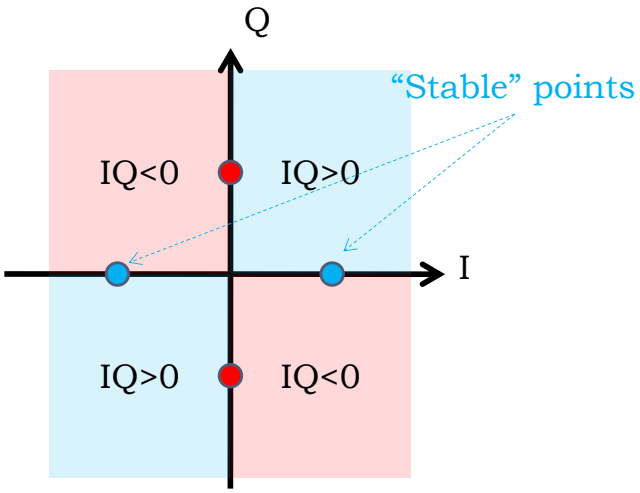




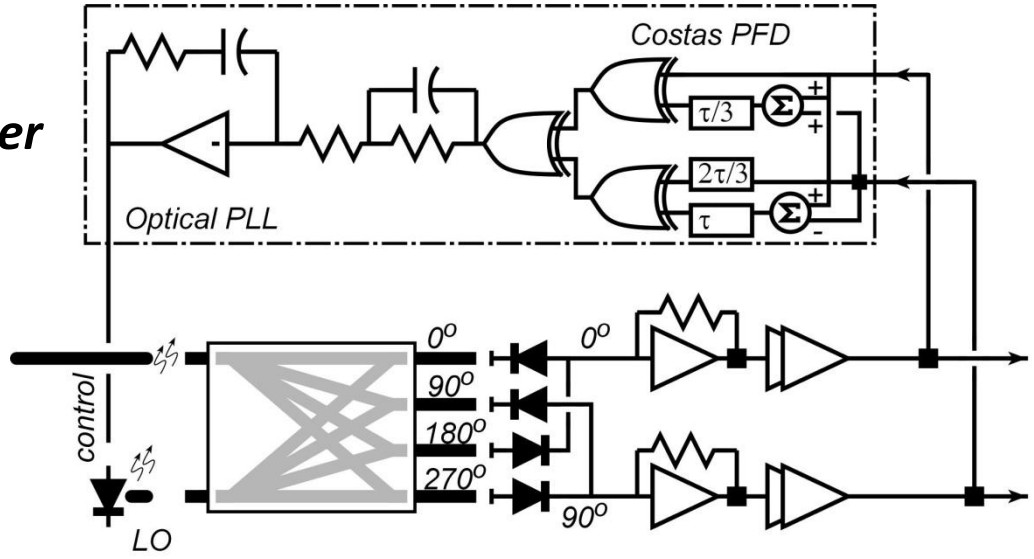
Optical PLLs: Phase-Locked QPSK Receiver

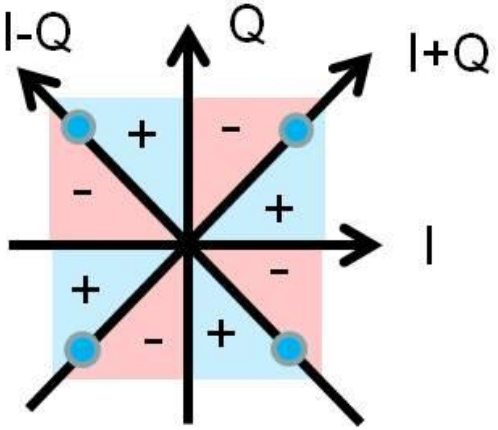
BPSK receiver





QPSK receiver

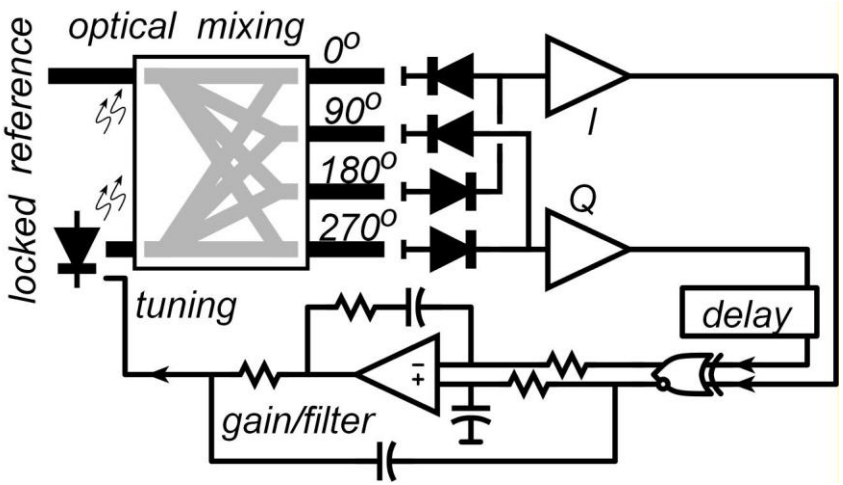


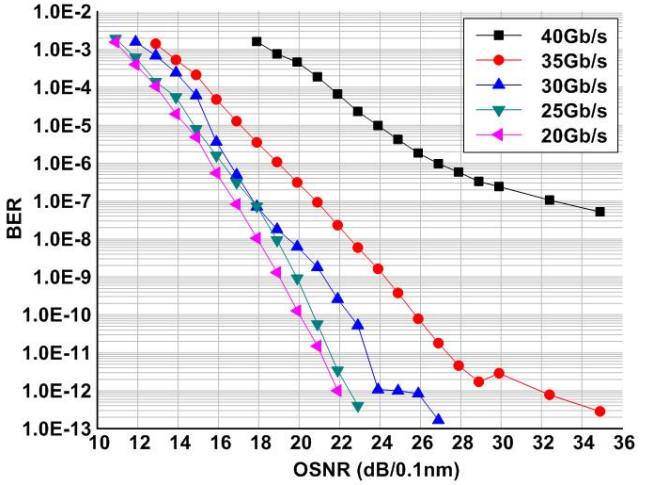


Designs attempted, ICs did not work properly

simply a design failure, should work just fine...

Phase-Locked **B/Q**PSK Receivers: Good and Bad





Present coherent receivers: DSP coherent detection

DSP compensates dispersion

DSP compensates LO phase & frequency errors.

sophisticated, high DC power, expensive

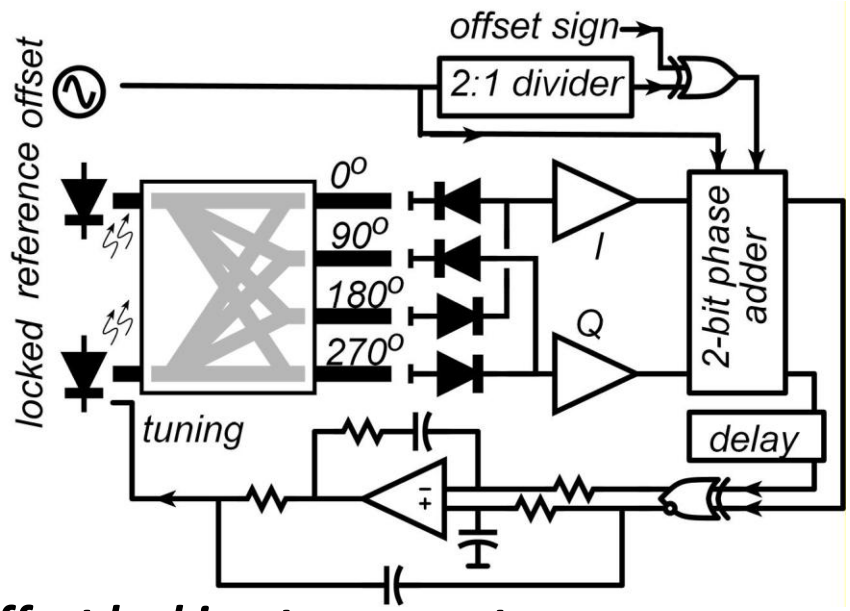
Phase-locked receivers in short-range links 

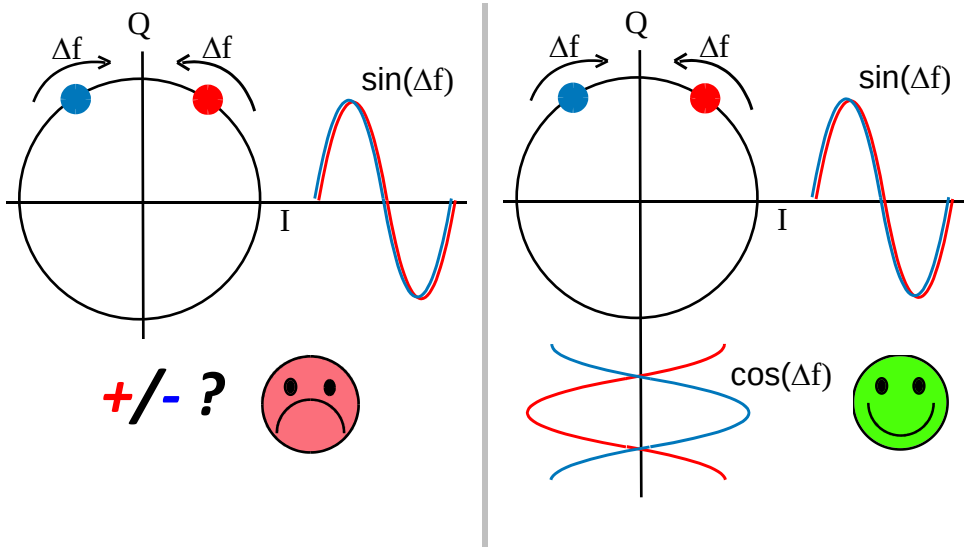
No DSP required ! → reduced cost, reduced DC power

Phase-locked receivers in long-range links 

fiber dispersion will close eye→ optical PLL will not lock

Offset Locking → Wavelength Synthesis





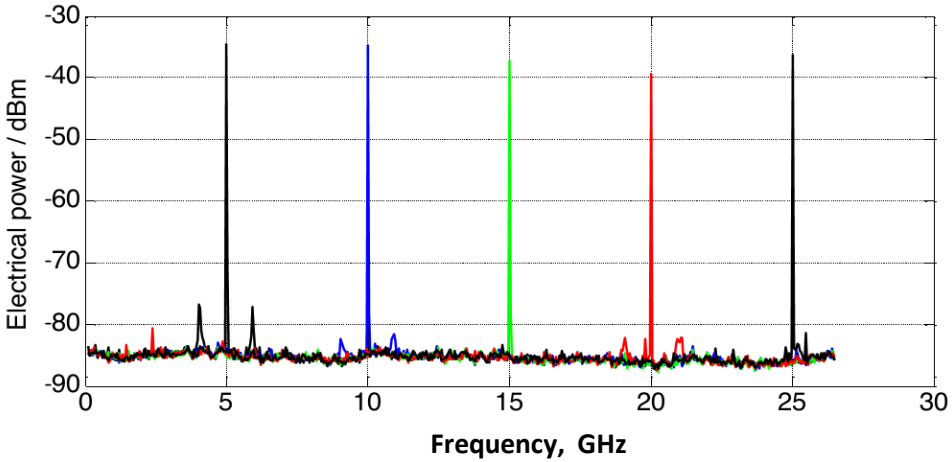
Offset locking to generate any optical frequency

Simple OPLL cannot distinguish +/- frequency offsets

(0°/90°) optical mixing:
no lost optical information
IC digital single-sideband mixing

300+ GHz offsets possible
fast UTC photodiodes, fast electronics

Mingzhi Lu, et. al, – Tu2H.4, OFC2014



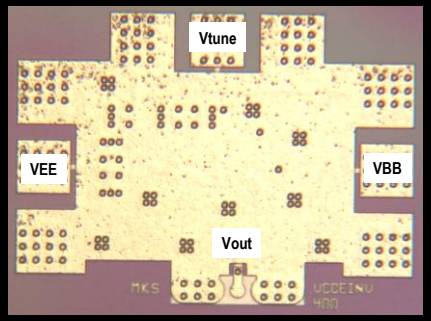
ICs Today: 670 GHz is done, 200 GHz is easy

TELEDYNE SCIENTIFIC COMPANY
A Teledyne Technologies Company

UCSB

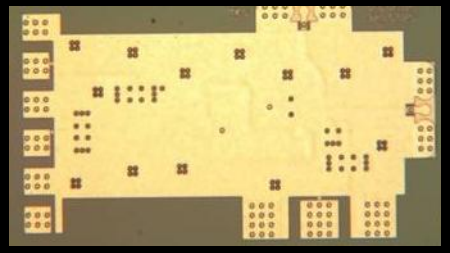
614 GHz fundamental VCO

M. Seo, TSC / UCSB



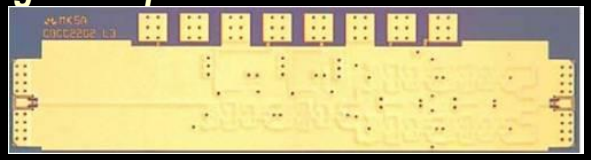
340 GHz dynamic frequency divider

M. Seo, UCSB/TSC
IMS 2010



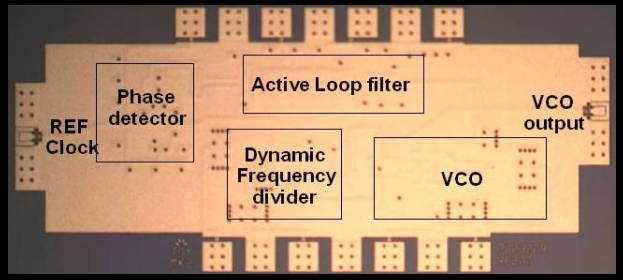
620 GHz, 20 dB gain amplifier

M Seo, TSC
IMS 2013



300 GHz fundamental PLL

M. Seo, TSC
IMS 2011

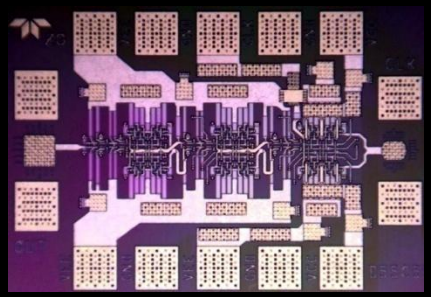


Not shown: 670 GHz HBT amplifier

J. Hacker, TSC, IMS 2013

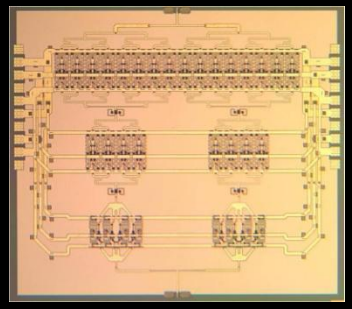
204 GHz static frequency divider (ECL master-slave latch)

Z. Griffith, TSC
CSIC 2010



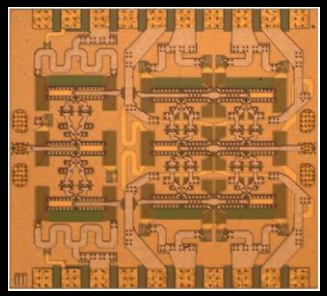
220 GHz 180 mW power amplifier

T. Reed, UCSB
CSICS 2013



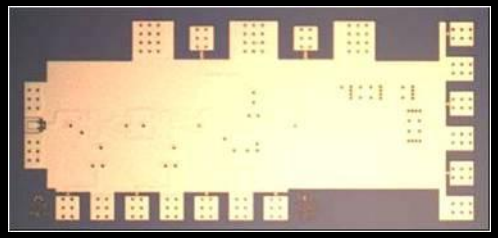
81 GHz 470 mW power amplifier

H-C Park UCSB
IMS 2014



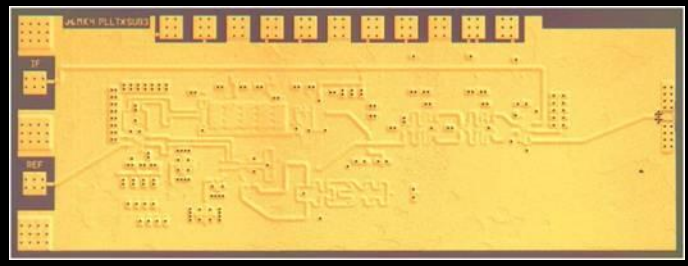
Integrated 300/350GHz Receivers:

LNA/Mixer/VCO
M. Seo TSC

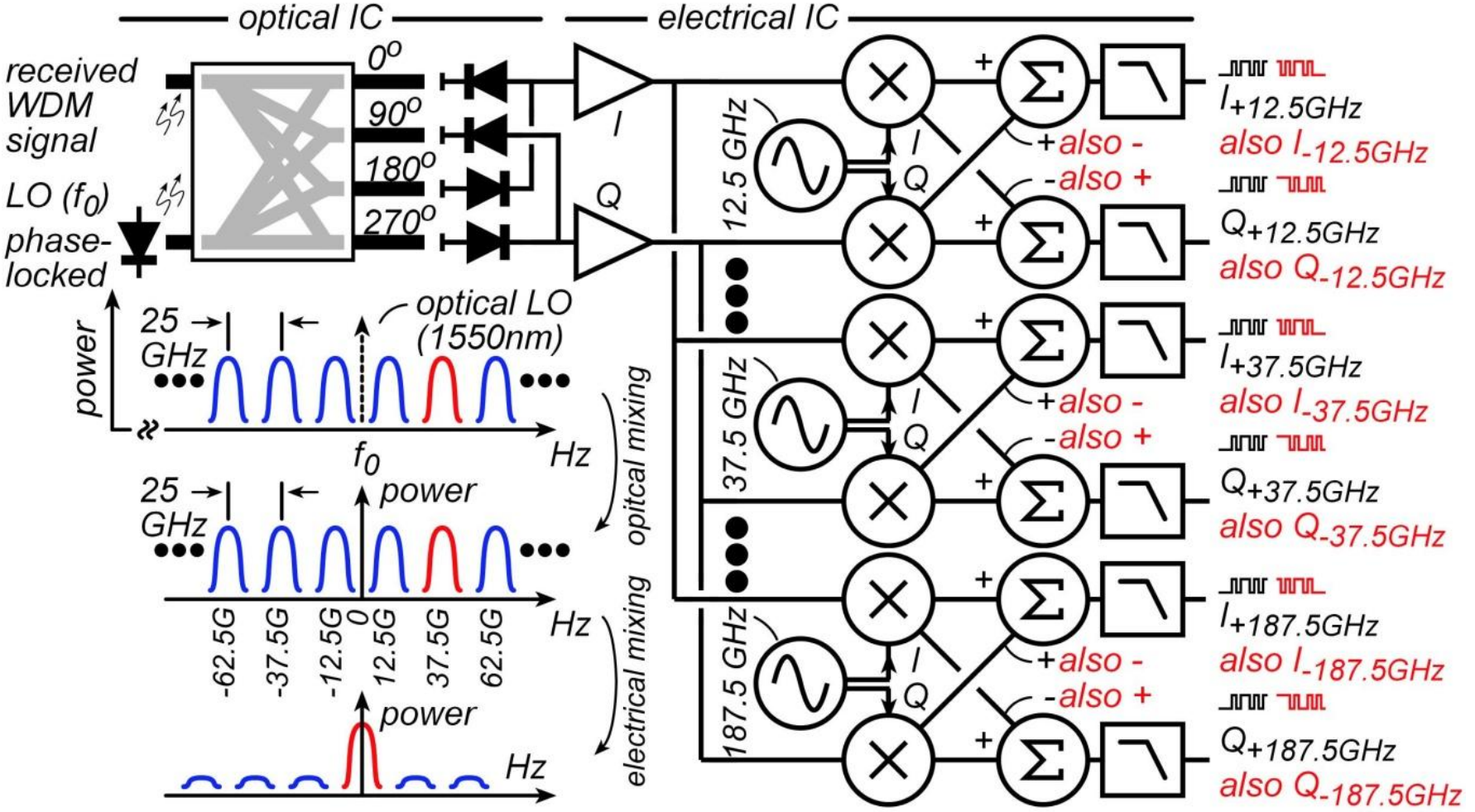


600 GHz Integrated Transmitter

PLL + Mixer
M. Seo TSC



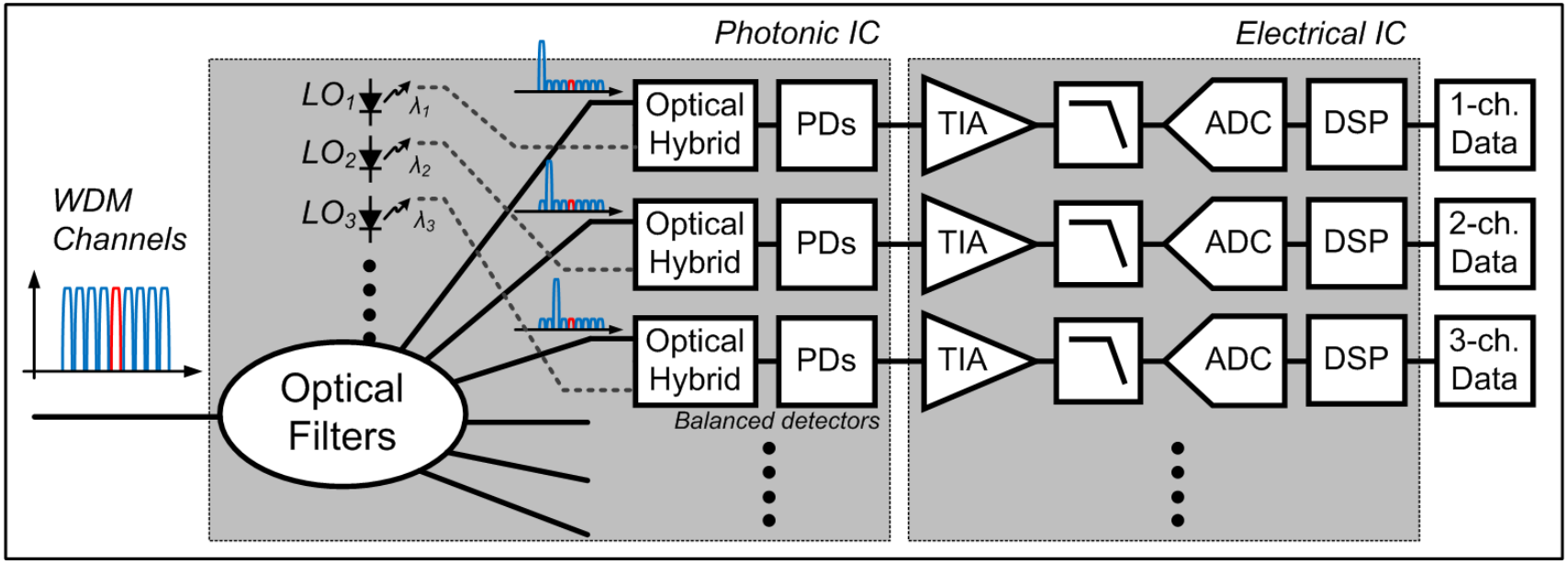
Electrical Recovery of **WDM** for compact Tb/s Links



Assume: *25GHz channel spacing, DC-200 GHz ICs , DC-200 GHz photodiodes*
→ ***800 Gb/s receiver****= 50 Gb/s QPSK x 16 WDM channels*
*...**one** LO laser, **one** I/Q optical detector, **one** electrical receiver IC*

OPLL can lock to optical pilot → works even with highly dispersive channels

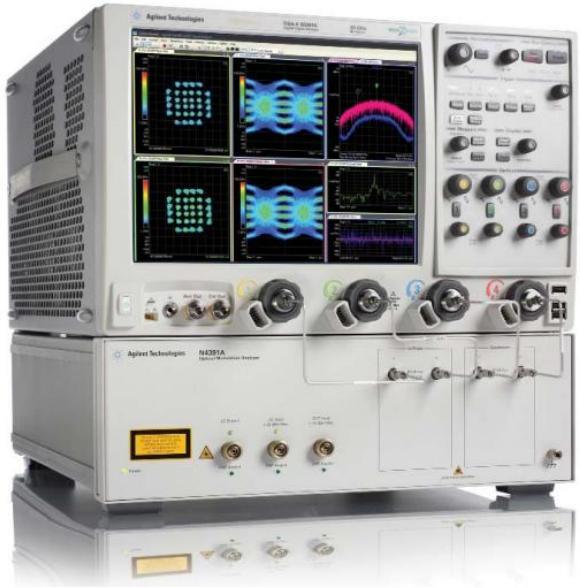
Optical-Domain WDM Receiver



Complex photonic IC.

One electrical receiver IC for each wavelength→ many in total.

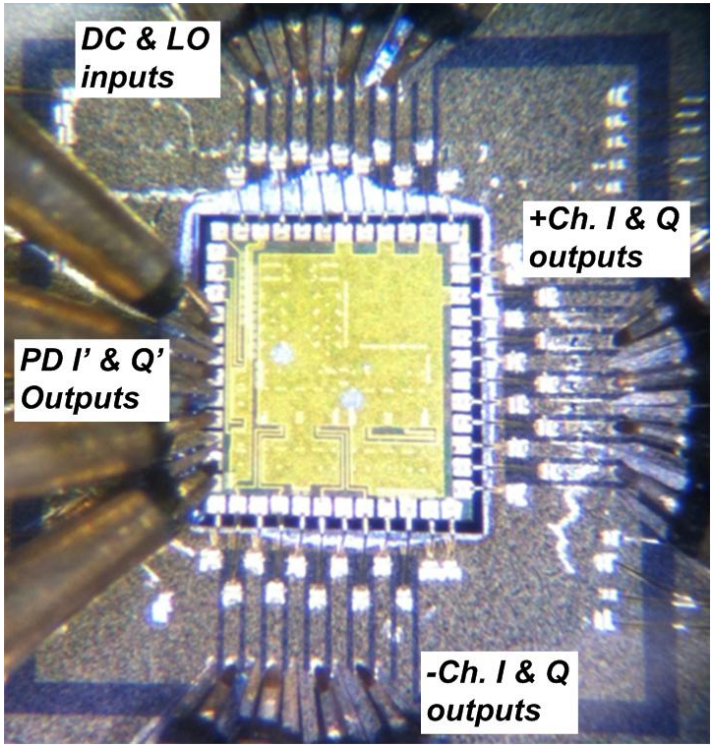
Electrical WDM: 2-Channel Demonstration



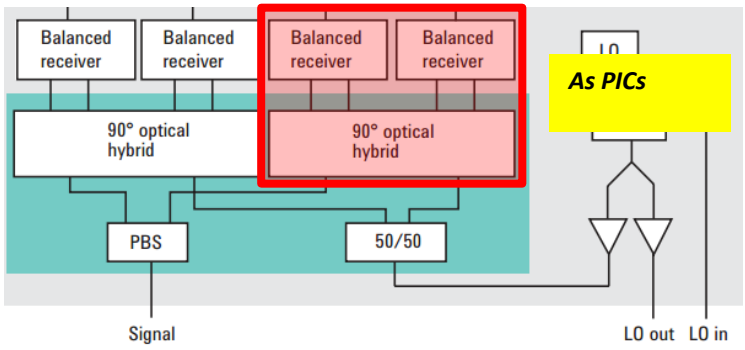
Real-time oscilloscope

OMA as PICs*
Free space optics
90° optical hybrid
& Balanced PDs

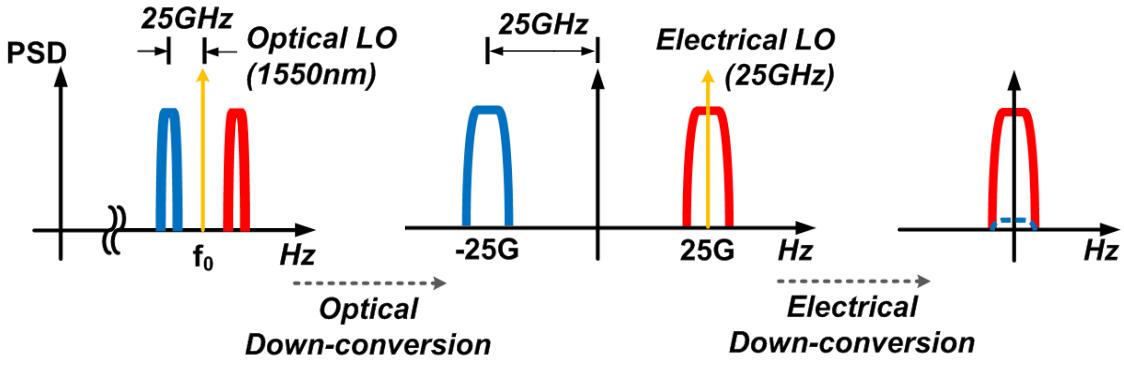
OMA blocks*



2-channel electrical IC

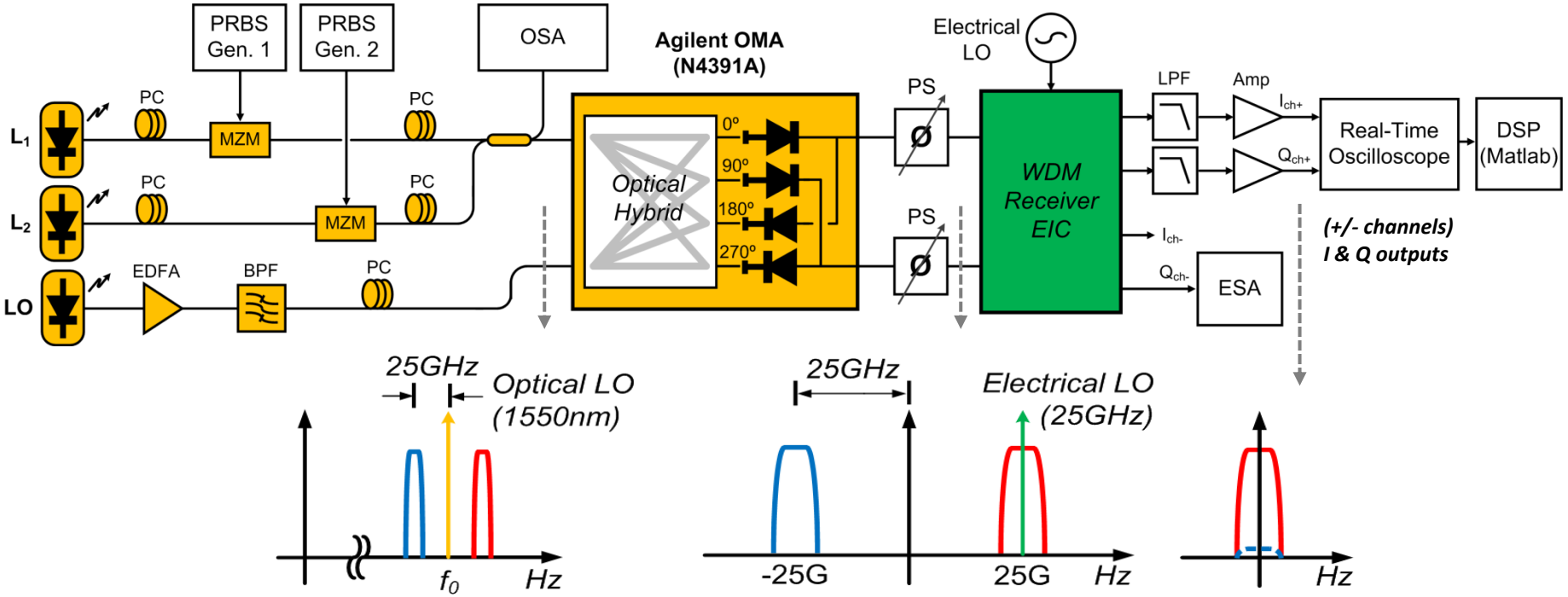


ure 30. Block diagram of the optical modulation analyzer.

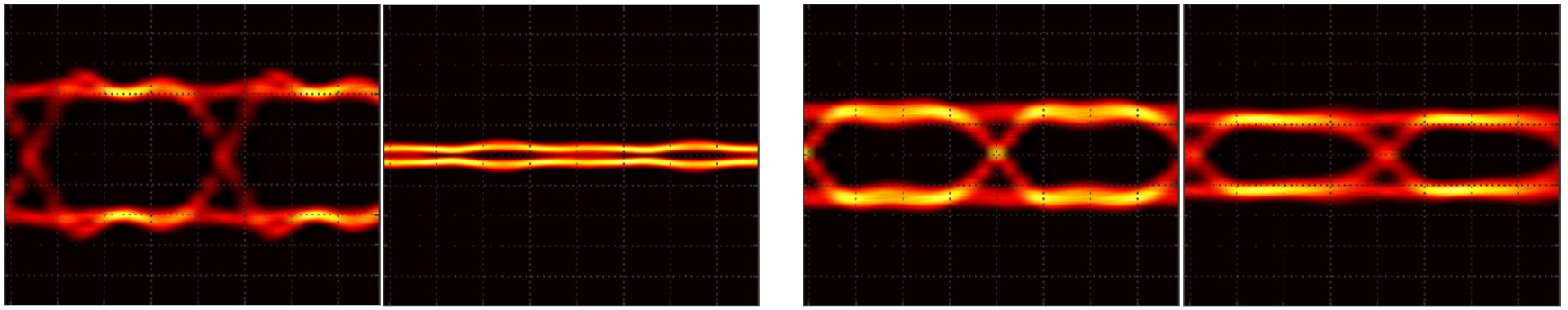


**OMA – optical modulation analyzer*
Agilent N4391A

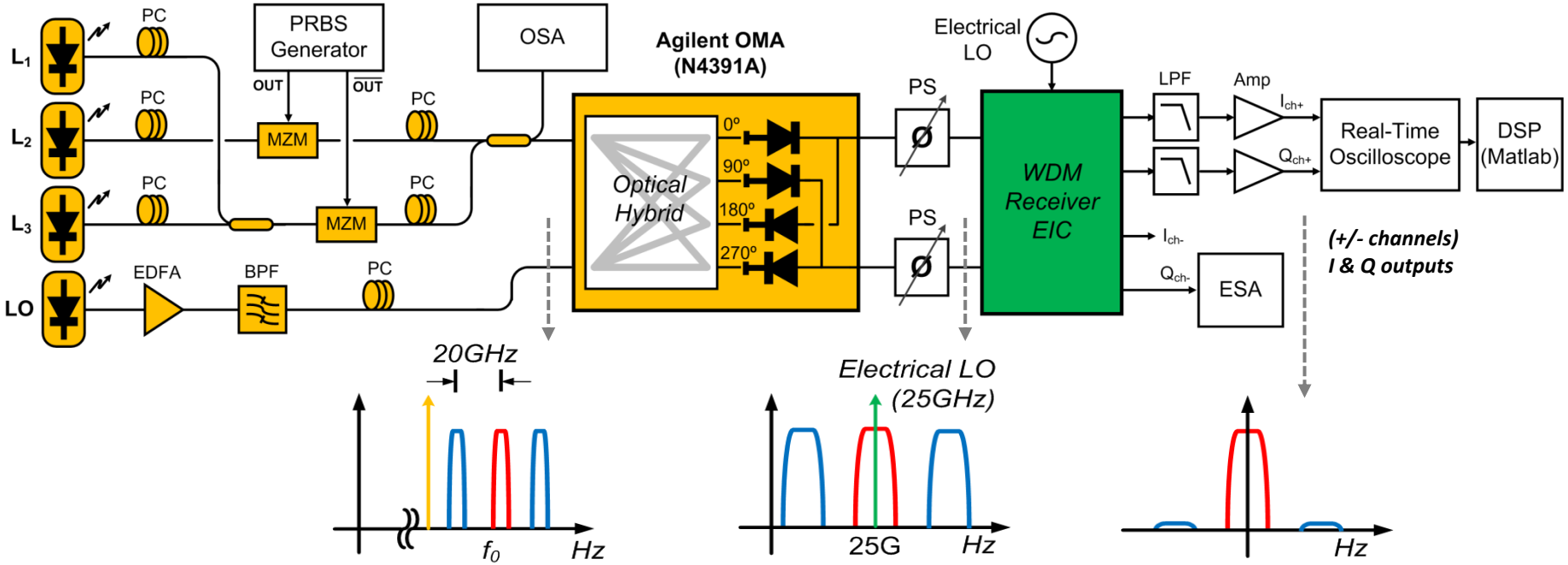
2-channel Tests: Opposite-sideband Suppression



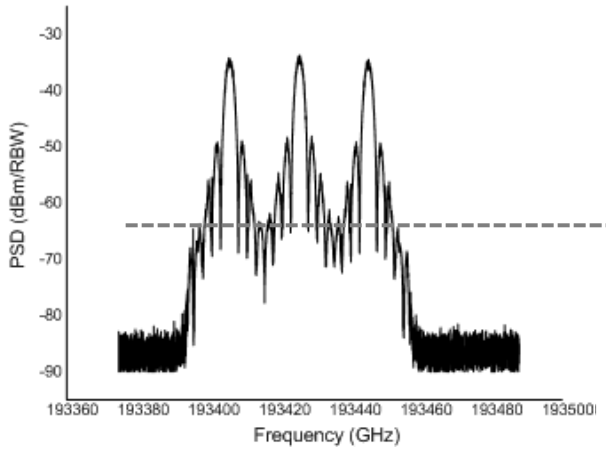
Activated channel *Suppressed channel* *(+) channel* *(-) channel*



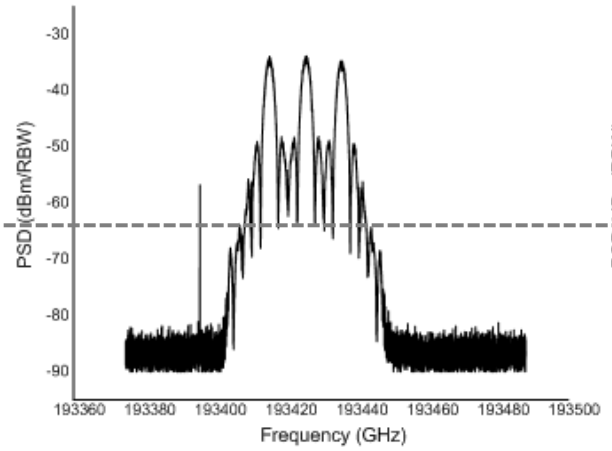
3-channel Test: Adjacent Channel Rejection



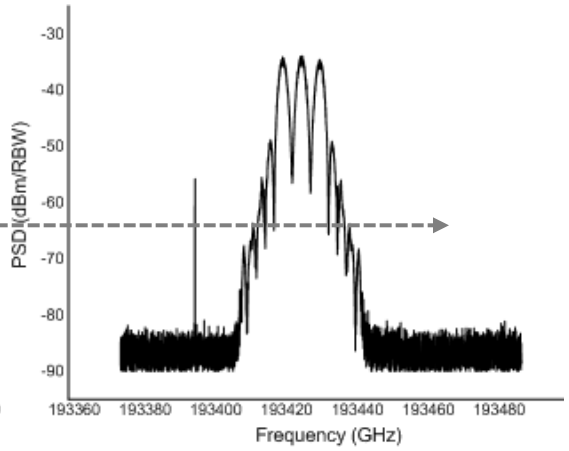
20GHz Spacing



10GHz Spacing



5GHz Spacing (2.5Gb/s BPSK)

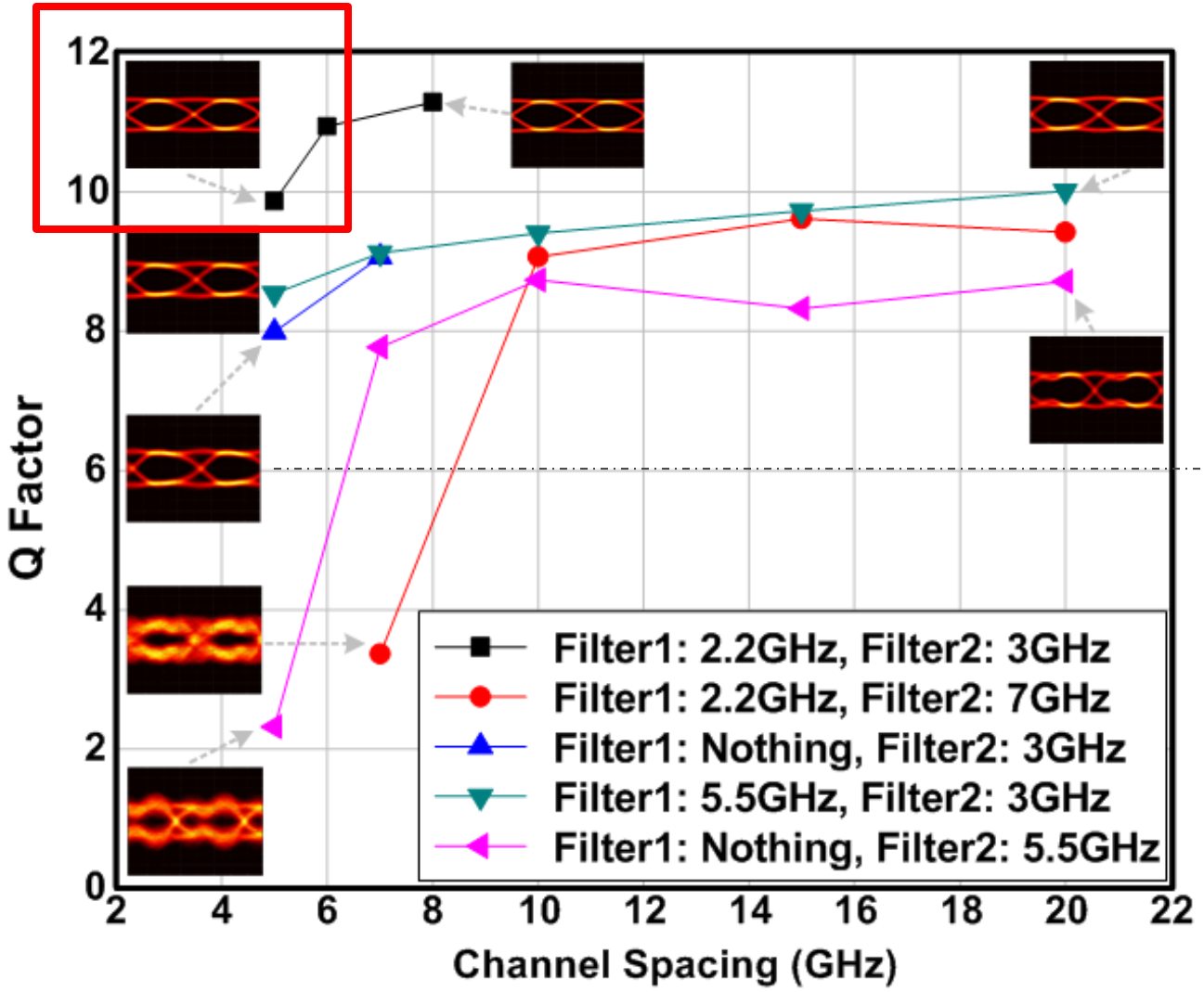


**spectra measured using optical spectrum analyzer*

Tested with various channel spacings

3-channel Test: Adjacent Channel Rejection

Eye Quality with Different Transmitter/receiver filter bandwidths



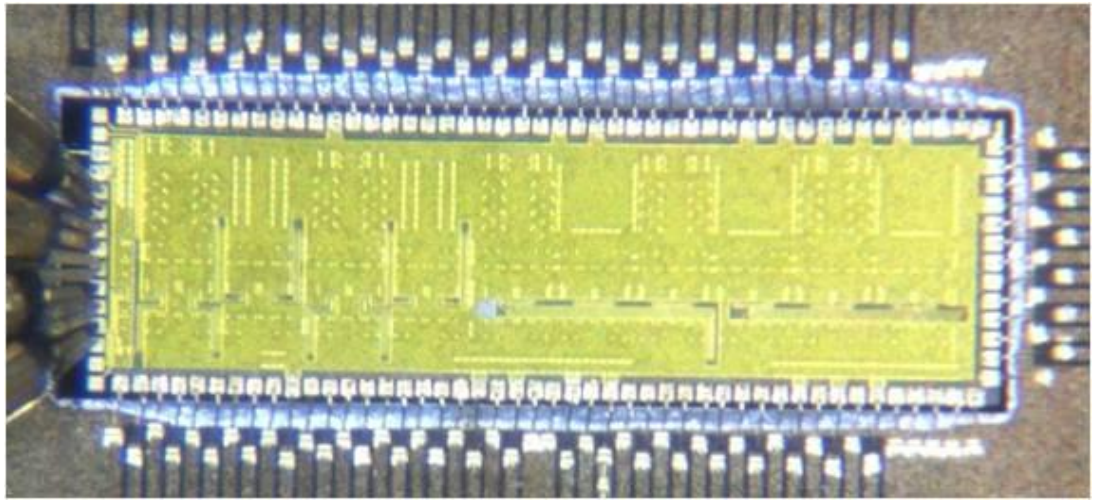
*Filter1: transmitter
*Filter2: receiver

2.5 Gb/s BPSK per channel, 5 GHz channel spacing→ minimal interchannel interference

6-channel WDM Receiver Design

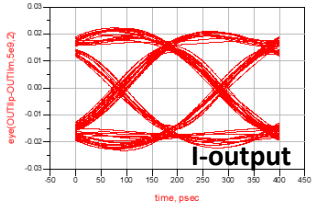
Teledyne 500nm InP HBT (350GHz f_τ, f_{max})

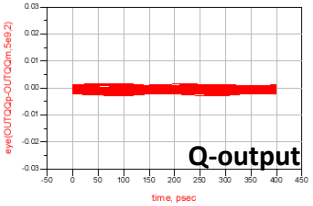
6 channels: +/- 12.5, 37.5, 62.5 GHz



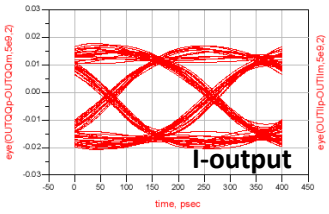
Simulations look fine...

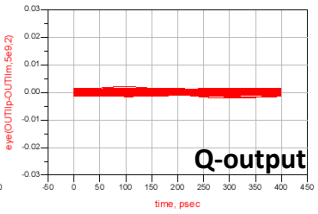
±12.5GHz



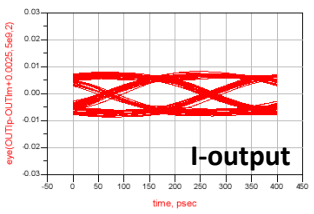


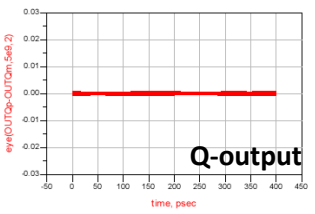
±37.5GHz





±62.5GHz





But problems:

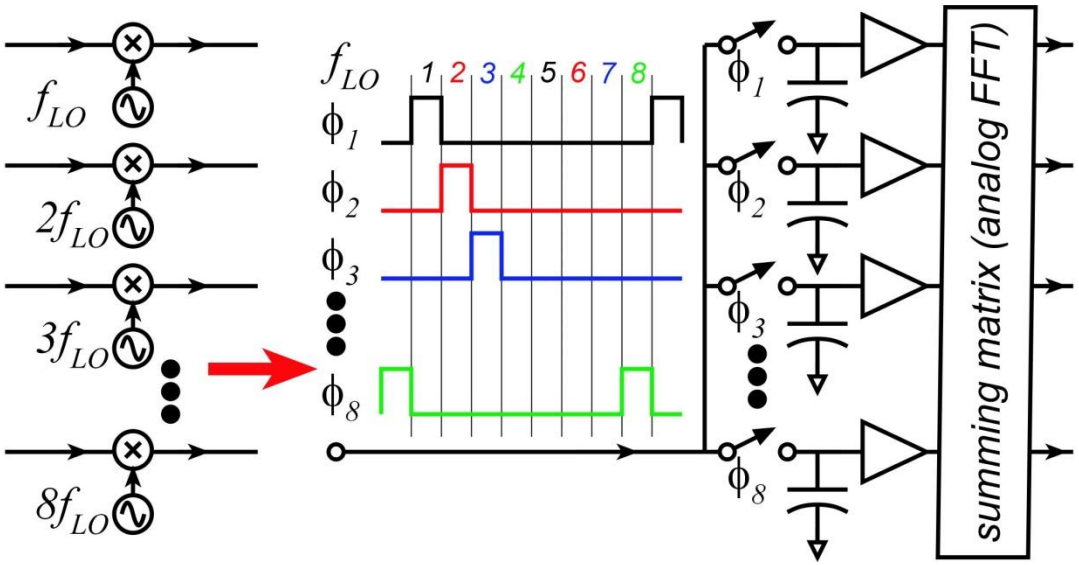
(1) very high DC power consumption (>10W)

(2) low IC yield...all ICs have at least one broken receive channel

Next steps ?

Electrical-Domain WDM Receiver: Reducing Power

Replace mixer array with analog FFT

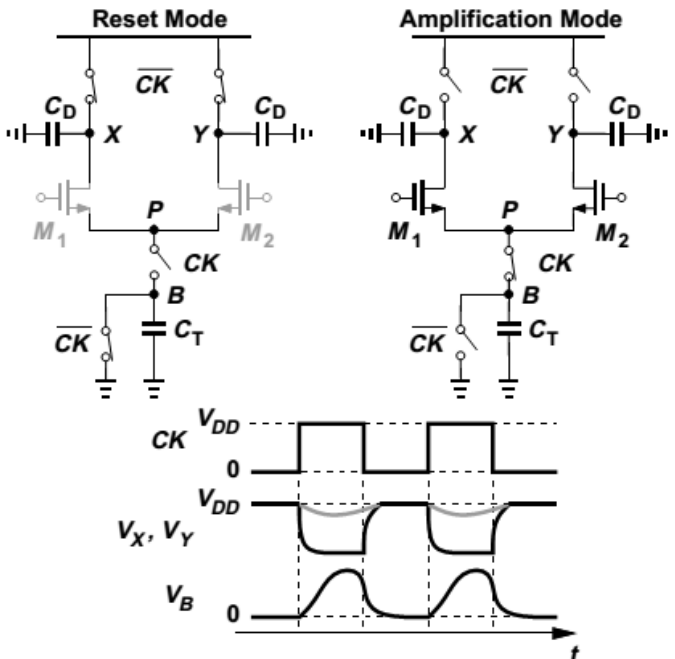


Use charge-domain CMOS logic

Razavi, IEEE Custom IC Conference, Sept. 2013.

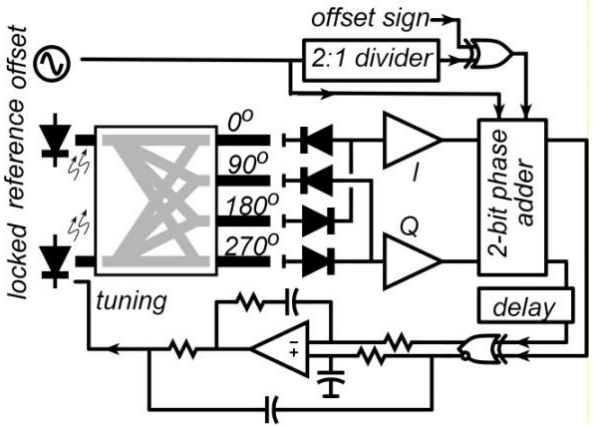
"Employing charge steering in 65-nm CMOS technology, a 25-Gb/s CDR/deserializer consumes 5 mW"

→0.2 pJ/bit

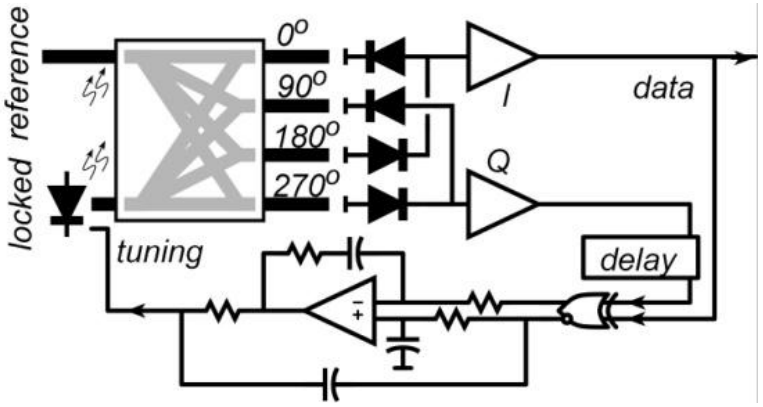


Optical Phase-Locked-Loops: Applications

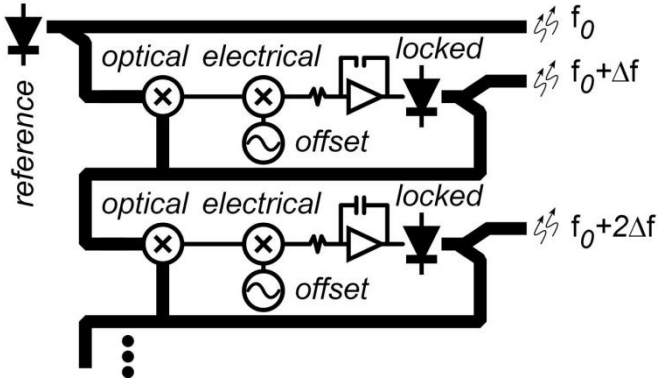
Wavelength synthesis



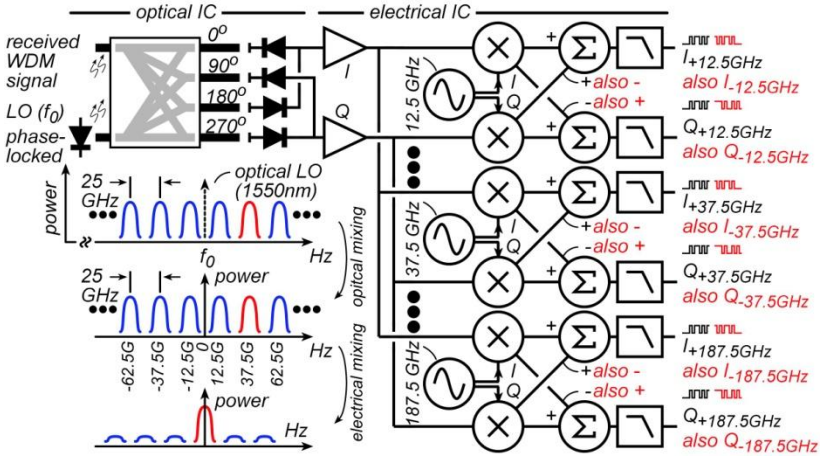
Phase-locked coherent receivers



Zero-guardband WDM generation



Single-chip Electrical WDM receivers



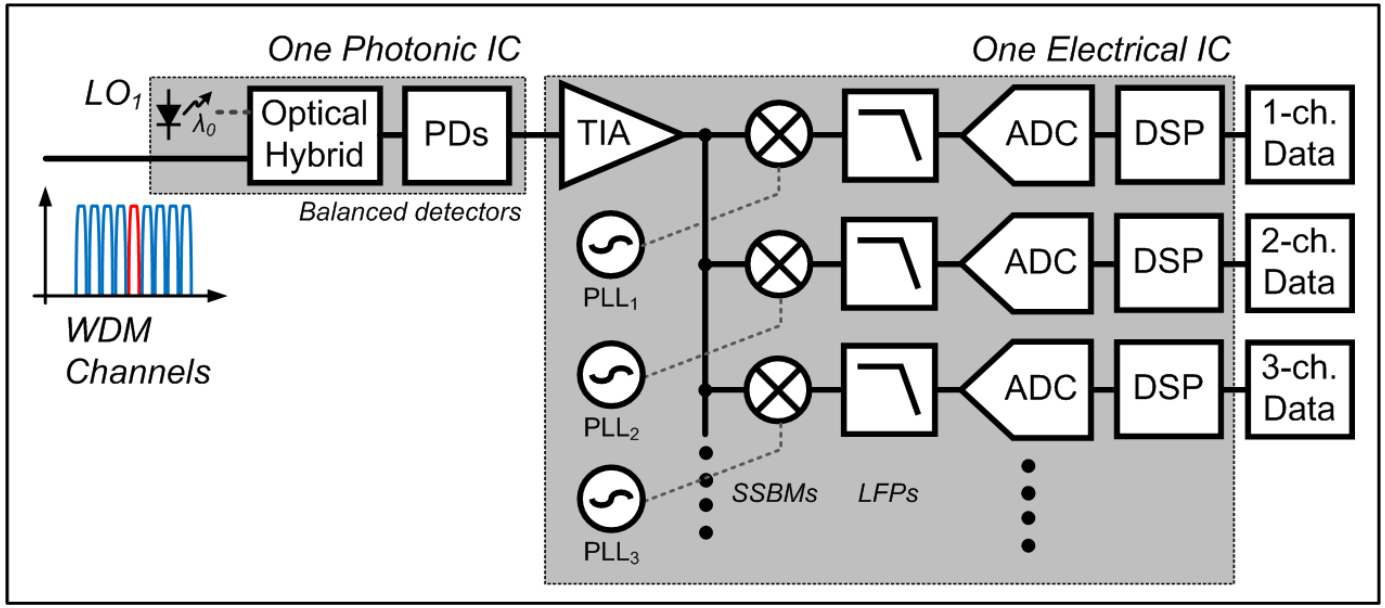
Electronic polarization DMUX ?

Analog polarization compensation ?

(end)

Backups

Electrical-Domain WDM Receiver



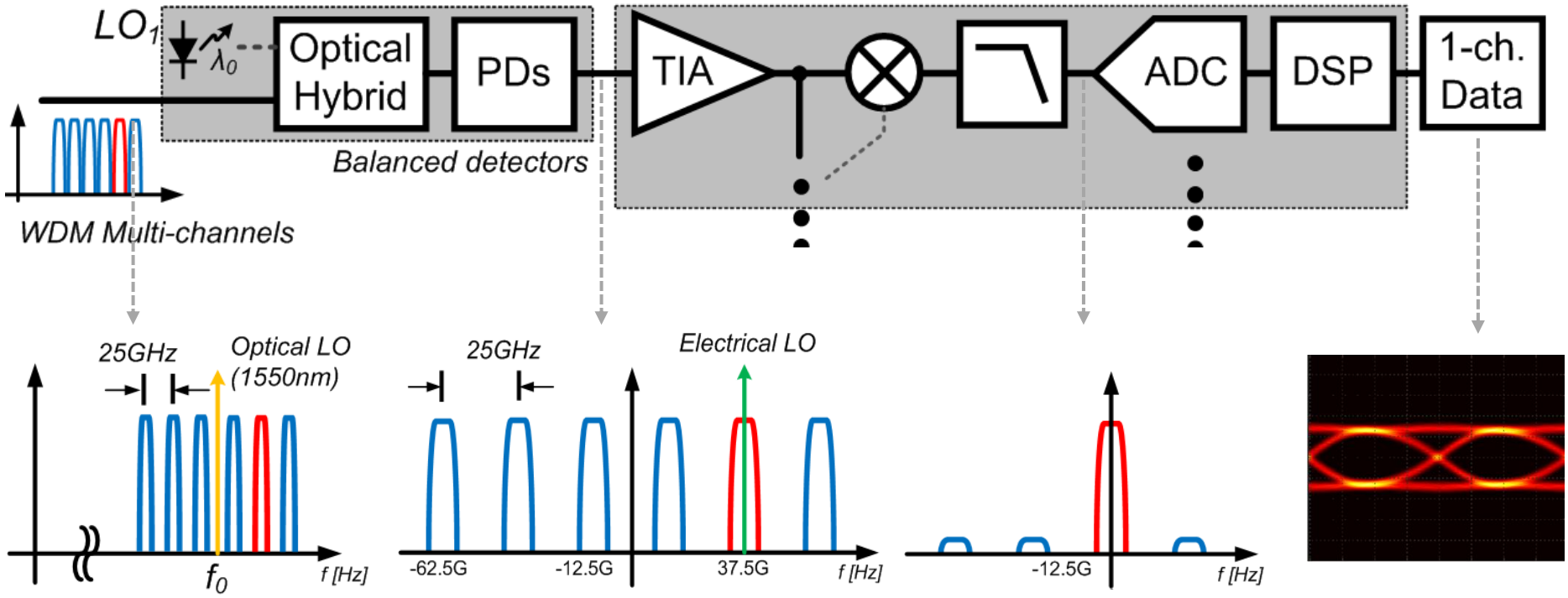
Small and simple photonic IC.

One electrical receiver IC covers all wavelengths.

IC might be complex;

can we design it for low power & low complexity ?

2-Stage Down-Conversion: Optical, Electrical



Phase-locked LO down-converts all WDM channels to RF @ 25 GHz spacing

Electrical receiver down-converts each channel separately to baseband

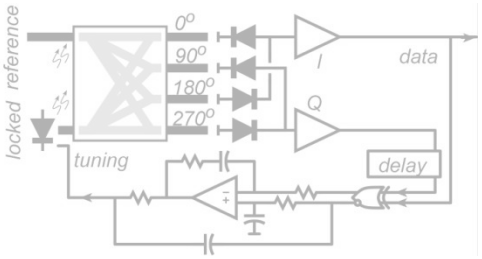
Note: OPLL can lock to narrow-spaced optical pilot tone

→ phase-locked receiver even with highly dispersive channels

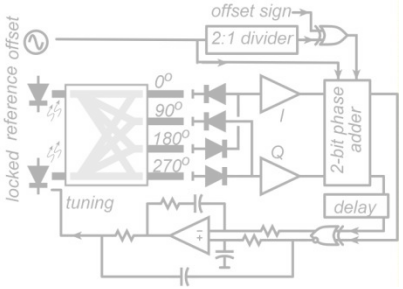
Low-Voltage Electrical Signalling

Fast, Low-Power Interconnects for Digital Systems

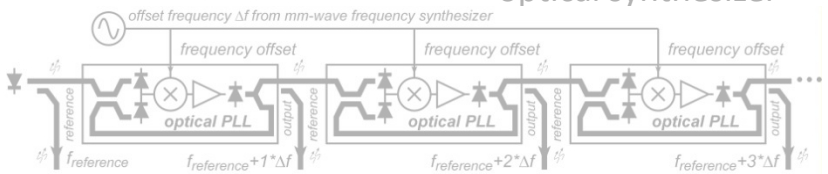
Optical PLLs ? → mid-range coherent links for data centers ?



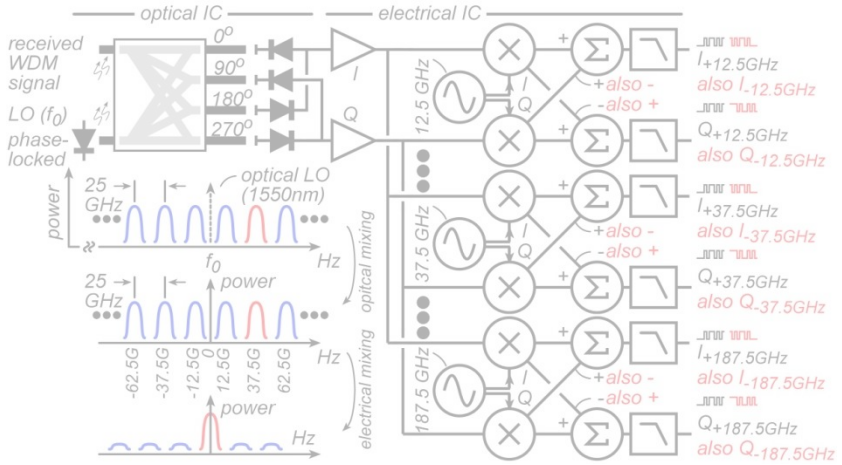
coherent OPLL receiver



optical synthesizer

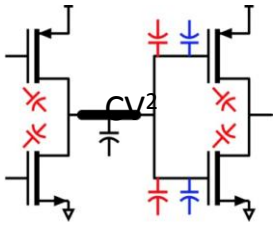


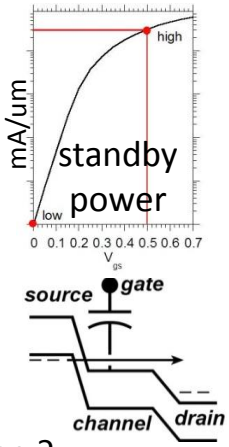
WDM comb synthesis



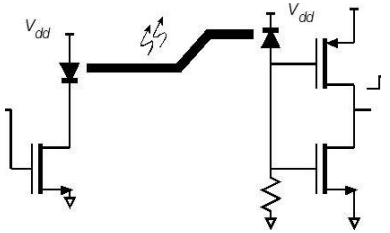
electrical recovery of WDM

Short-range on-chip interconnects and the (CV^2 , $I_{off}V_{DD}$) power crisis.



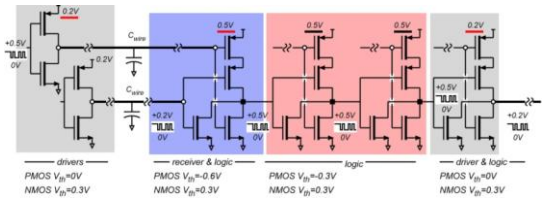


tunnel FETs for low voltage ?

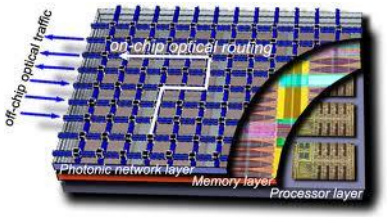


optical interconnects

→ standby power



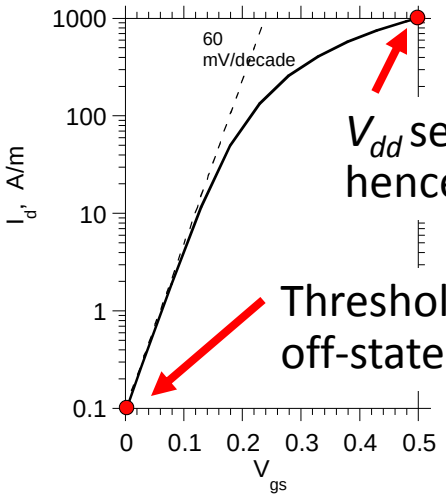
low-voltage signaling



long-range on-chip optical interconnects

Power Dissipation in Short-Range VLSI Interconnects

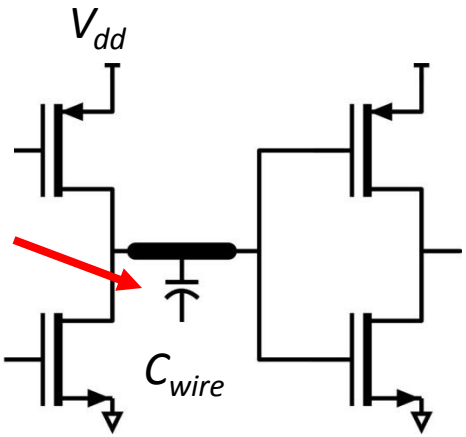
The $CV^2/2$ dissipation limit



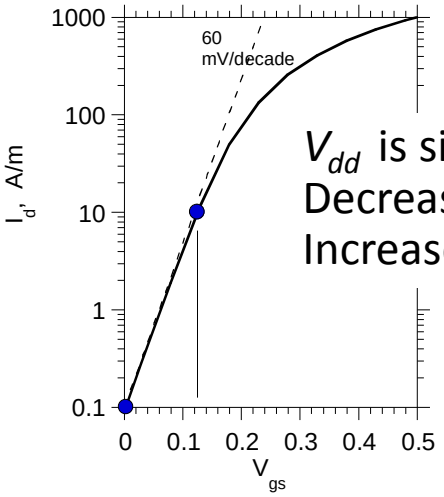
V_{dd} set for target I_{on}, hence acceptable CV_{dd}/I_{on}.

Threshold set for acceptable off-state dissipation $I_{off}V_{dd}$.

With minimum C_{wire}, a minimum switching energy $C_{wire}V_{dd}^2/2$ is set

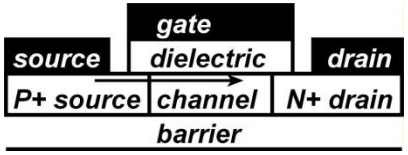


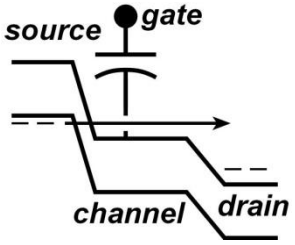
Subthreshold logic



V_{dd} is simply reduced.
Decreases energy $CV_{dd}^2/2$.
Increases delay CV_{dd}/I_{on}.

Tunnel FETs



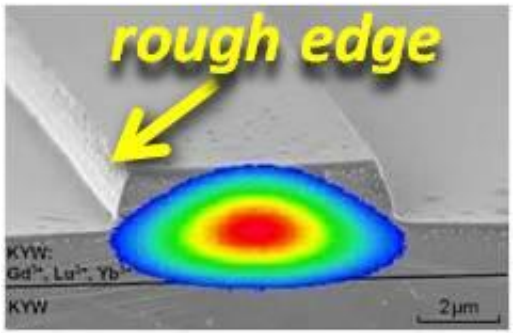


Bandgap of P+ source truncates thermal distribution.

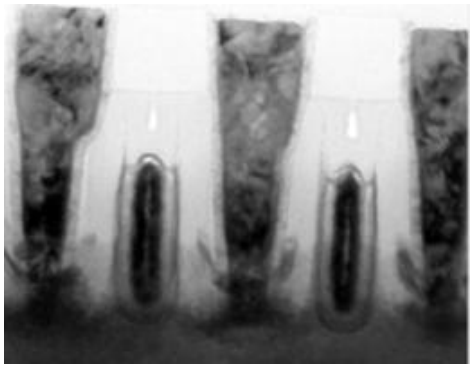
Potential for low I_{off} at low V_{dd}.

Obtaining high I_{on}/V_{dd} is the challenge.
(band edges shift, m* increases in quantization.)

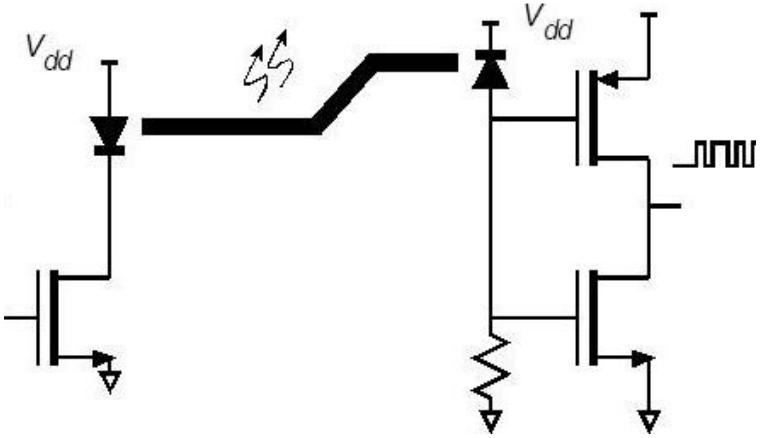
Optical for **Short-Range** VLSI Interconnects ?



roughness scattering



20 nm contact pitch ?



static dissipation

bend radius

Tall finFETs for Low-Power, Low-Voltage Logic

Low-voltage (near-V_T) operation:

low CV^2 dissipation, but low current

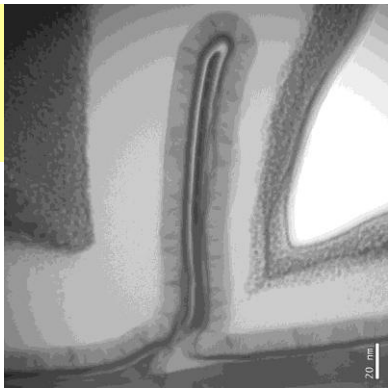
→ long interconnect delays

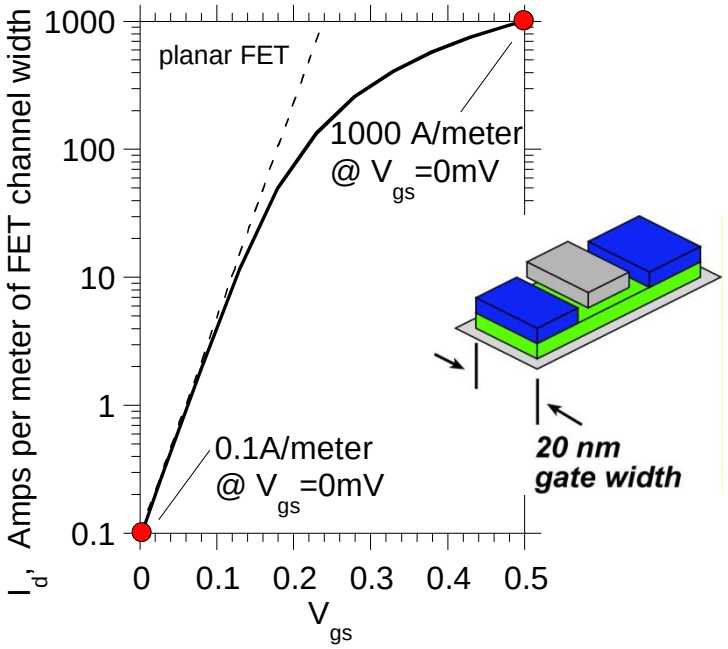
Increased fin height

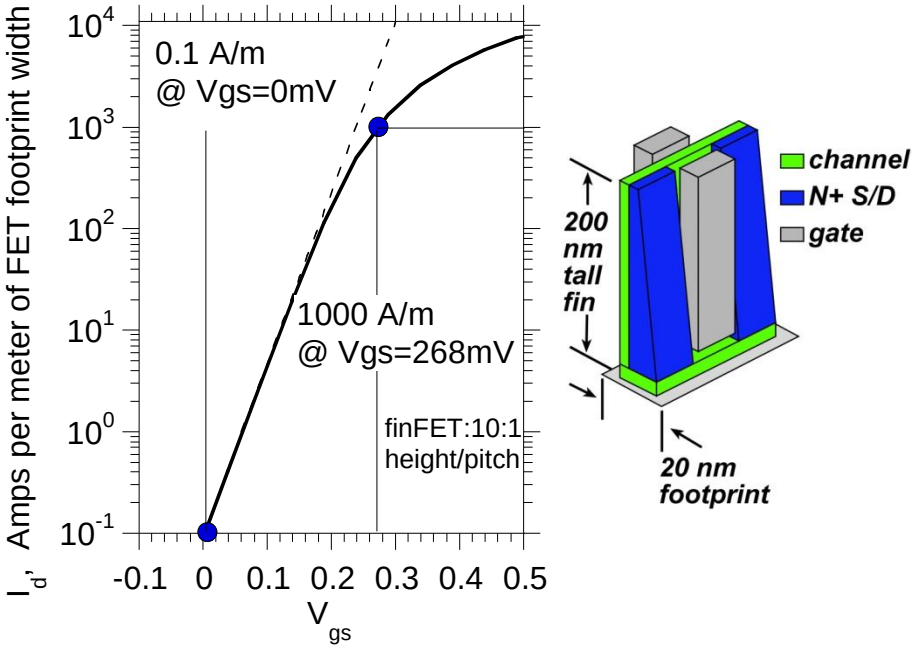
→ increased current per unit die area

→ interconnect charging delays reduced

InGaAs finFET:
8 nm thick fin
200 nm high



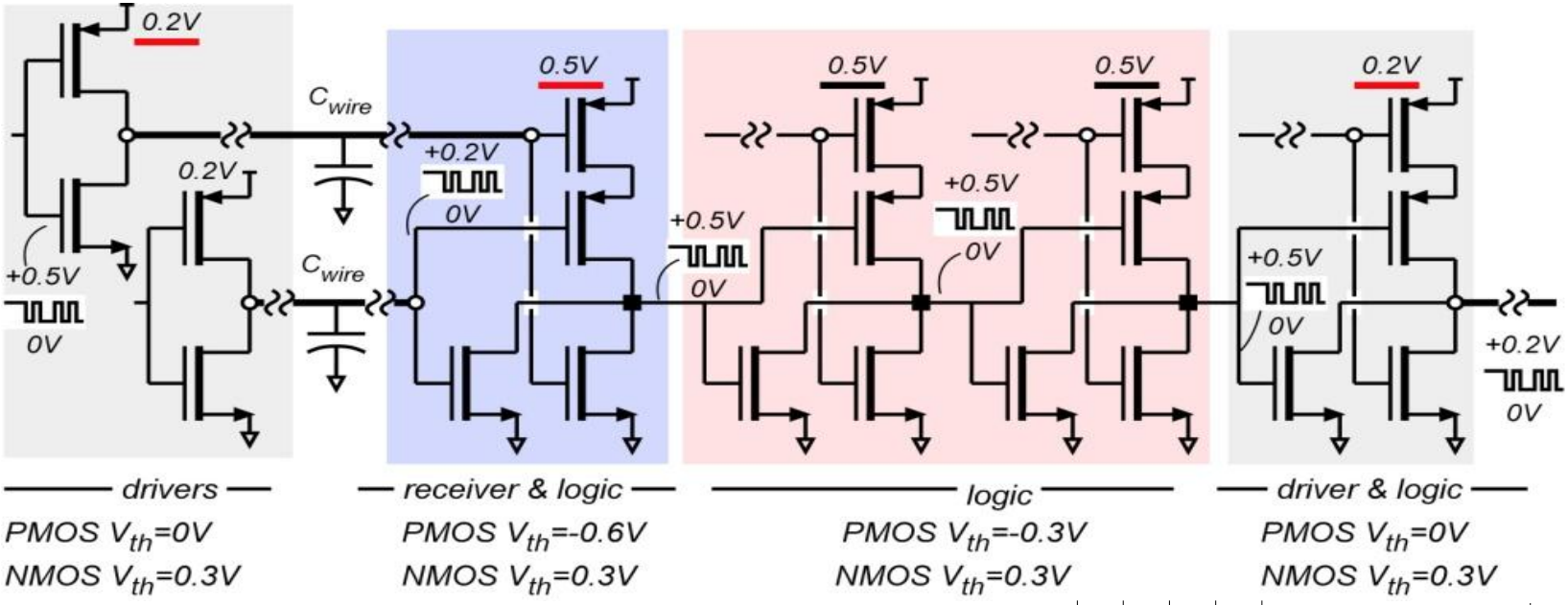




Supply reduced from 500mV to 270 mV while maintaining high speed.

3.5:1 power savings ? Circa 2.5:1 when FET capacitances considered.

Multiple Supplies for Low-Power Logic

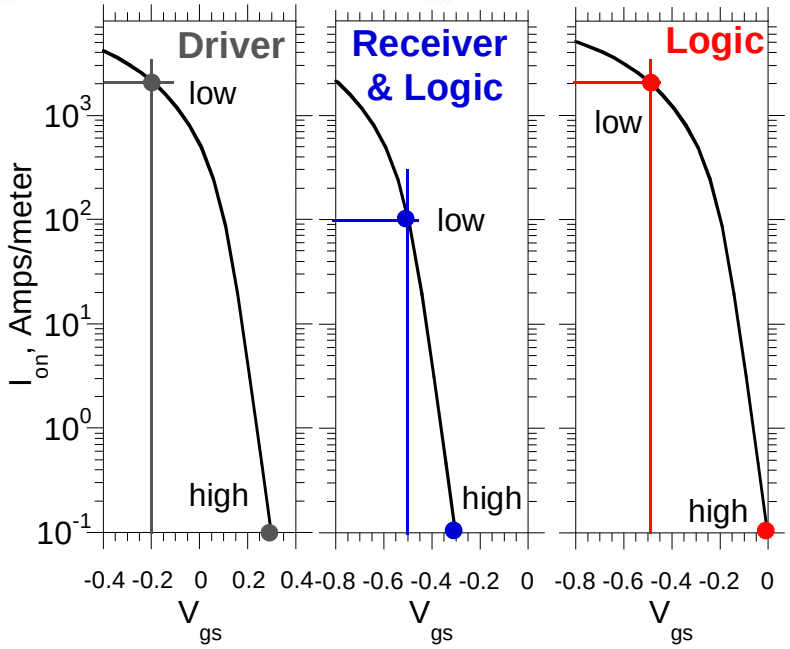


Given 200 mV swings on long interconnects,

Line receivers provide 0.1 mA/μm output with 0.1 μA/μm leakage

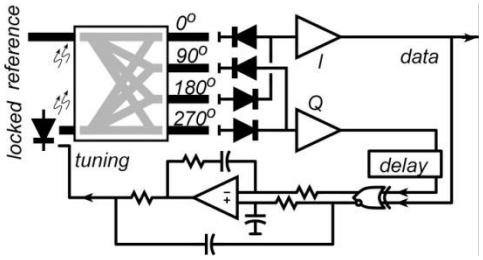
Line drivers, and logic gates provide 3 mA/μm output with 0.1 μA/μm leakage

Is cost in added die area acceptable ?

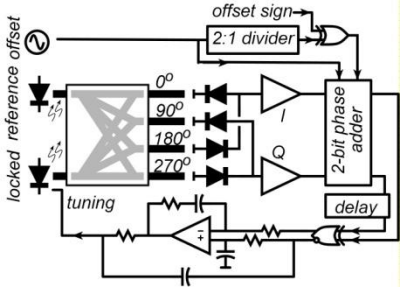


Fast, Low-Power Interconnects for Digital Systems

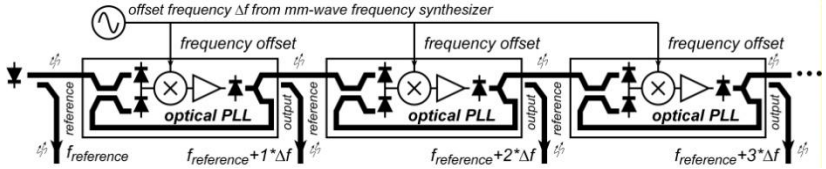
Optical PLLs → mid-range coherent links for data centers ?



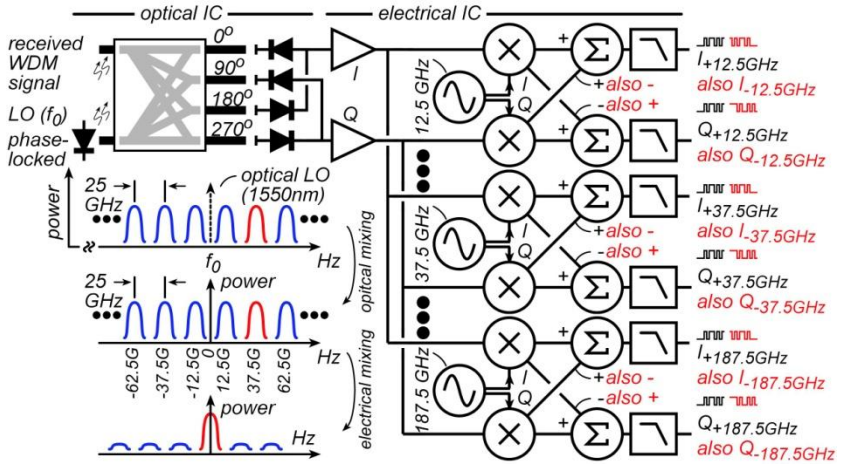
coherent OPLL receiver



optical synthesizer

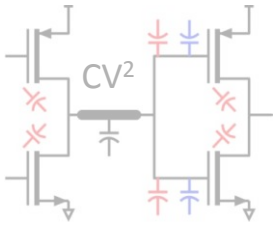


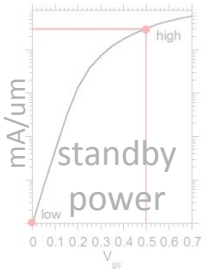
WDM comb synthesis

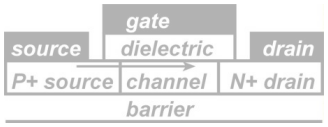


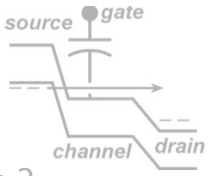
electrical recovery of WDM

Short-range on-chip interconnects and the (CV^2, $I_{off}V_{DD}$) power crisis.

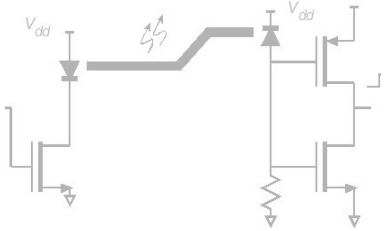






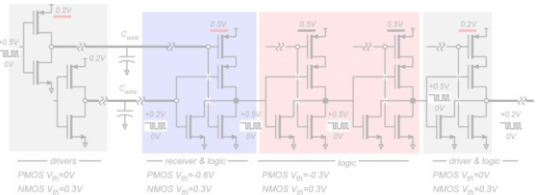


tunnel FETs for low voltage ?

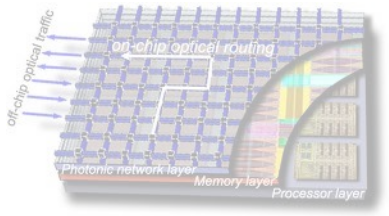


optical interconnects

→ standby power



low-voltage signaling



long-range on-chip optical interconnects

Technology Details

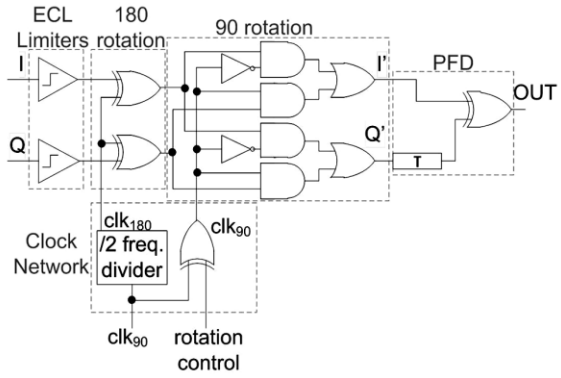
Details: Electrical λ-Synthesis IC

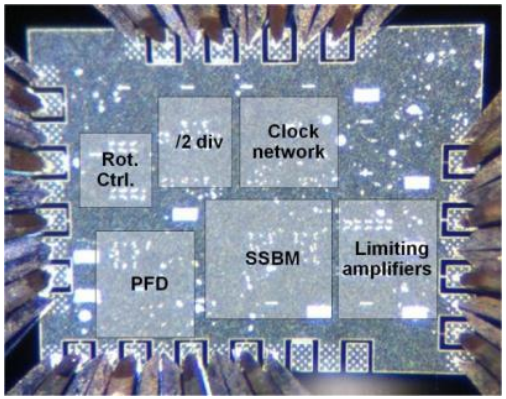
Features

- ***Phase detector***
- ***Frequency difference detector***
  - ***forces loop to lock***
- ***Single-sideband mixer***
  - ***introduces frequency shift***
  - ***controlled sign of shift !***

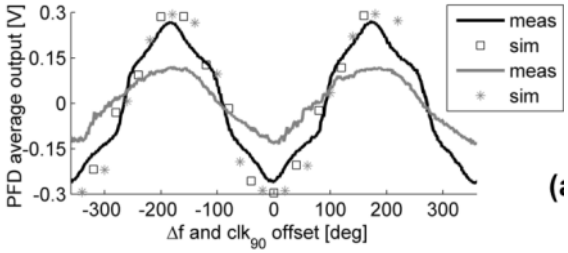
Implementation

- ***Teledyne 350 GHz, 500 nm InP HBT***
- ***Robust all-digital implementation***

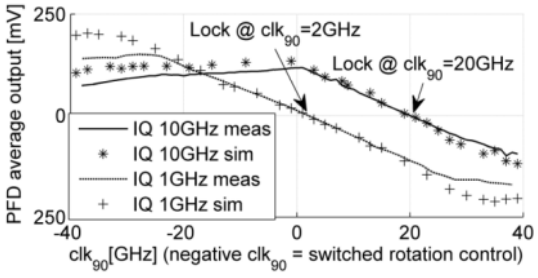




Phase detector test: works over +/- 30 GHz



Frequency detector test: works over +/- 40 GHz



High Speed InP IC Technology

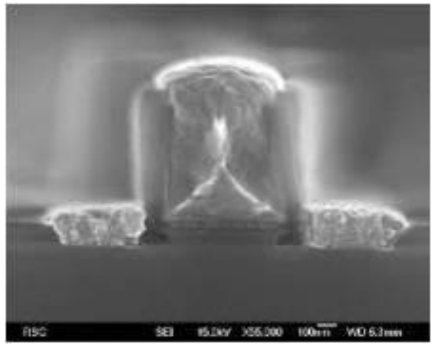
Teledyne Scientific & Imaging 512 nm InP HBT process.

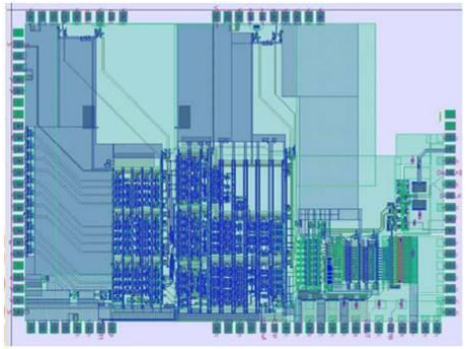
300GHz f_t, f_{max} devices.

4 Metal layers, MIM capacitors, thin-film resistors

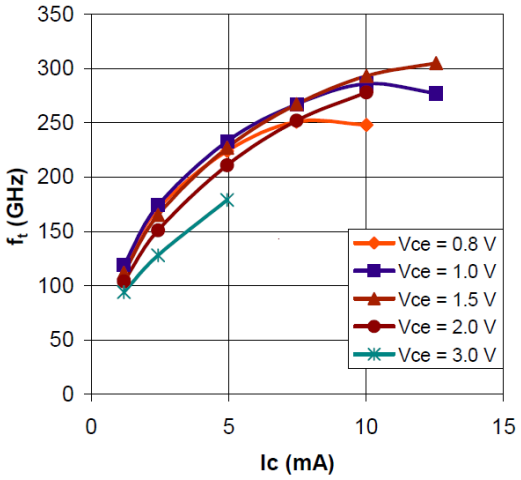
Up to 5000 transistor integration.

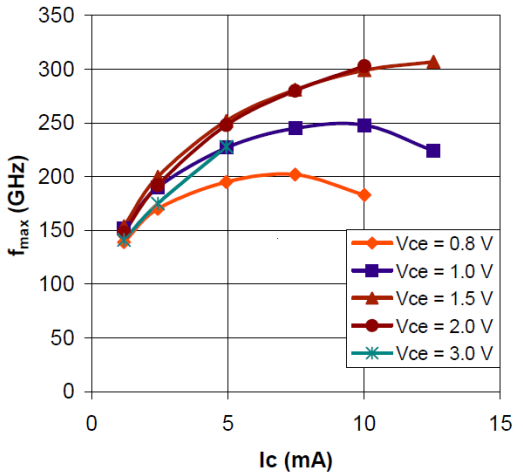
Teledyne 128 nm process (not yet Pilot-Scale) : 700 GHz f_τ, 1.2 THz f_{max}



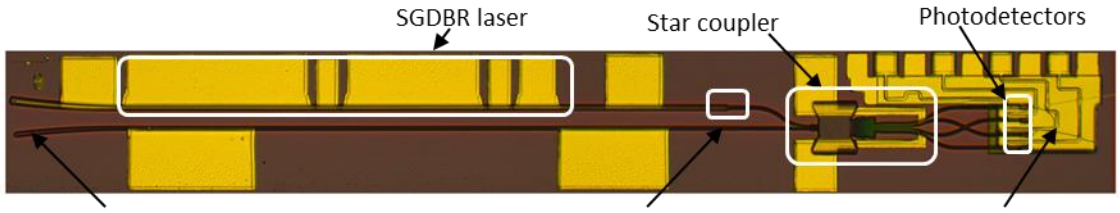


Thank you !
100% first-pass design success

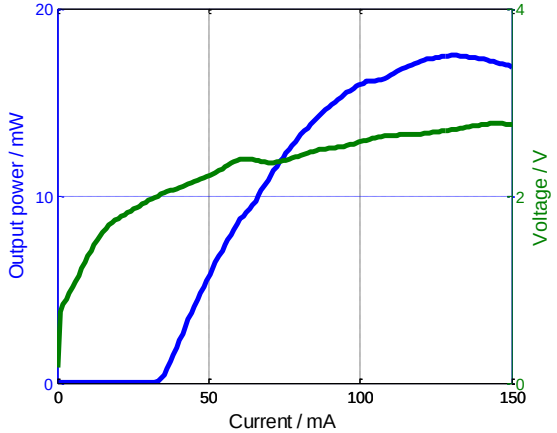


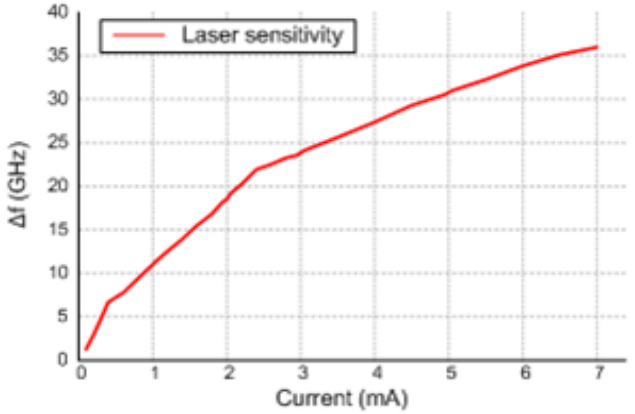


OPLL with PFD and SSBM
Photonic IC



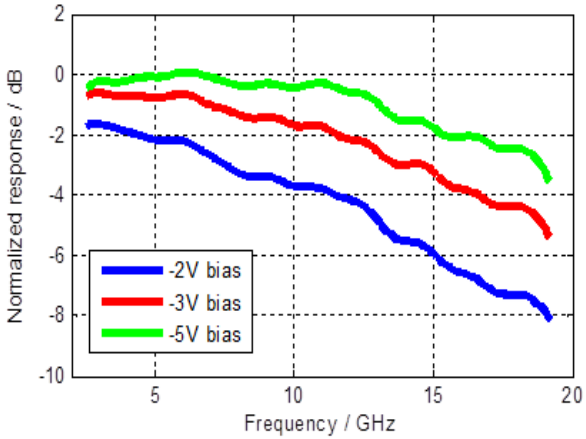
Laser LIV curve

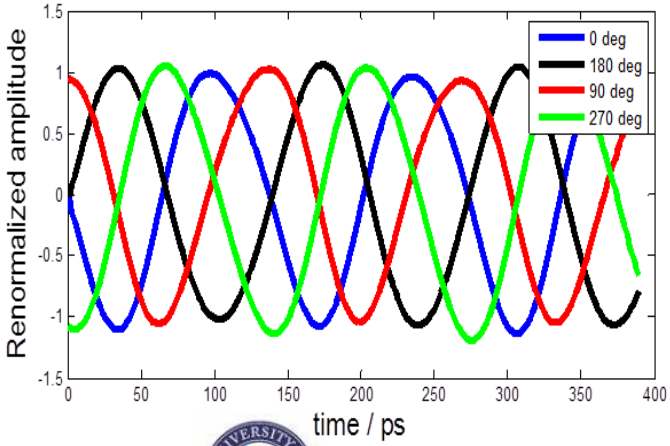




Laser phase pad tuning

PD bandwidth





90° hybrid output

Details: Electrical λ-Synthesis IC

Features

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- ***Frequency difference detector***
  - ***forces loop to lock***
- ***Single-sideband mixer***
  - ***introduces frequency shift***
  - ***controlled sign of shift !***

Implementation

- ***Teledyne 350 GHz, 500 nm InP HBT***
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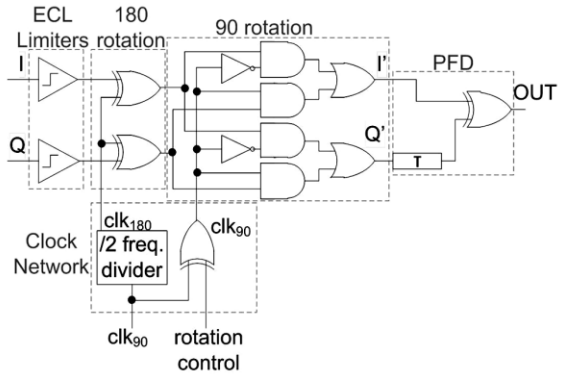
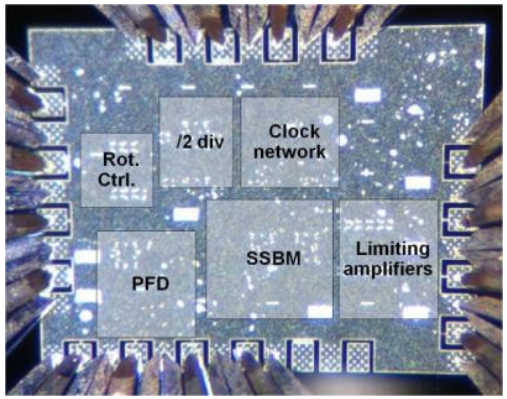
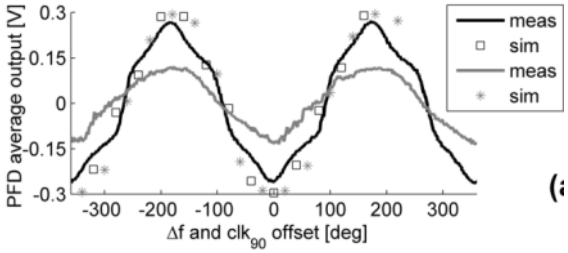
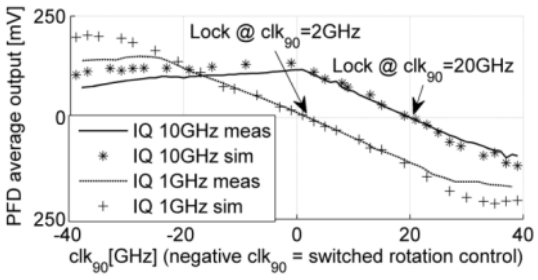




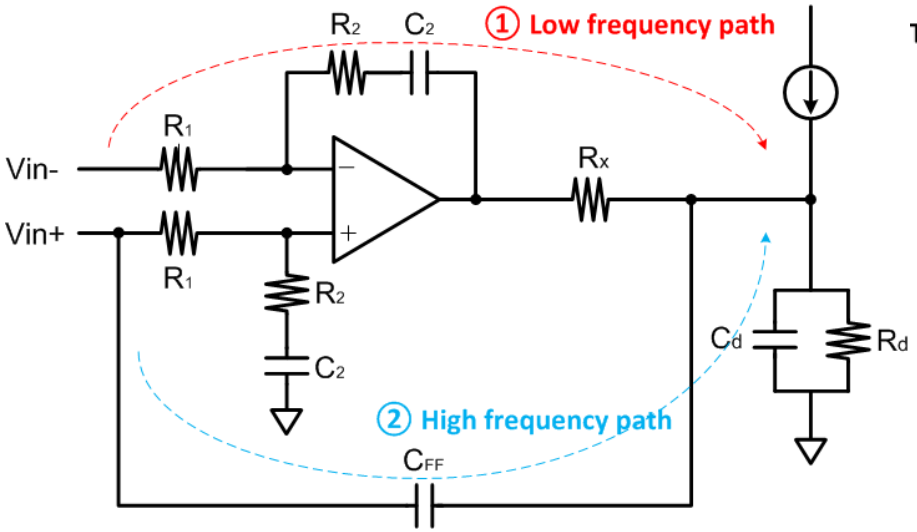
Phase detector test: works over +/- 30 GHz



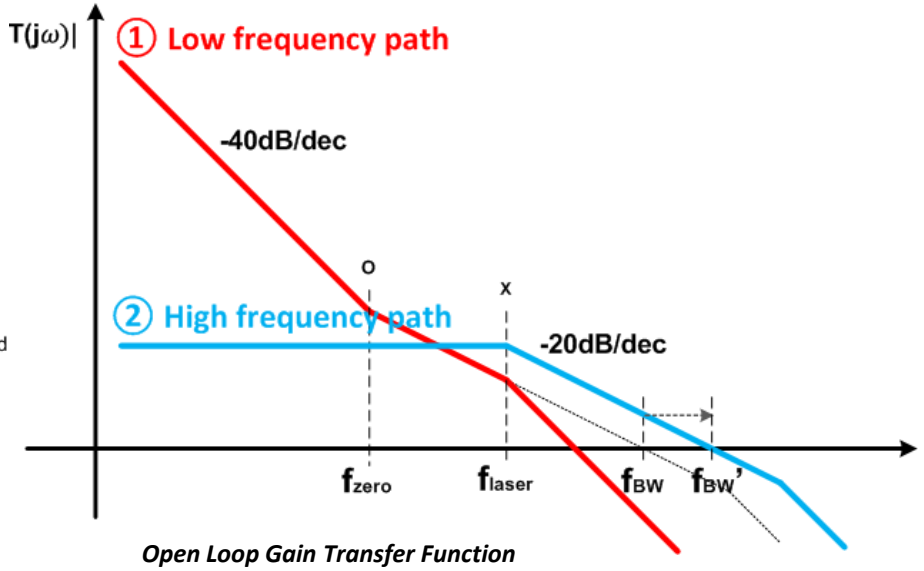
Frequency detector test: works over +/- 40 GHz



Feedforward Loop Filter
High Gain yet High Speed



Schematic



Open Loop Gain Transfer Function

Loop needs high gain at DC → op-amp needed.

Commercial op-amps too slow to support needed ~500 MHz loop bandwidth

Solution: feedforward loop filter

- ***low frequencies: op-amp for high gain***
- ***high frequencies: passive filter for low excess phase shift***