Record I_{on} (0.50 mA/μm at V_{DD} = 0.5 V and I_{off} = 100 nA/μm) 25 nm-Gate-Length ZrO_2/InAs/InAlAs MOSFETs

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Abstract: We report MOSFETs with 25-nm gate length (L_g), extremely thin 2.5 nm InAs channels and 0.7/3.0 nm (physical) $Al_2O_xN_y/ZrO_2$ gate dielectrics, and 12 nm $In_{0.53}Ga_{0.47}As$ vertical spacers in the raised epitaxial source/drain. The FETs establish key new DC performance records, at VLSI-relevant gate lengths (25 nm), including 0.50 mA/μm on-current (at 100 nA/μm I_{off} and 0.5 V V_{DD}) and 77 mV/dec. subthreshold swing (SS) at V_{DS}=0.5 V. At 1 μm L_g and V_{DS}=0.1 V, the minimum subthreshold swing is 61 mV/dec., a record low for InAs/InGaAs, indicating high interface quality.

Introduction: InAs/InGaAs MOSFETs can provide large on-currents at low voltages, and are being investigated for VLSI application [1]-[9]. Yet, impact ionization, band-band tunneling, and source/drain (S/D) tunneling leakage currents can be high because of low bandgaps and low electron effective mass; I_{on} (at specified low I_{off} and V_{DD}), has not previously surpassed Si. Here we report 25 nm-L_g ZrO_2/InAs/InAlAs MOSFETs with performance surpassing prior III-V MOSFETs [1]-[8] and comparable to, or surpassing, leading 20-25 nm L_g Si fin- [10] and nanowire [11] FETs. In these FETs, leakage currents are reduced, without substantially increasing the S/D pitch, by vertical InGaAs spacers in the raised regrown S/D [5], and by thin (2.5 nm) InAs channels for increased channel bandgap. The thin 0.7/3.0 nm (physical) $Al_2O_xN_y/ZrO_2$ gate dielectrics [12], and the thin 2.5 nm channel together improve electrostatics, while the increased gate-channel capacitance arising from these thin layers offsets the loss in transconductance g_m arising from the low mobility of the thin 2.5 nm InAs channel, with 2.38 mS/μm g_m achieved at 25 nm L_g. A record 0.50 mA/μm on-current (at I_{off} =100 nA/μm and V_{DD}=0.5 V) is achieved at a VLSI-relevant 25 nm L_g.

Device Fabrication: The epitaxial layer structure, grown on semi-insulating InP by solid-source MBE, has a 50 nm unintentionally doped (U.I.D) InAlAs buffer, a 250 nm 1.0×10^{17} cm^{-3} P-type doped InAlAs barrier, a 100 nm U.I.D InAlAs barrier, a 2 nm 1.0×10^{12} cm^{-2} N-type InAlAs pulse-doped layer, a 5 nm U.I.D InAlAs setback, a 3.5 nm InAs (strained) channel and 2 nm of the U.I.D $In_{0.53}Ga_{0.47}$ spacer. To form 12-1000 nm long dummy gates, ~20 nm of HSQ was spun and patterned by e-beam lithography. To form the remainder of the vertical spacer and the N+ S/D, 10 nm U.I.D (~1.2×10^{15} cm^{-3}) and 60 nm Si-doped (4.0×10^{19} cm^{-3}) $In_{0.53}Ga_{0.47}As$ were selectively regrown by MOCVD. Device mesas were isolated by wet-etch. The dummy gates were stripped in buffered HF, and ~2 nm of the $In_{0.53}Ga_{0.47}As$ cap and ~1 nm of InAs channel were removed in the gate region by a 2-cycle isotropic digital etch [13], leaving a 2.5 nm InAs channel. The sample was then immediately loaded into an ALD. After *in-situ* N_2 plasma/TMA treatment during which ~0.7 nm of $Al_2O_xN_y$ was formed [14], a ~3 nm ZrO_2 gate dielectric was deposited [12]. The sample was then annealed in forming gas at 400°C. Ni/Au gate and Ti/Pd/Au S/D metal contacts were deposited using thermal and e-beam evaporation, respectively. Fig. 1 shows a device cross-sectional schematic. The FETs have L_g ranging from 18 nm to 1 μm, where L_g is defined as the spacing between the edges of the regrown layer. The surfaces of the vertical spacer is also gated, thus the effective gate length is ~35 nm greater than L_g, given the spacer thickness and regrowth angle. Fig. 2 shows a top-down SEM image, taken before gate metal deposition, for a 25 nm-L_g device. In a production VLSI device, the increase in minimum S/D contact pitch will be determined by the spacer and N+ thicknesses and the regrowth angle; if regrowth can be made vertical, the spacer will not increase minimum S/D pitch.

Results and Discussions: Fig. 3 shows transfer characteristics of a 25 nm-L_g FET showing 2.38 mS/μm peak g_m at V_{DS}=0.5 V and 0.5 mA/μm I_{on} at I_{off}= 100 nA/μm and V_{DD}= 0.5 V. Its subthreshold characteristics (Fig. 4) show 72 mV/dec. minimum SS (SS_{min}) at V_{DS}=0.1 V and 77 mV/dec. at V_{DS}=0.5 V. Defined at I_D=1 μA/μm, its threshold voltage is -85 mV and drain induced barrier lowing (DIBL) is 76 mV/V. Output characteristics (Fig. 5) show 303 Ω-μm on-resistance (R_{on}) at V_{GS}=0.7 V. Considering now a 1 μm-L_g device (Fig. 6), subthreshold characteristics show 61 mV/dec. SS_{min} at V_{DS}=0.1 V, the lowest reported for any III-V MOSFET, and negligible DC hysteresis, both indicating a high-quality dielectric. Gate leakage (Fig. 6) normalized to the gate metal overlap area is <1 A/cm^2 at all measured bias conditions. Fig. 7 shows R_{on} as a function of L_g. The R_{on} extrapolated to zero L_g is 168 Ω-μm (± 25 Ω-μm fitting error), which contains ~85 Ω-μm total excess S/D resistance arising from the large 1.2 μm S/G and G/D spacings (Fig. 7, inset). Absent these large contact spacings, g_m and I_{on} would be larger, and R_{on} lower. Fig. 8 shows peak g_m at V_{DS}=0.5 V versus L_g, compared to published III-V MOSFETs. Despite low mobility in the 2.5 nm InAs channel, sub-40 nm-L_g devices have > 2 mS/μm peak g_m, which we attribute to high gate-channel capacitance from the thin dielectric and channel. Comparing results in the published III-V literature, the devices here reported show the lowest SS_{min} at all L_g (Fig. 9) of any III-V MOSFETs, and exhibit the smallest DIBL at all L_g (Fig. 9) of any *planar* III-V MOSFETs. Fig. 11 benchmarks I_{on} at I_{off}=100 nA/μm and V_{DD}=0.5 V as a function of L_g. The devices show the highest I_{on} of any III-V MOSFET at a 0.5 V supply voltage. (note I_{off} in [3] is extrapolated, not measured)

Conclusion: We have demonstrated highly scaled ZrO_2/InAs/InAlAs MOSFETs exhibiting records for key DC parameters. A FET with 25 nm-L_g shows 0.5 mA/μm I_{on} at I_{off}= 100 nA/μm and V_{DD}= 0.5 V and 77 mV/dec. SS_{min} at V_{DS}=0.5 V. At 1 μm-L_g and V_{DS}=0.1 V, SS_{min} is 61 mV/dec., indicating a very high quality dielectric-semiconductor interface.

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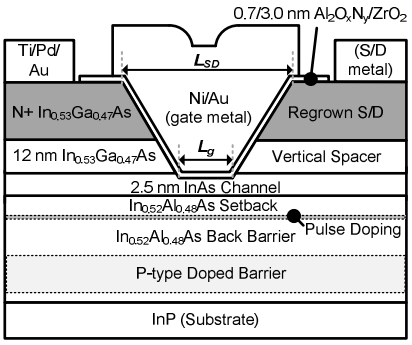

Fig. 1. Device schematic cross-section

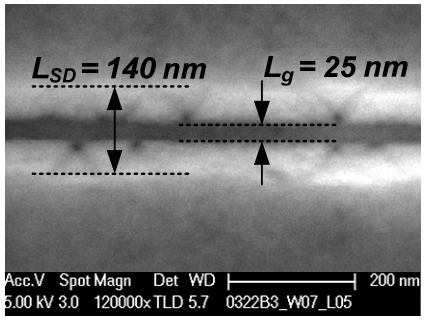

Fig. 2: SEM top-view image, before gate metal deposition, showing 25 nm L_g.

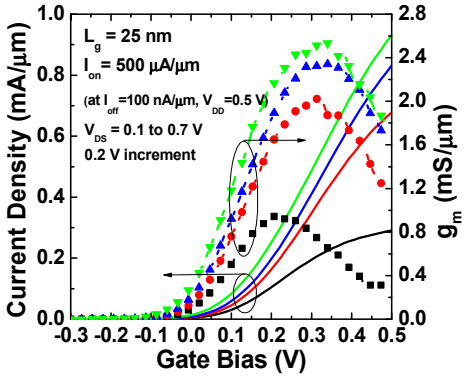

Fig. 3: Drain current I_D and transconductance g_m, versus V_{GS}, at 25 nm L_g.

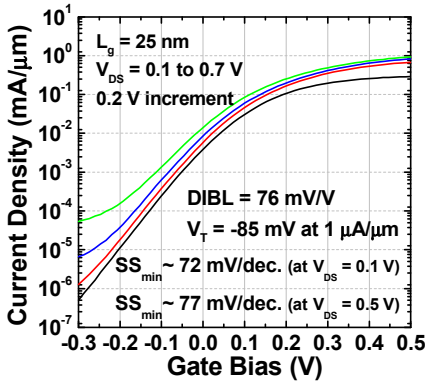

Fig. 4: log(I_D) versus V_{GS}, at 25 nm L_g, at V_{DS} = 0.1, 0.3, 0.5 and 0.7 V.

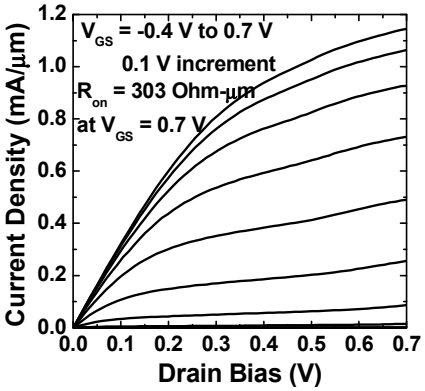

Fig. 5: Common-source DC characteristics at 25 nm L_g.

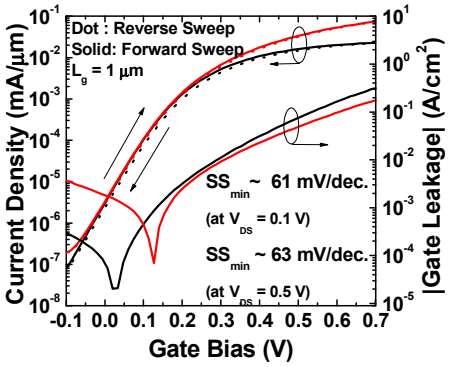

Fig. 6: log(I_D) and log(I_G) versus V_{GS}, at 1μm L_g, at V_{DS} = 0.1 V and 0.5 V.

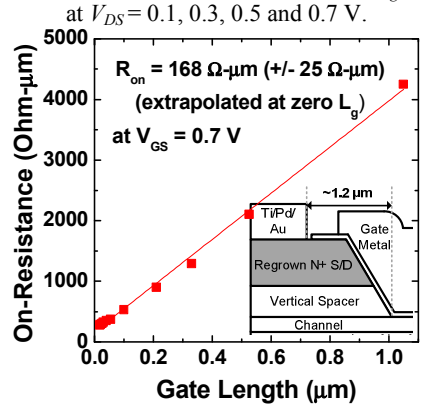

Fig. 7: Drain-source on-resistance versus L_g. The FETs have large S/G and G/D spacings.

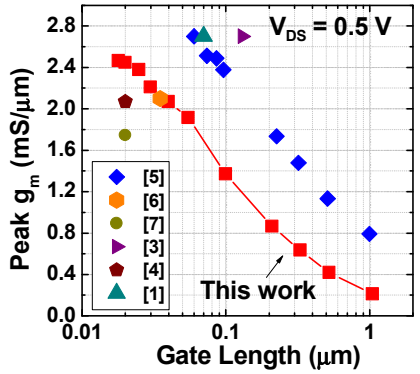

Fig. 8: Peak transconductance versus L_g, compared to the III-V literature.

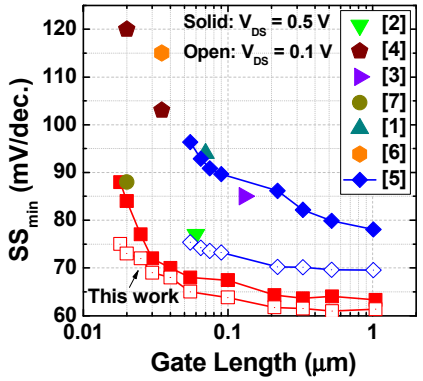

Fig. 9: SS_{min} as a function of L_g, compared to published III-V MOSFETs.

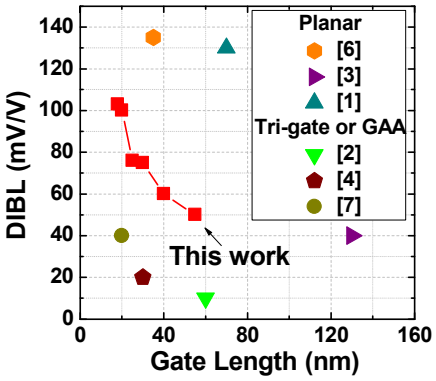

Fig. 10: DIBL as a function of L_g, compared to published III-V MOSFETs.

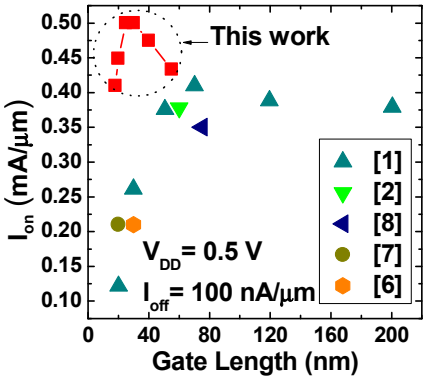

Fig. 11: I_{on}, at 0.5V V_{DS} and 100nA/μm I_{off}, versus L_g, compared to the III-V literature.