Highly Scalable Raised Source/Drain InAs Quantum Well MOSFETs Exhibiting $I_{ON} = 482\ \mu A/\mu m$ at $I_{OFF} = 100\ nA/\mu m$ and $V_{DD} = 0.5$ V

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***Abstract*— We report raised source/drain (S/D) InAs quantum well MOSFETs incorporating a vertical spacer formed by metal–organic chemical vapor deposition epitaxial regrowth. By adopting a 12-nm-thick vertical spacer between the channel and the N+ S/D, OFF-state characteristics are significantly improved. A device with a 40-nm-L_g and 12-nm-thick spacer shows 2.5-mS/μm peak transconductance (g_m), 86-mV/decade subthreshold swing at V_{DS} = 0.5 V, 83-mV/V drain-induced barrier lowering, and 482-μA/μm ON-current at 100-nA/μm OFF-current and V_{DD} = 0.5 V. In addition, a 3.0-mS/μm peak g_m at V_{DS} = 0.5 V is achieved in an 18-nm-L_g device with a 2-nm-thick spacer, the highest reported peak g_m of any field-effect transistor.**

***Index Terms*— III-V MOSFETs, S/D regrowth, vertical spacer, InAs channel.**

I. Introduction

III-V MOSFETs have been considered as one of the viable candidates for sub-10 nm CMOS node due to their outstanding electron transport properties at low supply voltage. To maximize on-state performance, InAs or indium-rich $In_xGa_{1-x}As$ (x>0.53) has been widely investigated as the channel material over $In_{0.53}Ga_{0.47}As$ [1]–[7]. Its low effective mass provides superior electron transport properties, but its narrow bandgap can increase off-state leakage current by either band-to-band tunneling (BTBT) or by impact ionization (I.I.) in the gate-drain high field region. To reduce off-state leakage and improve electrostatics at short gate lengths, many III-V MOSFETs reported in the literature have employed large lateral spacing between the gate and the drain [1]–[3]. However, this limits the integration density in VLSI, where small source/drain (S/D) contact pitch is required. In [4], we reported reduced MOSFET off-current using an undoped vertical semiconductor spacer between the channel and N+ S/D. MOSFETs with the spacer exhibited significantly improved off-state characteristics without noticeable degradation in on-state performance. However, because in [4] the vertical spacer in the gate region was formed by an isotropic wet-recess etch, the total gate length was increased by twice the spacer thickness, and thus sub-20 nm gate length transistors could not be fabricated.

Here we report MOSFETs using a regrown vertical spacer which allows us to realize sub-20 nm gate lengths (L_g) even with spacers as thick as 12 nm. A 40 nm-L_g device with a 12 nm-thick spacer shows excellent performance in both the on-state and off-state, featuring 2.5 mS/μm peak transconductance (g_m), 86 mV/dec minimum subthreshold swing (SS_{min}) at V_{DS} = 0.5 V, 83 mV/V drain-induced barrier lowering (DIBL) and 482 μA/μm on-current (I_{on}) at a fixed 100 nA/μm off-current (I_{off}) and V_{DD} = 0.5 V. In addition, an 18 nm-L_g device with a 2 nm-thick spacer shows 3.0 mS/μm peak g_m at V_{DS} = 0.5 V, the highest peak g_m of any reported field-effect transistor.

II. Device Structure and Fabrication

The epitaxial layers for all samples, grown on semi-insulating InP substrate by solid source molecular beam epitaxy, consist of the following: a 50 nm unintentionally doped (U.I.D) InAlAs buffer, a 250 nm 1.0 × $10^{17}cm^{-3}$ P-type doped InAlAs barrier, a 100 nm U.I.D InAlAs barrier, a 2 nm 1.0 × $10^{12}cm^{-2}$N-type doped InAlAs pulse-doping layer, a 5 nm U.I.D InAlAs setback, a 6 nm InAs (strained) and a 2 nm U.I.D $In_{0.53}Ga_{0.47}$ cap layer. To define dummy gates, ~40 nm hydrogen silesequioxane was spun and patterned by e-beam lithography. Immediately after etching the native oxide in dilute HCl, samples were transferred into an MOCVD reactor to form the vertical spacer and the N+ S/D. Three samples were selectively regrown, with a 0, 5, or 10 nm-thick U.I.D $In_{0.53}Ga_{0.47}As$ spacer (~1.2 × $10^{15}cm^{-3}$ N-type) and a 60 nm Si-doped (4 × $10^{19}cm^{-3}$) $In_{0.53}Ga_{0.47}As$ N+ S/D. Device mesas were then isolated and dummy gates removed in buffered oxide etch. Through 2 cycles of digital etching, the 2 nm cap layer and ~1 nm of the InAs channel were isotropically wet-etched. The samples were transferred into the ALD chamber, and passivated by cyclical N_2 plasma and tri-methyl-aluminum, and subsequently, 3 nm

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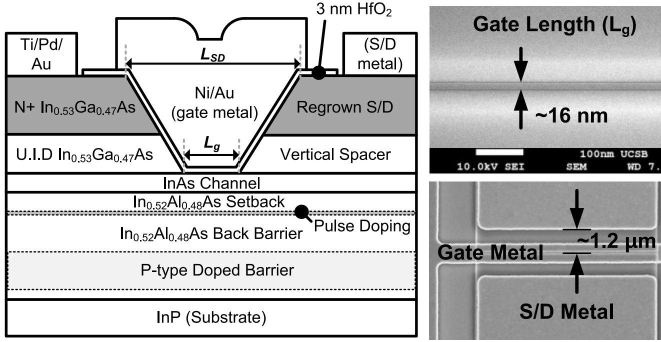

Fig. 1. The cross-sectional schematic of the device structure. The minimum gate length (L_g) is ~16 nm and the spacing between the gate and the S/D contact is ~1.2 μm, which adds ~85 $\Omega\cdot\ \mu$m S/D access resistance for both sides to the on-resistance.

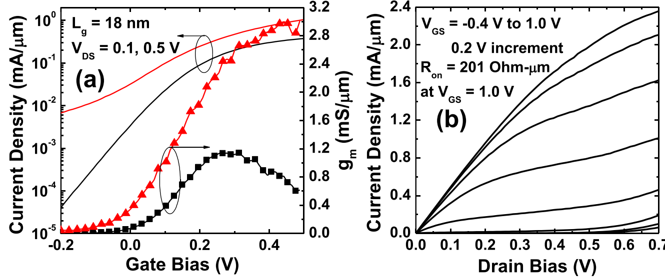

Fig. 2. (a) Transfer ($\log(I_D)$-V_{GS} and g_m) and (b) output (I_D-V_{DS}) characteristics for a 18-nm L_g device with a 2 nm-thick spacer.

HfO_2 gate dielectric was deposited [8]. After a 400 °C post deposition anneal in forming gas, Ni/Au gate metal and Ti/Pd/Au S/D contacts were then lifted-off. The samples have ~5 nm-thick InAs channels. Gate lengths range from 18 nm to 1 μm on the samples with 2 nm- and 7 nm-thick vertical spacers, and from 30 nm to 1 μm on the sample with a 12 nm-thick vertical spacer (devices with sub-30 nm L_g did not yield on this sample). A schematic cross-section is illustrated in Fig. 1.

III. Results and Discussion

The transfer and output characteristics of a FET with a 2 nm vertical spacer and $L_g = 18$ nm are shown in Fig. 2(a) and (b). The device shows 3.0 mS/μm peak g_m, 196 mV/dec SS_{min} at $V_{DS} = 0.5$ V, and 201 $\Omega\cdot\ \mu$m on-resistance (R_{on}) at $V_{GS} = 1.0$ V. Fig. 3(a) and (b) show transfer characteristics of a 40 nm-L_g device with a 12 nm spacer in linear and semi-log scale. Its peak g_m and SS_{min} are 2.5 mS/μm and 86 mV/dec at $V_{DS} = 0.5$ V, respectively. Defined at $I_D = 1\ \mu$A/μm, its threshold voltage is 35 mV and DIBL is 83 mV/V. Using the criteria $I_{off} = 100$ nA/μm and $V_{DD} = 0.5$ V, the device has $I_{on} = 482\ \mu$A/μm. R_{on} is 289 $\Omega\cdot\ \mu$m at $V_{GS} = 1.0$ V. Fig. 3(c) compares output characteristics for 40 nm-L_g devices with a 2 nm- and a 12 nm- thick spacer. Fig. 3(d) plots $log(I_D)$ versus V_{GS} and gate leakage of a FET with a 12 nm-thick spacer and 1 μm-L_g. The SS_{min} at $V_{DS} = 0.1$ V is 66 mV/dec. Assuming that the dielectric constants of $Al_2O_xN_y$ and HfO_2 are 9 and 20, the equivalent oxide thickness (EOT) is ~0.8 nm, and D_{it} is calculated to be ~3 × 10^{12} $cm^{-2}\cdot\ eV^{-1}$ from $D_{it} = C_{EOT}/q\cdot(SS/2.3kT\text{-}1/q)$ [9]. Gate leakage is negligible.

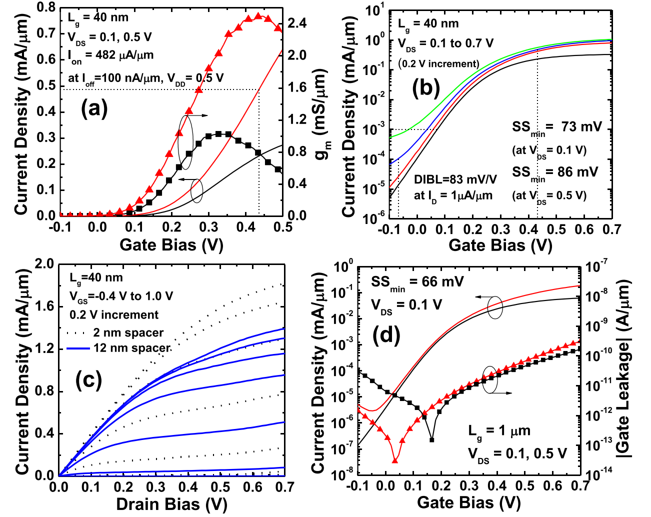

Fig. 3. (a) $I_D - V_{GS}$ and g_m (b) $\log(I_D)$-V_{GS}, and (c) I_D-V_{DS} plots for a 40-nm L_g device. (d) $\log(I_D)$-V_{GS} plot for a long channel device (1 μm) and its gate leakage. Plots (a,b,d) are for a device with a 12 nm thick spacer, while plot (c) compares devices with a 2 nm- and 12 nm- thick spacer.

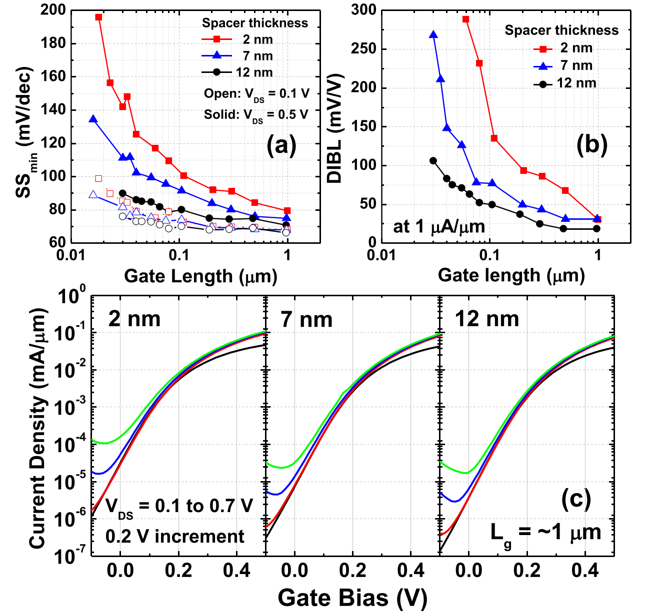

Fig. 4. (a) SS_{min} vs. L_g at $V_{DS} = 0.1$ and 0.5 V for 2 nm-, 7 nm- and 12 nm-thick spacer devices. (b) DIBL vs. L_g for 2 nm-, 7 nm- and 12 nm-thick spacer devices. (c) $\log(I_D)$-V_GS plots for 2 nm-, 7 nm- and 12 nm-thick spacer devices with ~1 μm-L_g.

Fig. 4(a) compares the SS_{min} of samples with 2, 7, and 12 nm-thick vertical spacers as a function of gate length both at $V_{DS} = 0.1$ and 0.5 V. As the spacer thickness is increased, the SS_{min} at $V_{DS} = 0.5$ V is greatly reduced at all gate lengths but there is only moderate improvement at $V_{DS} = 0.1$ V, which suggests that the spacer both improves the FET electrostatics and reduces leakage arising in the high-field region between the gate and the N+ drain. The present data does not allow us to fully determine the relative contributions of BTBT and I.I. to this leakage current. Fig. 4(b) compares DIBL as a function of L_g. The 12 nm-thick spacer devices show significantly lower DIBL than the 2 nm- and 7 nm-thick spacer devices. Fig. 4(c) compares off-state leakage versus V_{GS} and V_{DS} for

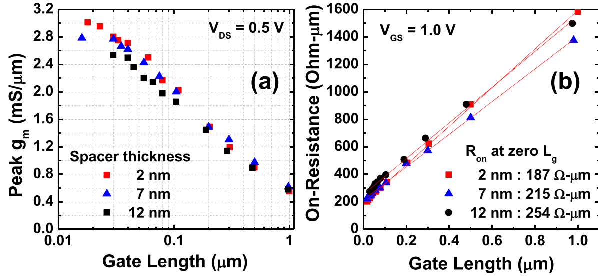

Fig. 5. (a) Peak g_m vs. L_g at $V_{DS} = 0.5$ V, and (b) R_{on} at $V_{GS} = 1.0$ V for or 2 nm-, 7 nm- and 12 nm-thick spacer devices.

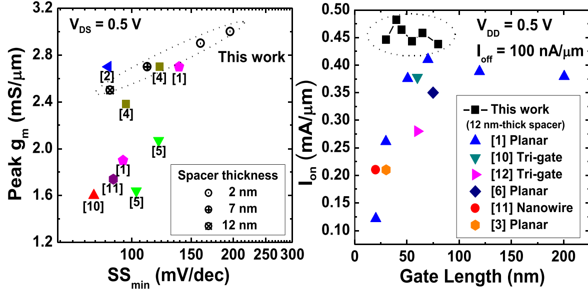

Fig. 6. (a) Peak g_m with respect to SS_{min} at $V_{DS} = 0.5$ V and (b) I_{on} with respect to L_g at $I_{off} = 100$ nA/μm and $V_{DD} = 0.5$ V, comparing with recently reported III-V MOSFETs.

devices having $L_g = 1$ μm, devices for which the increase in the effective channel length from the spacer thickness is negligible. The 12 nm-thick spacer devices show ~8:1 to 9:1 smaller minimum leakage at $V_{DS} = 0.7$ V than the 2 nm-thick spacer devices. The improved DIBL and minimum off-state leakage of 12 nm-thick spacer devices at gate lengths suggest that the reduced leakage cannot be attributed exclusively to an increase in effective gate length. Fig. 5(a) shows the peak g_m as function of L_g. 12 nm-thick spacer devices show 7-10 % reduced peak g_m at short L_g which may be due to increased effective channel length or resistance arising from the spacer. Fig. 5(b) compares R_{on} versus gate length. The R_{on} of 2, 7, and 12 nm-thick spacer devices, extrapolated to zero L_g, are 187, 215, and 254 $\Omega\cdot$ μm, respectively; the 12 nm spacer adds 67 $\Omega\cdot$ μm to R_{on}. The variation in sheet resistivities is due to varying threshold voltages. The R_{on} includes ~ 85 $\Omega\cdot$ μm S/D access resistance, as computed from the regrown N+ S/D sheet resistance and the 1.2 μm spacing between the channel and the S/D contacts (Fig. 1).

Benchmarks of recently published results on III-V MOSFETs are shown in Fig. 6. Fig. 6(a) compares peak g_m with respect to SS_{min}. The device with 2 nm spacer and 18 nm-L_g shows the highest peak g_m of 3.0 mS/μm at $V_{DS} = 0.5$ V among all types of MOSFETs published to date. The device with a 12 nm spacer exhibits excellent peak g_m of 2.5 mS/μm and SS_{min} of 86 mS/μm even with a short 40 nm-L_g and the planar ultra-thin-body architecture. Fig. 6(b) compares I_{on} at a fixed $I_{off} = 100$ nA/μm and $V_{DD} = 0.5$ V. The devices with a 12 nm spacer have >450 μA/μm at sub-50 nm-L_g which is the best reported I_{on} among any III-V MOSFETs to date; the 100 nA/μm I_{off} reported in [2] is extrapolated, not measured. Due to high off-state leakage at high V_{DS}, 2 nm-thick spacer devices have significantly lower I_{on} at the fixed I_{off} despite the superior transconductance.

Given the angle of the edge of the S/D regrowth, the regrown layer increases the minimum feasible S/D contact pitch by an amount (L_{SD}-L_g) (Fig. 1). By adjusting the regrowth conditions to steepen the regrowth edge [13], [14], and by using thinner and more heavily-doped N+ S/D layers, this increase in minimum contact pitch can be reduced.

IV. Conclusion

We have demonstrated high-performance raised S/D InAs quantum-well MOSFETs with a vertical spacer formed by MOCVD regrowth. Using 12 nm-thick vertical spacers significantly improved the off-state characteristics (SS and DIBL) without large increases in the minimum feasible S/D contact pitch. A 40 nm-L_g device with a 12 nm-thick spacer shows excellent on-state and off-state performance, featuring 2.5 mS/μm peak g_m, 86 mV/dec SS_{min} at $V_{DS} = 0.5$ V, 83 mV/V DIBL ,and 482 μA/μm I_{on} at a fixed 100 nA/μm I_{off} and $V_{DD} = 0.5$ V. In addition, a 18 nm-L_g device with a 2 nm spacer shows 3.0 mS/μm peak g_m at $V_{DS} = 0.5$ V, which is the highest peak g_m out of any type of FETs reported.

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