2014 Device Research Conference, June 22-24, Santa Barbara, CA.

Nanometer InP Electron Devices for VLSI and THz Applications

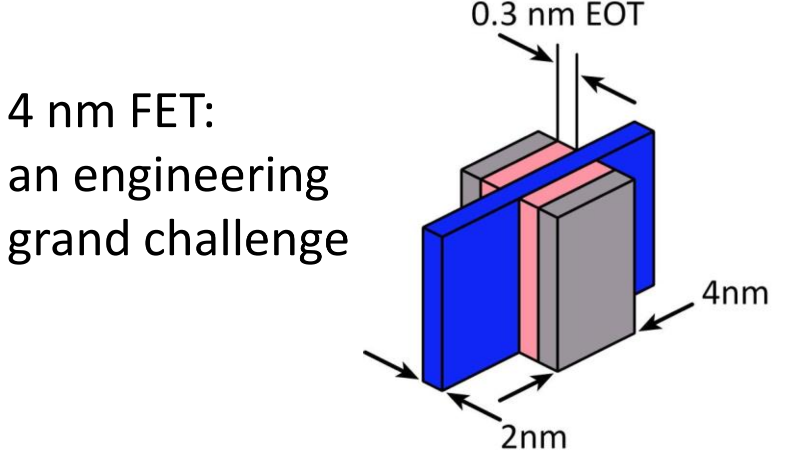
M.J.W. Rodwell, UCSB

S. Lee, C.-Y. Huang, D. Elias, V. Chobpattanna, J. Rode, H.-W. Chiang, P. Choudhary, R. Maurer, , A.C. Gossard, S. Stemmer: ***UCSB***

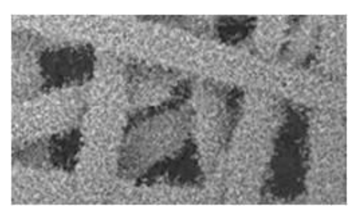
M. Urteaga, B. Brar: ***Teledyne Scientific***

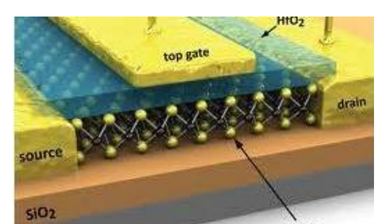
nm FETs & VLSI: how small can we go ?

4 nm FET:
an engineering
grand challenge



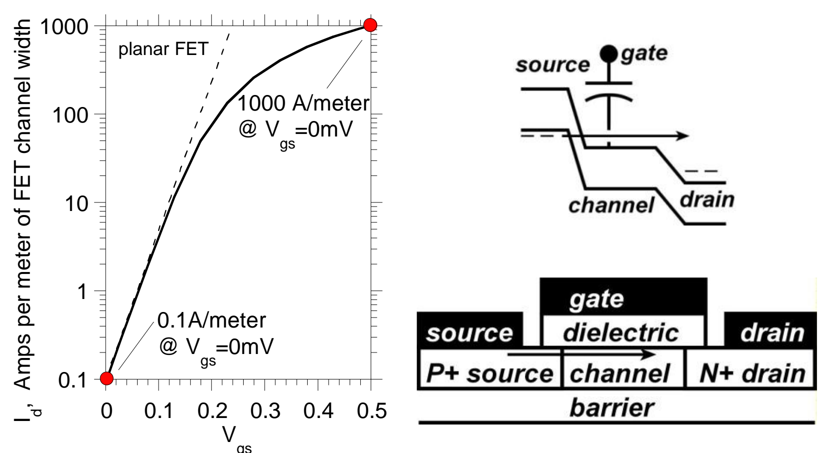
Will 2-D semiconductors
scale better than bulk ?





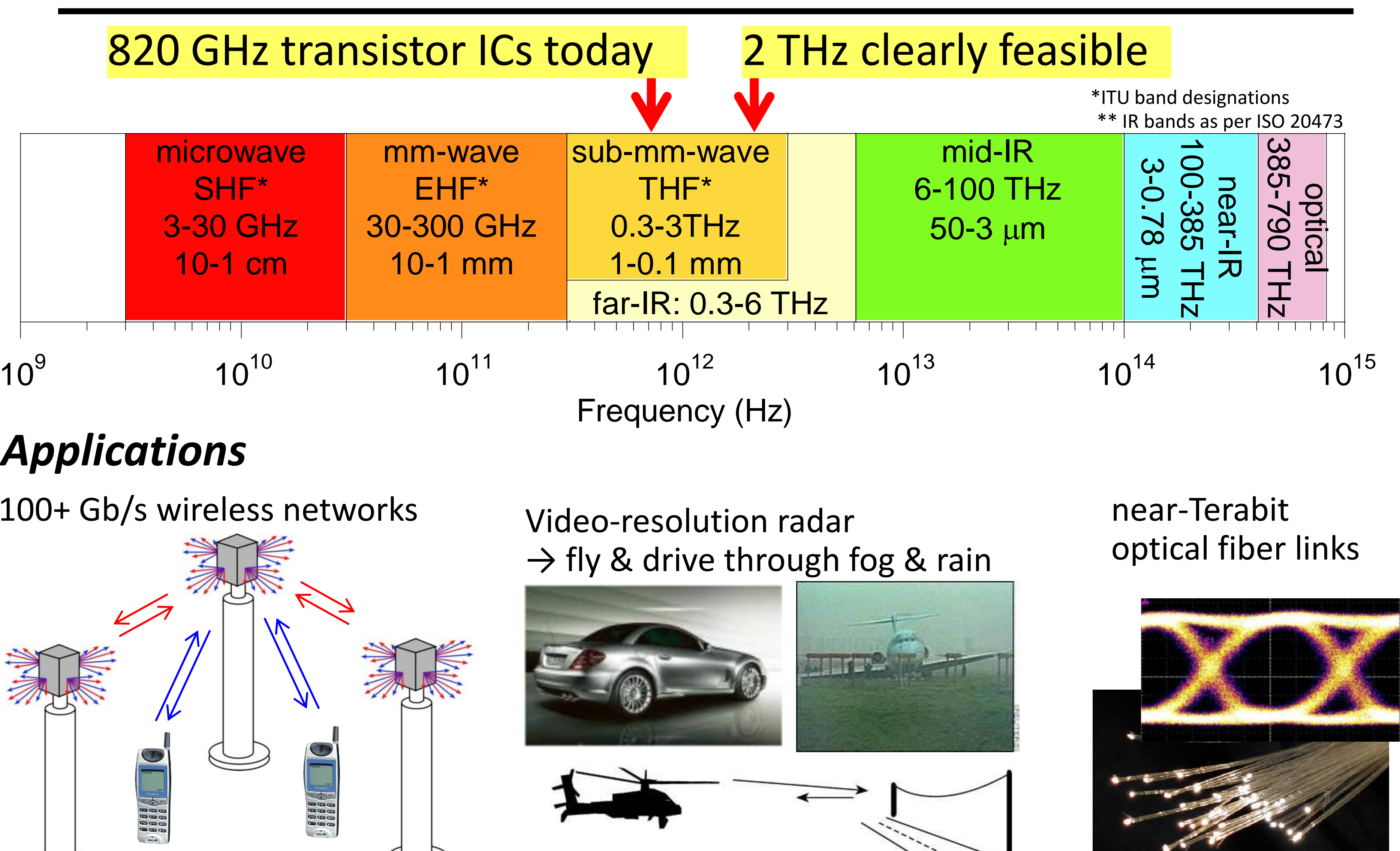
Can we make even good 8nm FETs ?

Can we manage CV^2 dissipation ?
Are tunnel FETs viable ? Alternatives ?



Perhaps bulk semiconductors can do very well.

High-frequency electronics: How high can it go ?

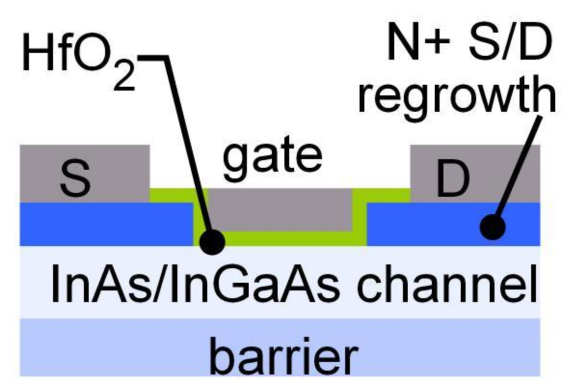


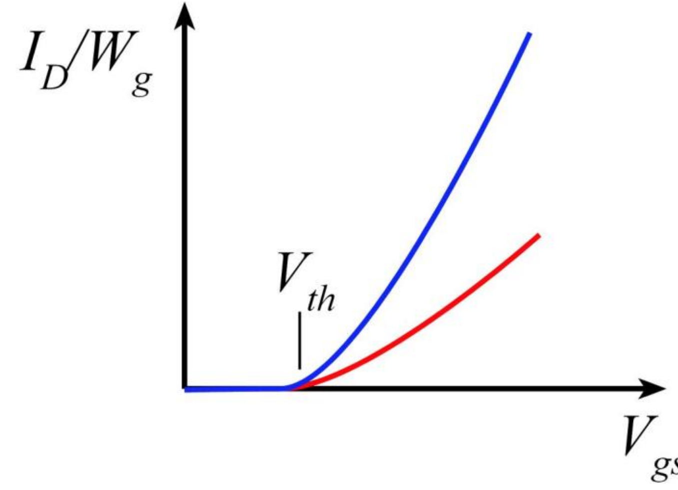
Transistor Goal: < 3 dB noise, >1 W power, 10% efficiency, 50-500GHz

nm
(III-V) MOSFETs

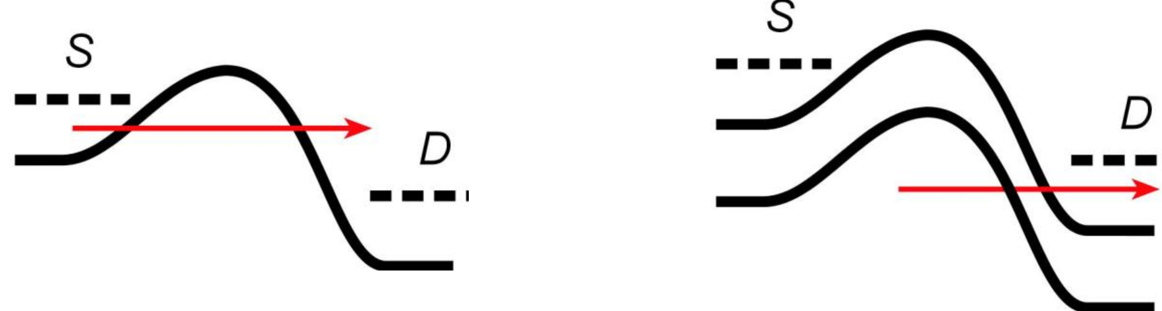
Why III-V MOS ?

III-V vs. Si: Low m*→ higher velocity. Fewer states→ less scattering → higher current. Can then trade for lower voltage or smaller FETs.

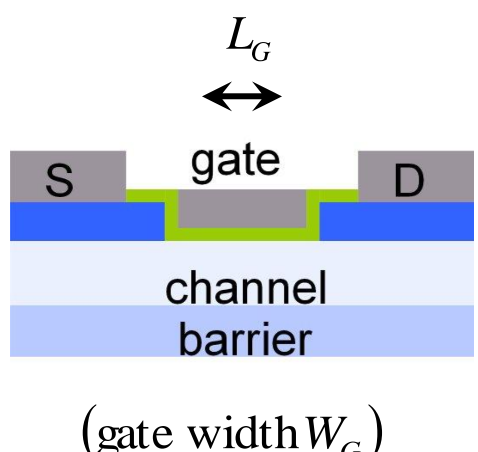


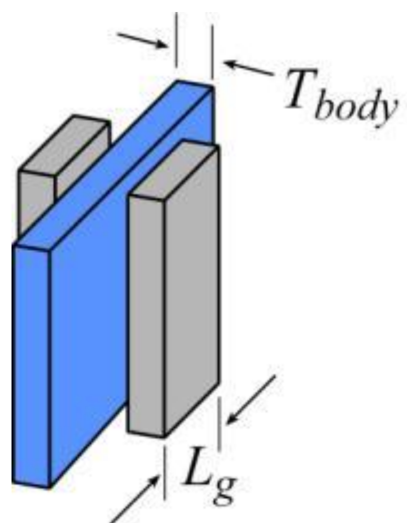


Problems: Low m*→ less charge. Low m* → more S/D tunneling. Narrow bandgap→ more band-band tunneling, impact ionization.



nm/VLSI MOSFET Scaling: Targets

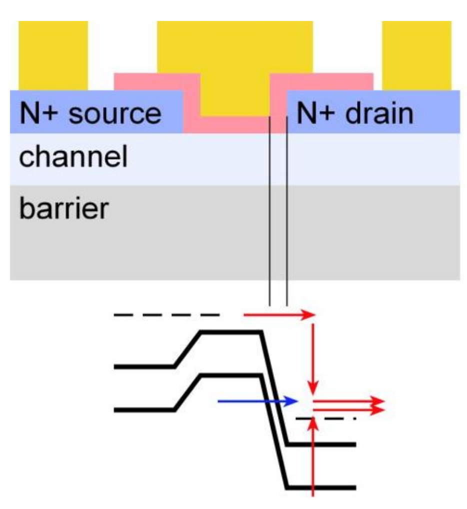




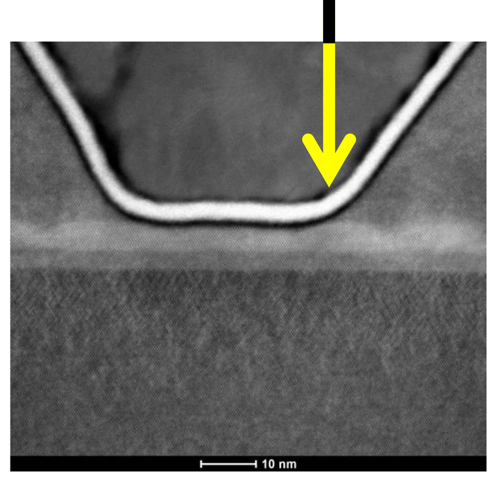
FET parameter	?? nm Node
gate length	~10 nm
current density (mA/mm)	1 mA/µm @0.5V
transport mass	
2DEG electron density	$3*10^{12}/cm^2$
gate-channel capacitance density	
dielectric equivalent thickness	0.5 nm (fin: 1.0 nm)
channel thickness	2.5 nm (fin: 5 nm)
channel state density	
contact resistivities	0.4 Ω-µm^2

Research III-V MOS: Lateral Spacers & Tunneling

Small S/D contact pitch

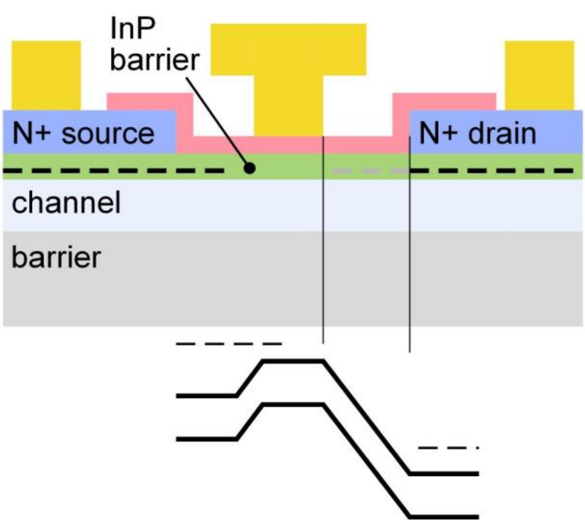


no lateral gate-drain space

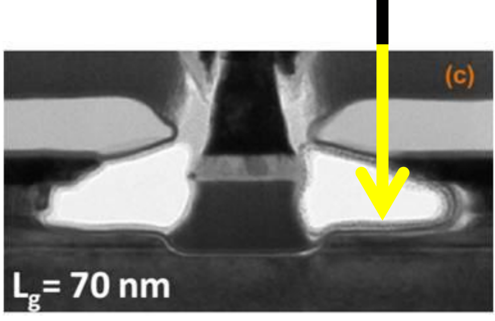


UCSB

MOS-HEMT with large contact pitch



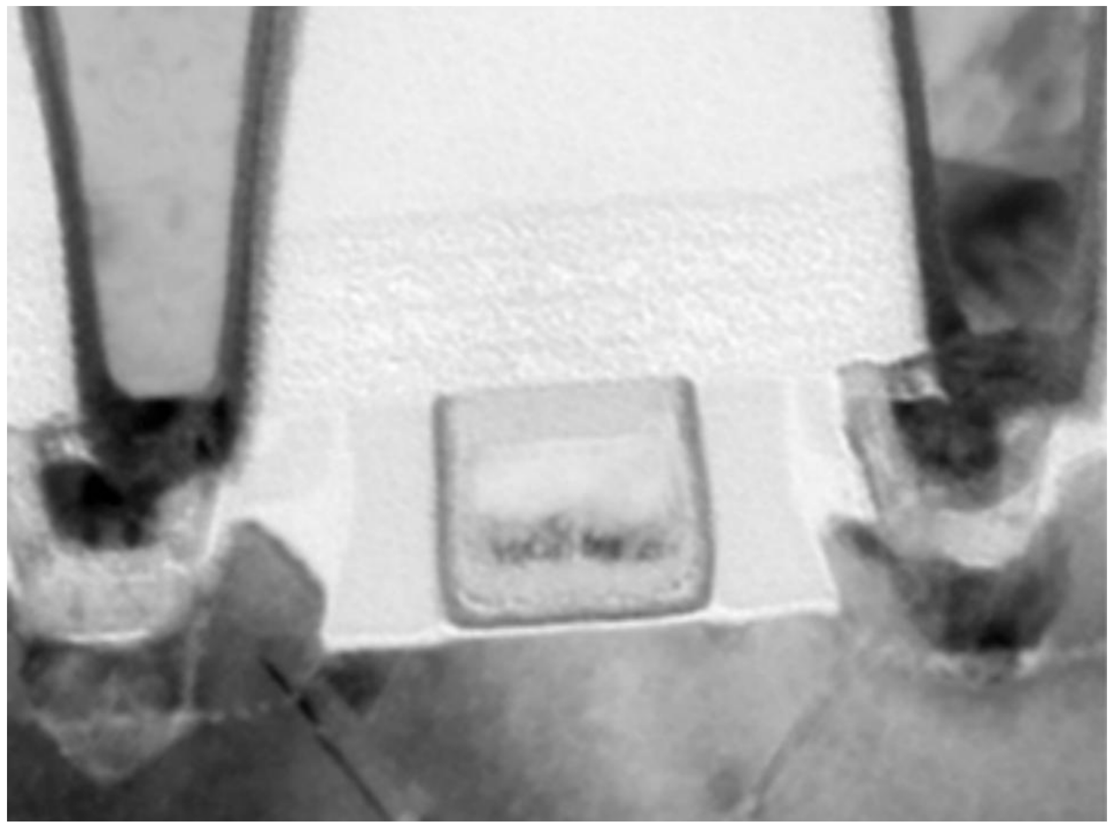
~70 nm gate-drain space



Lin, IEDM2013

We must build devices with small S/D pitch.

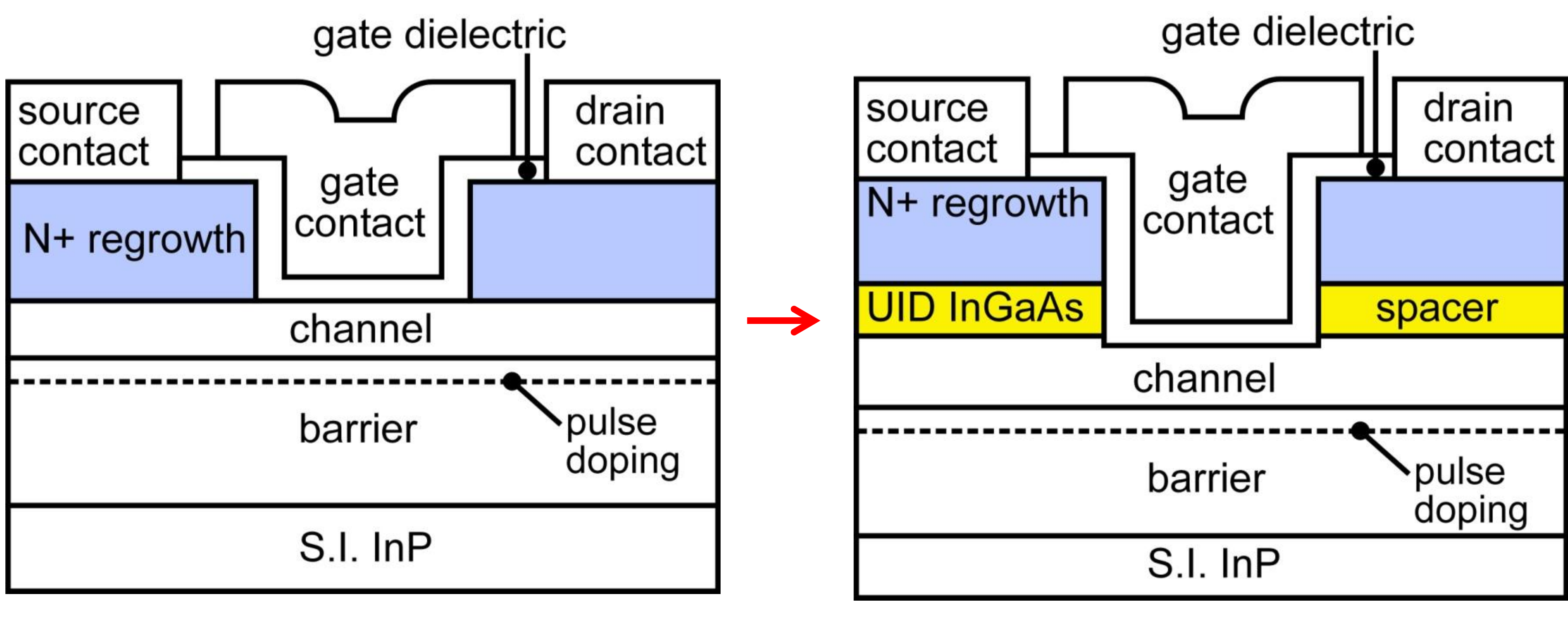
contact pitch ~ 3 times lithographic half-pitch
(technology node dimension)



Intel 35nm NMOS

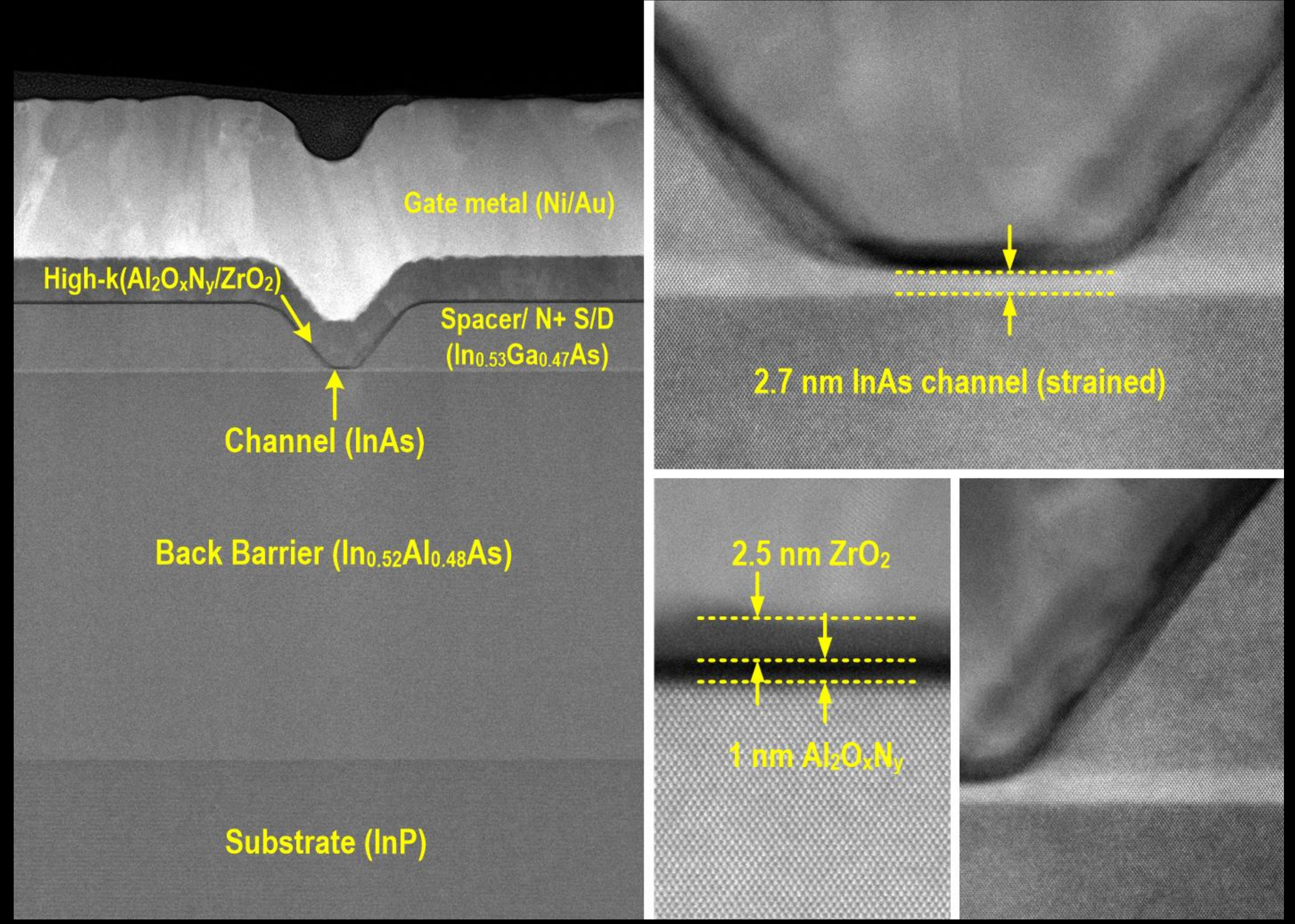
Small S/D pitch hard to realize if we require ~20-50nm lateral gate-drain spacers !

Vertical spacers: less leakage, small S/D pitch



Suppress band-band tunneling, S/D tunneling.
Long gate length, small footprint.

MOSFET: 2.5nm ZrO_2 / 1nm Al_2O_3 / 2.5nm InAs

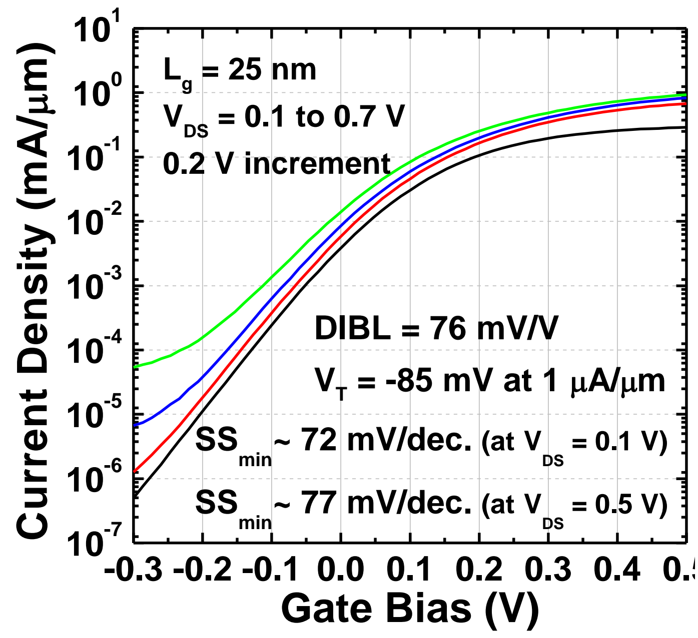


Courtesy of S. Kraemer (UCSB) *Heavy elements look brighter Lee *et al.*, 2014 VSLI Symposium

MOSFET: 2.5nm ZrO_2 / 1nm Al_2O_3 / 2.5nm InAs

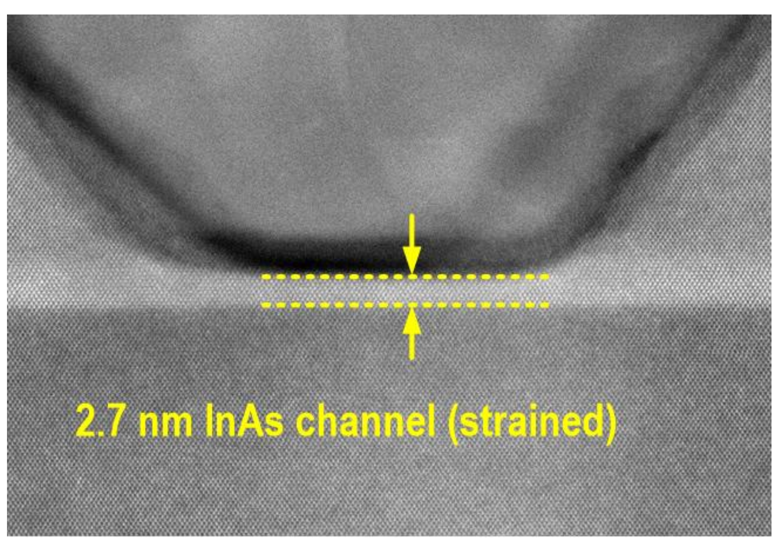
L_g = 25 nm
I_{on} = 500 μA/μm
(at I_{off}=100 nA/μm, V_{DD}=0.5 V)
V_{DS} = 0.1 to 0.7 V
0.2 V increment

Current Density (mA/μm)
g_m (mS/μm)
Gate Bias (V)



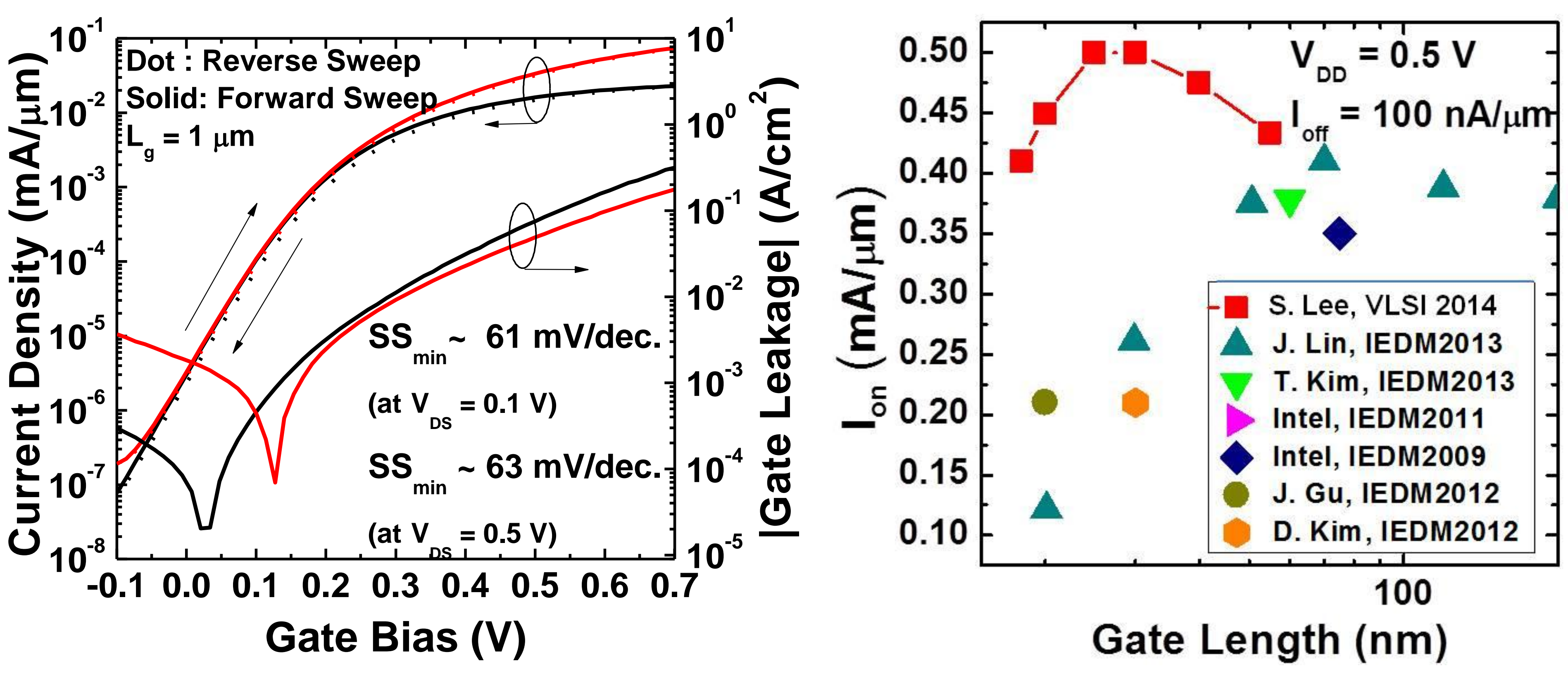
V_{GS} = -0.4 V to 0.7 V
0.1 V increment
R_{on} = 303 Ohm-μm
at V_{GS} = 0.7 V

Current Density (mA/μm)
Drain Bias (V)



Lee *et al.*, 2014 VSLI Symposium

MOSFET: 2.5nm ZrO_2/ 1nm Al_2O_3 / 2.5nm InAs



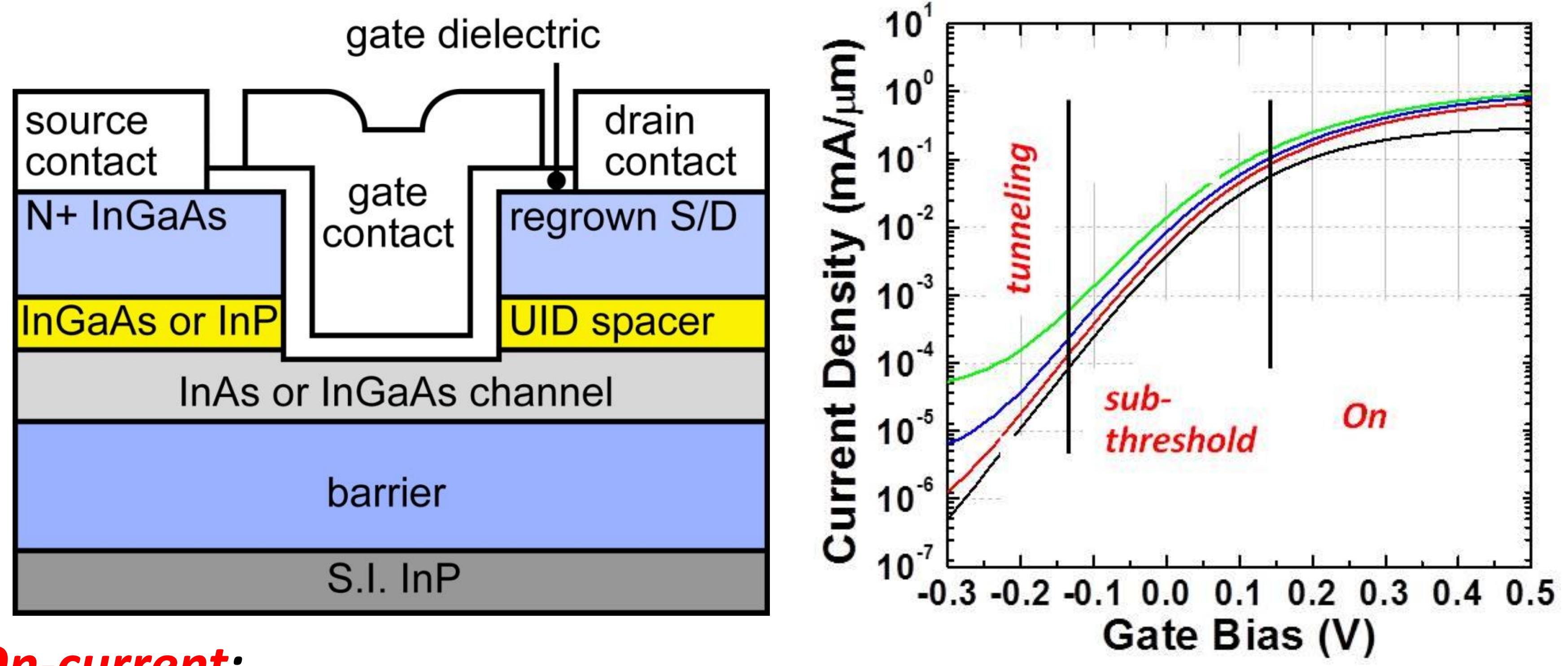
Performance:

Equals Intel 22nm NMOS finFET (HP), surpasses 14nm FDSOI

Dielectrics: V. Chobpattana, *et al.*, APL 2014

FETs: Lee *et al.*, 2014 VSLI Symposium

Channel, Dielectric, and Spacer Design



***On-current*:**

Thin dielectrics, thin channels; too thin ?→ scattering .

high indium content (not clear why).

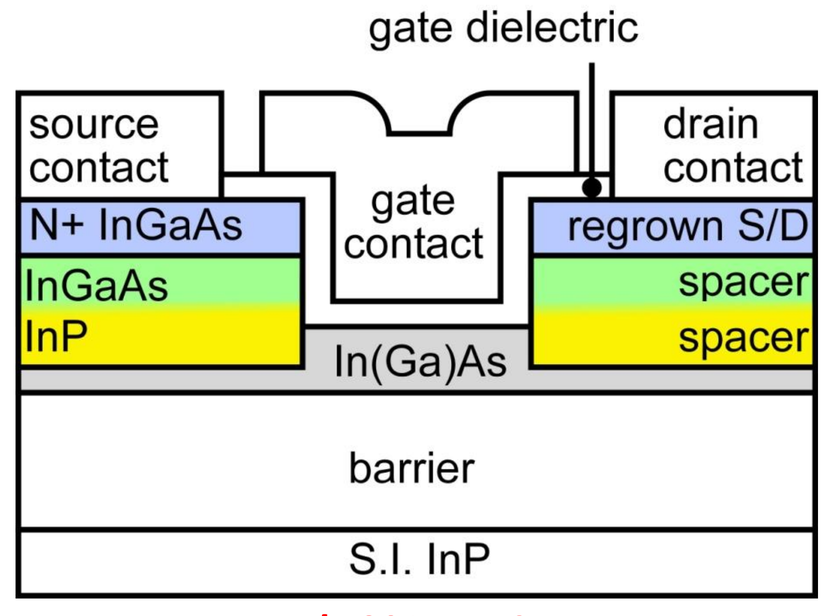
***Subthreshold*:**

dielectrics, thin channels, thick spacers

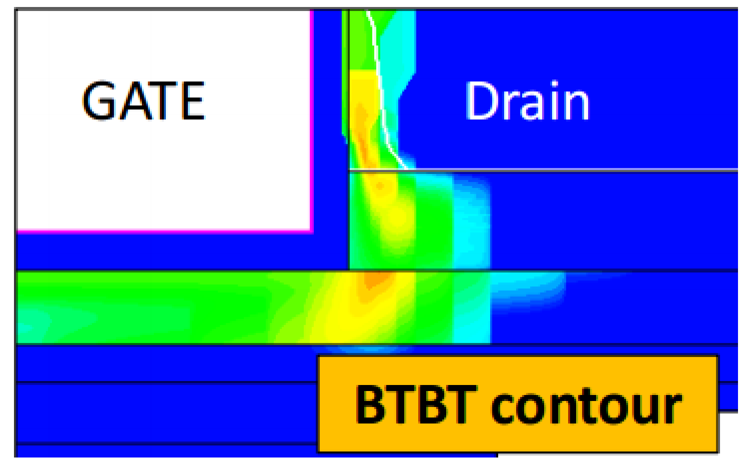
***Tunneling*:**

thin channels, low indium content, thick spacers

Double Heterojunction MOSFETs: Low Leakage



Huang *et al.*, 2014 DRC,
2014 Les Eastman Conf., 2014 IEDM (submitted)



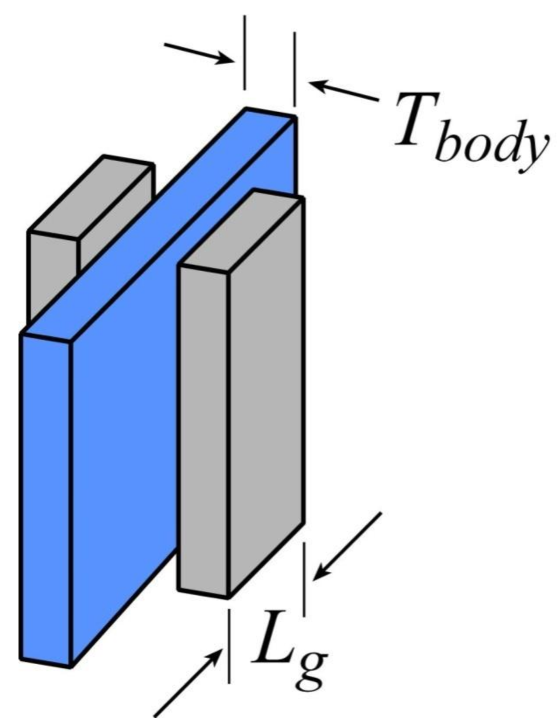
Byeongkyu Cho: MS report

Meet GP (1nA/μm), LP (30pA/μm), ULP (10 pA/μm) specs ?

InP spacer in highest-field region: BTBT

InGaAs spacer in lower-field regions: less added resistance

FinFETs by Atomic Layer Epitaxy: Why ?



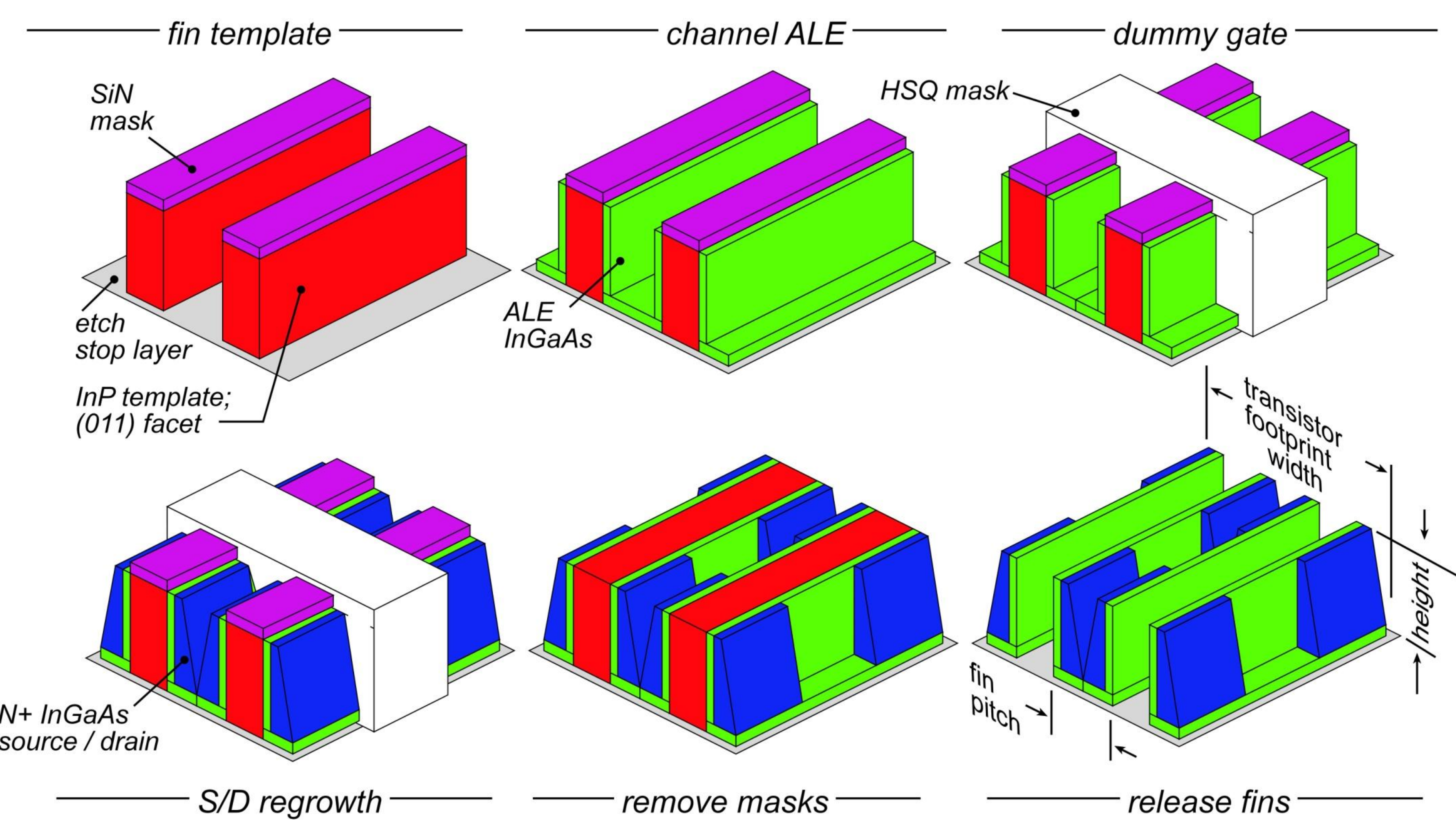
<u>FinFETs</u>:

body must be < 4 nm thick body for 8 nm L_g

Need smooth interfaces, precise fin thickness control

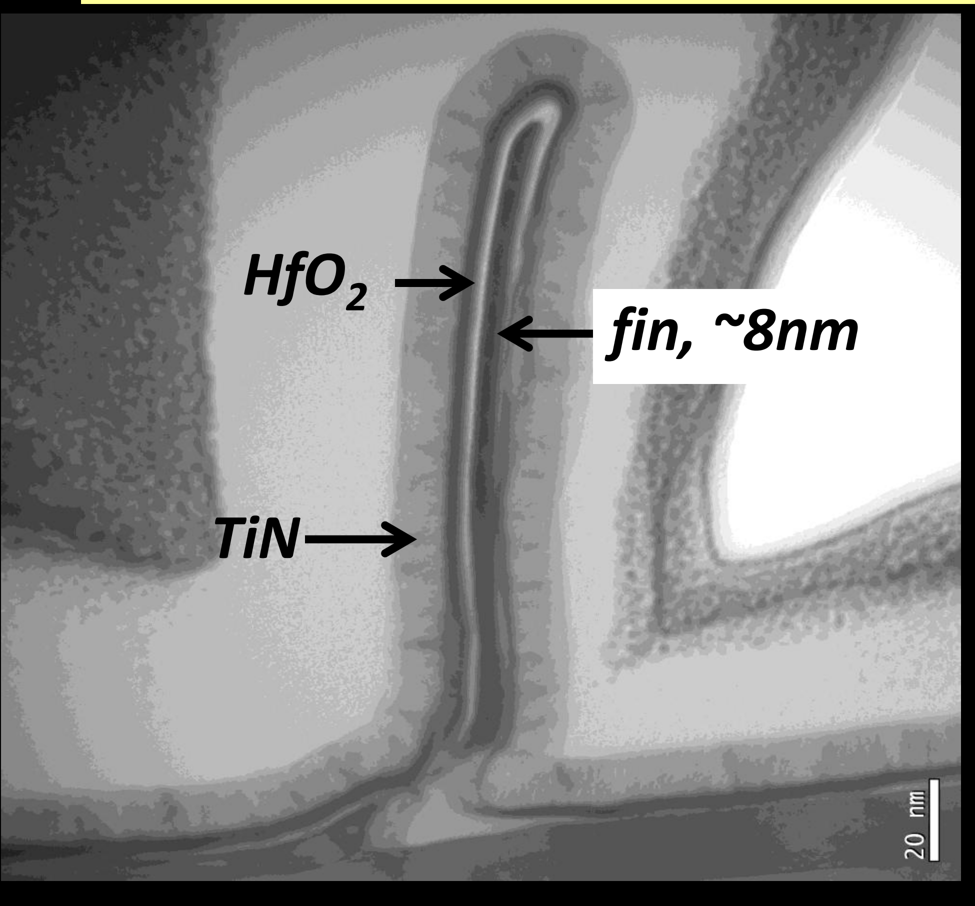
Is fin dry-etching feasible ? Damage ?

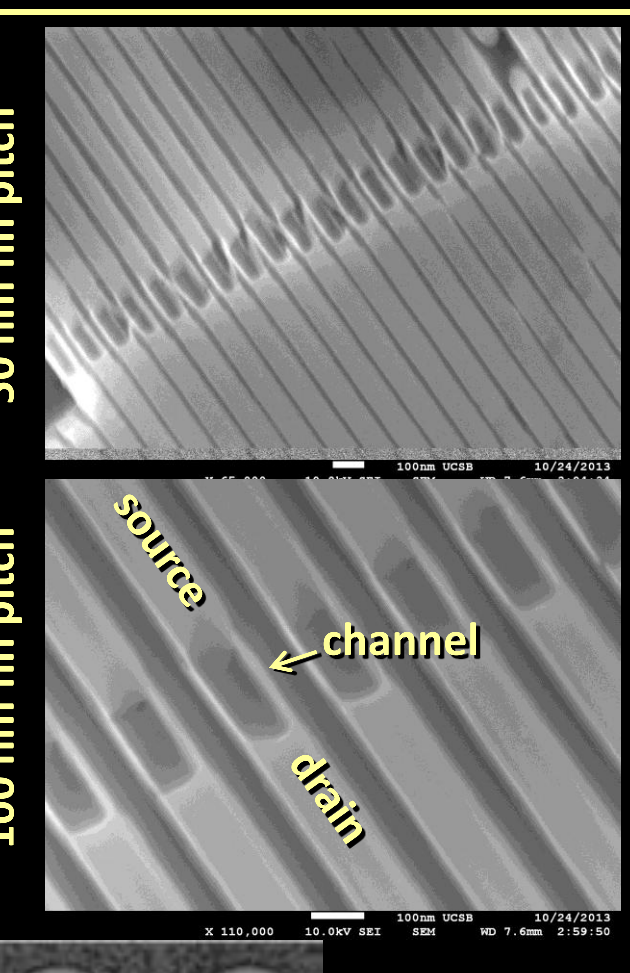
finFET by Sidewall Epitaxial Growth



Cohen-Elias *et al.*, DRC 2013

finFET by Sidewall Epitaxial Growth





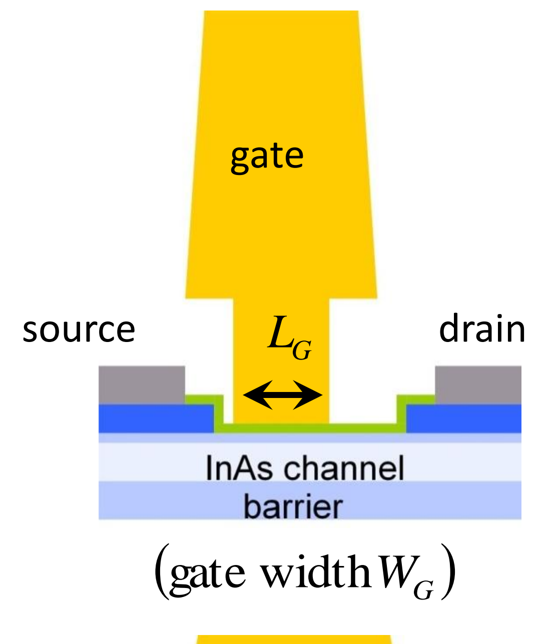
200 nm

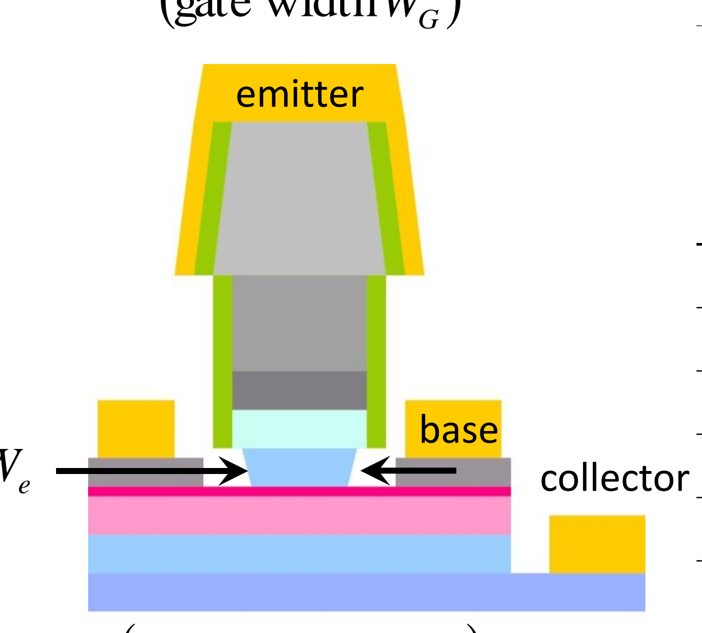
BTBT: need <5nm fins

Cohen-Elias *et al.*, DRC 2013

THz Transistors

THz Transistor Scaling Laws (to double bandwidth)





FET parameter	change
gate length	decrease 2:1
current density (mA/mm), g_m (mS/mm)	increase 2:1
transport mass	constant
2DEG electron density	increase 2:1
gate-channel capacitance density	increase 2:1
dielectric equivalent thickness	decrease 2:1
channel thickness	decrease 2:1
channel state density	increase 2:1
contact resistivities	decrease 4:1

HBT parameter	change
emitter & collector junction widths	decrease 4:1
current density (mA/mm^2)	increase 4:1
current density (mA/mm)	constant
collector depletion thickness	decrease 2:1
base thickness	decrease 1.4:1
emitter & base contact resistivities	decrease 4:1

2-3 THz Field-Effect Transistors are Feasible.

3 THz FETs realized by:

Regrown low-resistivity source/drain

Very thin channels, high-K dielectrics

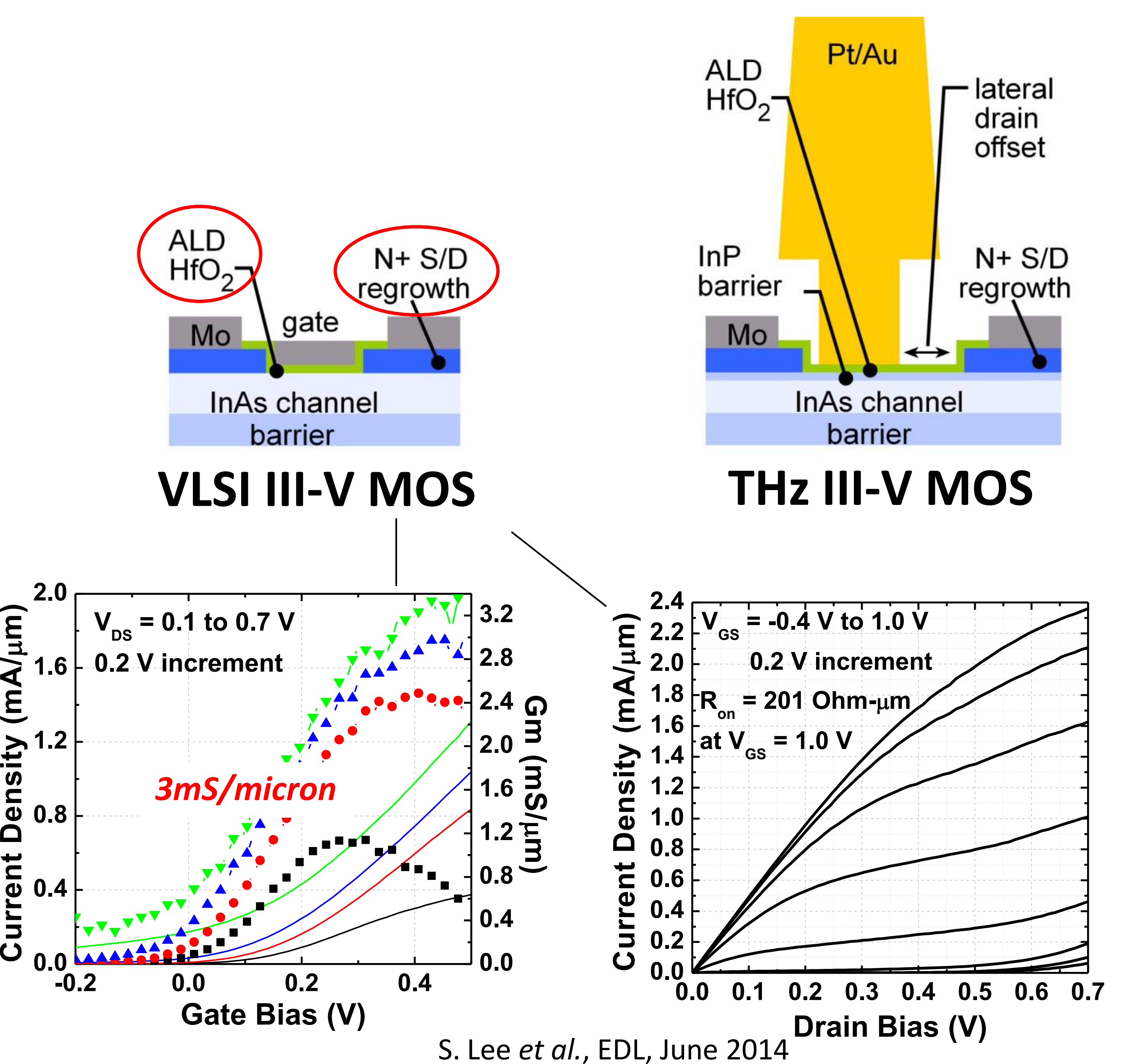
Gates scaled to 9 nm junctions

Impact:
Sensitive, low-noise receivers
from 100-1000 GHz.

3 dB less noise →
need 3 dB less transmit power.

gate length	36	18	9	nm
EOT	0.8	0.4	0.2	nm
well thickness	5.6	2.8	1.4	nm
effective mass	0.05	0.08	0.08	times m_0
# bands	1	1	1	--
S/D resistivity	150	74	37	Ω-µm
extrinisic g_m	2.5	4.2	6.4	mS/µm
on-current	0.55	0.8	1.1	mA/µm
f_τ	0.70	1.2	2.0	THz
f_{max}	0.81	1.4	2.7	THz

III-V MOS: Benefits THz HEMTs



S. Lee *et al.*, EDL, June 2014

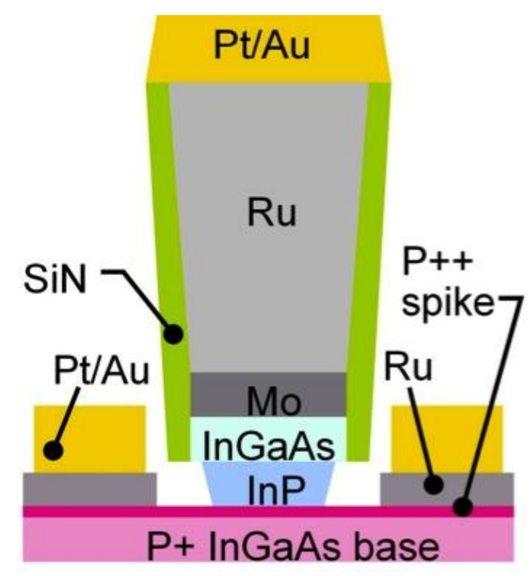
3 THz Bipolar Transistors are Feasible.

Needs

0.5 Ω-μm^2 resistivity contacts
ultra-shallow→ refractory

~100 mA/μm^2 current densities

16 nm junctions



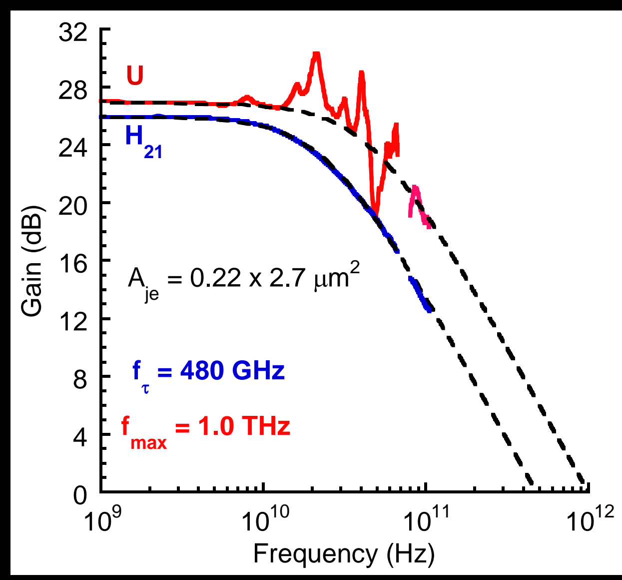
Scaling Node	64	32	16	nm
Emitter Width	64	32	16	nm
Resistivity	2	1	0.5	Ω-μm^2
Base Thickness	18	15	13	nm
Contact width	60	30	15	nm
Contact ρ	2.5	1.25	0.63	Ω-μm^2
Collector Width	180	90	45	nm
Thickness	53	37.5	26	nm
Current Density	36	72	140	mA/μm^2
f_τ	1.0	1.4	2.0	THz
f_{max}	2.0	2.8	4.0	THz

Impact:

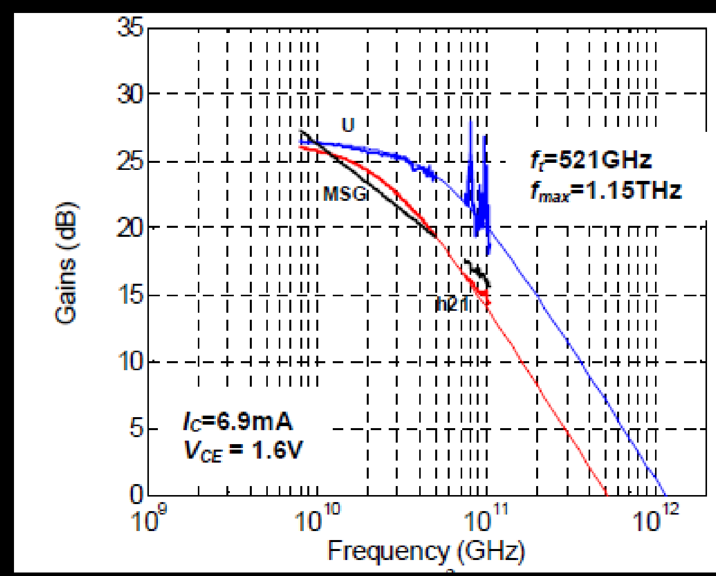
Efficient power amplifiers,
ADCs
complex mm-wave systems
from 100-1000 GHz.

THz InP HBTs: Performance @ 128 nm Node

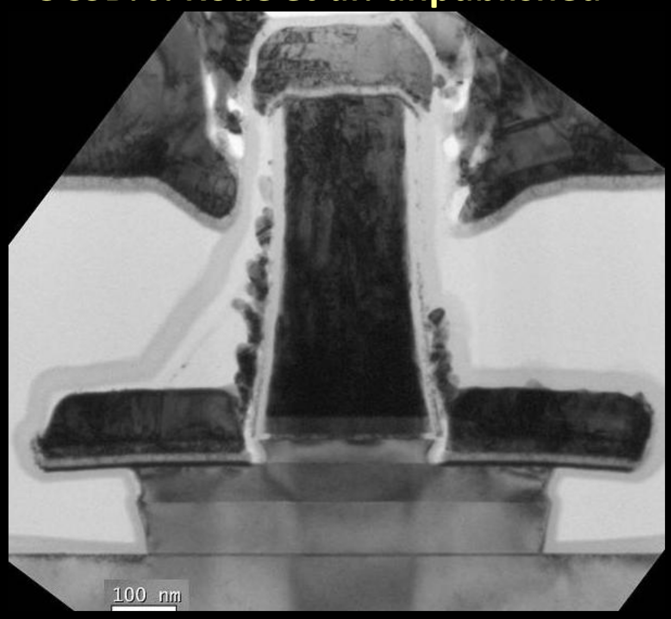
UCSB: V. Jain *et al*: 2011 DRC



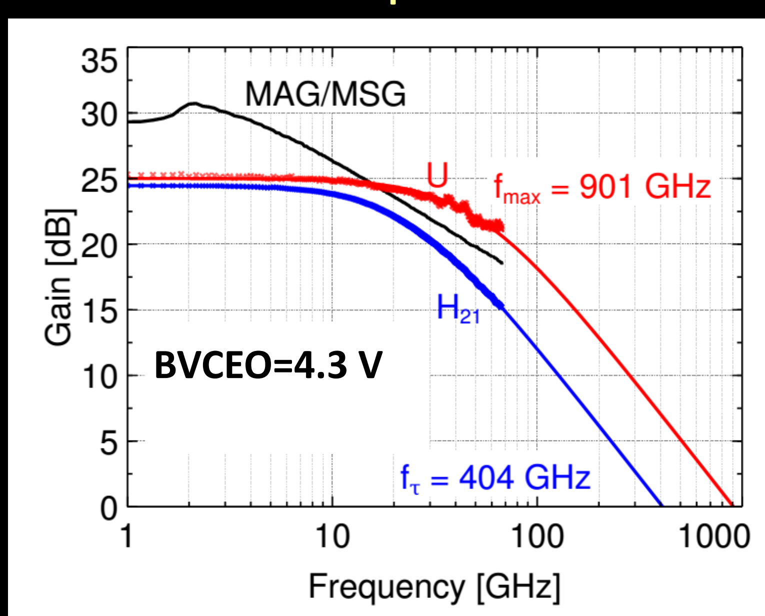
Teledyne: M. Urteaga *et al*: 2011 DRC



UCSB: J. Rode *et al*: unpublished



UCSB: J. Rode *et al*: unpublished

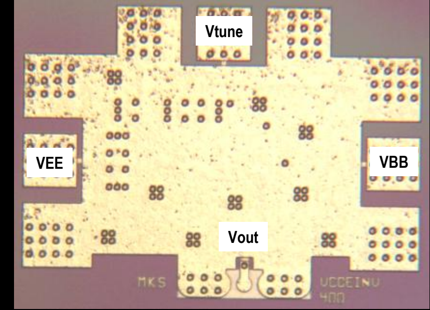


InP HBT Integrated Circuits: 600 GHz & Beyond

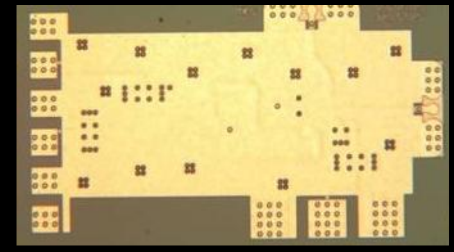
TELEDYNE SCIENTIFIC COMPANY
A Teledyne Technologies Company

UCSB

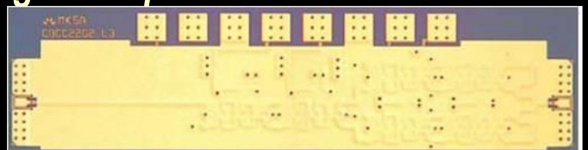
614 GHz fundamental VCO
M. Seo, TSC / UCSB



340 GHz dynamic frequency divider
M. Seo, UCSB/TSC
IMS 2010

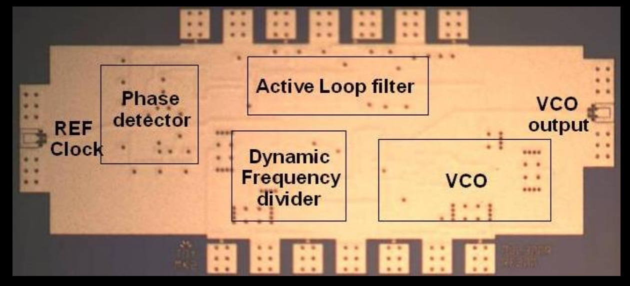


620 GHz, 20 dB gain amplifier
M Seo, TSC
IMS 2013

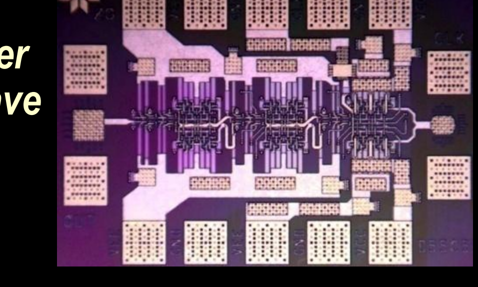


Not shown: 670 GHz HBT amplifier
J. Hacker, TSC, IMS 2013

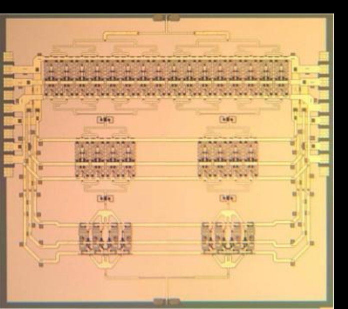
300 GHz fundamental PLL
M. Seo, TSC
IMS 2011



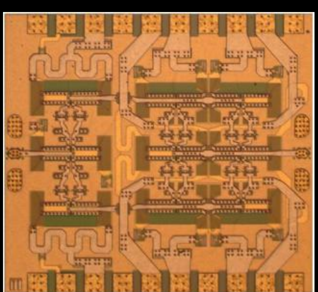
204 GHz static frequency divider (ECL master-slave latch)
Z. Griffith, TSC
CSIC 2010



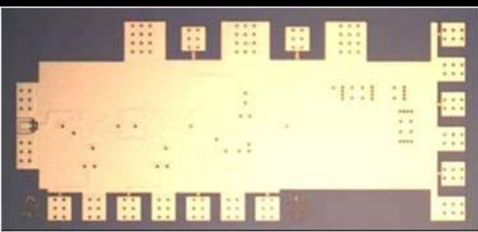
220 GHz 180 mW power amplifier
T. Reed, UCSB
CSICS 2013



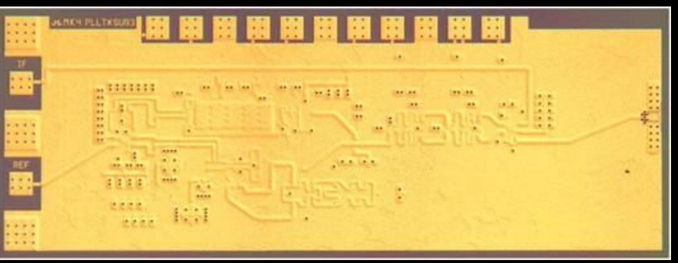
81 GHz 470 mW power amplifier
H-C Park UCSB
IMS 2014



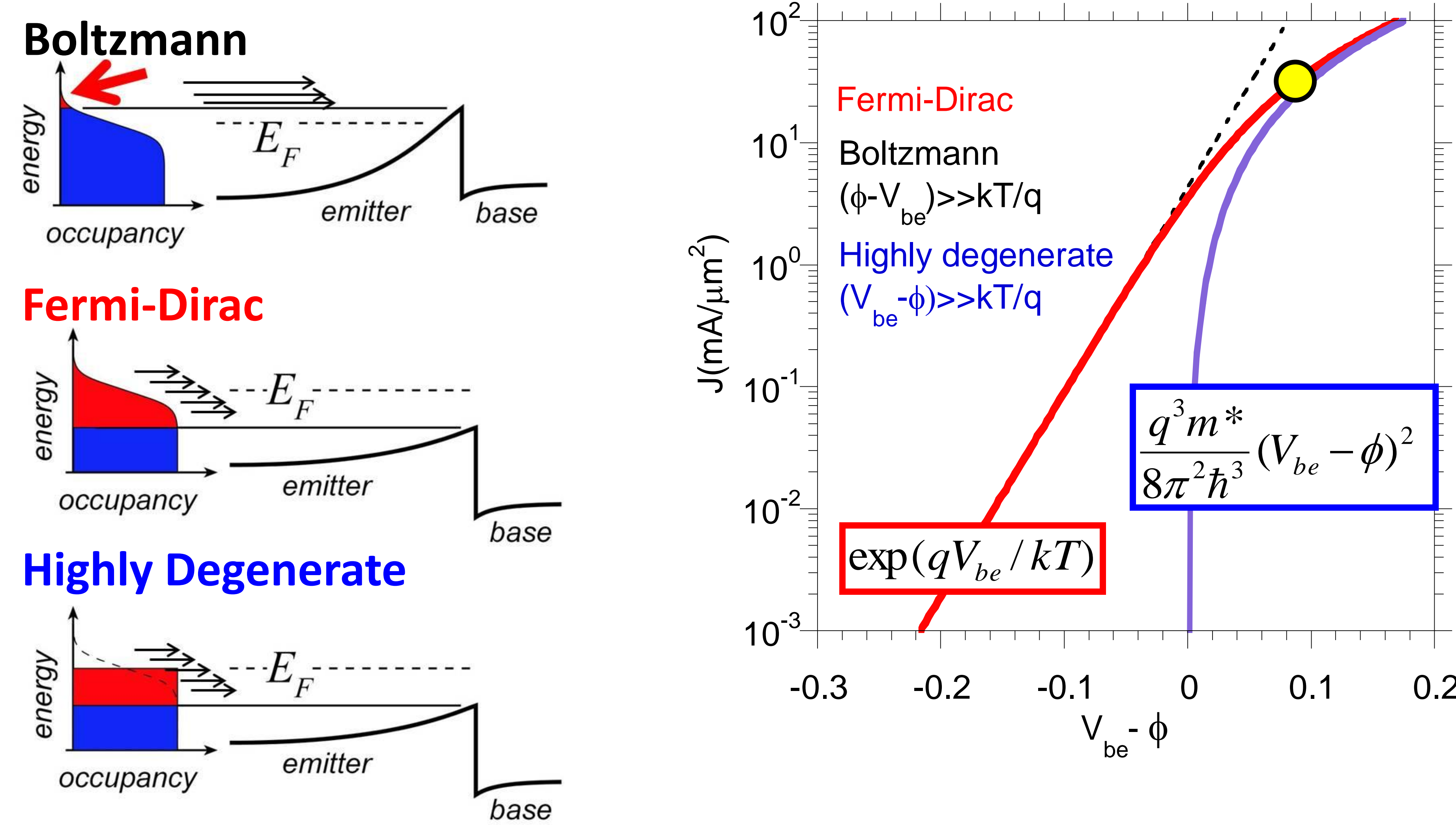
Integrated 300/350GHz Receivers:
LNA/Mixer/VCO
M. Seo TSC



600 GHz Integrated Transmitter
PLL + Mixer
M. Seo TSC



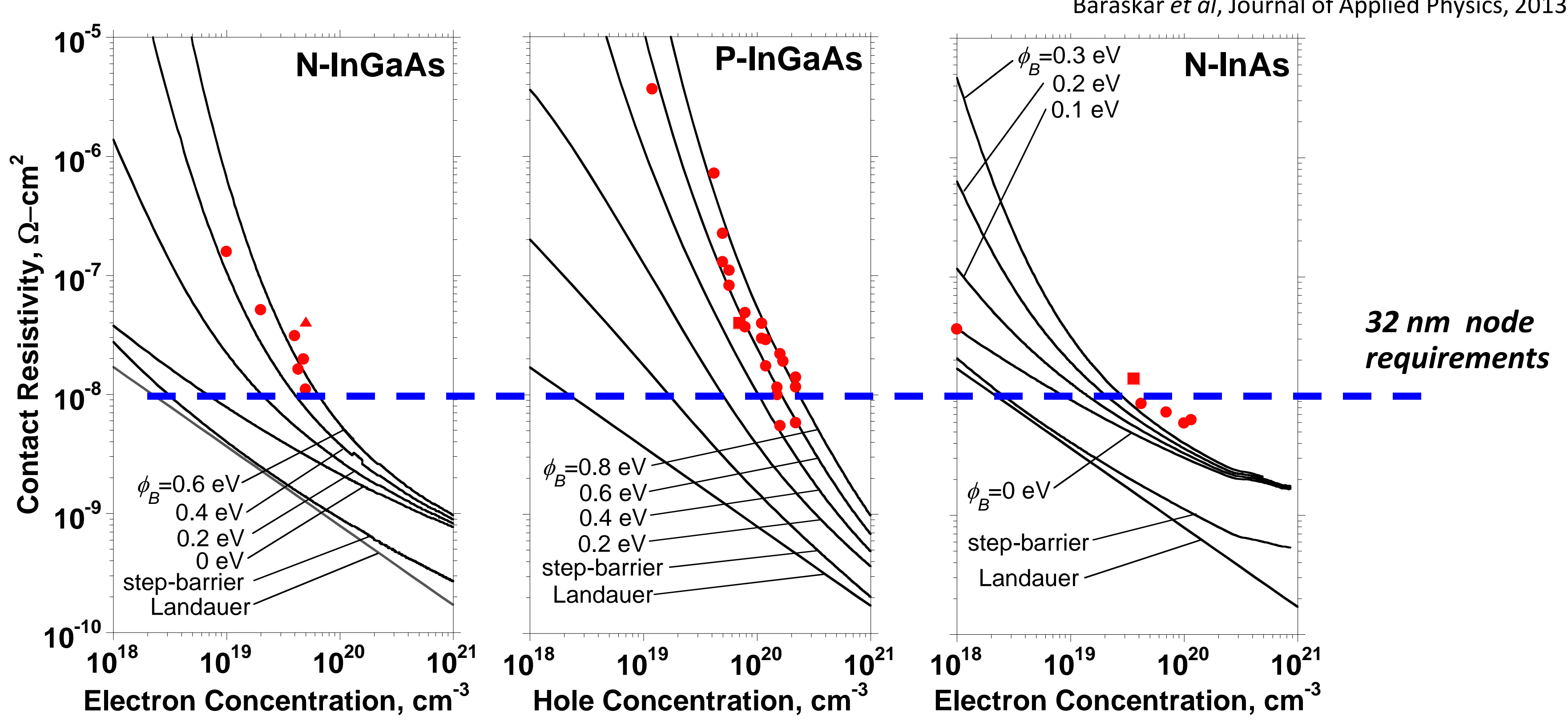
Extreme Currents: Quadratic I-V Characteristics



High currents→ transconductance less than qI/kT → bandwidth decreases

Highly degenerate limit→ Transconductance varies as $J^{1/2}(m^*)^{1/2}$ → must increase m^*

Ultra Low-Resistivity Refractory Contacts



Refractory: robust under high-current operation.

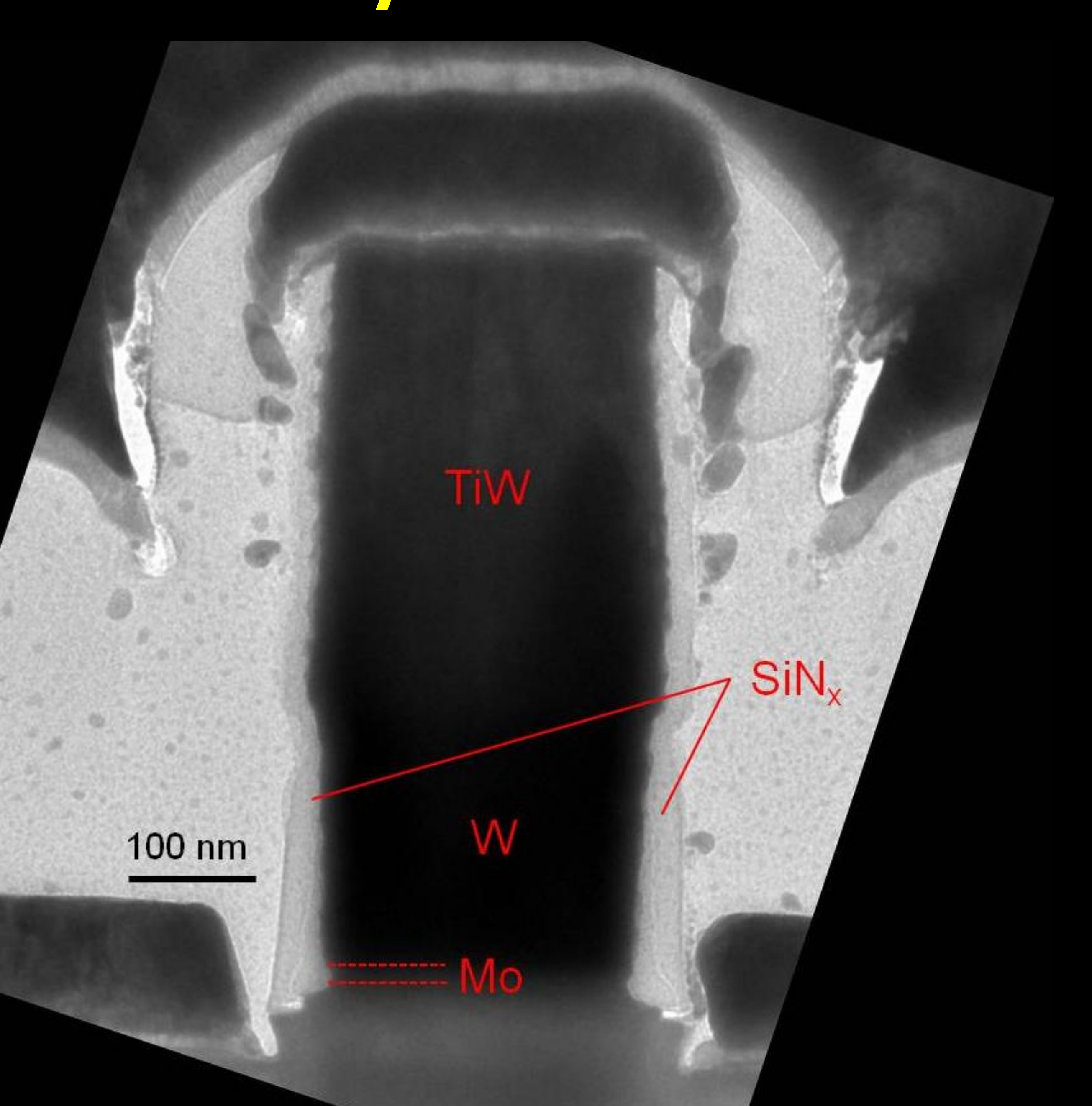
Low penetration depth: ~ 1 nm.

Performance sufficient for 32 nm /2.8 THz node.

Landauer:

$$\rho_c = \left(\frac{\hbar}{q^2}\right)\cdot\left(\frac{8\pi}{3}\right)^{2/3}\cdot\frac{1}{T}\cdot\frac{1}{n^{2/3}}$$

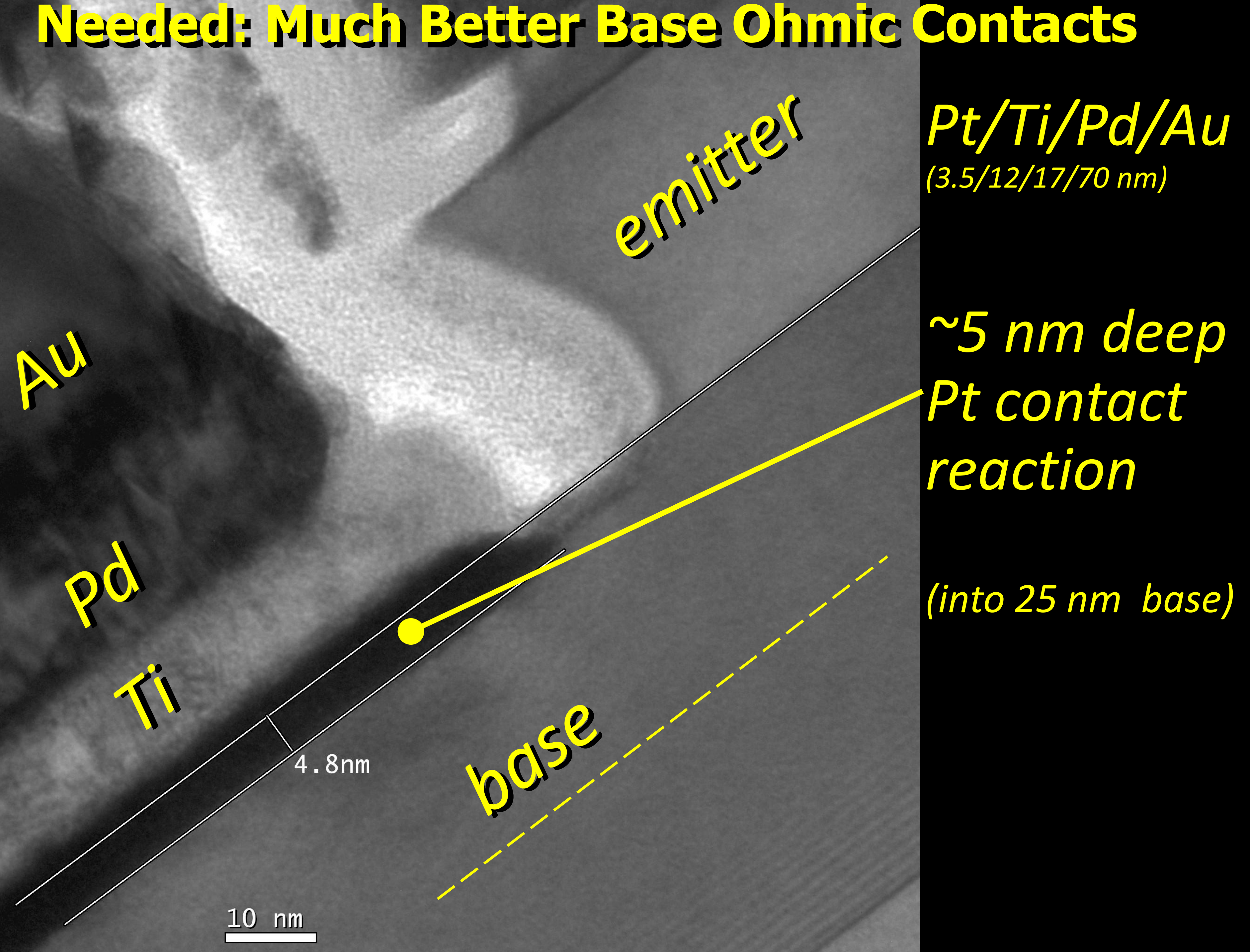
Refractory Emitter Contact and Via



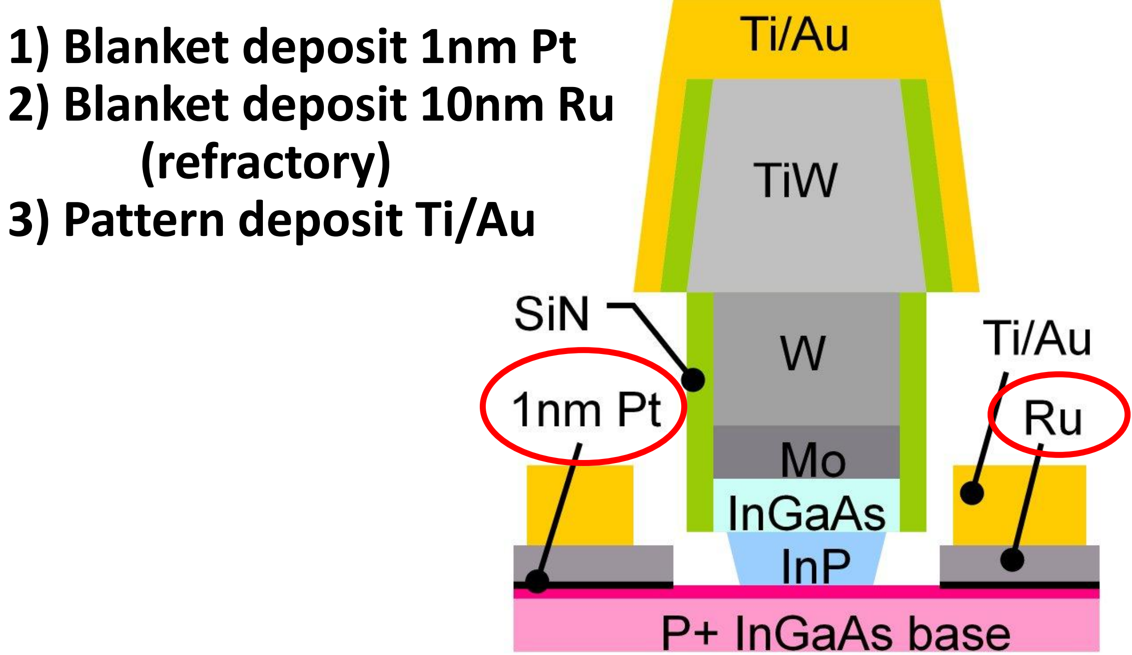
low-resistivity Mo contact

sputtered, dry-etched W/TiW via

Refractory metals→ high currents

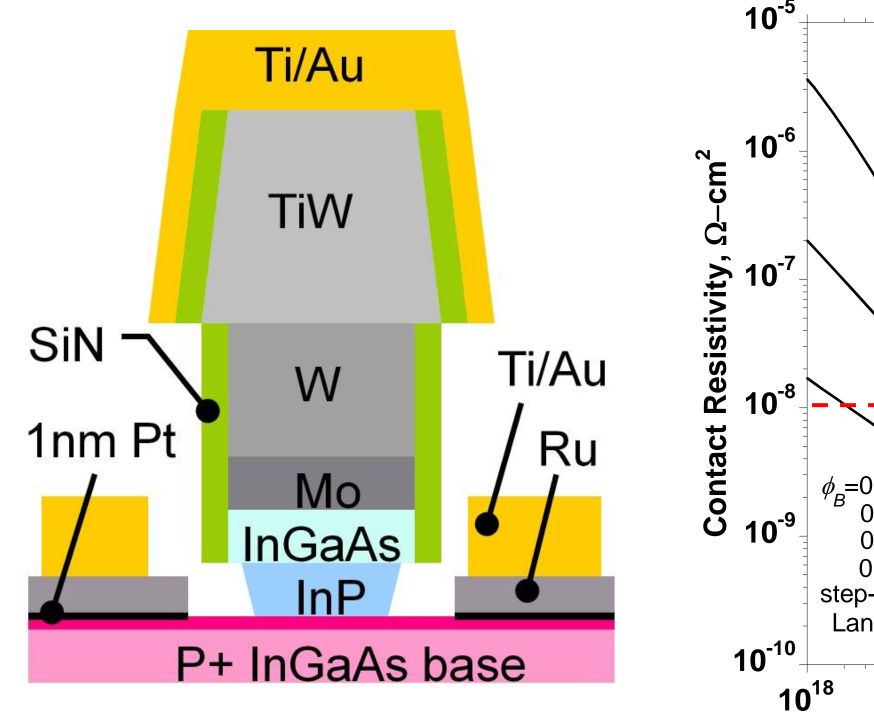

Needed: Much Better Base Ohmic Contacts
emitter
Au
Pd
Ti
base
4.8nm
10 nm
Pt/Ti/Pd/Au
(3.5/12/17/70 nm)
~5 nm deep
Pt contact
reaction
(into 25 nm base)

Two-Step Base Contact Process



Surface not exposed to photoresist→ less surface contamination
1 nm Pt layer: 2-3 nm surface penetration
Thick Au: low metal resistance

Two-Step Base Contact Process



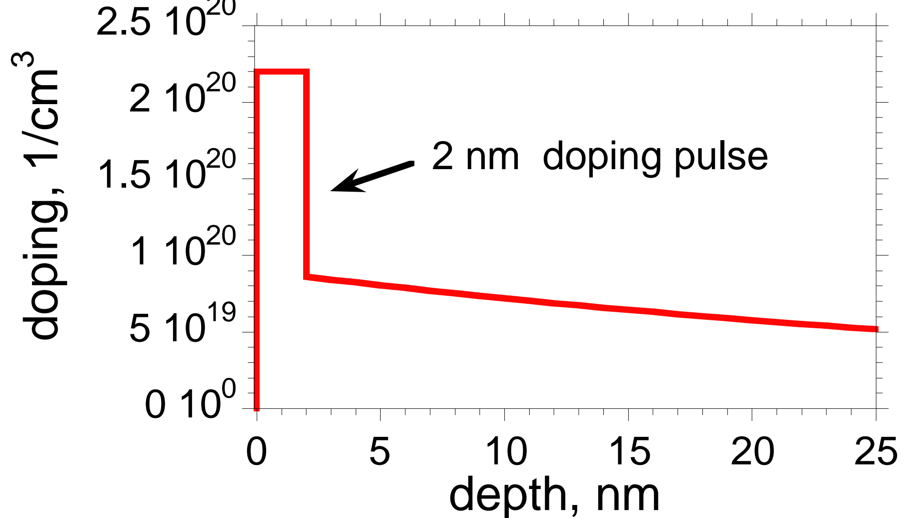
P-InGaAs

Contact Resistivity, Ω–cm²

Hole Concentration, cm⁻³

ϕ_B=0.8 eV
0.6 eV
0.4 eV
0.2 eV
step-barrier
Landauer

32 nm node requirement

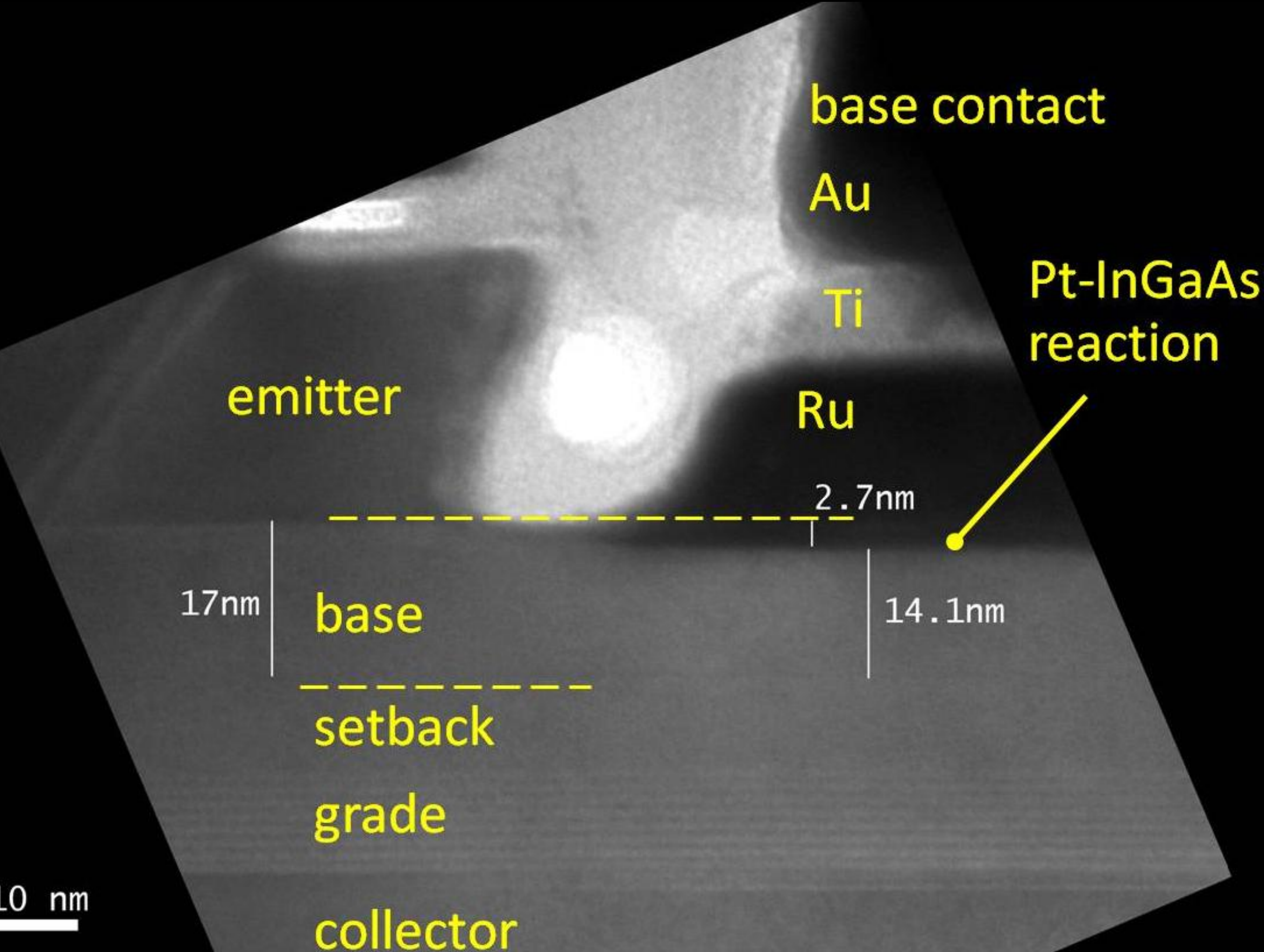


Increased surface doping:
reduced contact resistivity,
increased Auger recombination.

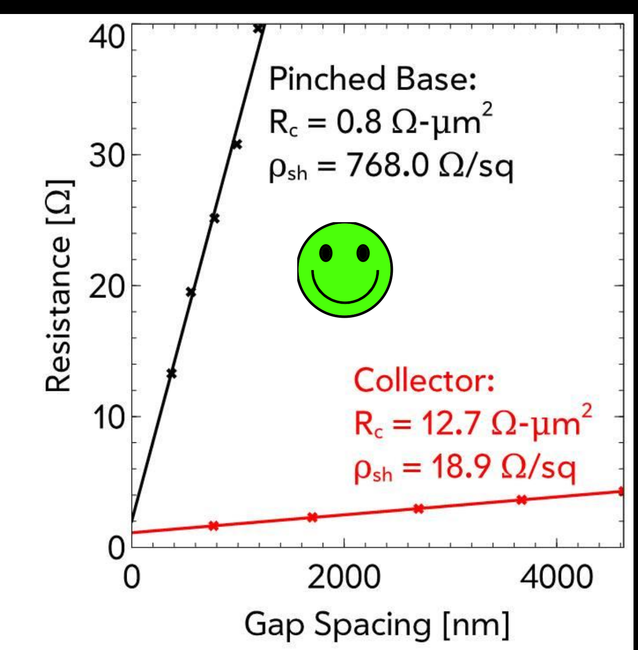
→ Surface *doping spike 2-5nm thick.*

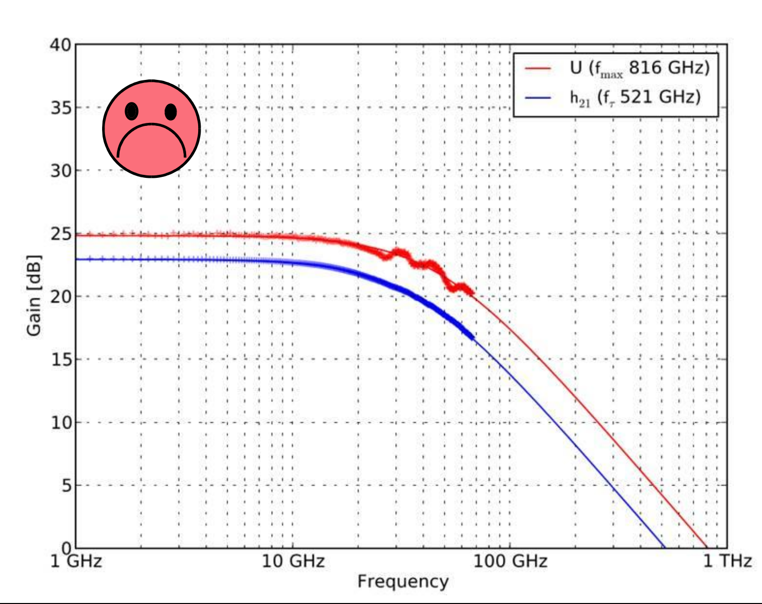
Need limited-penetration metal

"Near-Refractory" Base Ohmic Contacts



THz InP HBTs

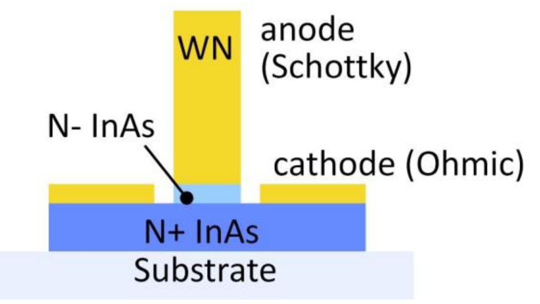




a few more things to fix ...

1-D, 30 THz diodes

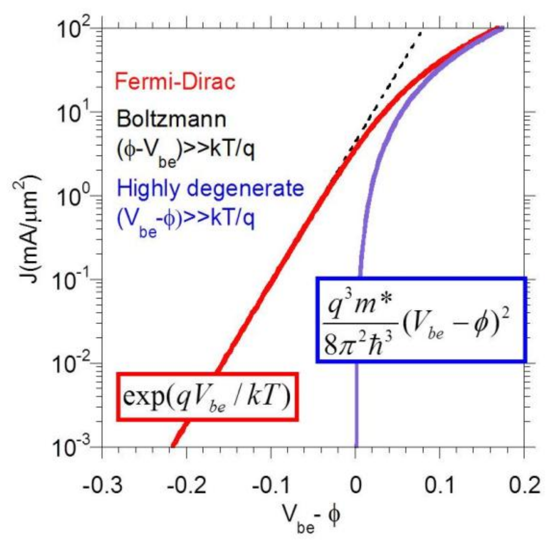
1-D (nm) Diodes for 30THz mixing/detection



$$\text{Transit time}: \tau_{transit} \propto T_{depl} / v_{Fermi} \rightarrow \text{make } T_{depl} \approx 3.5\text{ nm}$$

$$\text{Depletion capacitance}: C_{depl} \approx \varepsilon A / T_{depl} \rightarrow \text{make } A \text{ very small.}$$

$$\text{Junction impedance}: r_{on} \stackrel{?}{=} kT / qI \rightarrow \text{make } J = I / A \text{ very large}$$

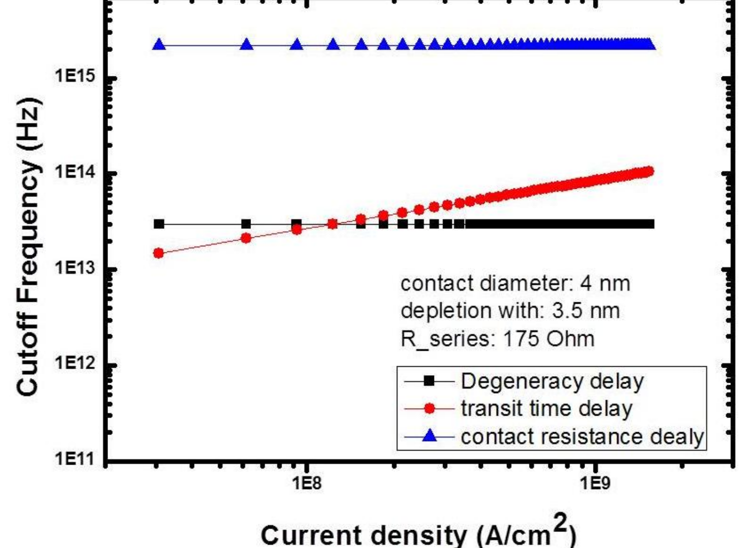


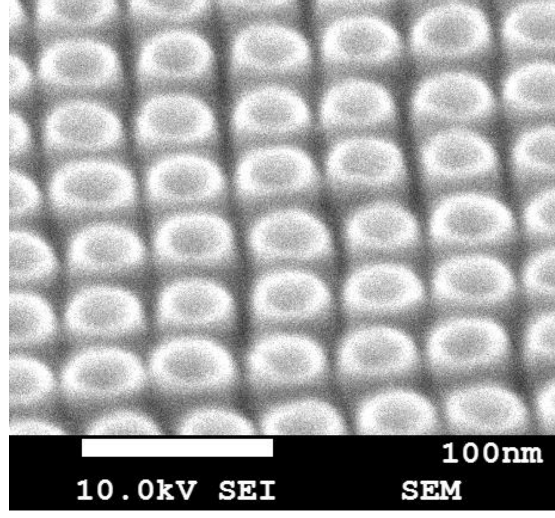
big problem: degenerate injection, $r_{on} >> kT / qI$

$$\text{Solution}: \text{array of 1-D diode junctions} \rightarrow r_{on} = \pi\hbar / q^2$$

On-state time constant:

$$r_{on} C_{depl} = (\pi\hbar / q^2) \cdot (\varepsilon A / T_{depl}) \propto A / T_{depl} \rightarrow \text{make area small}$$





THz & nm Transistors: What's Needed

What do we want ?

VLSI: lots of on-current, no off-current, low voltage

THz: high frequencies. Low noise, high power, high gain.

How do we get it ?

Extreme current densities

Extremely thin dielectrics (FETs)

Extremely low-resistivity contacts

few-nm critical dimensions

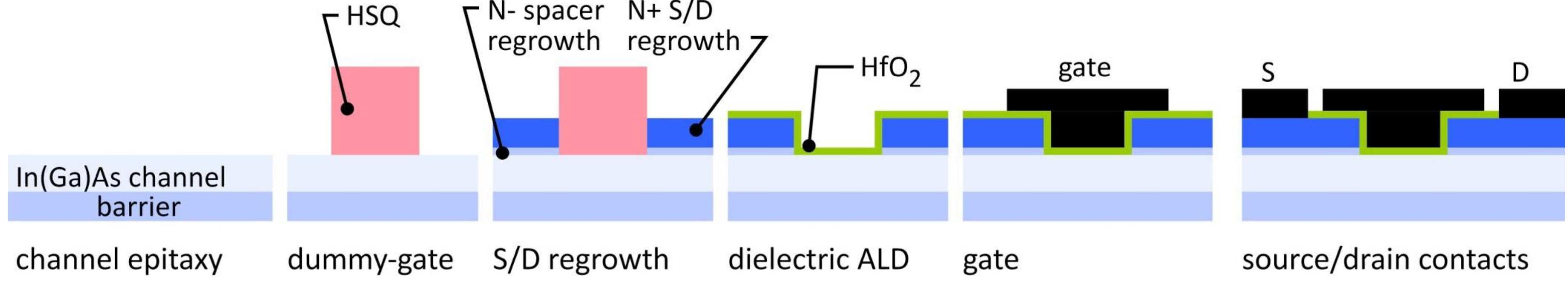
...and sufficient states to carry the current

(end)

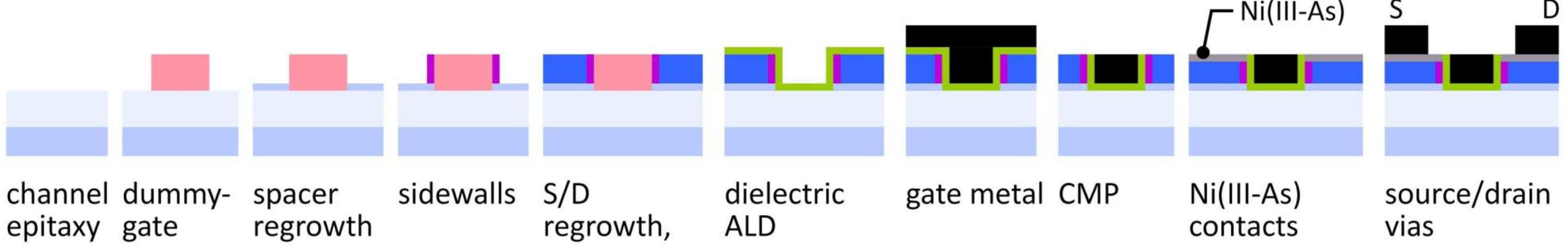
Backup slides

InAs/InGaAs MOSET: Process Flow

Development process flow



Manufacturing process flow



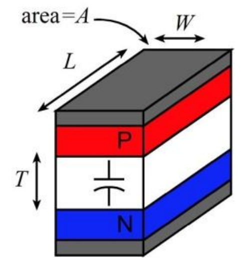
Development process flow <u>does not provide</u> a small S/D contact pitch,
But: in manufacturing, the vertical spacer <u>can provide</u> a small S/D contact pitch.

set aside slides

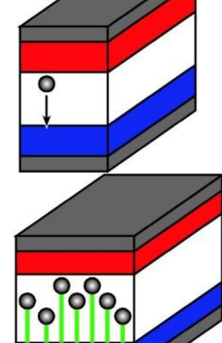
Transistor Design: What Matters ?

Scaling: How (V,I,R,C,τ) varies with geometry

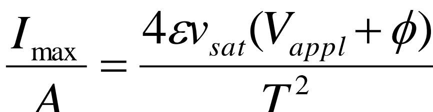
Depletion Layers



$$C = \varepsilon \cdot \frac{A}{T}$$

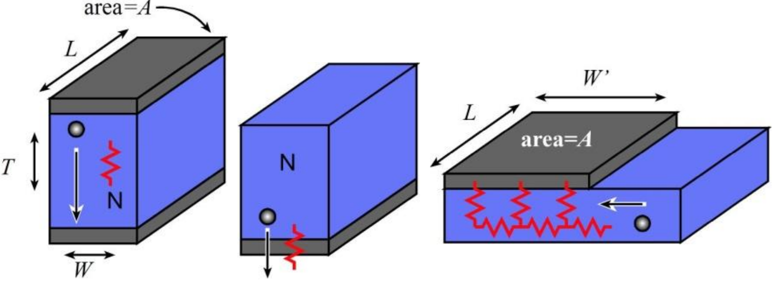


$$\tau = \frac{T}{2v}$$



$$\frac{I_{\max}}{A} = \frac{4\varepsilon v_{sat}(V_{appl} + \phi)}{T^2}$$

Bulk and Contact Resistances

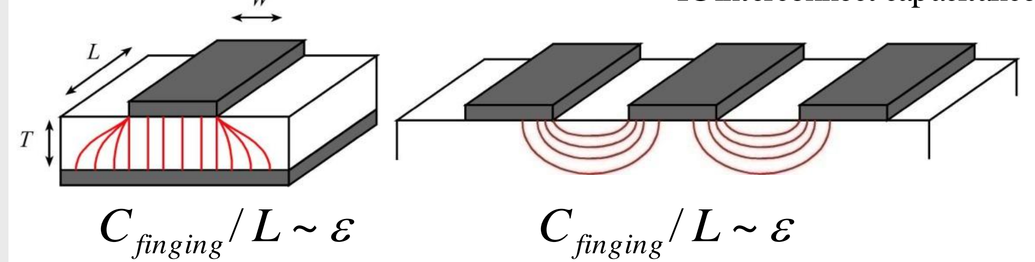


$R \cong \rho_{contact} / A$ contact terms dominate

Fringing Capacitances

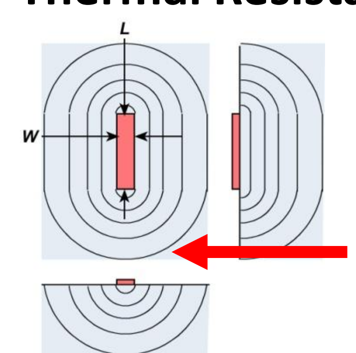
FET fringing capacitances

IC interconnect capacitances



$C_{finging} / L \sim \varepsilon$ $C_{finging} / L \sim \varepsilon$

Thermal Resistance

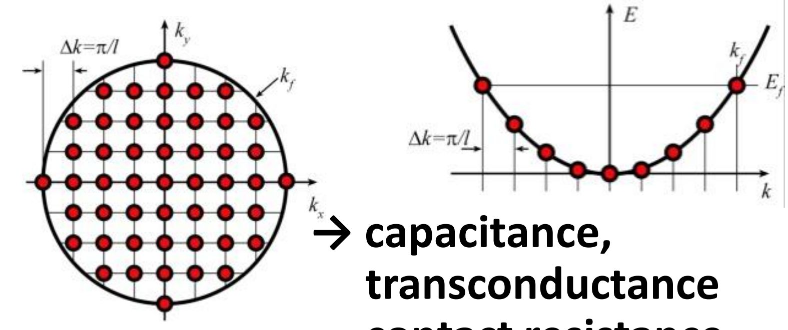


L

$$\Delta T_{IC} \propto \frac{P_{IC}}{K_{th} L}$$

$$\Delta T_{\text{transistor}} \sim \frac{P}{\pi K_{th} L} \ln\left(\frac{L}{W}\right)$$

Available states to carry current

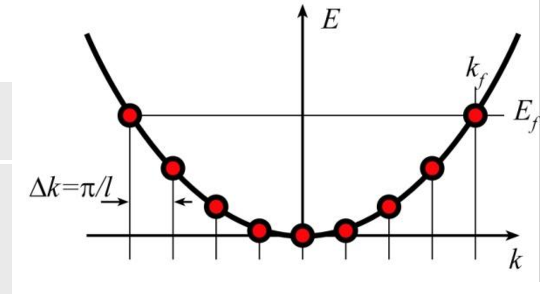


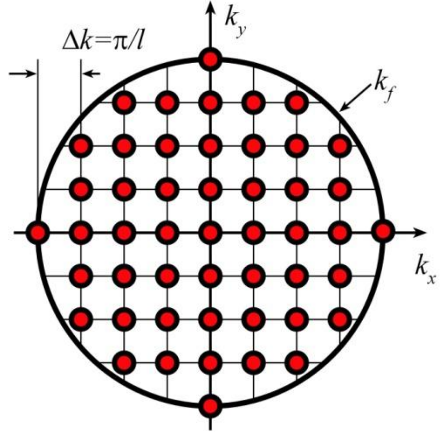
→ **capacitance, transconductance contact resistance**

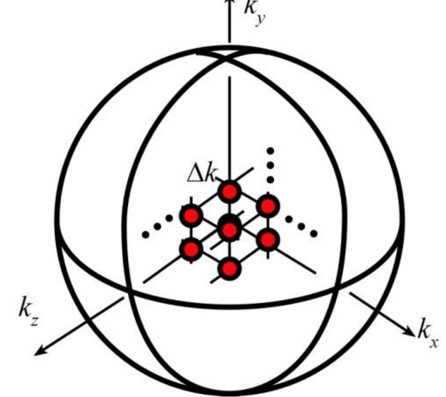
THz & nm Transistors: State Density Limits

$1\text{-D conductivity}: \sigma = q^2/\pi\hbar$ (Landauer)

	2-D: FET	3-D: Bipolar
	S gate D channel barrier	
capacitance	$C_{DOS} = \dfrac{q^2 m^*}{2\pi\hbar^2}$	
current	$J_{sheet} = \dfrac{2^{3/2} q^{5/2} (m^*)^{1/2} V^{3/2}}{3\pi^2\hbar^2}$	$J = \dfrac{q^3 m^* V^2}{4\pi^2\hbar^3}$
conductivity	$\sigma_c = \left(\dfrac{q^2}{\hbar}\right)\cdot\left(\dfrac{2}{\pi^3}\right)^{1/2}\cdot n^{1/2}$	$\sigma_c = \left(\dfrac{q^2}{\hbar}\right)\cdot\left(\dfrac{3}{8\pi}\right)^{2/3}\cdot n^{2/3}$







available states / energy determines
on-state capacitance,
current & transconductance,
contact/access resistance