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Japanese Journal of Applied Physics 53, 065503 (2014)
http://dx.doi.org/10.7567/JJAP.53.065503

REGULAR PAPER

Formation of InGaAs fins by atomic layer epitaxy on InP sidewalls

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Received December 18, 2013; accepted April 17, 2014; published online June 2, 2014

We describe a fabrication process which forms InGaAs fins with sub 10 nm thickness and 180 nm height. The process flow requires no semiconductor dry-etch, thereby avoiding surface damage arising from such processes. Instead, InGaAs fins are formed using nanometer controlled atomic layer epitaxial growth, using tertiarybutylarsine, upon InP sidewall which are eventually selectively etched. Such fins can serve as channels of field effect transistors, allowing excellent electrostatics and with potentially high operating current per fin.
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1. Introduction

As the gate length of field effect transistors (FETs) in VLSI is reduced, the channel thickness must be proportionally reduced to maintain strong electrostatic control of the channel potential by the gate and thereby suppress short-channel effects.[1] Even for finFETs,[2] whose electrostatics are superior to those of planar FETs, for low drain-induced barrier lowering (DIBL) and steep subthreshold characteristics the fin thickness must be at most half the channel length.[1] Thus for a 22 nm gate length, the fin must be less than 11 nm thick. State of the art finFETs have been fabricated using dry-etch processes, exhibiting excellent off-state performance, but greater than 50 mV/V DIBL was observed for a device with 60 nm gate length and 30 nm fin thickness.[2]

To further reduce the gate length, to 11 nm or less, the finFET body thickness must be reduced to a few nanometers, hence nanometer control of this dimension is essential. Isotropic wet-etching cannot produce highly anisotropic structures such as fins. Even with highly directional dry-etching, if the fin height exceeds the fin thickness by a large ratio, then small deviations from vertical in the etched edge sidewall profile will lead to large fractional variations with height in the fin thickness; a 10 nm tall fin with 3 degree variation from vertical in sidewall slope would show 1.0 nm thickness variation between base and top. Particularly with III–V semiconductors, dry-etch processes also produce significant surface damage. Nanometer-thick fins can also be defined using facet-selective etches,[3] while nanowire FETs can be formed using selective chemical etches to remove sacrificial semiconductor layers grown between planes of semiconductor channel material.[4]

Here we report fabrication of sub-10 nm-thick channels by atomic layer epitaxial (ALE) growth on a template whose vertical sidewalls are in turn defined by a facet-selective etch. The fins are subsequently released by removing the growth template with selective chemical etches.

ALE provides nanometer control of the thickness of grown layers.[5,6] It is conformal, and hence can grow nanometer thick channel layers on a sidewall of a ridge. Ide[7] has reported ALE growth of InGaAs on the sidewalls of GaAs grooves, while Usui[8] demonstrated sidewall growth by ALE of InGaP on various GaAs facets.

In contrast to previous work using arsine as the group V-precusor,[9] here we report ALE of InGaAs using tertiarybutylarsine (TBAs). We also report a process flow to fabricate InGaAs fins using ALE growth on the $(0\bar{1}1)$ sidewall of patterned InP ridges or fins.[10] The group-III precursors were trimethylindium (TMI) and trimethylgallium (TMGa) and all experiments were conducted at a reactor pressure of 30 Torr in a horizontal Thomas Swan 2-in. MOCVD reactor.

2. Process flow and InGaAs ALE calibration

Figure 1 outlines the process flow and in this section we will describe this process in detail.

The process starts by formation of a ridged InP template upon which the InGaAs fins are grown. After growth by MOCVD on a semi-insulating InP substrate of a InP buffer layer, a 20-nm-thick InGaAs etch-stop layer and a 180 nm InP template layer were then grown. The wafer is then coated by a plasma enhanced chemical vapor deposition (PECVD) SiN_x 100-nm-thick hard-mask layer. Lines of 200 nm width and 200 nm spacing, oriented in the [011] direction, are then defined in the SiN_x by Ebeam lithography with subsequent dry etching of the SiN_x using CHF_3. The InP layer is then wet-etched in 3 : 1 H_3PO_4 : HCl with weight assays of 85.3 and 37.5% respectively, to form the growth template. This etch is facet-selective, and reveals the $(0\bar{1}1)$ sidewall surface. Figure 2(a) shows the fin template profile; there is only minor etch undercut at the InP/SiN_x interface, as also shown previously.[11] Initial experiments using photoresist (SPR955-CM series) as the etch mask failed due to poor resist adhesion, while a PECVD-deposited SiO_2 hard mask showed >100 nm lateral undercutting of the InP during the H_3PO_4 : HCl etch [Fig. 2(b)].[12]

After forming the ridged InP growth template using a SiN_x hard mask, the InGaAs channel layers were then grown by ALE onto $(0\bar{1}1)$ sidewalls of the InP template. As shown in the gas injection scheme, Fig. 3, in each ALE growth cycle, TMGa and TMIn were first injected simultaneously, followed by a H_2 purge, the injection of TBA, and a second H_2 purge. As the cycle times were varied to characterize the ALE growth, equal times were maintained for these four steps. The ALE growth cycles were controlled by mass flow controllers (MFCs) rather than by pneumatic valves.

The InGaAs ALE growth was first calibrated by characterizing InGaAs layers grown on (100) InP substrates using X-

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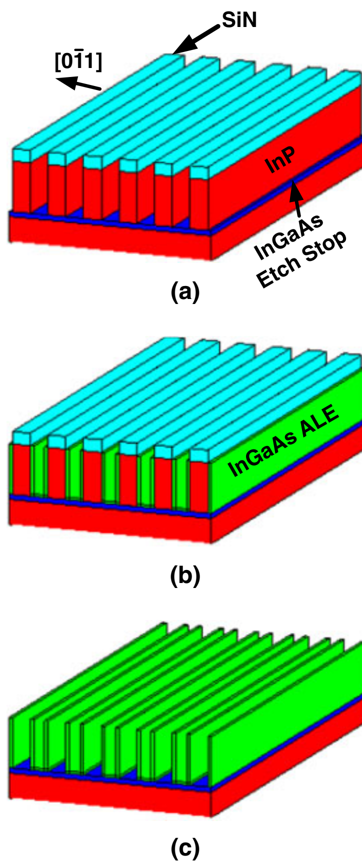


Fig. 1. (Color online) Process flow to form array of fins using InGaAs ALE. (a) Fin template formation. (b) InGaAs Channel growth by ALE. (c) Fin release.

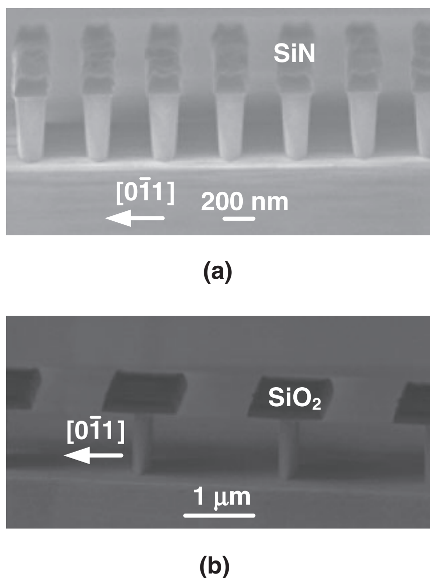


Fig. 2. SEM images of (a) ridged InP growth template formed using SiN_x as the hard mask for the H_3PO_4 : HCl facet-selective wet etch, and (b) a similar InP template wherein SiO_2 was used as the hard mask for the H_3PO_4 : HCl etch. With SiN_x, much smaller etch undercut is observed at the mask/InP interface.

ray diffraction (XRD) with a coupled scan (ω–2θ) of the incident angle (ω) and the diffracted angle (2θ). The InGaAs layer thickness and composition were extracted by numerical fitting to the width and location of the Bragg diffraction peak.

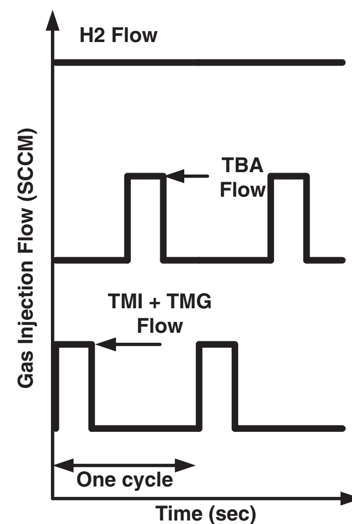
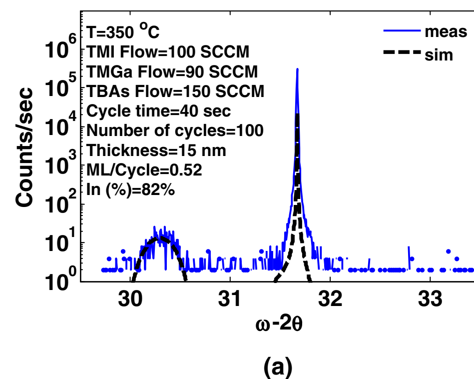


Fig. 3. Gas injection scheme.



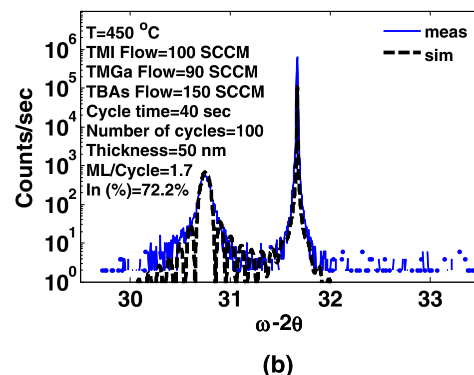


Fig. 4. (Color online) XRD data for 100 cycles of ALE InGaAs grown on a (100) InP substrate at 350 °C (a) and 450 °C (b).

ALE growth temperature is determined largely by the decomposition temperatures of the metalorganic (MO) sources.[6] TMIn and TBAs begin to decompose below 300 °C, while TMGa decomposes above 400 °C.[13] Growth characterization started with 100 cycles of ALE growth of InGaAs on a (100) InP substrate at 350 °C. Each growth cycle was 40 s duration and the TMGa, TMI, and TBAs flows were 90, 100, and 150 sccm respectively. Give the low 350 °C growth temperature, the TMGa does not fully decompose, and a 15-nm-thick indium-rich layer, $In_{0.82}Ga_{0.18}As$, was grown [Fig. 4(a)]. Increasing the growth temperature to 450 °C, with the same MO flow rates and the

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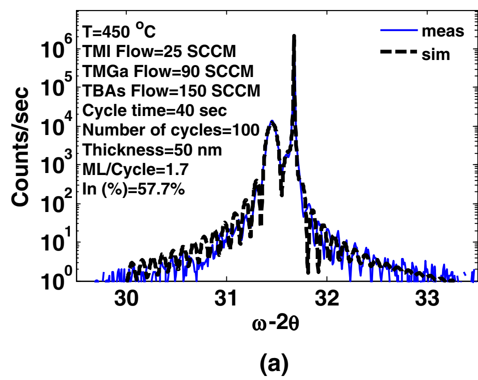

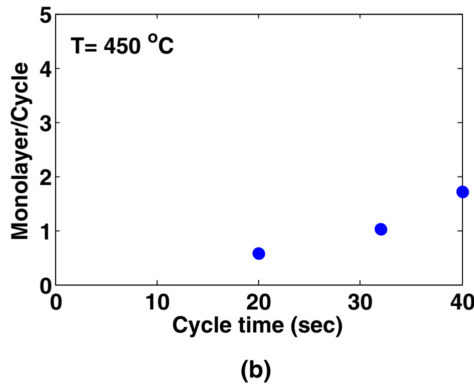

Fig. 5. (Color online) XRD of lattice-matched InGaAs grown by ALE (a) and monolayers of growth per cycle vs cycle time (b). Both experiments were done on a (100) InP substrate with TMI, TMGa, and TBAs fluxes of 25, 90, and 150 sccm.

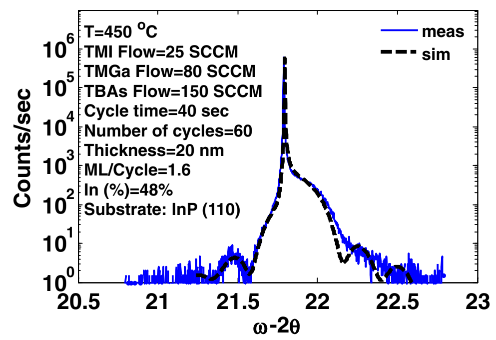

Fig. 6. (Color online) XRD of lattice-matched InGaAs grown by ALE on (110) InP substrates with TMI, TMGa, and TBAs fluxes of 25, 80, and 150 sccm.

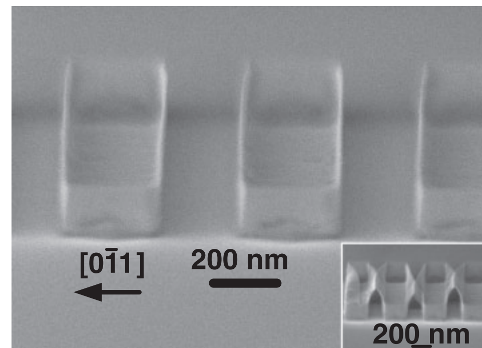

Fig. 7. SEM image of fins of <10 nm width and 180 nm height. When fins are fabricated at spacing less than 200 nm, the fins bend and stick together during drying (inset).

same cycle times, results in more complete TMGa decomposition. The 450 °C growth produced a thicker and less indium-rich layer, 50 nm $In_{0.72}Ga_{0.28}As$, as measured by XRD [Fig. 4(b)].

Adjusting the TMI and TMGa flow rates to 25 and 90 sccm, respectively, then resulted in the ALE growth, after 100 cycles, of 50 nm $In_{0.57}Ga_{0.43}As$ [Fig. 5(a)], a composition close to being lattice-matched to InP. The 50 nm (100) layer corresponds to 1.7 monolayer per cycle (ML/cycle), where one InGaAs monolayer equals to 0.29 nm. This growth rate, above one ML/cycle, indicates that the growth was not self-limiting as in a classic ALE process, most likely related to the relatively high growth temperature at which TBAs and TMI completely decompose.[13] The growth sequences above are nevertheless sufficiently well-controlled to grow layers of a few nm thickness. The relationship between cycle time and growth rate was then investigated. Growths were performed on a (100) InP substrate, at 450 °C with TMI, TMGa, and TBAs fluxes of 25, 90, and 150 sccm. As illustrated in Fig. 5(b) the number of InGaAs monolayers deposited per cycle monotonically increased with cycle time, indicating that the growth was not self-limiting as we mentioned above.

Given that the InGaAs fins are grown on the (0$\bar{1}$1) sidewalls of the InP template, ALE growth of InGaAs on (110) InP was then characterized. Growth was performed at 450 °C, with TMI, TMGa, and TBAs flows of 25, 80, and 150 sccm, and with a 40 s cycle time. 60 cycles ALE growth produced 20 nm $In_{0.48}Ga_{0.52}As$ layer as measured by XRD (Fig. 6). In the (110) orientation, one monolayer is 0.21 nm, hence the observed growth rate corresponds to 1.6 ML/cycle. On this sample, ~0.3 nm average roughness (R_a) and ~0.3 nm root mean square roughness (R_q) were measured by atomic force microscopy, and an electron mobility of 3300 $cm^2 V^{-1} s^{-1}$ and electron concentration of $1.19 \times 10^{15} cm^{-3}$ were extracted from Hall measurement.

For all subsequent experiments, involving InGaAs ALE on the (0$\bar{1}$1) sidewalls of InP fins, growth was performed at 450 °C, with TMI, TMGa, and TBAs flows of 25, 80, and 150 sccm. With ALE growth on planar (110) and (100) InP wafers characterized, samples were then prepared for the ALE growth of InGaAs onto the (0$\bar{1}$1) sidewalls of InP ridged growth templates. InP ridged growth templates were first prepared as described above [Fig. 1(a)], oxidized by UV ozone, etched in dilute HCl and then the InGaAs was grown on the InP template sidewalls [Fig. 1(b)]. The SiN_x hard mask was then stripped and the InGaAs fins were released [Fig. 1(c)] by a selectively etching away the InP template layer in 3 : 1 H_3PO_4 : HCl, thereby leaving free-standing InGaAs fins.

3. Results and discussion

Figure 7 shows a typical structure, showing InGaAs fins of ~10 nm width and 180 nm height, at 200 nm spacing, grown with 20 cycles ALE. When the wafer is rinsed and dried after H_3PO_4 : HCl etching, the fins are exposed to large forces arising from surface tension. With 10 nm width and 180 nm height, these forces cause the fins to bend and stick together if their spacing is less than 200 nm (Fig. 7 inset). It is possible that this bending might be avoided by drying the

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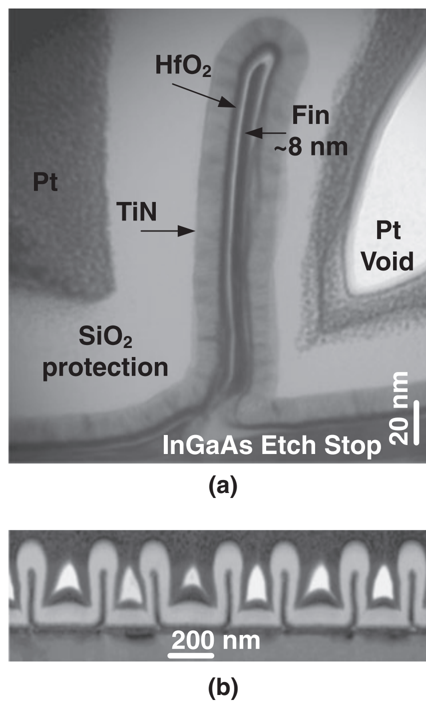

Fig. 8. TEM images of (a) 8 nm width fins of 180 nm height coated with HfO_2 gate dielectric and TiN gate metal and (b) fin array at 200 nm pitch.

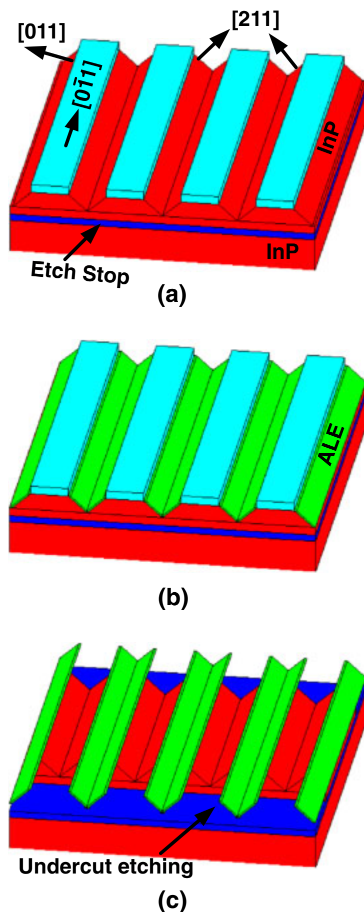

Fig. 9. (Color online) Fabrication sequence for fabrication of (211) InGaAs fins. The SiN_x mask is (a) oriented in the [0$\bar{1}$1] and the InP template layer etched in H_3PO_4 : HCl, InGaAs is grown by ALE (b) on the resulting (211) InP surfaces and (c) the InP template is partially removed, liberating the fins.

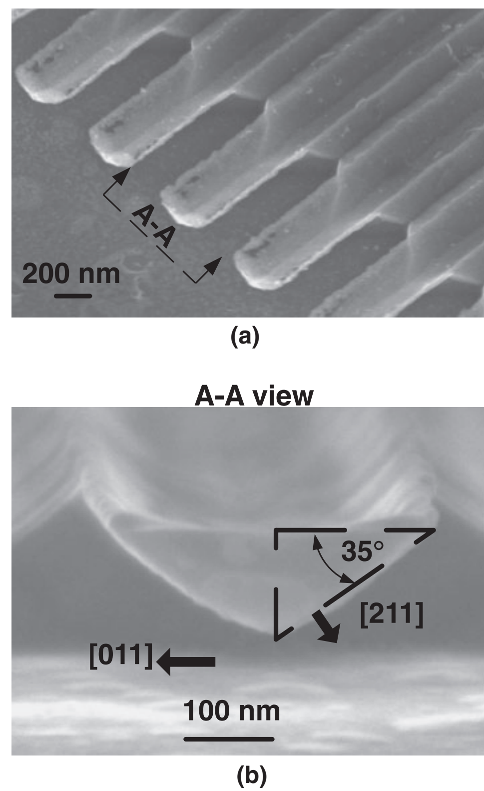

Fig. 10. SEM image of 30 nm wide ALE channel on top of [211] InP groves (a). A side view (b) shows 35° between the [211] InGaAs ALE channel and [011].

samples in CO_2 at the critical point,[14] as has been reported in the fabrication of MEMs structures.

Bending can also be avoided by first providing mechanical support before releasing the InGaAs fins from the InP support layer. This support can be provided by selective-area MOCVD growth of N+ InGaAs source and drain regions contacting the InGaAs fin.[10] Fins fabricated in this fashion are shown in Fig. 8; these are surrounded by 4 nm HfO_2 gate dielectric and 10 nm TiN gate metal, both deposited by atomic layer deposition (ALD) as part of a full finFET process.[10] Support by the N+ regrowth prevents the fins from bending and adhering even when fabricated at 200 nm pitch [Fig. 8(b)].

In order to explore the robustness of the process flow to manufacture channels upon different facets than (0$\bar{1}$1) InP, ALE growth on other InP sidewalls was also investigated. If the SiN_x mask lines are oriented in the [0$\bar{1}$1] direction (Fig. 9), then the H_3PO_4 : HCl facet-selective etch forms grooves in the InP with inclined (211) sidewalls.[15] 60 cycles of InGaAs was then grown by ALE upon these InP surfaces, using the growth conditions of Fig. 6. In this process, to retain mechanical support of the InGaAs fins, the InP growth template is not removed over the full length of the InGaAs regrowth (Fig. 9). Where the InP is removed, the InGaAs is a free-standing, cantilevered membrane. Figure 10(a) shows a SEM image from above, of the free-standing (211) InGaAs fins, while Fig. 10(b) shows an end-view. While not of immediate interest for finFet applications, the results illustrate the versatility of the investigated fabrication procedure.

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4. Summary

In summary, InGaAs fins of <10 nm width and 180 nm height were fabricated using atomic layer epitaxy on the sidewalls of InP growth template layers. A full nm finFET fabrication process is in development.

Acknowledgments

The Work was funded by NSF under EEC-0228390 and NSF-NRI grant under ECCS-1125017 and has made use the NNIN National Nanofabrication facilities and the MRL Central Facilities supported by the MRSEC Program of the National Science Foundation under award No. MR05-20415.

1) Q. Xie, J. Xu, and Y. Taur, IEEE Trans. Electron Devices **59**, 1569 (2012).
2) M. Radosavljevic, G. Dewey, D. Basu, J. Boardman, B. Chu-Kung, J. M. Fastenau, S. Kabehie, J. Kavalieros, V. Le, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, H. W. Then, and R. Chau, IEDM Tech. Dig., 2011, p. 765.
3) V. Jovanović, T. Suligoj, M. Poljak, Y. Civale, and L. K. Nanver, Solid-State Electron. **54**, 870 (2010).
4) J. J. Gu, X. W. Wang, J. Shao, A. T. Neal, M. J. Manfra, R. G. Gordon, and P. D. Ye, IEDM Tech. Dig., 2012, p. 529.
5) J.-I. Nishizawa, H. Abe, and T. Kurabayashi, J. Electrochem. Soc. **132**, 1197 (1985).
6) S. P. DenBaars and P. D. Dapkus, J. Cryst. Growth **98**, 195 (1989).
7) Y. Ide, B. T. McDermott, M. Hashemi, S. M. Bedair, and W. D. Goodhue, Appl. Phys. Lett. **53**, 2314 (1988).
8) A. Usui, H. Sunakawa, F. J. Stützler, and K. Ishida, Appl. Phys. Lett. **56**, 289 (1990).
9) Y. Huang, J.-H. Ryou, and R. D. Dupuis, J. Cryst. Growth **321**, 60 (2011).
10) D. Cohen-Elias, J. J. M. Law, H. W. Chiang, A. Sivananthan, C. Zhang, B. J. Thibeault, W. J. Mitchell, S. Lee, A. D. Carter, C.-Y. Huang, V. Chobpattana, S. Stemmer, S. Keller, and M. J. W. Rodwell, Device Research Conf., 2013, p. 1.
11) J. A. Summer, Dr. Thesis, Electrical and Computer Engineering Department, University of California, Santa Barbara (2007).
12) A. R. Clawson, Mater. Sci. Eng. R **31**, 1 (2001).
13) G. B. Stringfellow, *Organometallic Vapor-Phase Epitaxy Theory and Practice* (Academic Press, San Diego, CA, 1999) 2nd ed., Chap 5.
14) I. H. Jafri, H. Busta, and S. T. Walsh, Proc. SPIE **3880**, 51 (1999).
15) R. Klockenbrink, E. Peiner, H.-H. Wehmann, and A. Schlachetzki, J. Electrochem. Soc. **141**, 1594 (1994).

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