High Efficiency W-band Power Amplifiers using Ring-Shaped Sub-Quarter-Wavelength Power Combining Technique

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***Abstract*—We present W-band power amplifiers which are designed using the sub-quarter-wavelength transmission line balun in a ring-shaped configuration and fabricated in a $0.25\,\mu$m InP DHBT technology. Operating at $86\,\mathrm{GHz}$, a single-stage PA exhibits $20.86\,\mathrm{dBm}$ saturated output power with $10.2\,\mathrm{dB}$ peak power gain, a recored PAE of $35\,\%$ and a record 3-dB bandwidth of $33\,\mathrm{GHz}$. A two-stage PA exhibits $22.75\,\mathrm{dBm}$ saturated output power with $20.4\,\mathrm{dB}$ peak power gain, a PAE of $32.8\,\%$ and a 3-dB bandwidth of $16\,\mathrm{GHz}$.**

***Index Terms*—W-band power amplifier, high efficiency, power combining techniques, sub-quarter-wavelength balun, InP HBT.**

I. Introduction

The sub-mm-wave/mm-wave spectrum has large available bandwidth and will enable very wideband communications. Given the extreme foul-weather attenuation, large phased arrays, low noise receivers, and high-power amplifiers (PAs) are the critical enabling technologies. Sub-mm-wave/mm-wave PA design is difficult because of low breakdown voltages, high skin-effect losses, and the large interconnect reactances.

In order to design a high power and efficiency power amplifier, three approaches can be considered: (a) classic output power-combining techniques using $\lambda/4$ or shorter transmission lines where the die area is large and the loss of substrate needs to be prevented by shielding it [1], (b) stacking (series connecting) of the transistors [2], [3] where keeping all the stacked transistors operating in phase to get the maximum power is a challenge, and (c) recently introduced sub-quarter-wavelength (sub-$\lambda/4$) transmission line balun [4] where power combining is performed using a low loss balun with much shorter than $\lambda/4$ line sections.

In this paper we have designed high efficiency PAs using the third approach in a ring-shaped configuration where the corresponding grounds of the sub-$\lambda/4$ stubs are tied together which decreases the port imbalance ratio of the balun and consequently results less loss and higher PAE.

II. Operation of Sub-$\lambda/4$ Transmission Line Balun

Figure 1(a) shows the $\lambda/4$ balun implemented in a three layer metal stack ($\mathrm{M_1}$–$\mathrm{M_3}$) and two ideal PAs ($\mathrm{PA_n}$ and $\mathrm{PA_p}$) with zero output capacitance have been connected to the input ports of the balun. Considering $\mathrm{M_1}$ as the main ground of the system, the balun is consisted of two $\lambda/4$ stubs in $\mathrm{M_2}$ which are shorted to ground at their end point and behave as open stubs to the PAs. A $50\,\Omega$ transmission line is also constructed between $\mathrm{M_3}$ and $\mathrm{M_2}$ which is ideally supposed to be shielded from the main ground of the system ($\mathrm{M_1}$). In this case, a traveling wave will enter to the transmission line from the output port of the balun (connected to the load in Fig. 1(a)) and propagate along the line while it is shielded from outside. When it reaches to the end of the transmission line, it sees two PAs in parallel with two open stubs. Due to the symmetry, power will be balanced between the PAs. Current flow analysis shown in Fig. 1(a) represents this fact where the current (i_L) flows from the load (R_L) to the top metal ($\mathrm{M_3}$) of the transmission line and it enters to the $\mathrm{PA_n}$ through the via $\mathrm{M_{23}}$. At the same time, a same amount of current in the opposite direction flows on the bottom metal ($\mathrm{M_2}$) of the transmission line which sinks the current from the $\mathrm{PA_p}$.

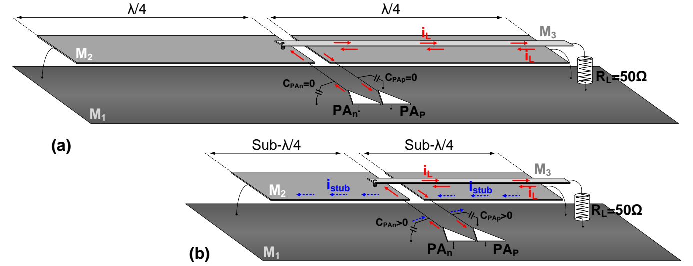

Fig. 1. Current flow diagram of (a) $\lambda/4$ and (b) sub-$\lambda/4$ transmission line balun.

In reality, the two PAs include a finite amount of capacitance. Therefore, the length of the stubs can be decreased in an amount that they resonate with the total capacitance of the PAs. This is shown in Fig. 1(b) where the current i_{stub} will only flow in the loop of the sub-$\lambda/4$ stubs and the PA capacitance and it will not enter to the PAs. In this way, the length of the stubs and consequently the length of the balun can be decreased up to $\lambda/16$ which has a significant impact on the total insertion loss of the balun.

The sub-$\lambda/4$ balun shown in Fig. 1(b) will have port imbalance in real implementation where the $50\,\Omega$ transmission line on $\mathrm{M_3}$ is not fully shielded from the main ground of the system ($\mathrm{M_1}$). Increasing the width of the stubs in $\mathrm{M_2}$ will overcome this problem and decrease the port imbalance,

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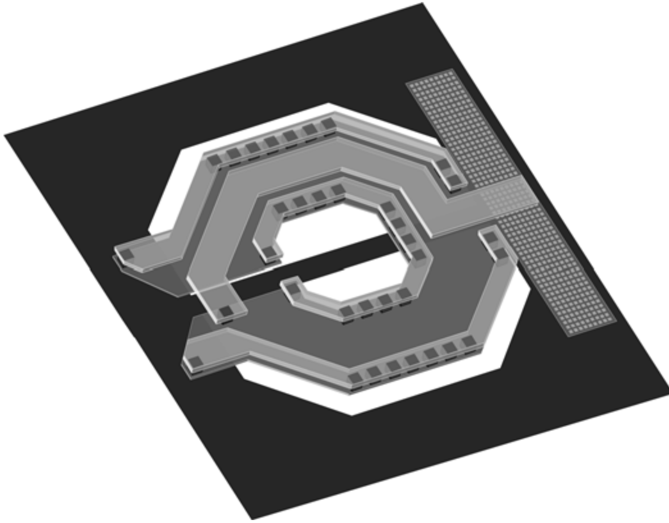

Fig. 2. Ring-shaped sub-$\lambda/4$ 2-way balun.

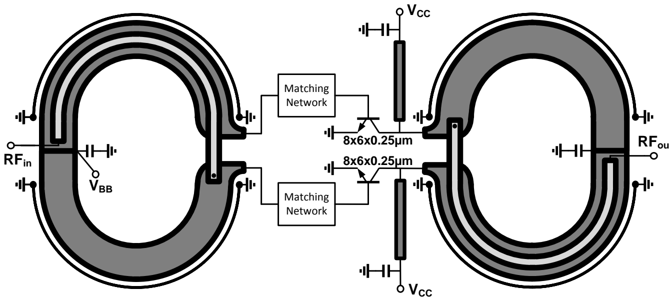

Fig. 3. Schematic diagram of the single-stage PA.

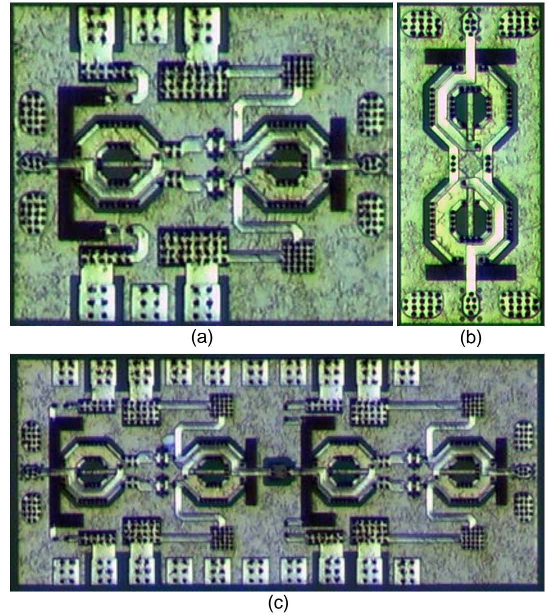

Fig. 4. Die-photos of (a) Single-stage PA $(0.718 \times 0.595\,\mu\mathrm{m}^2)$, (b) Test chip with two back-to-back baluns and (c) Two-stage PA $(1.378 \times 0.595\,\mu\mathrm{m}^2)$.

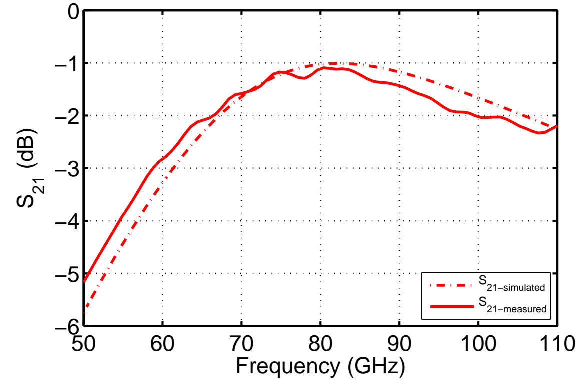

Fig. 5. Simulated and measured insertion loss for the back-to-back ring-shaped sub-$\lambda/4$ baluns.

however, this will decrease the characteristic impedance of the stubs and consequently will decrease the overall bandwidth of the balun. The other solution is shielding the transmission line in M_3 using two sidewalls similar to the one reported in [4]. Here in this design, we propose the ring configuration to implement the sub-$\lambda/4$ balun where the two stubs share the same ground at their end point which consequently decreases the port imbalance due to the difference between the location of the grounds at the end points of the stubs. Moreover, the two stubs have higher characteristic impedance at this configuration which significantly increases the bandwidth of the balun. Fig. 2 shows the layout of the ring-shaped sub-$\lambda/4$ balun where the shielding sidewalls on M_3 is also used to enhance the balance between the ports. The stubs are AC grounded using a $1\,\mathrm{pF}$ bypass capacitance in order to make the balun suitable for providing the DC supply of the PAs.

III. PA Circuit Architecture

The PAs were designed using a $0.25\,\mu\mathrm{m}$ InP DHBT technology, which exhibits $\mathrm{BV_{CEO}} = 4.5\,\mathrm{V}$, $\mathrm{f_{max}} = 590\,\mathrm{GHz}$, and $\mathrm{f_T} = 350\,\mathrm{GHz}$. A three-metal interconnect stack is used in the fabrication of the circuit. Compact, stacked interconnect vias provide access from the top layer of metal interconnect for signal (M_3 with $3\,\mu\mathrm{m}$ thickness) to the two lower layers (M_2 and M_1 with $1\,\mu\mathrm{m}$ thickness). M_3 and M_2 interconnects are separated by $5\,\mu\mathrm{m}$ BCB interlayer dielectric layer while the thickness of BCB between M_2 and M_1 is $1\,\mu\mathrm{m}$. MIM capacitors and thin-film resistors are $0.3\,\mathrm{fF}/\mu\mathrm{m}^2$ and $50\,\Omega/\Box$, respectively.

Fig. 3 shows the circuit diagram of the single-stage PA designed in this work. Since the amount of inductance provided by the ring-shaped sub-$\lambda/4$ balun was large, an additional parallel stub has been used at each port to decrease the total shunt inductance. Multi-finger transistors are resized to $8 \times 6 \times 0.25\,\mu\mathrm{m}$ at each port in order to make the slope of their optimum loadline equal to $25\,\Omega$ which is the impedance seen at each port of the sub-$\lambda/4$ balun. The two-stage PA is designed by cascading two single-stage PAs with a DC blocking capacitor between them.

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TABLE I
COMPARISON TO SIMILAR W-BAND PAS REPORTED IN THE LITERATURE.

Ref.	Process	Freq. (GHz)	$S_{21\text{-}max}$ (dB)	$\text{BW}_{\text{-3dB}}$ (GHz)	P_{sat} (dBm)	Peak PAE (%)	Die-size (mm^2)	$\text{P}_{\text{DC}}/\text{V}_{\text{cc}}$ (mW/V)	P_{sat}/Area (mW/mm^2)	Topology
[5]	$0.15\,\mu$m GaN HEMT	91	16	≈ 7	30.8	> 20	2.5×0.9	6125/17.5	530	4-stage CS, 4-way combiner
[3]	65 nm SOI CMOS	$86 - 94$	10.2	≈ 12	15.8	11	0.72×0.42	$-$/2.8	126	2-stage Stacked FET, No combiner
[7]	130 nm SiGe BiCMOS	84	27	> 8	18	9	0.79×0.86	395/2.5	92.9	3-stage CB, 4-way combiner
[4]	250 nm InP DHBT	86	9.4	23	20.37	30.4	0.448×0.816	277/2.5	294	1-stage CE, Straight sub-λ/4 Balun
		86	17.5	–	23.14	30.2	0.824×0.816	516/3	307	2-stage CE, Straight sub-λ/4 Balun
This work	250 nm InP DHBT	86	10.2	33	20.86	35	0.718×0.595	271/2.5	285	1-stage CE, Ring-shaped sub-λ/4 Balun
		86	20.4	16	22.75	32.8	1.378×0.595	450/3	230	2-stage CE, Ring-shaped sub-λ/4 Balun

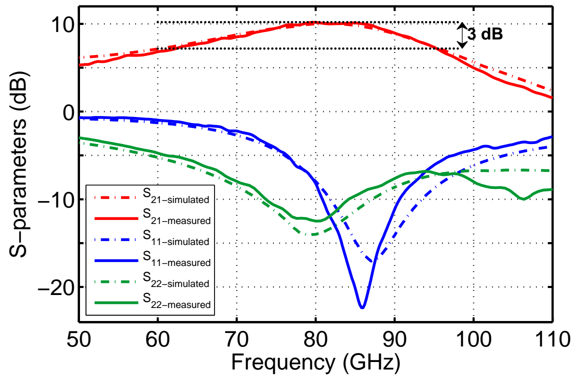

Fig. 6. Simulated and measured S-parameters of the single-stage PA.

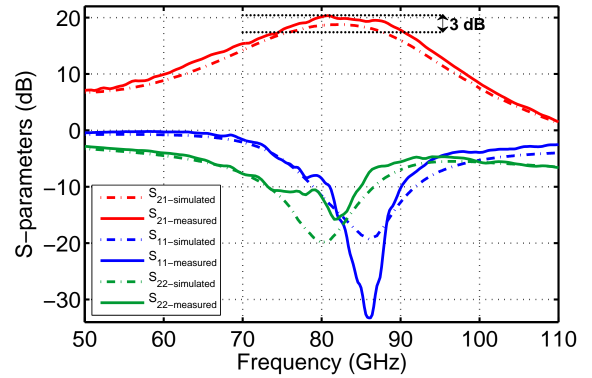

Fig. 8. Simulated and measured S-parameters of the two-stage PA.

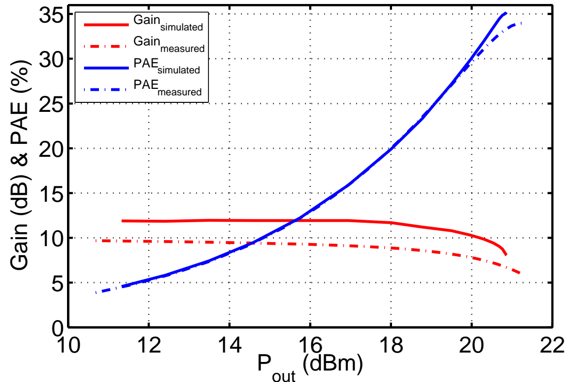

Fig. 7. PAE and gain versus output power for the single-stage PA.

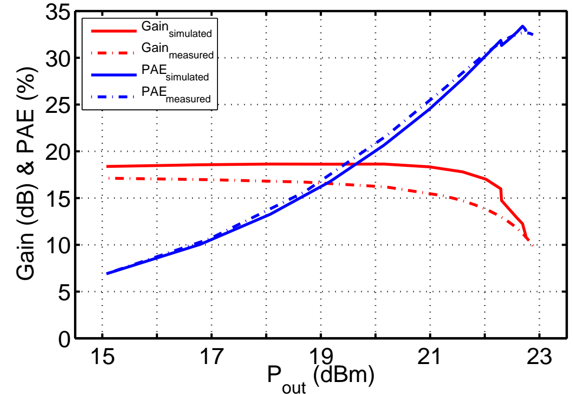

Fig. 9. PAE and gain versus output power for the two-stage PA.

IV. MEASUREMENT RESULTS

The IC micrograph of the two PAs are shown in Fig. 4. In order to measure the insertion loss of the balun, a test structure with back-to-back connection of two baluns with two shunt capacitances (to resonate with the inductance of the stubs) between them is also included. The measured S_{21} of this test structure shown in Fig. 5 has a peak value of 1.03 dB at 81 GHz which exhibits an insertion loss less than 0.5 dB for each balun considering that the loss of RF pads and shunt capacitances are included in the measured results.

The small-signal S-parameters of the single-stage PA are measured with the bias condition of $\text{V}_{\text{CC}} = 2.5\,\text{V}$, $\text{I}_{\text{C}} =$

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$105\,\mathrm{mA}$, $\mathrm{I_B} = 4.6\,\mathrm{mA}$ and compared to predictions in Fig 6. The PA exhibits a peak value of $10.2\,\mathrm{dB}$ small-signal gain at $81\,\mathrm{GHz}$ with a corresponding record 3-dB bandwidth of $33\,\mathrm{GHz}$. Large-signal measurements have been also performed at the same bias condition. Fig. 7 plots the simulated and measured PAE and gain as a function of output power at $86\,\mathrm{GHz}$. The single-stage PA shows a record PAE of 35% at a saturated output power of $20.86\,\mathrm{dBm}$.

The bias condition for the two-stage PA in small-signal measurements is set to $\mathrm{V_{CC1}} = \mathrm{V_{CC2}} = 2.5\,\mathrm{V}$, $\mathrm{I_{C1}} = \mathrm{I_{C2}} = 105\,\mathrm{mA}$, $\mathrm{I_{B1}} = \mathrm{I_{B2}} = 4.6\,\mathrm{mA}$. Fig. 8 compares the measured results with the predictions where the two-stage PA shows a peak value of $20.4\,\mathrm{dB}$ small-signal gain at $81\,\mathrm{GHz}$ with a corresponding 3-dB bandwidth of $16\,\mathrm{GHz}$. The bias condition for large-signal measurements has been changed to $\mathrm{V_{CC1}} = 2.4\,\mathrm{V}$, $\mathrm{I_{C1}} = 52\,\mathrm{mA}$, $\mathrm{I_{B1}} = 2.3\,\mathrm{mA}$ and $\mathrm{V_{CC2}} = 3\,\mathrm{V}$, $\mathrm{I_{C2}} = 105\,\mathrm{mA}$, $\mathrm{I_{B2}} = 4.6\,\mathrm{mA}$. At this condition, the PA delivers a saturated output power of $22.75\,\mathrm{dBm}$ with a PAE of 32% which are presented in Fig. 9.

Table I compares the performance of the presented PAs with the similar state of the art PAs. The record PAE in these designs is achieved due to the higher port balance of the ring-shaped configuration while its corresponding large characteristic impedance for the stubs has provided a record bandwidth for the circuits.

V. Conclusion

Two W-band PAs are reported with the record PAE and bandwidth which are achieved due to using of a ring-shaped configuration in the sub-$\lambda/4$ balun. The single-stage PA delivers $20.86\,\mathrm{dBm}$ saturated output power with a PAE of 35% and a 3-dB bandwidth of $33\,\mathrm{GHz}$. The two-stage PA exhibits $22.75\,\mathrm{dBm}$ saturated output power with a PAE of 32.8% and a 3-dB bandwidth of $16\,\mathrm{GHz}$.

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