Leakage Current Suppression in InGaAs-Channel MOSFETs: Recessed InP Source/Drain Spacers and InP Channel Caps

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InGaAs MOSFETs (with In>53%) have recently demonstrated major improvement [1-6], with performance now rivaling 22nm Si FinFETs. Given the low electron effective mass with the resultant higher electron velocity, InGaAs channels enable high on-state current at low drain bias (V_{DS}=0.5 V). However, the small band-gap of InGaAs make such FETs vulnerable to high off-state leakage due to barrier-limited sub-threshold leakage, band-to-band tunneling (BTBT), and impact ionization (II). Because of a sharp local field concentration, BTBT readily occurs at the junction between the narrow-bandgap channel and the raised regrown drain. This limits the minimum off-state leakage. Incorporating a raised unintentionally-doped (U.I.D) InGaAs [5] or a U.I.D InP vertical spacer [6] at the source/drain (S/D) significantly decreases the off-state leakage due to decreased peak electric field near the drain. In this paper, we report two novel techniques to further reduce the off-state leakage current: using a recessed InP source/drain spacer or using an InP cap layer within the channel. By re-growing the wide band-gap InP material near drain region, the off-state leakage at V_{DS}=0.5V can be reduced to below 1 nA/µm for L_g~22 nm devices, showing 1~2 orders of magnitude reduction in leakage compared to devices having a raised InGaAs or InP U.I.D vertical spacer within the regrown drain. These techniques allow the minimum off-state leakage of InGaAs MOSFETs to meet the requirements of low power(LP) and standard performance(SP) logic applications.

Fig. 1 shows device structures. All samples have an $In_{0.52}Al_{0.48}As$ back barrier; samples A and B have a 6 nm $In_{0.53}Ga_{0.47}As$ epitaxial channel. HSQ dummy gates were patterned by e-beam lithography. For sample A, a 10 nm InGaAs U.I.D vertical spacer was regrown prior to the N+ InGaAs S/D. For sample B, ~3 nm of the InGaAs channel in the S/D region was removed by digitally etching in UV ozone and dilute HCl. A 13 nm U.I.D InP spacer and N+ InP, N+ InGaAs S/D were then regrown on the sample. sample C has a 5 nm U.I.D InP cap layer blanket regrown on a 3 nm InGaAs channel. After dummy gate formation, an 8 nm InP U.I.D layer and N+ InP, N+ InGaAs S/D were regrown on the 5 nm InP cap. To maintain similar electrostatics, all samples have 11~12 nm vertical spacers (InGaAs or InP) above the channel/dielectric interface plane. After S/D regrowth, devices were then isolated. The samples were then digitally etched (1.5 nm/cycle) to reduce the InGaAs channel and InP caps to the thicknesses indicated on fig. 1, immediately loaded into the ALD system, cleaned by TMA/nitrogen plasma, and 3 nm ZrO_2 gate dielectric deposited.[7] The Ni gate and Ti/Pd/Au S/D contact were then deposited by liftoff.

Fig. 2 shows the transfer and output characteristics of L_g~22nm devices. Compared to sample A, samples B and C show significantly improved sub-threshold swing (SS) at large positive V_{DS} and large negative V_{GS}. In contrast, sample A shows increasing SS as V_{gs} is made more negative, a clear signature of strong BTBT. At large negative V_{GS} , sufficient to suppress the subthreshold thermal leakage below BTBT, samples B and C show much smaller leakage, with I_D reduced, dramatically, 1-2 orders of magnitude.

In the present designs, the InP S/D spacers (samples B and C) suppress BTBT leakage but reduce the on-current. Peak transconductance and on-current are both reduced (fig. 2) , and the drain-source on-resistance (fig. 5) increased. All samples have similar total vertical spacer layer thickness. Although the reduced current, and increased resistance, might be attributed to conduction-band barriers at InP-InGaAs heterointerfaces, heavy doping at interfaces between the N+ InGaAs cap layer and the N+ top surface of the InP regrowth ensures that conduction-band peaks at these interfaces remain well below the Fermi energy, while, because of quantization in the thin channel, the channel bound state is only ~0.1eV below the InP S/D conduction band edge in sample B, and only ~0.07eV below the S/D conduction band edge in sample C. Instead, we suspect that the reduce I_{on} results from increased access resistance from the spacer layers; transport through the source spacer is aided by conduction through a surface electron accumulation layer induced by the gate, with the surface charge density smaller with an InP spacer than with an InGaAs spacer due to their difference in electron affinities. With an InP/InGaAs vertical spacer using wider-gap materials only in the highest-field regions, and with heterointerface grading to suppress remaining InP/InGaAs band offsets, it may be possible to improve the on-state performance.

Fig. 3 compares gate and drain leakage currents. For sample A, drain leakage greatly exceeds gate leakage, being dominated by BTBT. For samples B and C, at large negative V_{gs}, gate and drain leakage are equal, indicating that gate-drain leakage dominates the observed off-state drain current, with BTBT negligible. All samples have large excess gate-S/D overlap (~1 µm overlap length) ; eliminating this would further reduce the minimum leakage of samples B and C.

Fig. 6 shows peak SS versus L_g. With sample A, BTBT causes short-channel SS to degrade as V_{DS} is increased from 0.1V to 0.5V, as frequently seen in InGaAs-channel FETs [1,2,5,6]. In contrast, sample B shows minimal variation in SS between 0.1V and 0.5V V_{DS}. Sample C shows a slight degradation in peak SS as V_{DS} is increased.

The two techniques addressed in this paper—a recessed InP spacer and an InP cap layer—enable us to reduce off-state leakage plateau and allow III-V InGaAs MOSFETs for low power(LP) and standard performance(SP) logic applications

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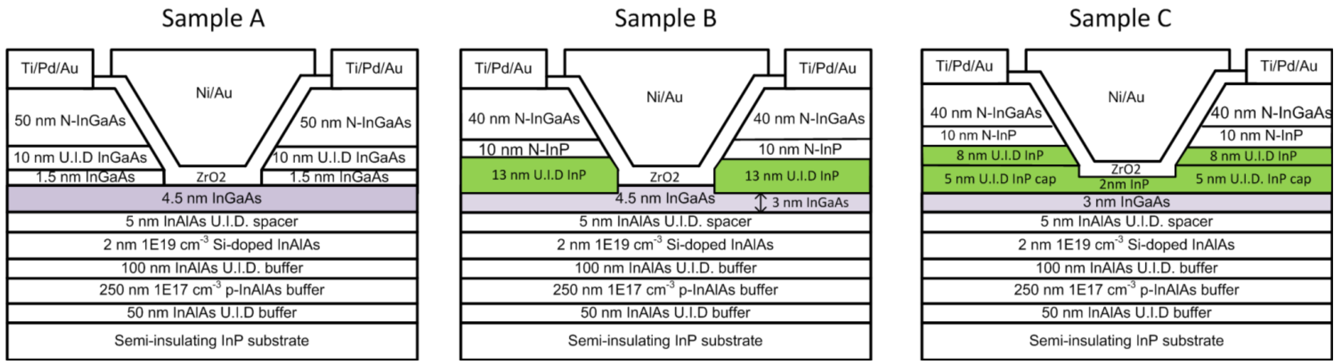

Fig. 1. Devices structures of sample A(raised InGaAs spacer), B (recessed InP spacer), and C (InP cap layer).

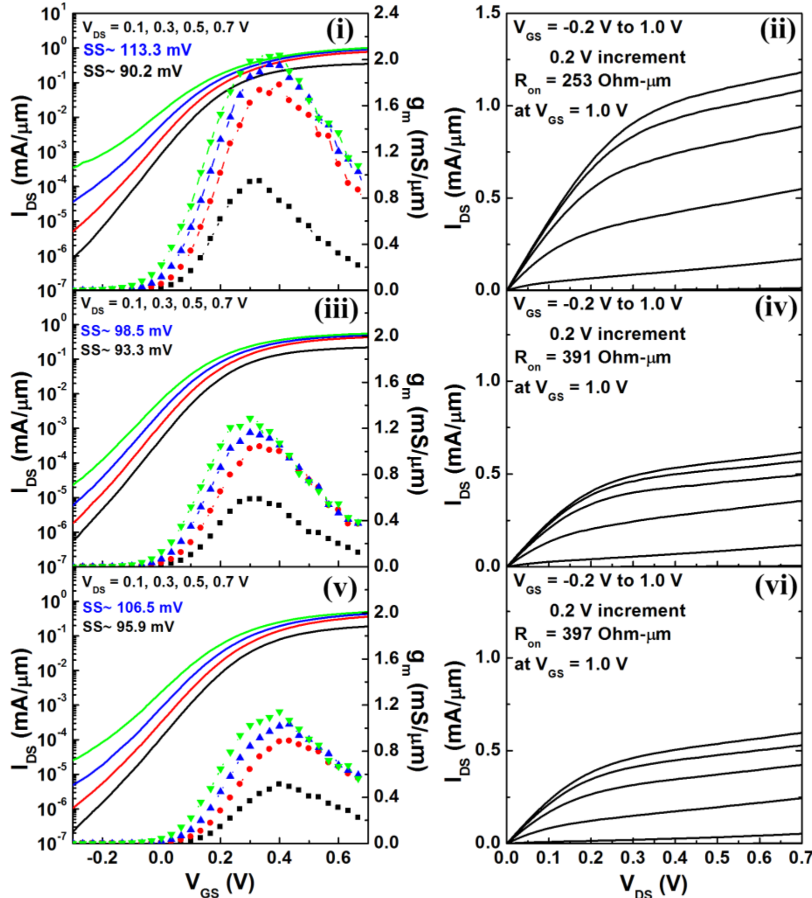

Fig. 2. Transfer characteristics and output characteristic of L_g=22 nm devices for (i, ii) sample A, (iii, iv) sample B, and (v, vi) sample C.

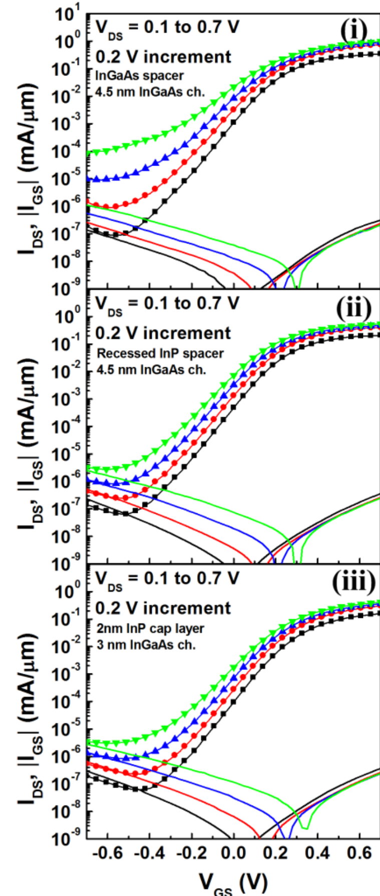

Fig. 3. I_{GS}-V_{GS} gate leakage and I_{DS}-V_{GS} plot for L_g=22 nm devices. (i) sample A, (ii) sample B and (iii) sample C.

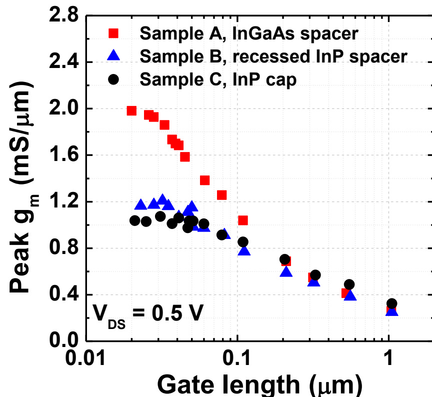

Fig. 4. Comparison of g_m versus L_g for samples A, B, and C.

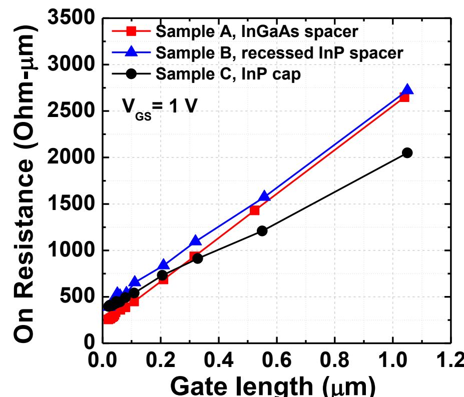

Fig. 5. Comparison of on-resistance versus L_g for samples A, B, and C.

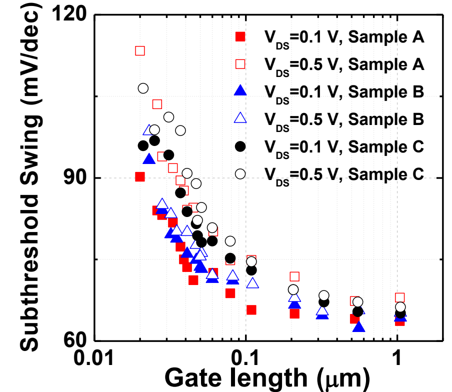

Fig. 6. Comparison of SS versus L_g for samples A, B, and C.