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An InGaAs/InP DHBT With Simultaneous f_τ/f_{max} 404/901 GHz and 4.3 V Breakdown Voltage

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ABSTRACT We report an InP/InGaAs/InP double heterojunction bipolar transistor fabricated in a triple-mesa structure, exhibiting simultaneous 404 GHz f_τ and 901 GHz f_{max}. The emitter and base contacts were defined by electron beam lithography with better than 10 nm resolution and smaller than 20 nm alignment error. The base-collector junction has been passivated by depositing a SiN_x layer prior to benzocyclobutene planarization, improving the open-base breakdown voltage BV_{CEO} from 3.7 to 4.3 V.

INDEX TERMS HBT, InGaAs/InP DHBT, THz device.

I. INTRODUCTION

The demand for submm-wave radio systems [1], high data rate communication systems [2] and high performance signal processing systems [3], [4] drives the development of high bandwidth transistors. Key to increasing RF performance is scaling [5]: transit delays are reduced by thinning epitaxial base and collector layers. Concurrently, *RC* charging delays are lowered by lithographically narrowing emitter and base/collector widths while maintaining constant parasitic resistances R_{ex}, R_{bb}, device current I_e and transconductance g_m. Scaling challenges involve achieving low ohmic contact resistitivies to emitter and base, fabricating narrow and well aligned emitter and base/collector junctions as well as sustaining high device current densities.

We report a self-aligned triple-mesa InP/InGaAs/InP DHBT with f_τ = 404 GHz and simultaneous f_{max} = 901 GHz at 180 nm x 2.7 μm emitter area, operating without failure at current and power densities in excess of 23 mA/μm^2 and 42 mW/μm^2, respectively. Under different biasing conditions, f_τ = 424 GHz and simultaneous f_{max} = 831 GHz have been exhibited. Although the f_{max} obtained here is ≈10 % below previous results [6] due to process variations (emitter end undercut, contact resistivity) and lower than [7], it exceeds that of other reported HBTs, including those of recent publications [8], [9]. The usable range of transistor operation [10] is extended by increasing the breakdown voltage BV_{CEO} = 4.3 V by means of passivating the base/collector semiconductor with conformal PECVD SiN_x prior to BCB planarization. A device identical in epitaxial structure and similar in fabrication except with BCB junction passivation exhibited BV_{CEO} = 3.7 V [6].

II. DESIGN AND FABRICATION

The DHBT wafer has been grown by solid source molecular beam epitaxy on a 4" InP substrate by IQE. The n-$In_{0.53}Ga_{0.47}As$ emitter cap is highly doped for low emitter resistance R_{ex}. The 30 nm thick base is doping-graded from 9–5 × 10^{19} cm^{-3}, resulting in 55 meV conduction band slope. The 100 nm thick collector is comprised of a 13.5 nm setback, a 16.5 nm chirped superlattice InGaAs/InAlAs grade and a 67 nm drift collector region (Table 1).

The 500 nm tall composite Mo/W/TiW emitter metal stack is fabricated in a dry etch process [11]. After forming dielectric SiN_x sidewalls on the emitter metal, the emitter semiconductor is removed in a selective wet etch. Self-aligned

TABLE 1. Epitaxial structure design.

T (nm)	Material	Doping (cm^{-3})	Description
10	$In_{0.53}Ga_{0.47}As$	8×10^{19} : Si	Emitter Cap
20	InP	5×10^{19} : Si	Emitter
15	InP	2×10^{18} : Si	Emitter
30	$In_{\approx 0.5}Ga_{\approx 0.5}As$	$9–5 \times 10^{19}$: C	Base
13.5	$In_{0.53}Ga_{0.47}As$	5×10^{16} : Si	Setback
16.5	InGaAs/InAlAs	5×10^{16} : Si	B-C Grade
3	InP	3.6×10^{18} : Si	Pulse Doping
67	InP	5×10^{16} : Si	Drift Collector
7.5	InP	2×10^{19} : Si	Sub-Collector
5	$In_{0.53}Ga_{0.47}As$	4×10^{19} : Si	Sub-Collector
300	InP	1×10^{19} : Si	Sub-Collector
5	$In_{0.53}Ga_{0.47}As$	NID	Etch Stop
≈ 625k	SI InP		Substrate

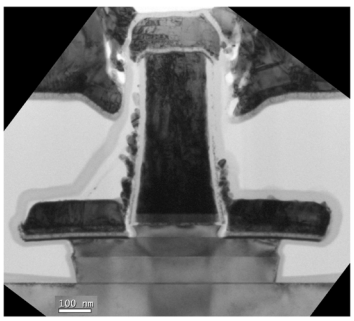

FIGURE 1. Transmission electron micrograph of a fabricated device. Emitter junction width w_e = 240 nm, single-sided base metal width w_{bm} = 220 nm, single-sided base mesa undercut w_{bmu} = 125 nm, and emitter-base contact spacing w_{Gap} ≈ 12 nm.

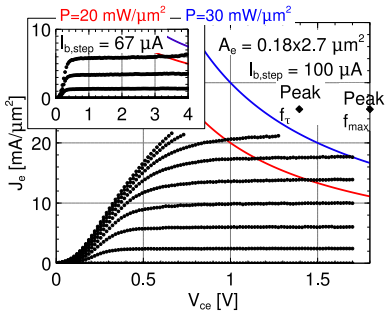

FIGURE 2. Common emitter characteristics for an HBT with 180 nm × 2.7 μm emitter junction area.

base metal contacts Pt/Ti/Pd/Au 3.5/12/17/70 nm are then lifted-off. The distance between the edges of emitter and base contact ≈12 nm is determined by the thickness of the emitter sidewalls and the emitter undercut. This contributes to low base access resistance. The base/collector mesa is formed through selective wet etches. After post lift-off and device isolation, surface oxides are removed in 1:10 HCl:H_2O and a 30 nm thick SiN_x layer is deposited by PECVD. The transistors are then planarized with BCB.

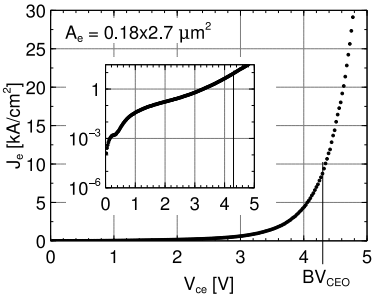

FIGURE 3. Collector-emitter breakdown measurement with floating base BV_{CEO} for an HBT with 180 nm × 2.7 μm emitter junction area.

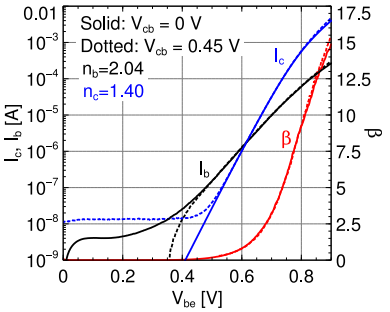

FIGURE 4. Gummel characteristics for an HBT with 180 nm × 2.7 μm emitter junction area.

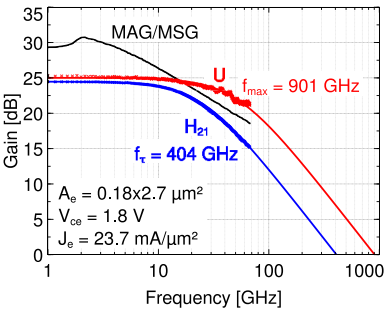

FIGURE 5. Measured RF gains for an HBT with 180 nm × 2.7 μm emitter junction area and 310 nm base-collector mesa width using off-wafer LRRM structures and on-wafer pad open/short de-embedding. Single-pole fit to the measured data yields f_τ 404 GHz, f_{max} 901 GHz.

Sub-20 nm alignment tolerance between emitter and base has been attained in electron beam lithography. Such alignment tolerance is necessary given that the base metal-semiconductor contacts are only 105 nm wide (Fig. 1).

III. RESULTS

Electrical yield throughout the sample is approximately 80 %, exceeding previous experiments by 30 %. Extractions from transmission line model measurements show base and collector contact resistivity $\rho_{base} \approx 9\,\Omega\,\mu m^2$ and $\rho_{coll} \approx 55\,\Omega\,\mu m^2$. The sheet resistance of unpinched and pinched base TLM structures is estimated at 1200 and 810 Ω/□ [12], indicating process damage to the extrinsic base regions. FIB/TEM analysis reveals that the base metallization interdiffuses with ≈ 6 nm of InGaAs (Fig. 1).

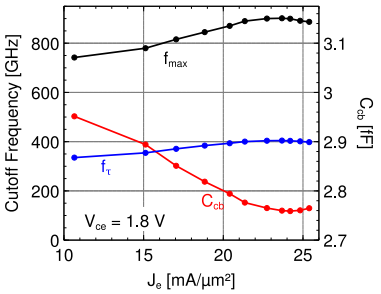

FIGURE 6. Variation of f_τ, f_{max}, and C_{cb} with J_e at V_{ce} = 1.8 V for an HBT with 180 nm × 2.7 μm emitter junction area and 310 nm base-collector mesa width.

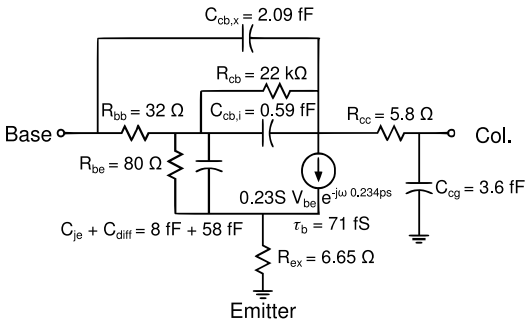

FIGURE 7. A hybrid-π equivalent circuit for the HBT at peak f_{max} performance.

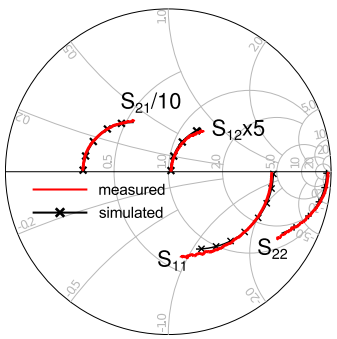

FIGURE 8. Comparison of (solid line) measured S-parameters of Fig. 5 and (x) simulated S-parameters from the model of Fig. 7 from 1–67 GHz.

A total emitter access resistivity $\rho_{em} \approx 3.3\,\Omega\,\mu m^2$ was extracted from RF data. A peak DC current gain $\beta = 25$ was observed on HBTs with emitter area $A_e = 3.7 \cdot 0.24\ \mu m^2$, i.e., on the largest emitter width devices on the sample that have the smallest perimeter-to-area ratio. Figs. 2 and 4 show common-emitter and Gummel characteristics for a transistor with $A_e = 2.7 \cdot 0.18\ \mu m^2$. The common-emitter breakdown voltage $BV_{CEO} = 4.3\,V$ for $J_c = 10\,kA/cm^2$ is observed for the same transistor (Fig. 3). We suspect that the conformal SiN_x layer improves surface passivation of the base-collector junction, thereby reducing the surface trap density [13], [14] and enhancing the surface electric field distribution.

RF measurements from 1-67 GHz were carried out using an Agilent E8361A PNA. The reference plane was brought to the probe tips using LRRM calibration on an impedance standard. The device parameters have been de-embedded from measurements of on-wafer open and short pad structures [15]. Fig. 5 shows peak f_{max} performance at $I_c = 11.3\,mA$, $V_{ce} = 1.8\,V$, $V_{cb} = 0.89\,V$, and $J_e = 23.7\,mA/\mu m^2$. The Kirk effect is observed at $J_e = 25\,mA/\mu m^2$ when f_τ falls to 95 % of its peak value (Fig. 6). A small signal equivalent hybrid-π circuit has been developed from RF measurements (Fig. 7) exhibiting good agreement between measured and simulated S parameters (Fig. 8).

IV. CONCLUSION

InP/InGaAs DHBTs with simultaneous $f_\tau = 404\,GHz$ and $f_{max} = 901\,GHz$ at $w_e = 180\,nm$, 310 nm base-collector mesa width and emitter current density $J_e > 23\,mA/\mu m^2$ have been demonstrated. Sub-20 nm alignment between emitter and base has been achieved using electron beam lithography. The breakdown voltage $BV_{CEO} = 4.3\,V$ has been increased by passivating the base/collector mesa with PECVD SiN_x.

High base and collector contact resistivities limit f_{max} performance. TEM analysis revealed interdiffusion of Pt base metal with InGaAs. Moreover, the extrinsic base semiconductor has been damaged during processing. Future work will pursue reduction in access resistivities while narrowing base contact widths to improve device performance.

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