ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.12, No.3, 1–6

A 529 GHz dynamic frequency divider in 130 nm InP HBT process

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Abstract: This letter presents a 529 GHz 2:1 dynamic frequency divider in a 130 nm InP HBT process, which, to the best of authors' knowledge, is the fastest frequency divider reported thus far. The presented divider is based on a novel structure to overcome bandwidth limitations of traditional dynamic frequency divider design. On-wafer measurement shows that the divider operates with the input frequency from 528.0 GHz to 529.2 GHz with bias voltage tuning, while consuming $P_{DC} \leq 196$ mW. A driver amplifier, integrated for testing purpose, dissipates 348 mW of dc power.

Keywords: dynamic frequency divider, regenerative frequency divider, InP heterojunction bipolar transistors, terahertz

Classification: Microwave and millimeter wave devices, circuits, and systems

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DOI: 10.1587/elex.12.20141118
Received November 28, 2014
Accepted December 15, 2014
Publicized January 7, 2015
Copyedited February 10, 2015

1 Introduction

Terahertz (THz) frequency bands covering 300 GHz to 3 THz have recently been drawing significant attention for their applications in security/medical imaging systems, radar, chemical/bio sensors, and broadband communications. High-speed frequency dividers are an important building block of such THz radio systems for phase-locking and frequency synthesis. Dynamic frequency dividers are capable of higher frequency operation than static dividers [1, 2, 3, 4, 5]. A 168 GHz dynamic frequency divider has been presented in SiGe:C process [2]. In nanoscale CMOS technologies, dynamic frequency dividers operating up to 260 GHz have been demonstrated [3, 4]. Using InP HBTs, a 330 GHz dynamic divider has been reported [5].

In this paper, the design and characterization of a regenerative divider-by-two operating at around 529 GHz is reported in a 130 nm InP HBT technology.

2 InP heterojunction bipolar transistor (HBT) technology

A 130 nm emitter width indium phosphide (InP)-based heterojunction bipolar transistor (HBT) technology was used in this work [6]. The HBT IC process includes thin-film resistors (50 Ohm/sq), MIM capacitors, and 3-levels of gold interconnect (M1-M3). A 7 µm thick BCB layer is used between M2 and M3 to facilitate the formation of low-loss thin-film microstrip lines. The highly-scaled HBTs support very high current (>30 mA/µm^2) and power (>50 mW/µm^2) densities. The common-emitter breakdown of the transistors is $BV_{CEO} = 3.5$ V ($J_E = 10$ µA/µm^2). According to measured S-parameters, a 0.13×2 µm^2 HBT exhibits an extrapolated current gain cutoff frequency $f_t = 520$ GHz and an extrapolated maximum frequency of oscillation $f_{max} = 1.1$ THz at $I_C = 6.9$ mA and $V_{CE} = 1.6$ V.

3 Design of the dynamic frequency divider

3.1 Conventional dynamic frequency divider

Conventional dynamic frequency dividers are in general based on a regenerative feedback loop formed by a double-balanced active mixer, as shown in Fig. 1(a). This conventional topology has been successfully employed for dynamic frequency dividers operating up to 330 GHz [5], but may pose certain difficulties for operation at sufficiently high frequencies. First, the emitter follower (EF) stages (Q_{EF1} and Q_{EF2} in Fig. 1(a)) exhibit diminishing power gain if the divider output frequency approaches the current gain cutoff frequency f_t, making divider operation at these frequencies nearly impossible. Second, the input common-emitter (CE) stages (Q_{CE1} and Q_{CE2} in Fig. 1(a)) have relatively low power gain at sufficiently high frequencies due to their Miller feedback capacitance (i.e. C_{BC}), which will in turn increase the minimum input power for divider operation (i.e. divider sensitivity).

3.2 Proposed dynamic frequency divider

In this letter, a new divider topology is proposed to overcome the bandwidth limitations of conventional dynamic dividers, as shown in Fig. 1(b). First, a common-base (CB) stage (Q_1 and Q_2) substitutes the CE stages at the divider

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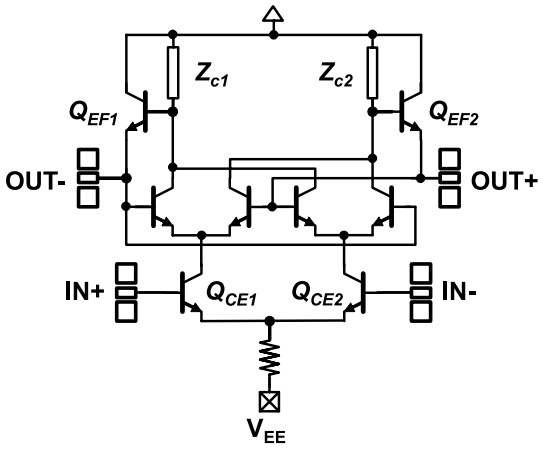
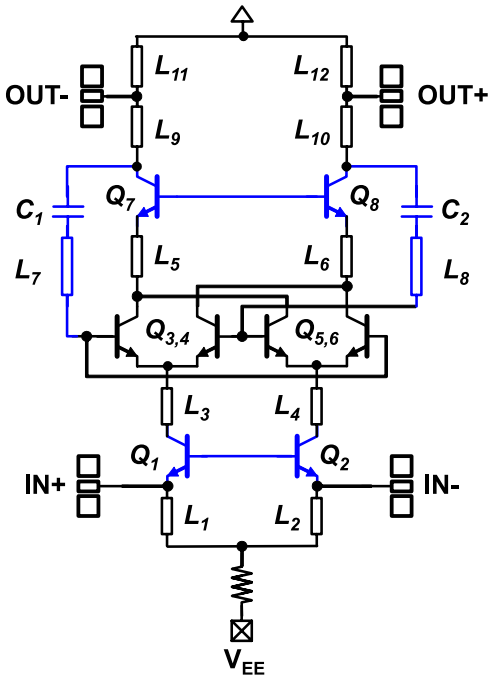


(a) Conventional structure



(b) Proposed structure for higher frequency operation

Fig. 1. Dynamic frequency divider architecture (biasing detail not shown).

input. A single HBT in a CB configuration exhibits 9 dB of maximum stable gain/maximum available gain (MSG/MAG) at around 600 GHz, significantly higher than 3 dB of MSG/MAG in a CE configuration (HBT size: $0.13 \times 3\ \mu m^2$, biased at $J_E = 18\ mA/\mu m^2$, $V_{CB} = 0.8\ V$). Therefore, the CB input stages effectively lower the divider input sensitivity by 6 dB compared to the conventional design. Second, CB stages are employed instead of EF HBTs inside the regenerative loop (Q_7 and Q_8), so that the divider operation is no longer limited by HBT f_t. Output of these CB HBTs are fed back to the differential pairs ($Q_{3,4}$ and $Q_{5,6}$) through a dc-block capacitor ($C_{1,2}$) and a series transmission line ($L_{7,8}$). Simulation shows that the conventional design operates up to $f_{in} = 400$ GHz, but the proposed divider design is capable of operating beyond $f_{in} = 600$ GHz, significantly extending the maximum divider input frequency.

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In Fig. 1(b), $L_{1,2}$ and $L_{3,4}$ provide the input and inter-stage matching, respectively. Elements in the feedback loop ($C_{1,2}, L_{5-8}$) were adjusted for optimum divider bandwidth. Transmission lines L_{9-12} provide the divider output matching.

3.3 Design of the divider test chip

The proposed dynamic divider is designed in a 130 nm HBT process. In simulation, the divider is operating from $f_{in} = 590$ GHz to 620 GHz at an input power of $P_{in} = -3$ dBm. Inverted-microstrip lines (IMSL) are used for the divider design where the top-metal layer (M3) forms a solid ground plane. In normal microstrip environment, ground holes in M1 or M2 are inevitable, and associated ground inductances may affect the divider operation. All HBTs are $0.13 \times 3\ \mu m^2$. All passive elements and wires are modeled by 2.5-D electromagnetic simulations.

To facilitate on-wafer testing of the divider, a 10-stage single-ended drive amplifier [7] is integrated in the test chip, along with an on-chip balun, to drive the frequency divider, as shown in Fig. 2. The drive amplifier has 20 dB of small-signal gain with −1 dBm of saturated output power at 600 GHz, in simulation. Simulated loss of the balun is 1.2 dB. For testing convenience, only one single-ended output of the divider is taken off-chip, with the unused output port terminated by an on-chip 50 ohm resistor.

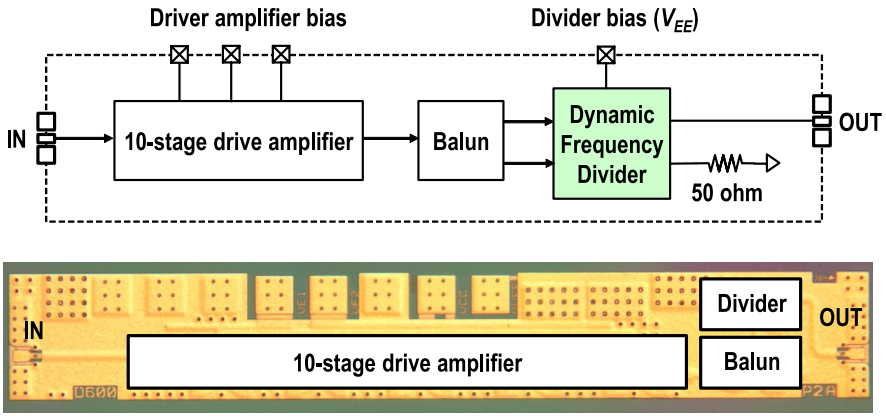

Fig. 2. Dynamic frequency divider test chip (size: $1{,}580 \times 240\ \mu m^2$): Block diagram (top), photograph (bottom).

4 Measurement results

The fabricated divider chip was characterized using the on-wafer testing setup shown in Fig. 3. A low-frequency signal source (~14.6 GHz) drives a chain of multipliers to reach the divider input frequency (WR-1.5 band). The divider output is down-converted by a WR-3 harmonic mixer (80 dB conversion loss), and the IF output is measured by a spectrum analyzer. A WR-1.5 Dominion Microprobes GSG probe (8 dB loss) and a WR-3 GGB waveguide GSG probe (3 dB loss) were used for the divider input and output, respectively.

First, the divider is biased at a nominal voltage $V_{EE} = -7.5$ V ($I_{EE} = 22.2$ mA), consuming 166.5 mW of dc power (P_{DC}), while the 10-stage integrated driver amplifier dissipates 348 mW of dc power. The measured operating frequency of the divider was from $f_{in} = 528.78$ GHz to 529.06 GHz with 280 MHz of bandwidth, as

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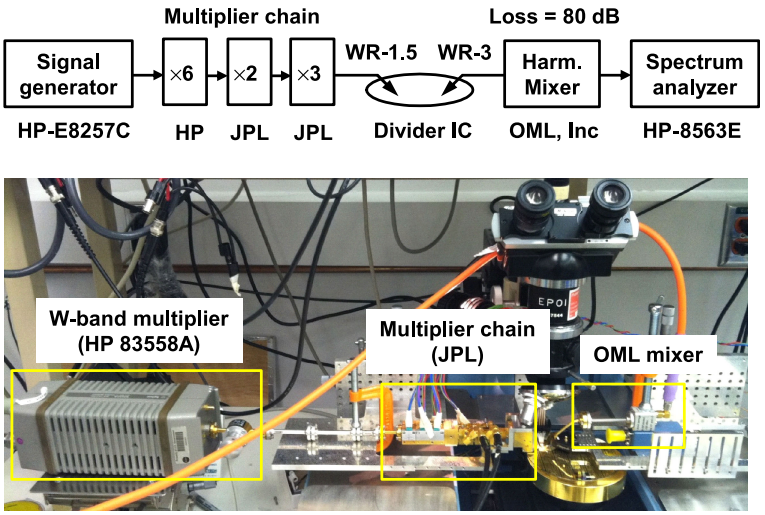
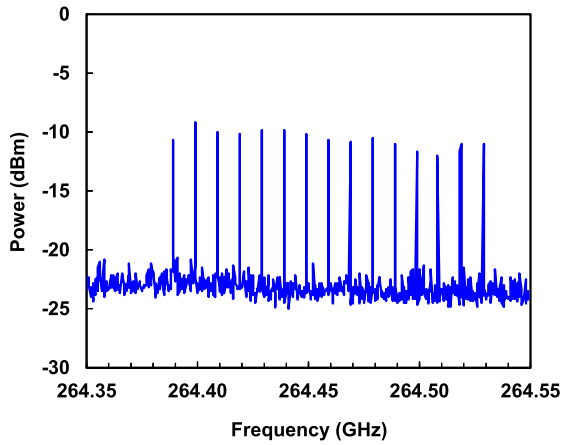
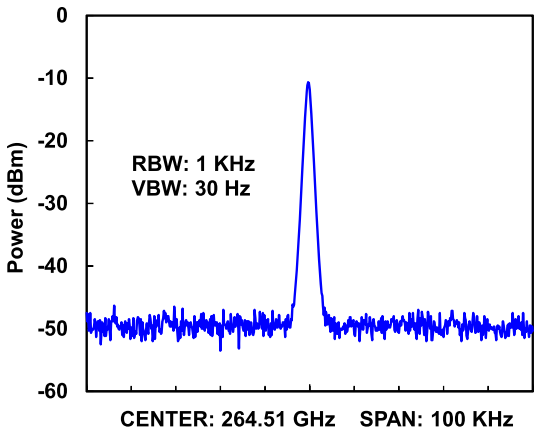


Fig. 3. Divider testing setup: Block diagram (top), photograph (bottom)

shown in Fig. 4(a). Close-up spectrum of the divider output with f_{in} = 529.02 GHz is shown in Fig. 4(b). The signal peak passes the built-in "Signal Identification" check of the spectrum analyzer, confirming the observed peak is at $f_{in}/2$.



(a) f_{in} = 528.78 - 529.06 GHz (280 MHz of divider bandwidth)



(b) f_{in} = 529.02 GHz

Fig. 4. Measured divider output spectrum at a nominal bias, V_{EE} = −7.5 V.

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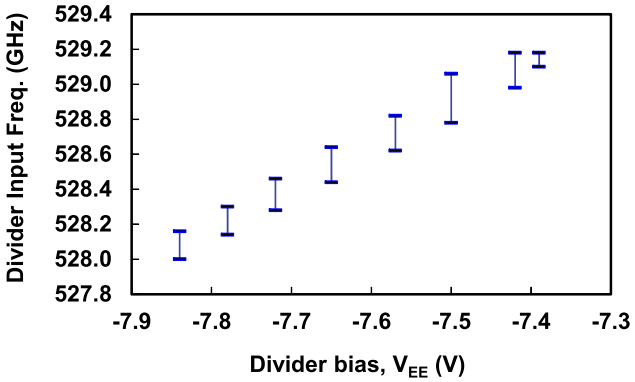

Fig. 5. Measured operating frequency range of the divider with bias voltage tuning (V_{EE}).

Next, the divider bandwidth was measured while varying the divider bias (Fig. 5). The divider was functional from $f_{in} = 528$ GHz to 529.2 GHz (1.2 GHz of total bandwidth), as V_{EE} was tuned from −7.84 V to −7.4 V, with $P_{DC} \leq 196$ mW. The measured divider output power ranges from −16 dBm to −9 dBm, after de-embedding WR-3 probe loss and down-conversion loss (3 dB and 80 dB, respectively).

The discrepancy in divider operating bandwidth between measurement and simulation is partly attributed to various layout parasitics that may not have been accurately modeled during the design, and also partly attributed to lower-than-expected output power of the on-chip driver amplifier. Testing of the driver amplifier breakout revealed that the measured saturated output power was approximately −4 dBm, which is 3 dB lower than simulation.

5 Conclusion

A new circuit topology for dynamic frequency division is proposed to overcome the frequency limit of traditional regenerative frequency divider. The proposed divider is implemented in a 130 nm InP HBT process. On-wafer measurement shows the divider operates from 528.0 to 529.2 GHz with bias tuning, which represents the highest operating frequency for a frequency divider reported thus far, to the best of authors' knowledge.

Acknowledgments

This work was supported by the Defense Advanced Research Projects Agency under the THz Electronics Program under Contract HR0011-09-060, the National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIP) (2014R1A5A1011478), and MEST (2013-056424).

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