Transistors for VLSI, for Wireless: A View Forwards Through Fog

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With transistors approaching scaling limits, demonstrating a record device demands ~20-40 process steps, many at extreme resolution. Facing this, how might a Ph.D. student steer the future of VLSI or of wireless systems? Beyond exploring yet more new channel materials, whether 2D or 3D, we explore below other options.

For VLSI, transistors are made small, making them plentiful (cheap) and the wires connecting them short, with low delay (CV_{DD}/I), and low switching energy ($CV_{DD}^2/2$); *small-area electronics* is key. Low power demands low V_{DD} yet low I_{off} . Below threshold, we seek characteristics steeper than thermal; above it, dI/dV should be large.

Tunnel FETs [1] are the most studied steep transistors. Yet, in nm TFETs, quantization increases barrier energies and nonparabolicy increases carrier mass. WKB hand calculations predict only 10% tunneling probability for a 2nm barrier, 1% for 4nm. The barrier thickness is not easily reduced, being set by the source doping and channel and dielectric thicknesses, hence on-current and logic speed will be low. Adding a second barrier [2] introduces a bound state, and dI/dV peaks as the state aligns with the source. A multi-layer electron *anti-reflection coating* (fig.1) [3], increases transmission over a broad energy range; design parallels microwave impedance-matching.

An array of barriers is a superlattice. Transmission outside the miniband is small but approaches 100% inside it; on-current in superlattice steep FETs can be high [3,4]. We might build a steep finFET (fig. 2) using ALE [5] to grow superlattices on the fin ends. Simulations [6] ignoring scattering indicate large I_{on} and small I_{off}. The challenges are fabrication, modeling, and design for steep switching in the presence of scattering. Ferroelectric steep FETs [7] are promising; the challenges are in materials and in field concentrations at the gate edges..

Steep FETs may not prove viable. We would then seek low leakage and a subthreshold slope close to thermal. A large dI/dV lets us reduce the supply voltage. As with Si [8], in [110] III-V P-finFETs, quantization in a ~2 nm thick body forces transport into one narrow, low-mass lobe of the E-k surface [9], with transport rivaling NFETs (figs. 3,4). In NFETs, higher-ε dielectrics have lower energy barriers, frustrating attempts to scale. Yet, TiO_2 provides a huge ε *and* a large valence-band barrier; perfect for a small, high-current PFET. Once dielectrics can be made no thinner, electrostatics forces us to fins and nanowires; defining channel thicknesses by epitaxy [10,11], instead of etching, lets us make such structures thinner and smoother, with, critically, less scattering from surface roughness.

We can corrugate the semiconductor surface. Forming tall fins (fig. 5) [11] or vertically stacking nanowires [10] increases the current from an available die area. We can then drop the voltage close to threshold while maintaining enough current for fast logic, likely beating TFETs. As the lithographic depth of focus is small, the challenge is now fabrication, requiring planar lithography, pattern transfer and vertical dry-etching. Once gate lengths drop below 10nm, source-drain tunneling increases leakage; increasing transport mass reduces tunneling but, unfortunately, also on-current. Bending (fig. 6) the channel [12] makes the transport path longer than the FET footprint, suppressing tunneling, and improving electrostatics, yet packing transistors tightly and keeping on-current high. Increasing the channel bandgap where fields are high suppresses band-band tunneling; this is a heterojunction MOSFET [13].

With their design now so difficult, it is too much to demand that digital FETs also provide high transistor bandwidths for wireless/RF circuits; VLSI FET cutoff frequencies have stagnated at ~250GHz [14]. Yet, growing use of mobile phones now drives links to mm-wave frequencies. We need wireless-specific small-scale IC technologies for power- and low-noise amplifiers, and for all RF functions at the highest frequencies. For these ICs, InP and GaN transistors can be made much faster. For THz bipolar transistors, low-resistivity base contacts are the key challenge. Present ~ 1THz devices (fig. 10), with ultra-shallow base contacts, have bandwidths ~3:1 lower than understood limits [15]; regrowth (fig. 11) will allow extreme doping under the contacts, lower resistivity, and perhaps 3THz f_{max}. In THz HEMTs, the gate dielectric is key, and ALD Al_2O_3/ZrO_2, drawn from III-V MOS [12], will permit scaling for perhaps 1-2 more generations. Possibly, a [110] P-GaSb/TiO2 THz HEMT might scale best.

References: [1] J. Appenzeller *et. al*.,. IEEE TED, Dec. 2005, [2] U. Avci, I. Young, 2013 IEDM, [3] P. Long, E. Wilson, unpublished, [3] M. Bjoerk *et. al*., U.S. Patent 8,129,763, [4] E. Gnani *et. al*.,. 2011 IEDM, [5] S. Bedair, Semiconductor Science & Technology, 1993, [6] P. Long *et. al*.,. EDL, Dec. 2014, [7] S. Salahuddin, S. Datta, Nano Lett. 2008, [8] E. Wang, *et. al*., IEEE TED 2006, [9] S. Mehotra, unpublished, [10] J.J. Gu *et. al*., 2012 DRC, [11] D. Elias, 2013 DRC [12] S. Lee *et. al*.,. 2014 VLSI Symp., [13] C.-Y. Huang *et. al*.,.2014 IEDM, [14] O. Inac *et. al*.,. 2011 CSICS, [15] M. Rodwell *et. al*.,. 2008 IEEE Proceedings.

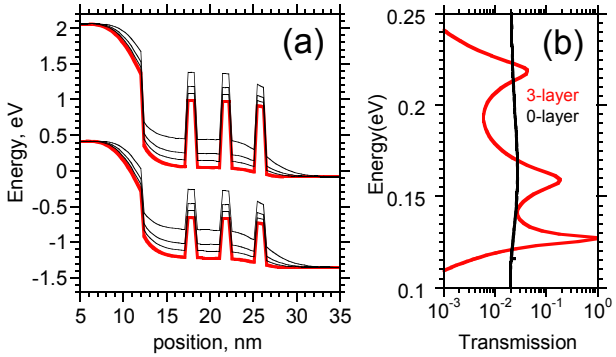

Fig. 1: GaSb/InAs tunnel FET (a) with 3-layer electron anti-reflection coating and (b) energy-dependent transmission at V_{GS}=V_{DS}=0.3V.

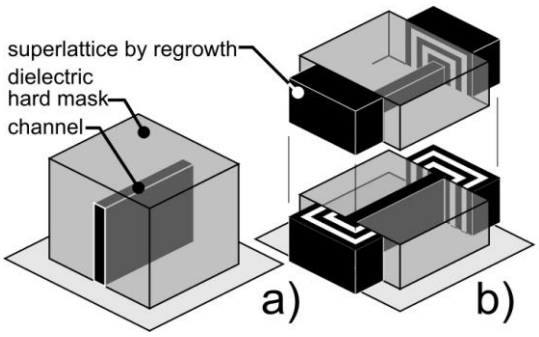

Fig. 2: Steep FET formed (a) from a fin with a source superlattice (b) grown by ALE.

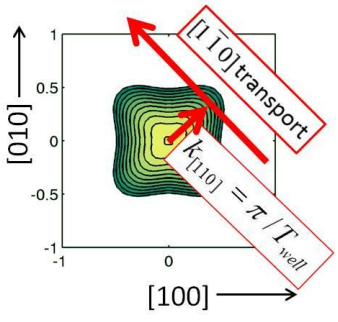

Fig. 3: InGaAs valence-band (E-K) surface showing low transport mass arising from strong quantum confinement.

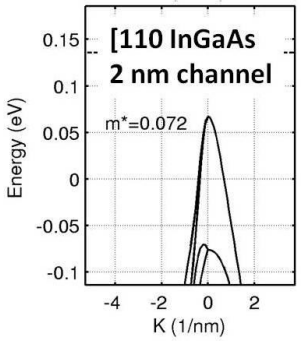

Fig. 4: Valence-band *E-K* dispersion for a 2nm thick, [110] InGaAs layer. The hole effective mass is very low at 0.072 m_o.

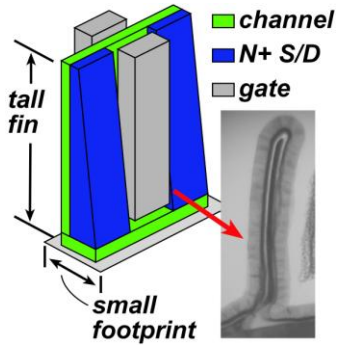

Fig. 5: MOSFET (finFET) with high aspect ratio for high drive current, enabling low-V_{DD} logic.

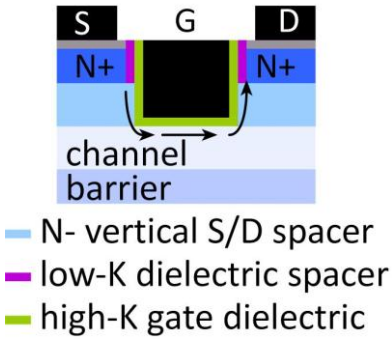

Fig.6: MOSFET with a small gate footprint yet long transport distance. This improves electrostatics and reduces tunneling.

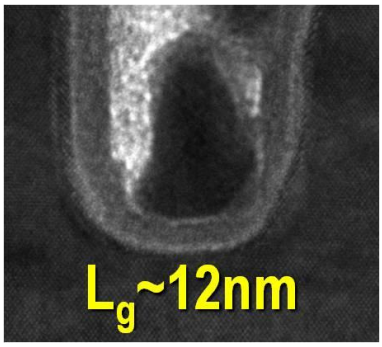

Fig. 7: 12nm L_g InGaAs/InAs/InP with InP vertical spacers for low I_{off}.

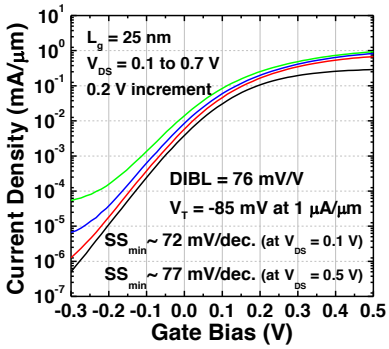

Fig. 8: InAs-channel MOSFET [12] with a 2.7nm thick channel, 25nm L_g, and the structure of fig. 6.

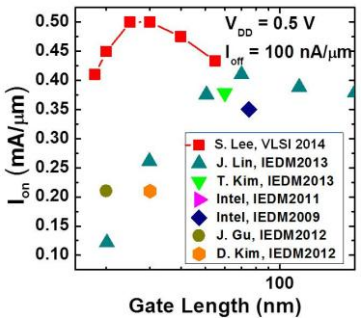

Fig.9: I_{on} at 0.5V V_{DD} and 100nA/μm I_{off}, versus L_g, for an InAs MOSFET [12], compared to the literature.

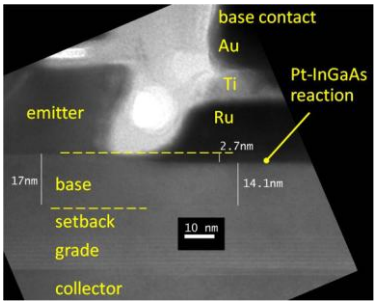

Fig. 10: 130nm InP HBT with ultra-shallow base contacts and > 1THz f_{max}.

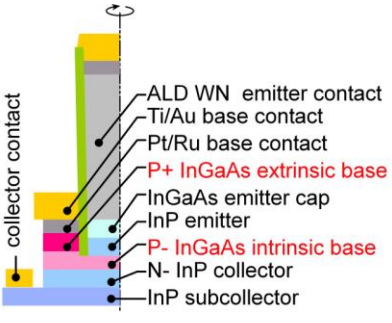

Fig. 11: Regrown-emitter HBT with thick, heavily-doped extrinsic base for low-resistivity contacts hence increased f_{max}.