12 nm-Gate-Length Ultrathin-Body InGaAs/InAs MOSFETs with $8.3 \cdot 10^5$ I_{ON}/I_{OFF}

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Device Research Conference 2015
Late News
Columbus, OH

III-V FETs at sub-10-nm nodes?

- III-V channels: low electron effective mass, high velocity, high mobility→ higher I_{on} at lower V_{DD}→ reducing switching power
- III-V FETs have high leakage current because:

✓ Low bandgap→ larger band-to band tunneling (BTBT) leakage

✓ High permittivity→ worse electrostatics, large subthreshold leakage

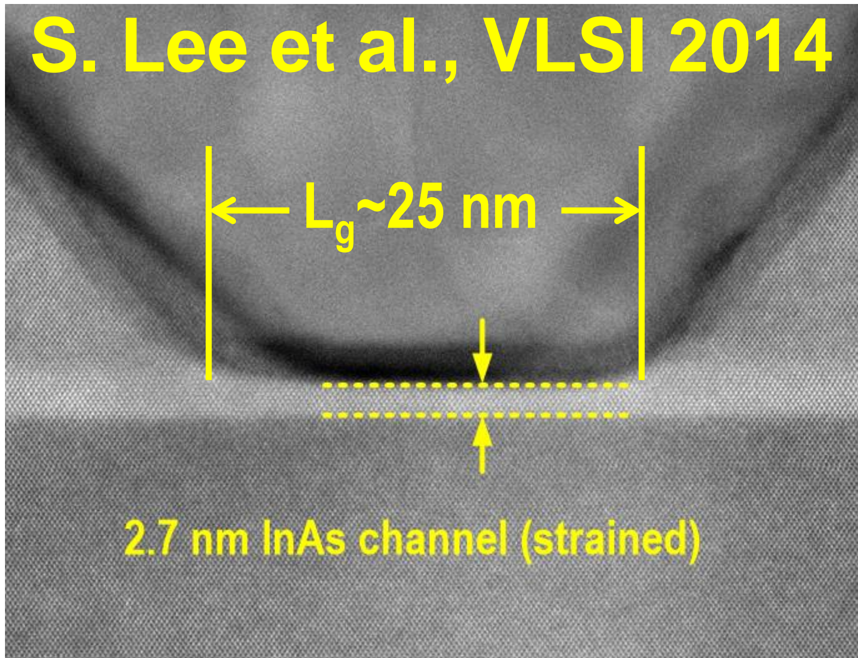
- I_{off}<100 nA/μm (High performance) and I_{off}<100 pA/μm (Low power)
- Question: Can III-V MOSFETs scale to sub-10-nm nodes?

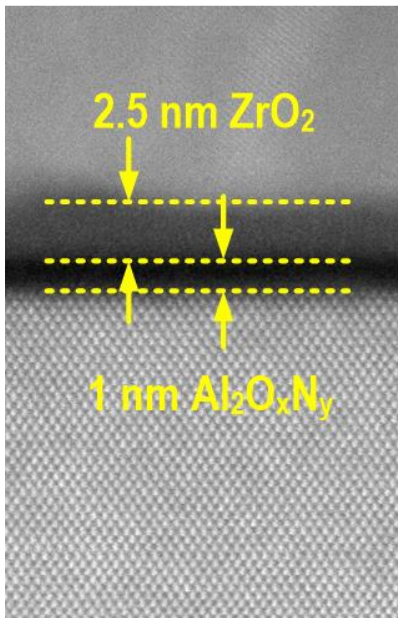
300K	Si	Ge	GaAs	InAs	$In_{0.53}Ga_{0.47}As$
m_e*	0.19	0.08	0.063	0.023	0.041
μ_e(cm^2/V·s)	1450	3900	9200	33000	12000
μ_h(cm^2/V·s)	370	1800	400	450	<300
Eg(eV)	1.12	0.664	1.424	0.354	0.75
ε_r	11.7	16.2	12.9	15.2	13.9
a(Å)	5.43	5.66	5.65	6.06	(InP)

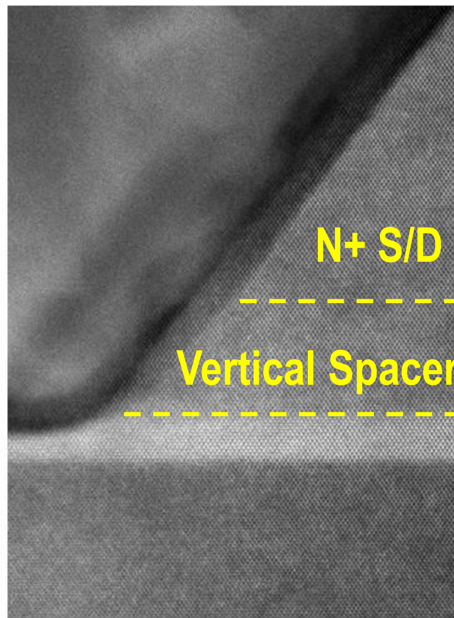
Logic industry node	Physical gate length (nm)
16/14	20
10	17
7	14
5	12

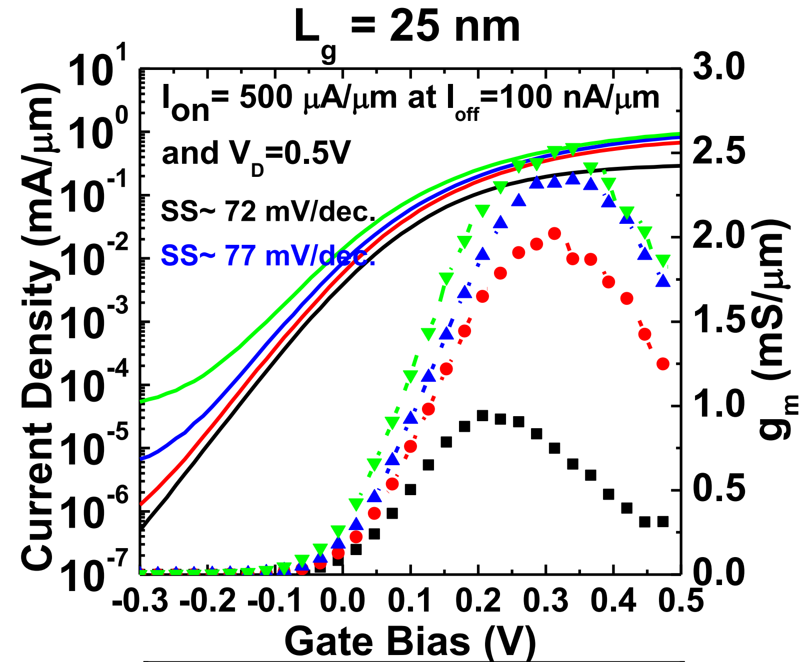
Ref: 2013 ITRS Roadmap

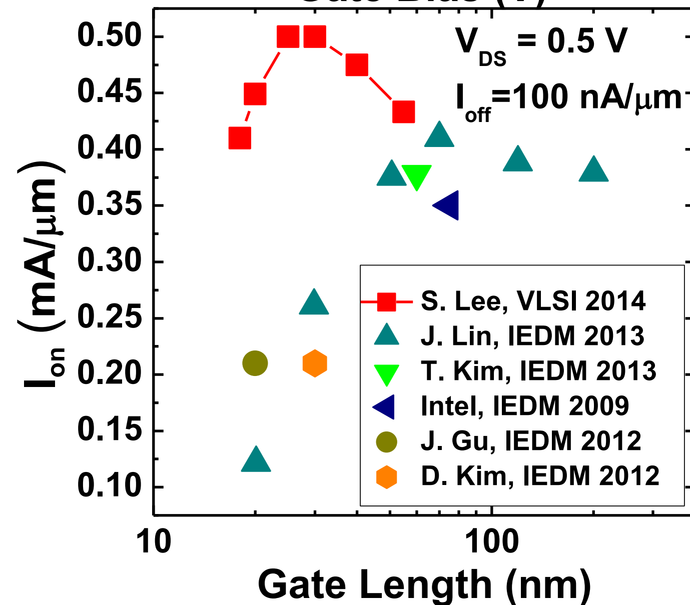
Record high performance III-V FETs



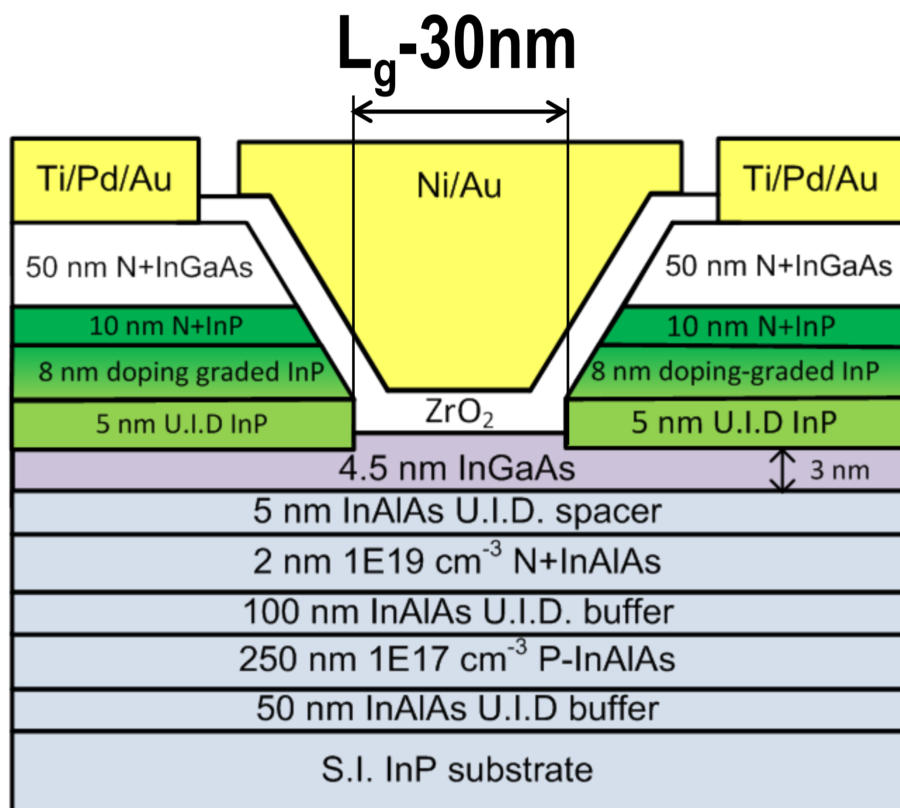




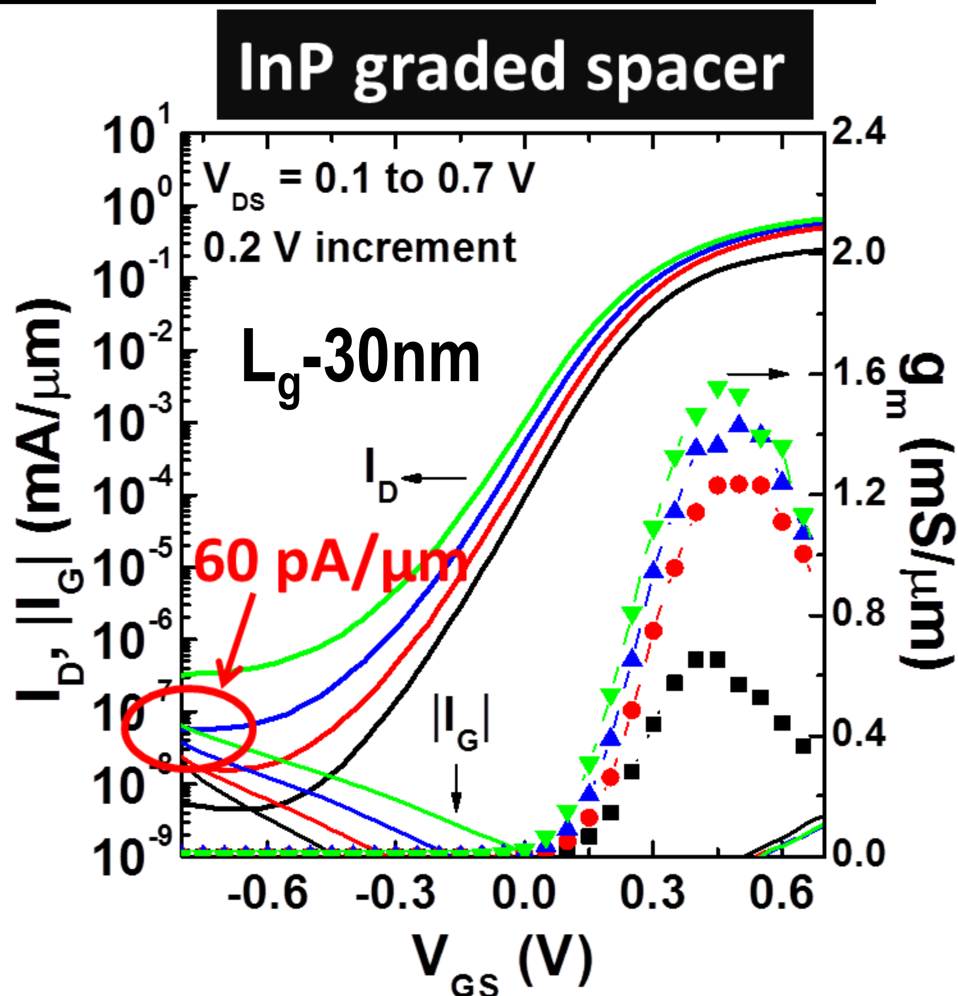




Record low leakage III-V FETs



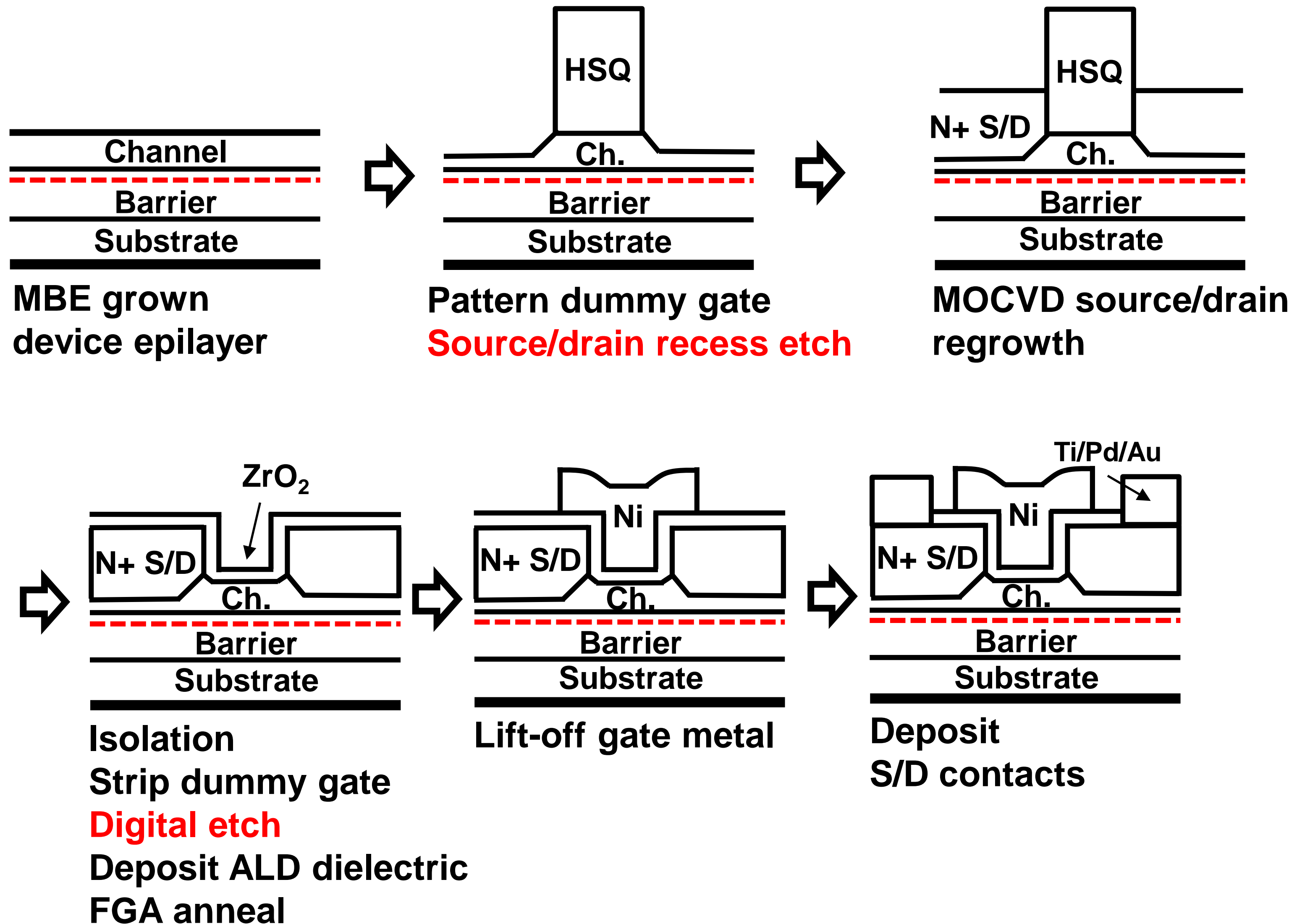
C. Y. Huang et al., IEDM 2014



- Minimum I_{off}~ 60 pA/μm at V_D=0.5 V for L_g-30 nm
- Recessed InP shows 100:1 smaller I_{off} compared to InGaAs spacers
- BTBT leakage is completely removed→ sidewall leakage dominates I_{off}

UCSB Gate Last Process Flow

UCSB

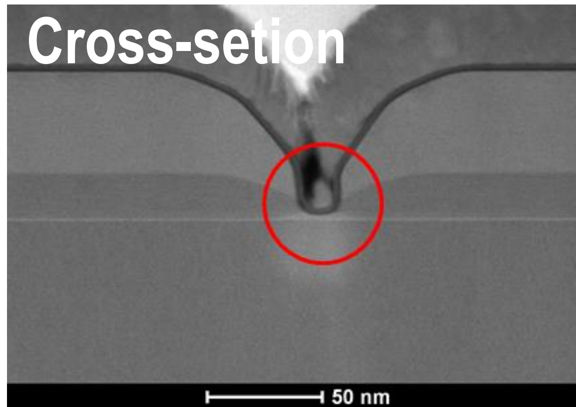


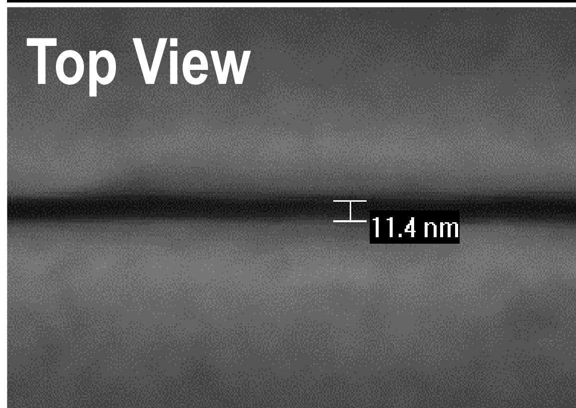
TEM images of L_g~12 nm devices

Ti/Pd/Au
Ni/Au
Ti/Pd/Au

Layer	Thickness
N+InGaAs	50 nm
N+InP	10 nm
Doping-graded InP	8 nm
U.I.D. InP spacer	5 nm

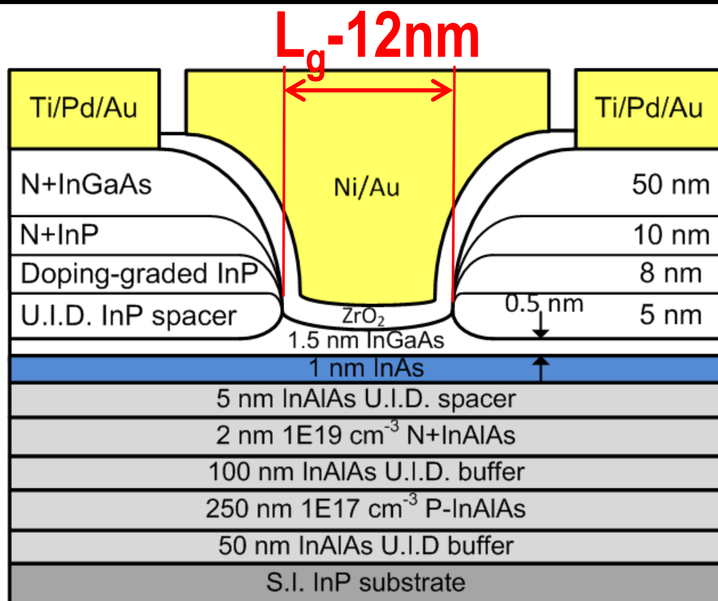
ZrO_2
0.5 nm
1.5 nm InGaAs
1 nm InAs
5 nm InAlAs U.I.D. spacer
2 nm 1E19 cm^{-3} N+InAlAs
100 nm InAlAs U.I.D. buffer
250 nm 1E17 cm^{-3} P-InAlAs
50 nm InAlAs U.I.D buffer
S.I. InP substrate

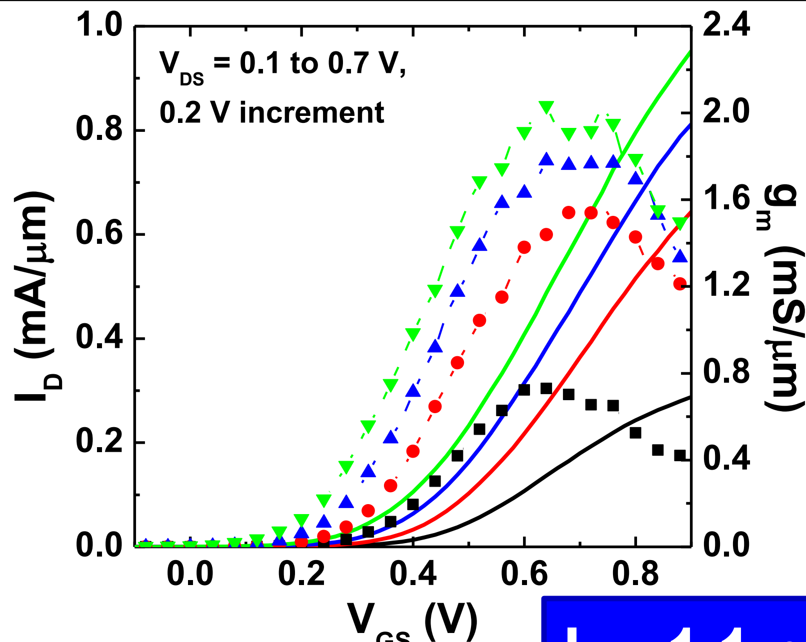


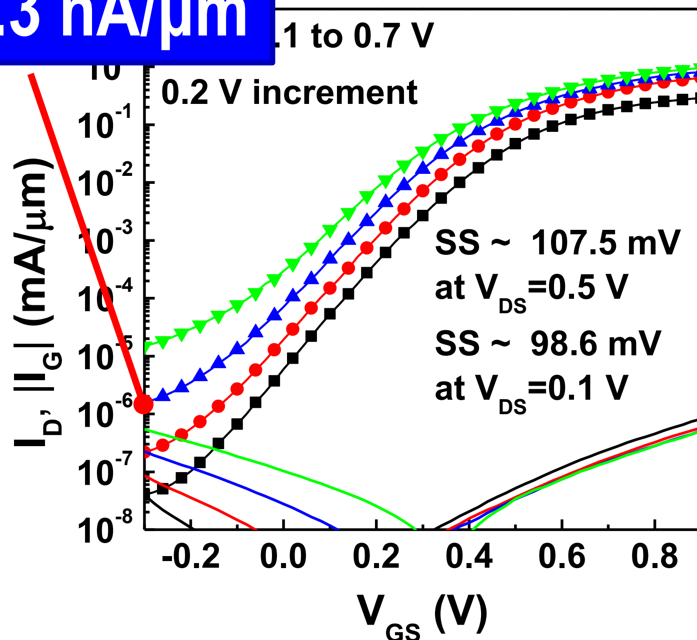


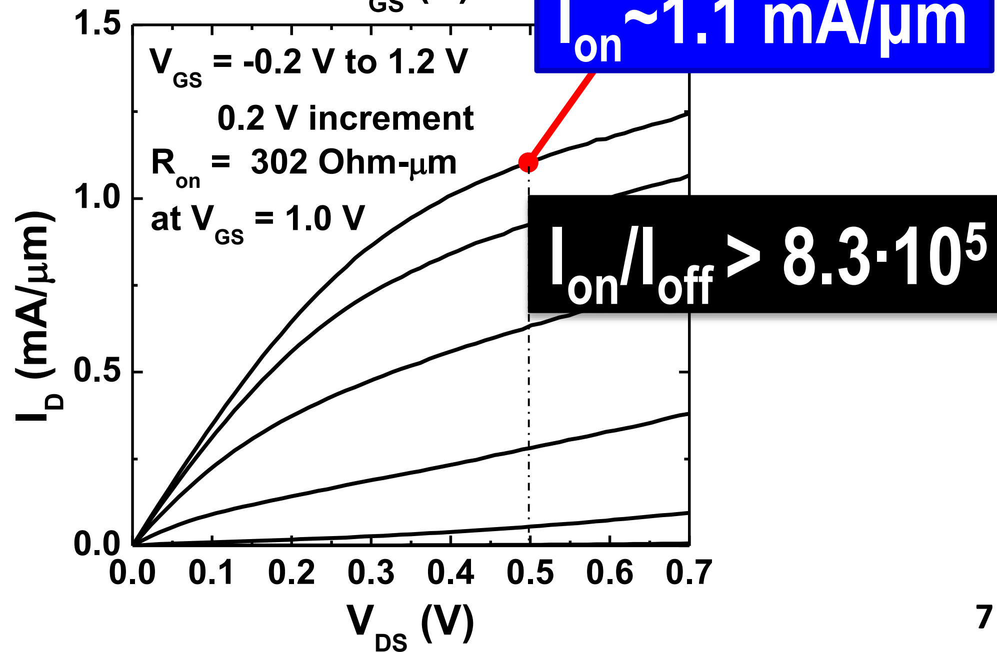
L_g~12nm
N+InGaAs
~ 8nm
N+InP
Ni
InP spacer
InAlAs Barrier
t_{ch}~ 2.5 nm
(1.5/1 nm InGaAs/InAs)
5 nm

I_D-V_G and I_D-V_D curves of 12nm L_g FETs

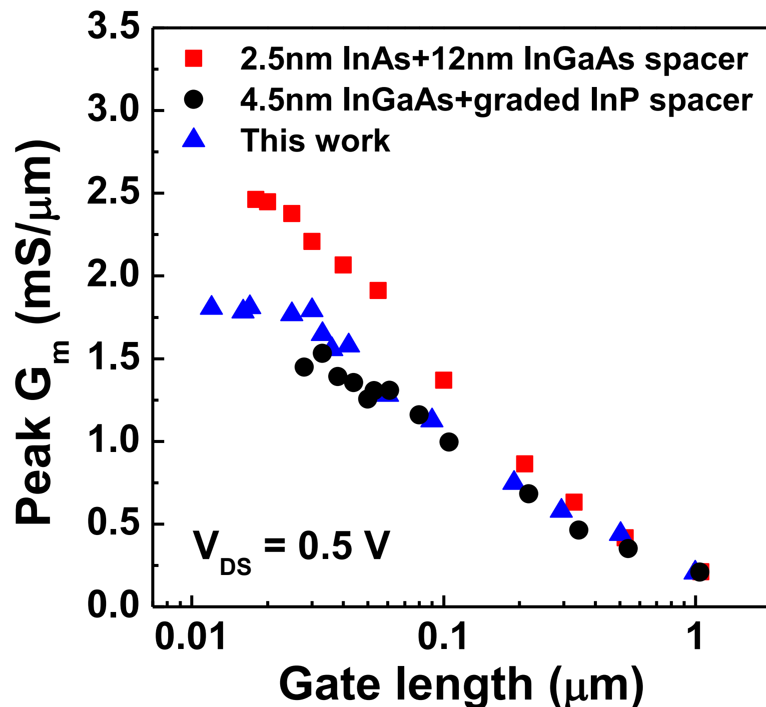


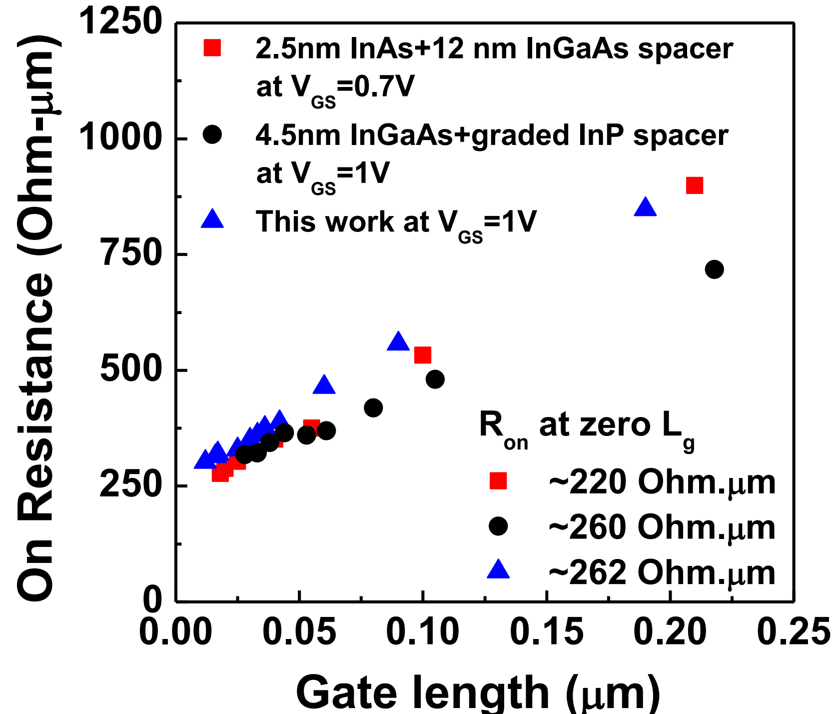






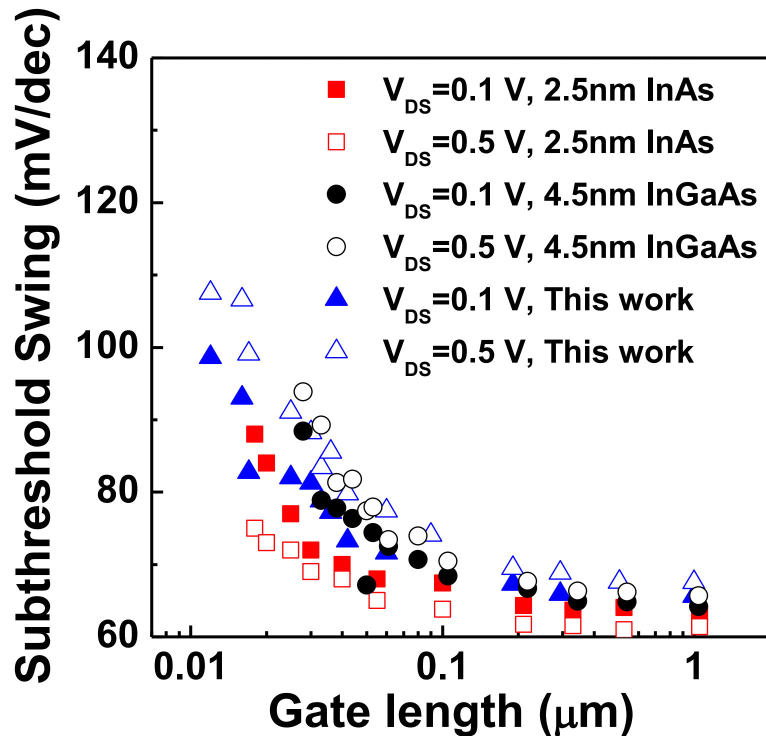
On-state performance

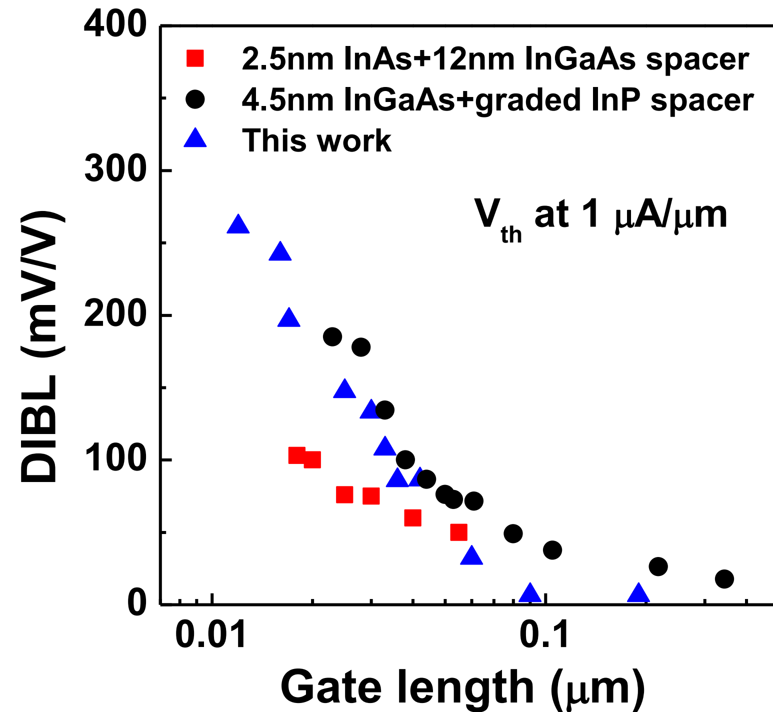




- Slightly higher G_m for a 2.5 nm composite channel than a 4.5 nm InGaAs channel → larger gate capacitance.
- A 2.5nm InAs channel with a 12 nm InGaAs spacer shows highest G_m → high indium content channel is desirable for UTB III-V FETs.
- InP spacers increase parasitic $R_{S/D}$ to ~260 Ω·μm → InP spacers need further optimization.

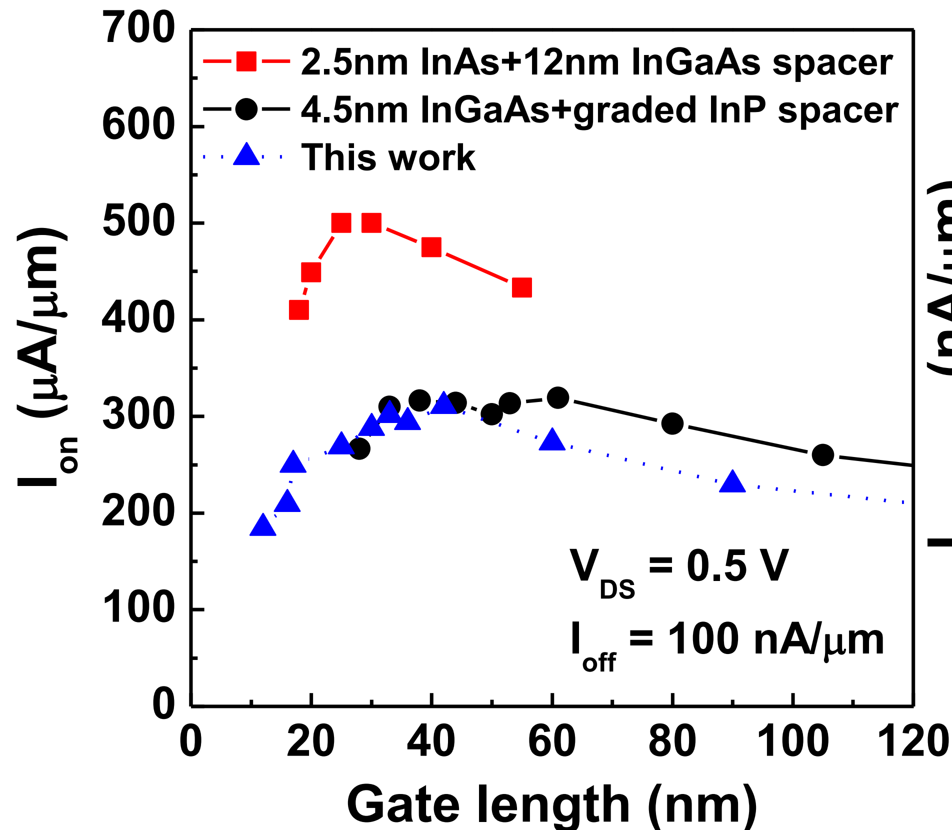
Subthreshold characteristics

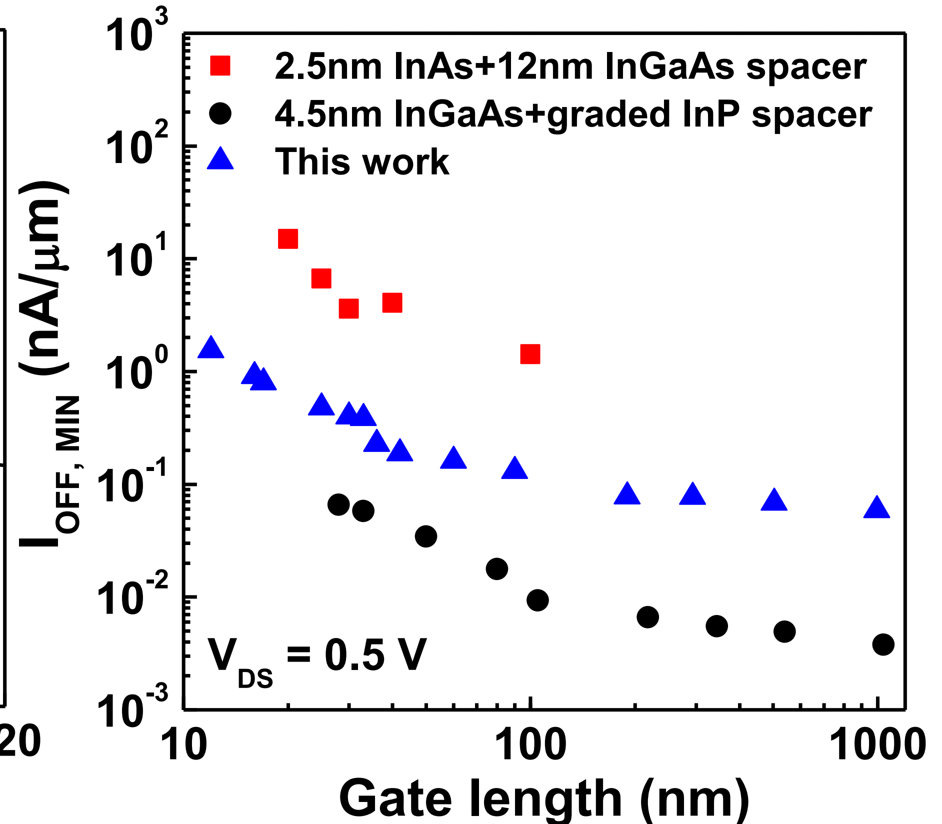




- A 2.5nm InAs channel with a 12 nm InGaAs spacer shows the lowest SS and DIBL because of the best electrostatics.
- A 5 nm un-doped InP spacer with the atop 8 nm linearly doping-graded InP have shorter effective gate length as compared to 12 nm un-doped InGaAs spacers→ worse electrostatics.
- SS~107 mV/dec. and DIBL~260 mV/V for 12 nm devices→ FinFETs will cure this.

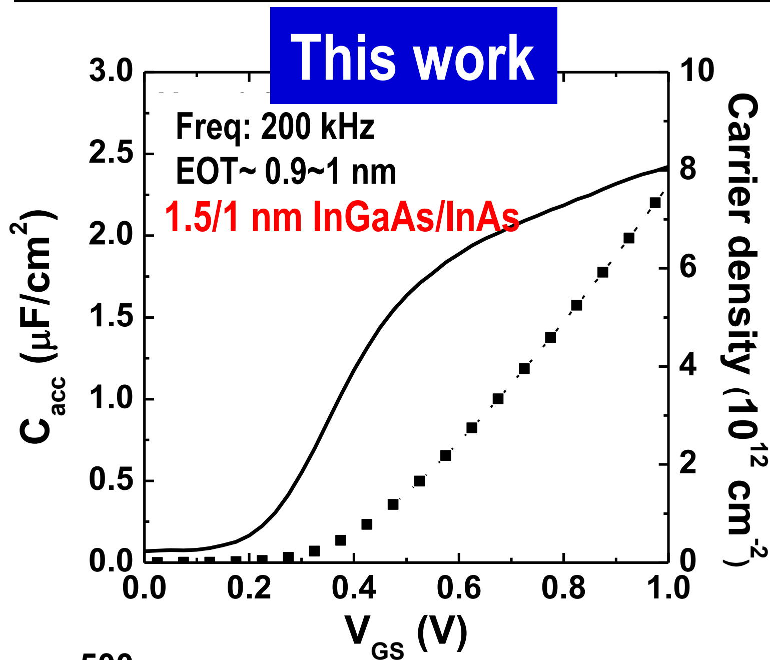
I_{on} and I_{off} versus L_g

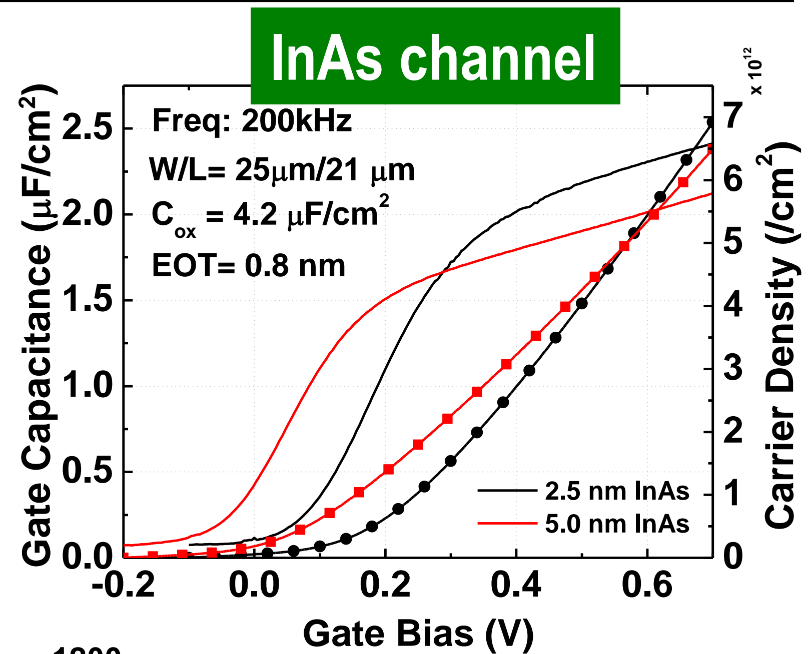


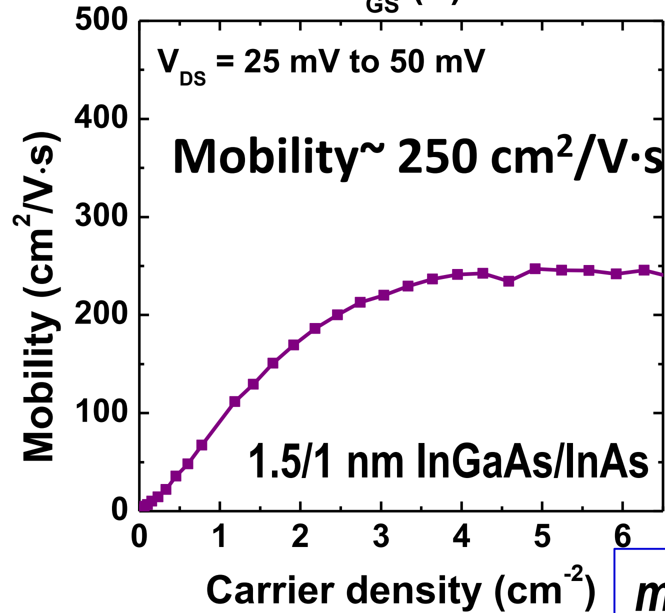


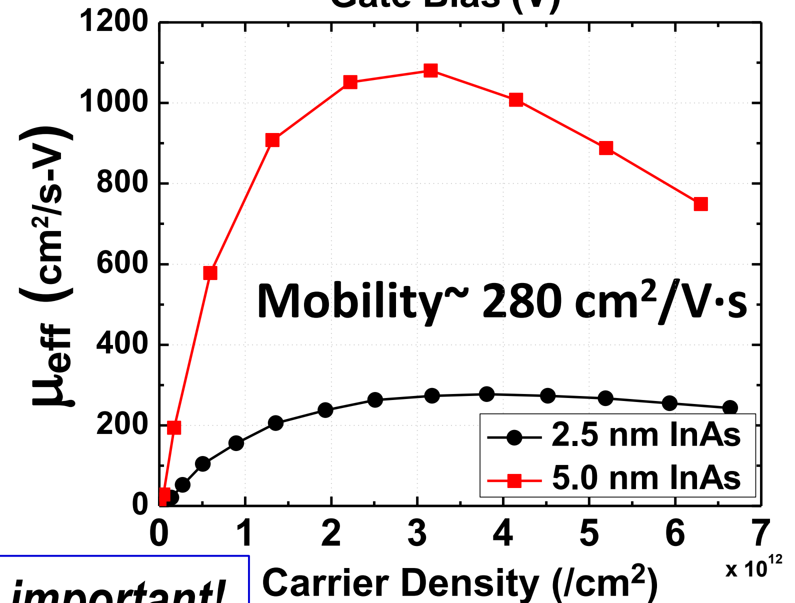
- High In% content channels are required to improve I_{on}, but I_{off} is relatively large (~10 nA/µm).
- InGaAs channels with recessed InP source/drain spacers are required for low leakage FETs.
- A clear tradeoff between on-off performance.

Mobility extraction at L_g-25 μm long channel FETs









m, $R_{S/D}$ more important!*

Summary

- **We demonstrated a 12nm-L_g ultrathin body III-V MOSFET with well-balanced on-off performance. (I_{on}/I_{off}> 8.3·10^5)**
- **The 12nm-L_g FET shows G_m~1.8 mS/µm and SS~107 mS/dec., and minimum I_{off}~ 1.3 nA/µm.**
- **High indium content channel is required to improve on-state current. *(High performance logic)***
- **Thin channels, InGaAs channels, and recessed InP source/drain spacers are the key design features for very low leakage III-V MOSFETs. *(Low Power Logic)***
- **III-V MOSFETs are scalable to sub-10-nm technology nodes.**

Acknowledgment

Thanks for your attention!
Questions?

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- *This work was partially supported by the MRSEC Program of the National Science Foundation under Award No. DMR 1121053.*

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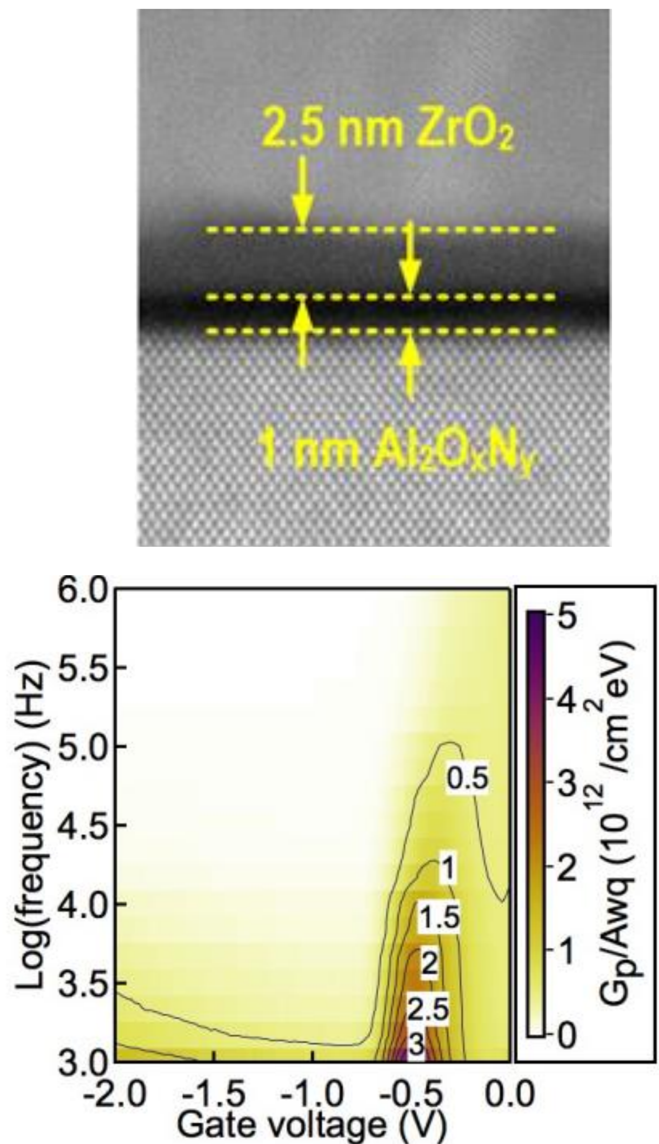
(backup slides follow)

Record low subthreshold swing



S. Lee et al., VLSI 2014

Dot : Reverse Sweep
Solid: Forward Sweep
L_g = 1 μm

SS_{min} ~ 61 mV/dec.
(at V_{DS} = 0.1 V)
SS_{min} ~ 63 mV/dec.
(at V_{DS} = 0.5 V)

Current Density (mA/μm)
|Gate Leakage| (A/cm^2)
Gate Bias (V)

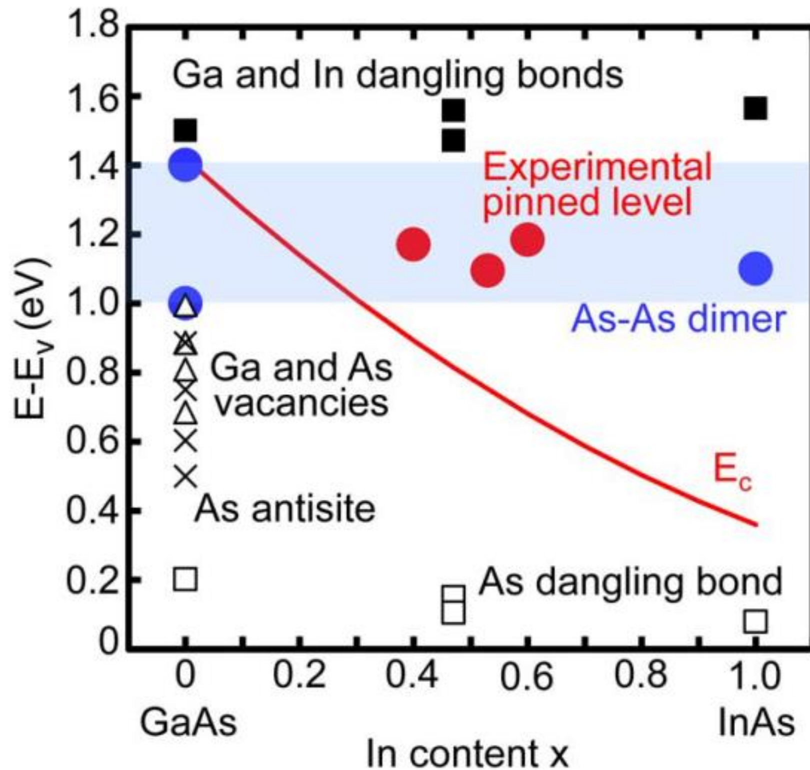
Achieved SS~ 61 mV/dec.

Superior high-k dielectrics on III-V channels.

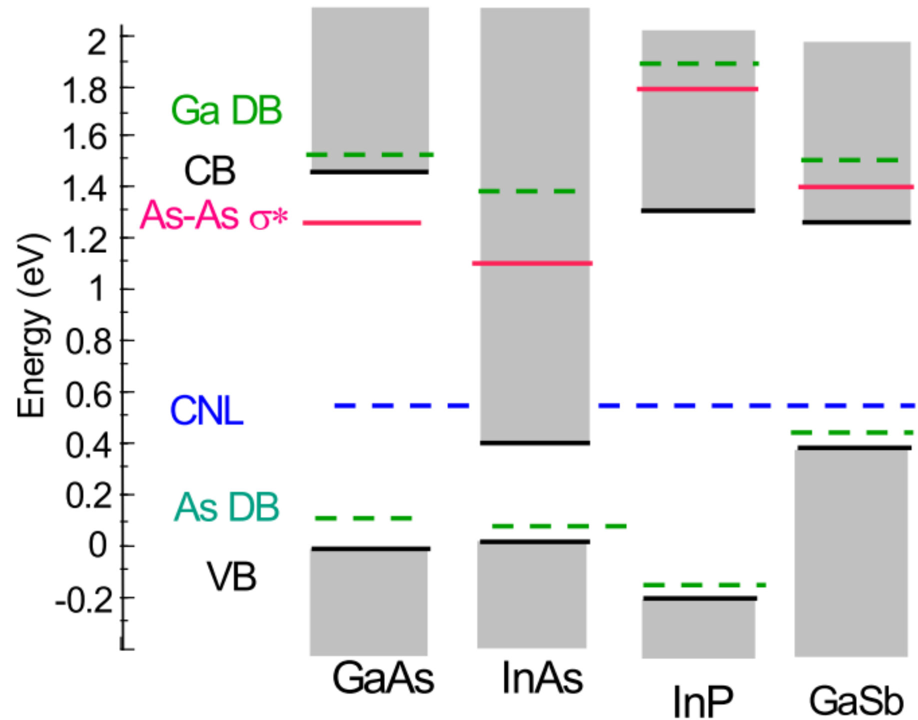
Dielectrics from Gift Chobpattana, Stemmer group, UCSB.

Why InAs channel is better…

- Electron scattering with oxide traps inside conduction band
- Electrons in high In% content channel have less scattering with oxide traps.

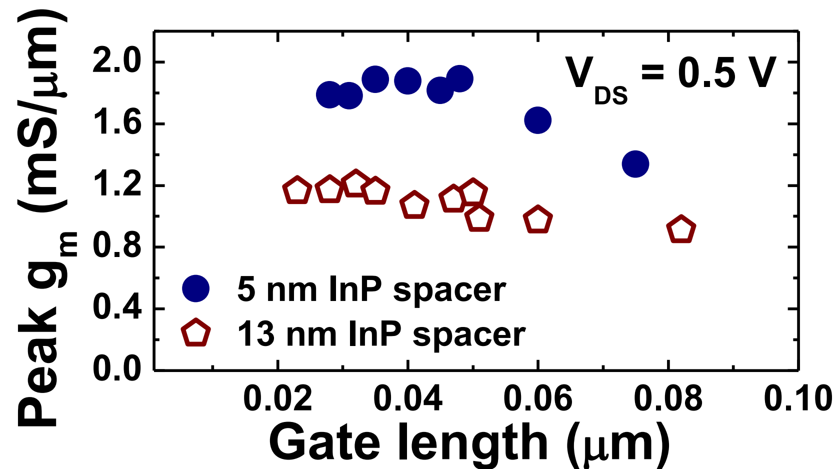


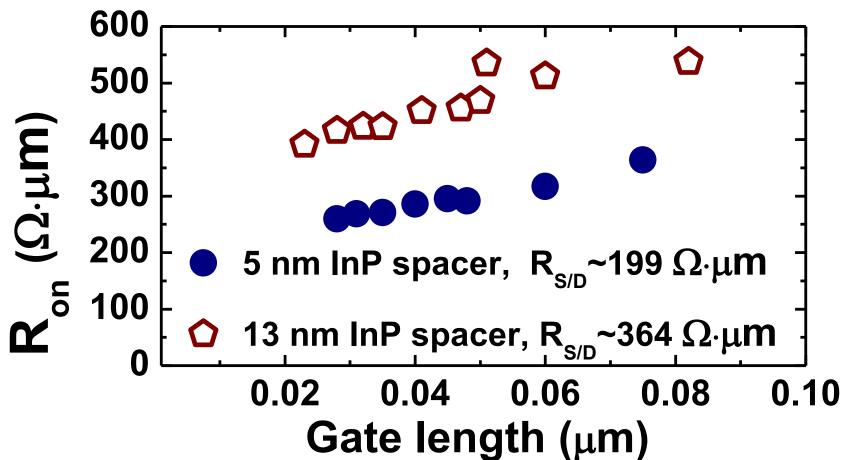
N. Taoka et al., Trans. Electron Devices. 13, 456 (2011)
N. Taoka et al., IEEE IEDM 2011, 610.

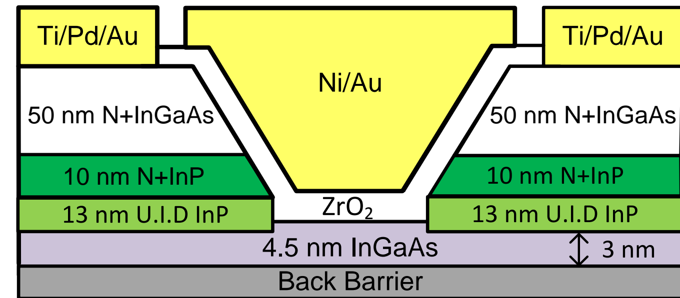


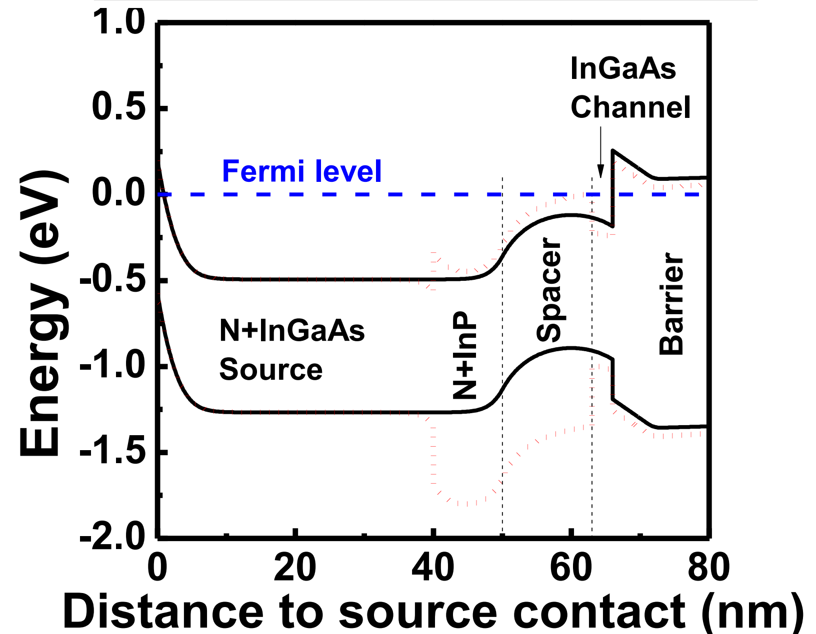
J. Robertson et al., J. Appl. Phys. 117, 112806 (2015)
J. Robertson, Appl. Phys. Lett 94, 152104 (2009)

InP spacer thickness: on-state



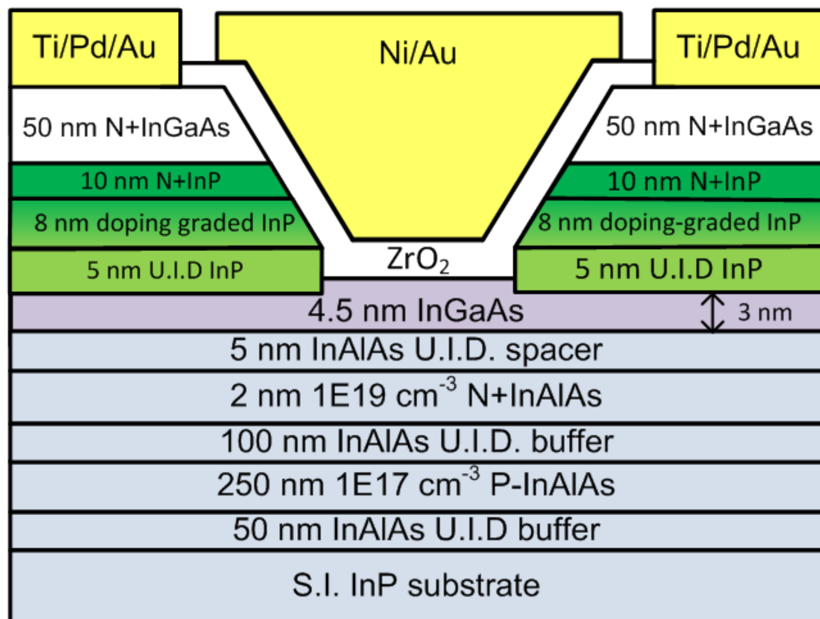




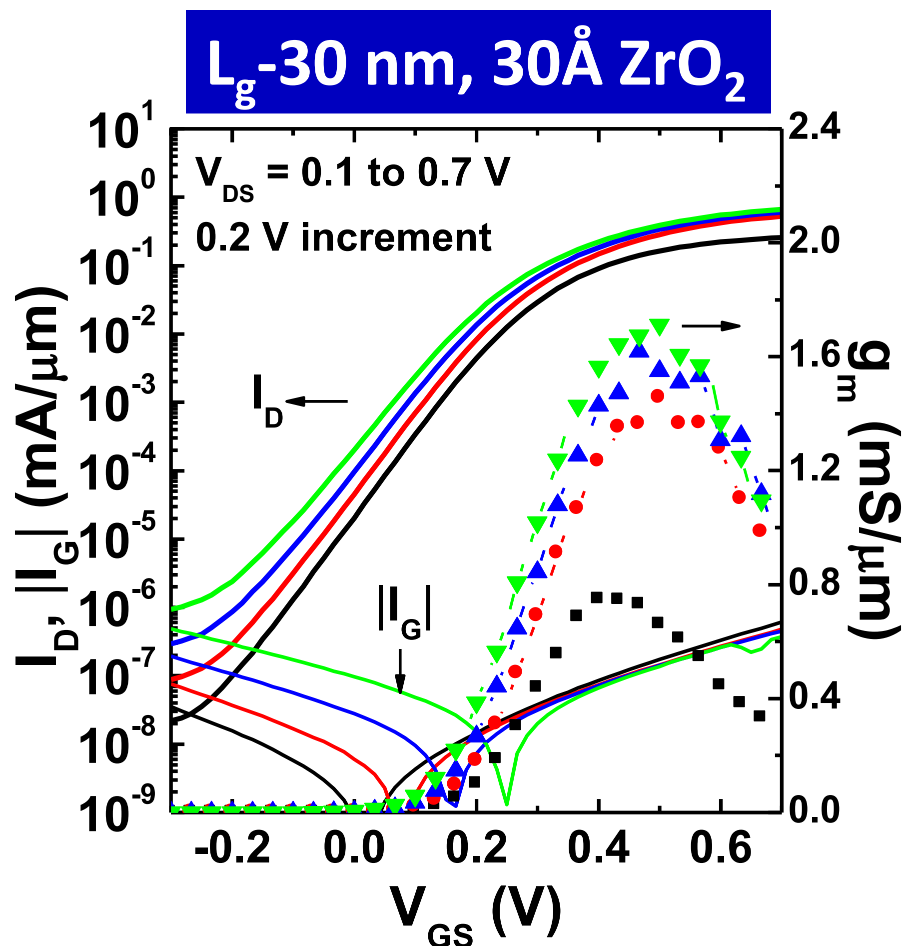


- Thicker InP spacer increases R_{on}, and degrades G_m
- Thinner spacer is desired at source to reduce $R_{S/D}$.

Doping-graded InP spacer

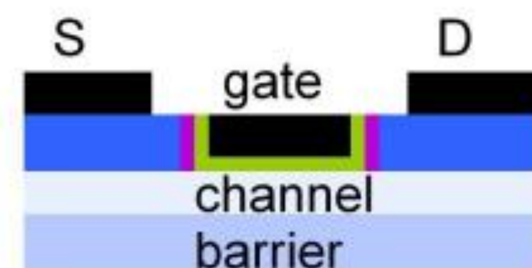


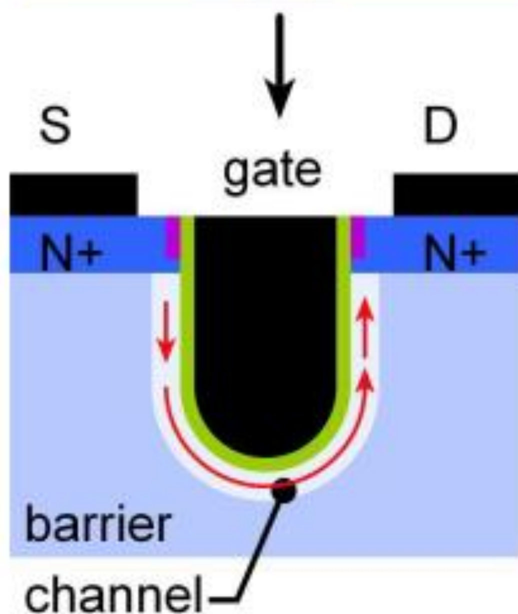
R_{on} at zero L_g ($\Omega\cdot\mu m$)	5 nm UID InP	13 nm UID InP	Doping graded InP
	~199	~364	~270

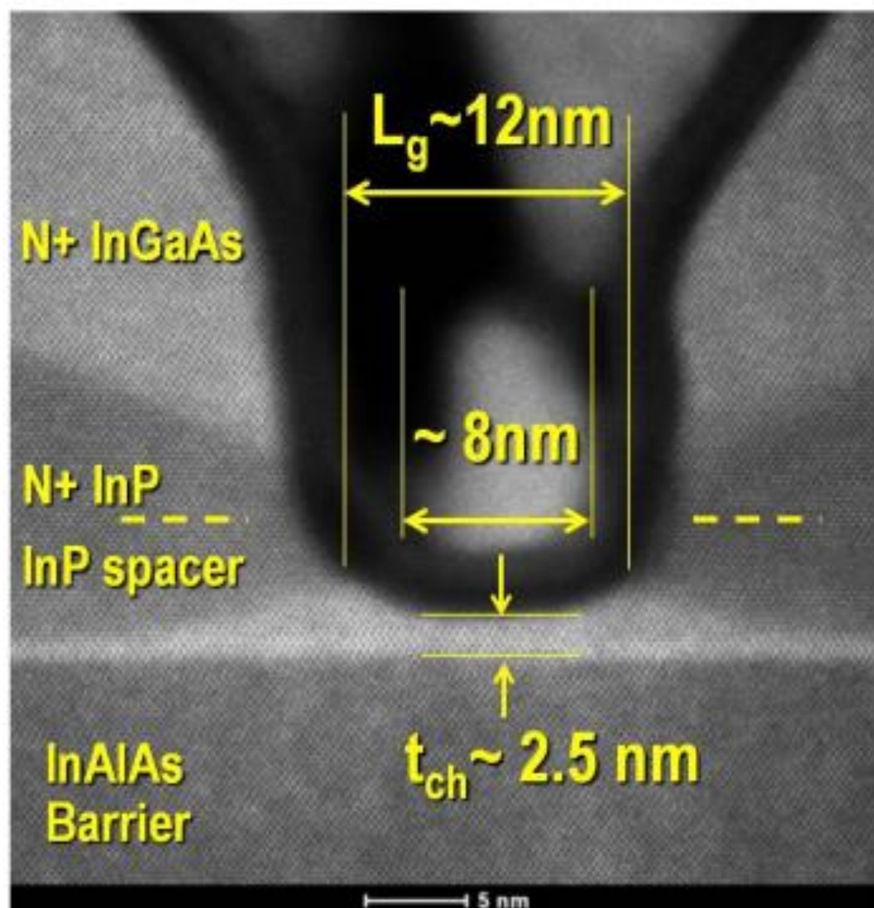


- **Doping-graded InP spacer reduces parasitic source/drain resistance and improves G_m.**
- **Gate leakage limits I_{off}~300 pA/µm.**

Fixing source-drain tunneling by corrugation







Transport distance > gate footprint length
Only small capacitance increase

In(Ga)As: low m*→ high velocity → high current (?)

Ballistic on-current:

Natori, Lundstrom, Antoniadis (Rodwell)

$$J = K_1 \cdot \left(84\frac{\text{mA}}{\mu\text{m}}\right)\cdot\left(\frac{V_{gs}-V_{th}}{1\,\text{V}}\right)^{3/2},$$

$$\frac{1}{c_{equiv}} = \frac{T_{ox}}{\varepsilon_{ox}} + \frac{T_{channel}}{2\varepsilon_{semiconductor}}$$

$g = \#\,\text{valleys}$

$$K_1 = \frac{g\cdot\left(m^*/m_o\right)^{1/2}}{\left(1+(c_{dos,o}/c_{equiv})\cdot g\cdot(m^*/m_o)\right)^{3/2}}$$

More current unless dielectric, and body, are extremely thin.