III-V MOS: Record-Performance Thermally-Limited Devices, Prospects for High-On-Current Steep Subthreshold Swing Devices

Mark Rodwell, UCSB

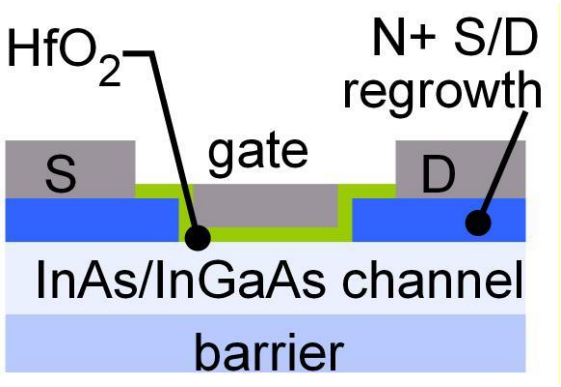
III-V MOS
C.-Y. Huang, S. Lee, A.C. Gossard,*
V. Chobpattanna, S. Stemmer, B. Thibeault, W. Mitchell : ***UCSB***

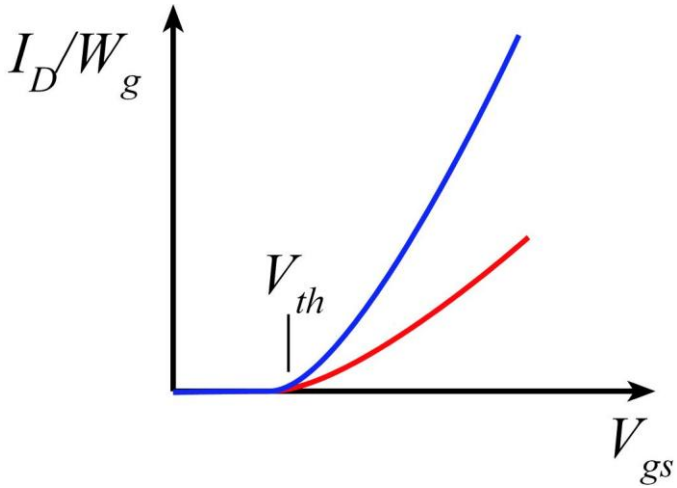
Low-voltage devices
P. Long, E. Wilson, S. Mehrotra, M. Povolotskyi, G. Klimeck: ***Purdue***

*Now with: *IBM, **Intel*

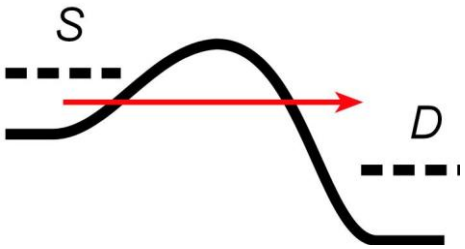
Why III-V MOS ?

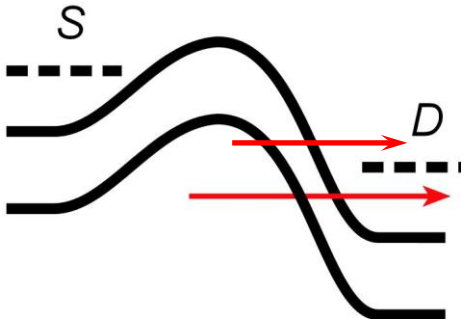
III-V vs. Si: Low m*→ higher velocity. Fewer states→ less scattering → higher current. Can then trade for lower voltage or smaller FETs.



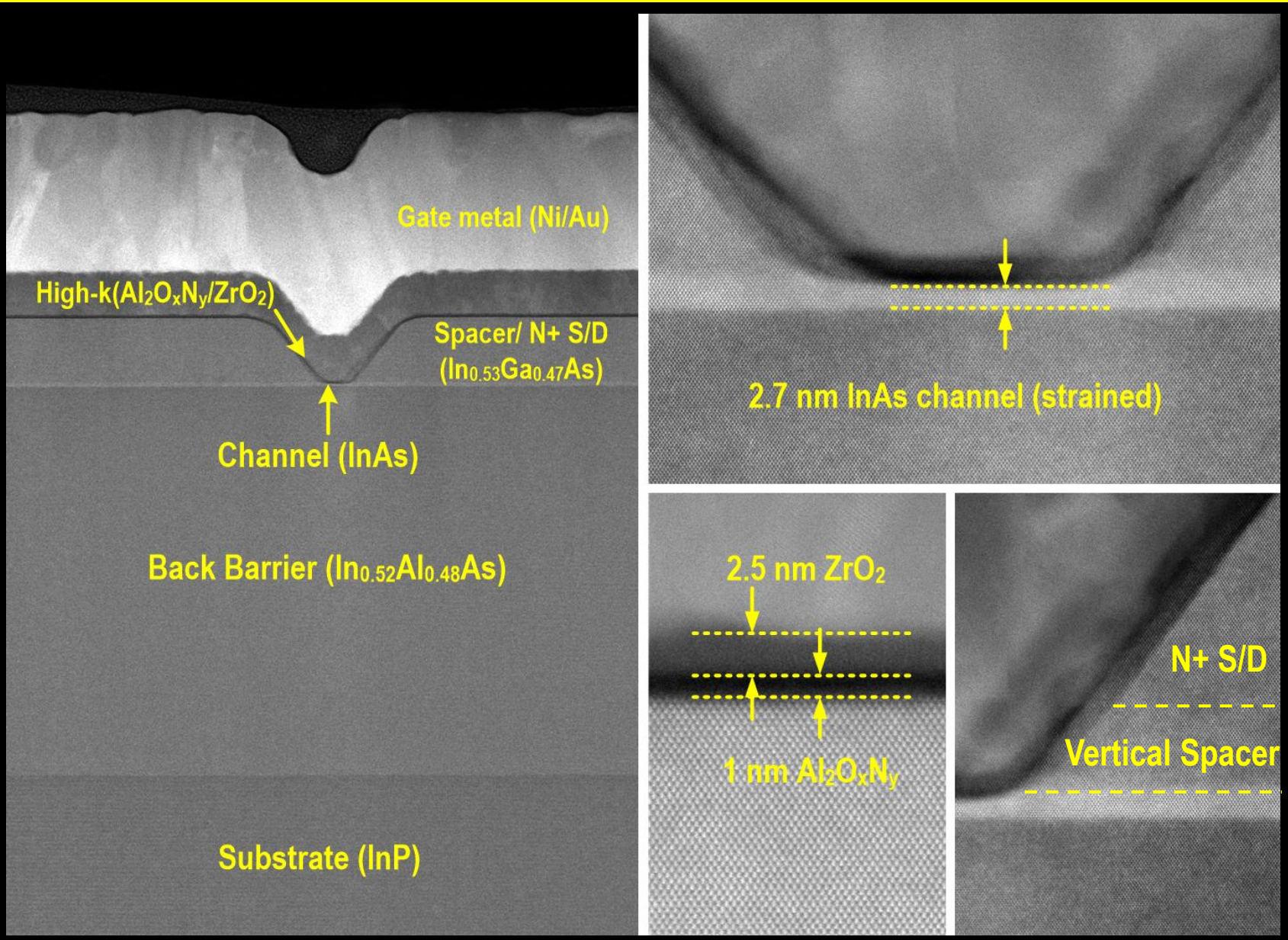


Problems: Low m*→ less charge. Low m* → more S/D tunneling. Narrow bandgap→ more band-band tunneling, impact ionization.



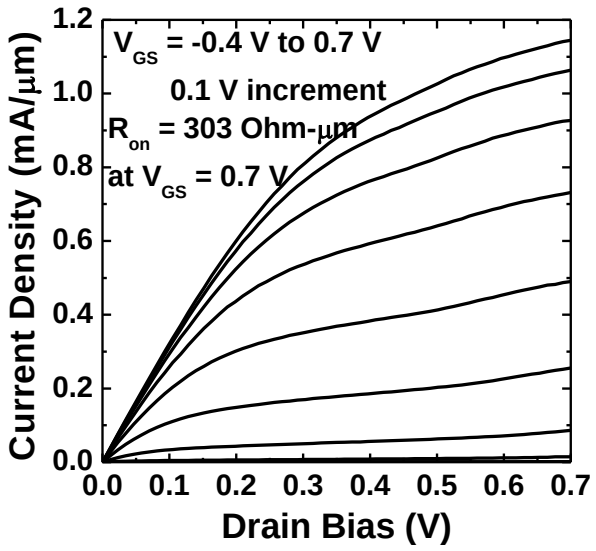


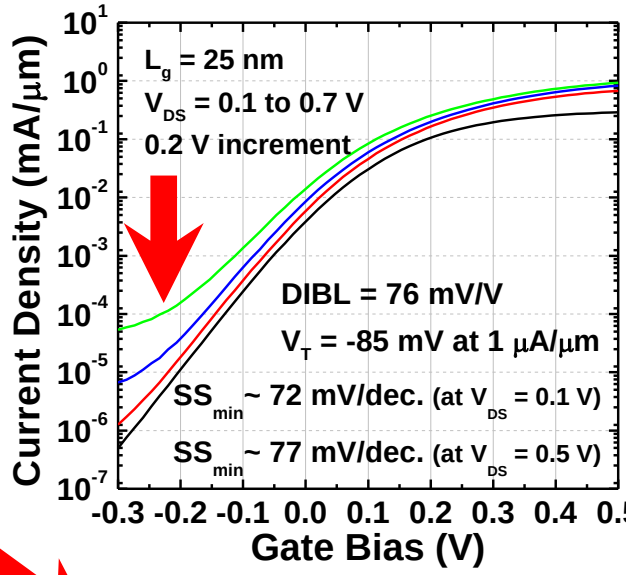
Reducing leakage: Vertical spacer, Ultra-thin channel

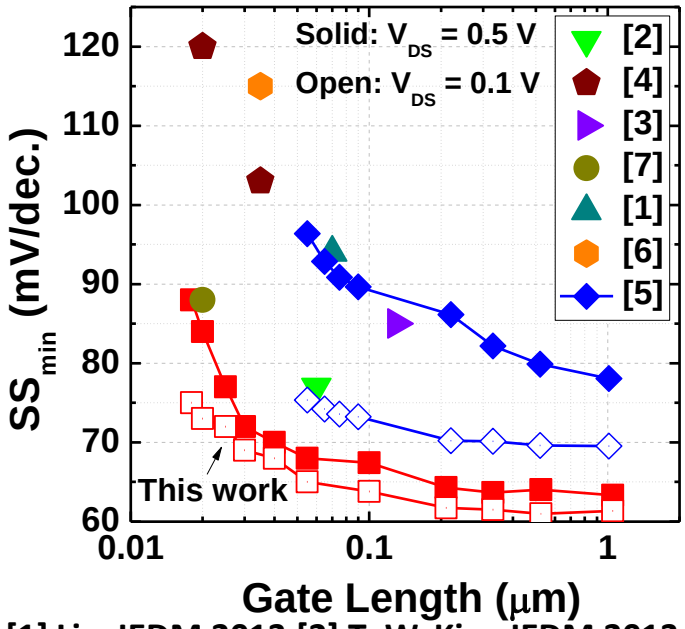


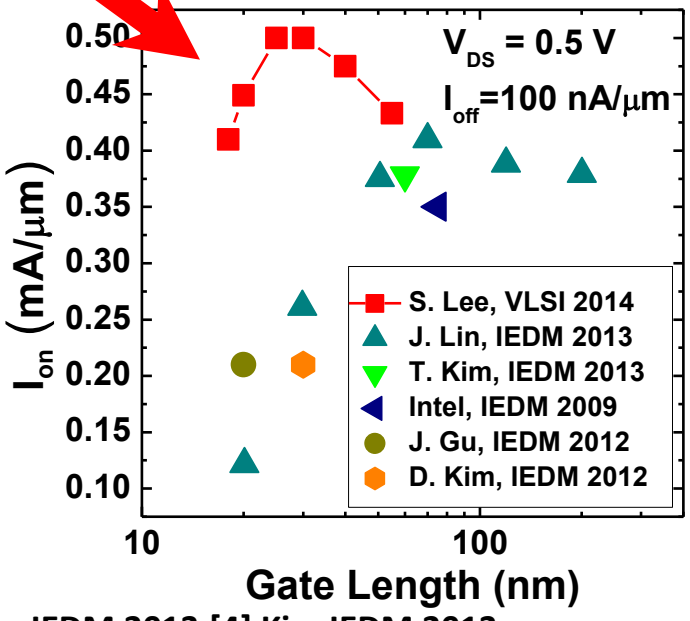
Courtesy of S. Kraemer (UCSB) *Heavy elements look brighter Lee *et al.*, 2014 VSLI Symposium

Reducing leakage: Vertical spacer, Ultra-thin channel



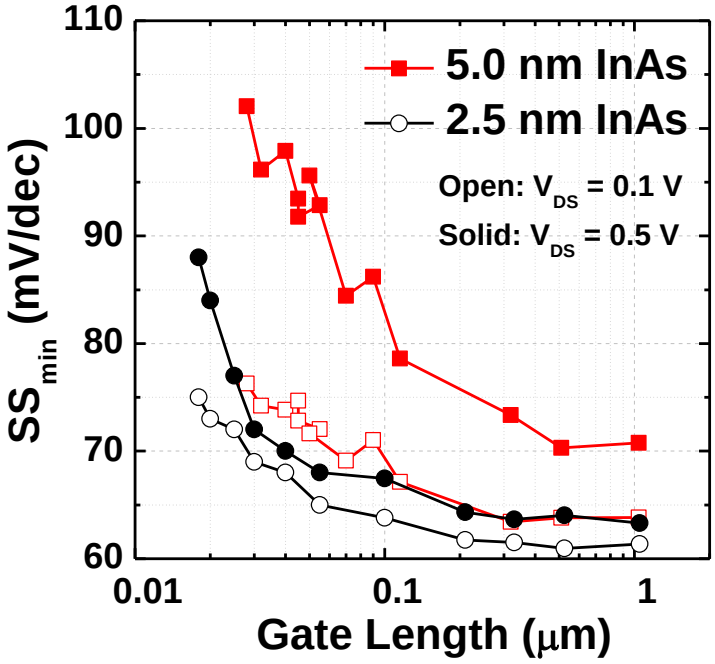


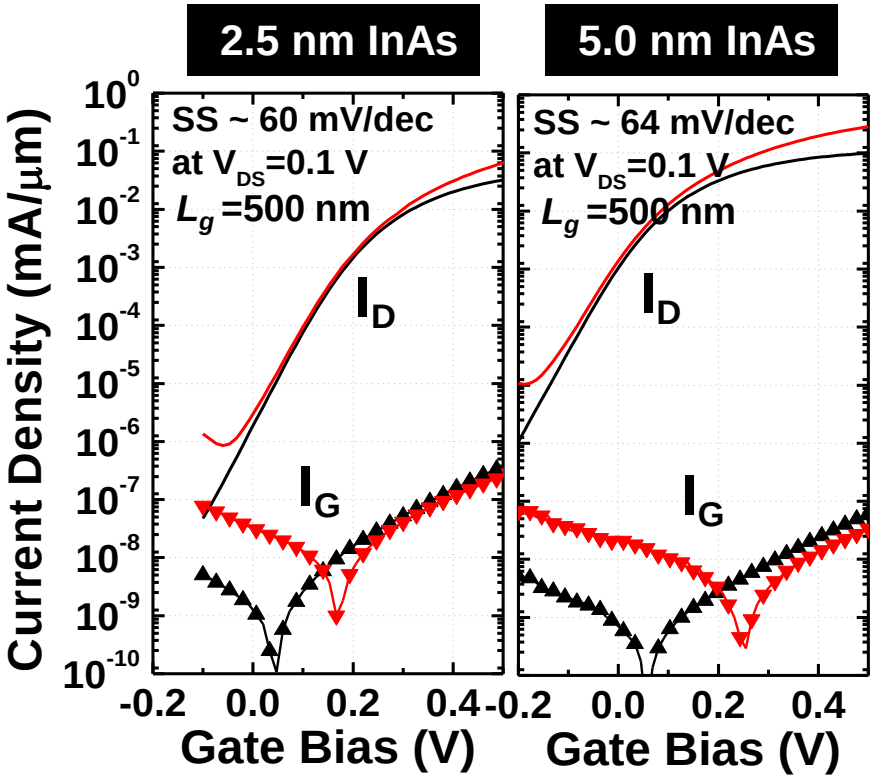




[1] Lin IEDM 2013,[2] T.-W. Kim IEDM 2013,[3] Chang IEDM 2013,[4] Kim IEDM 2013
[5] Lee APL 2013 (UCSB), [6] D. H. Kim IEDM 2012,[7] Gu IEDM 2012,[8] Radosavljevic IEDM 2009

Off-state comparison: 2.5 nm vs. 5.0 nm-thick InAs channel





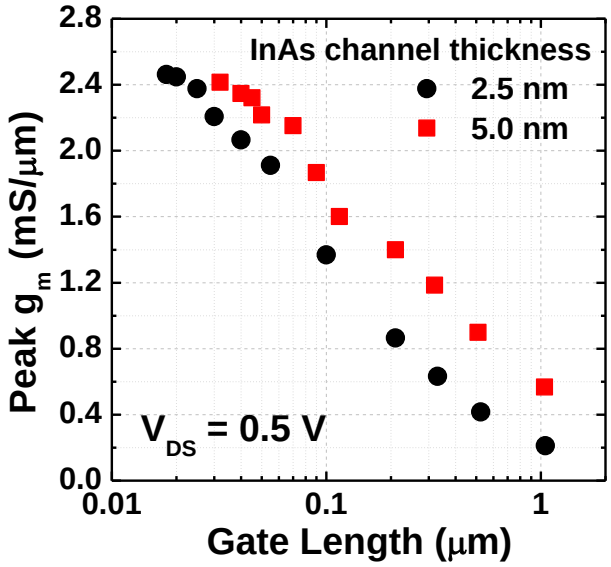
Better SS at all gate lengths

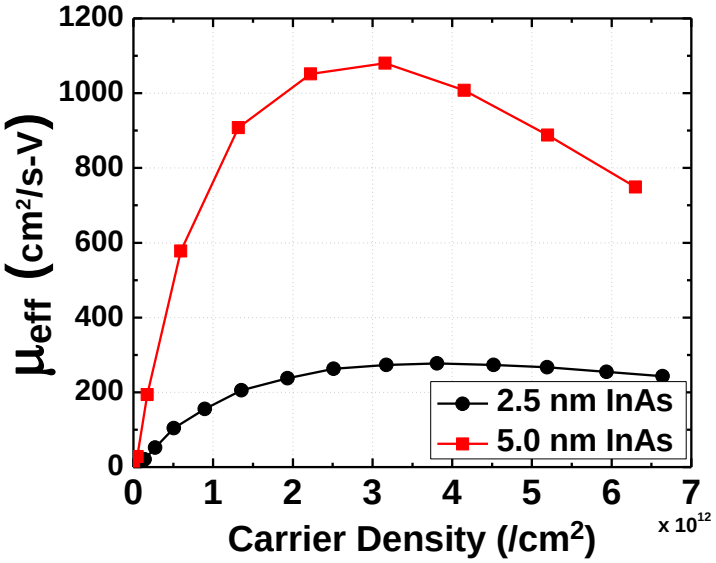
🡐 Better electrostatics (aspect ratio) and reduced BTBT (quantized E_g)

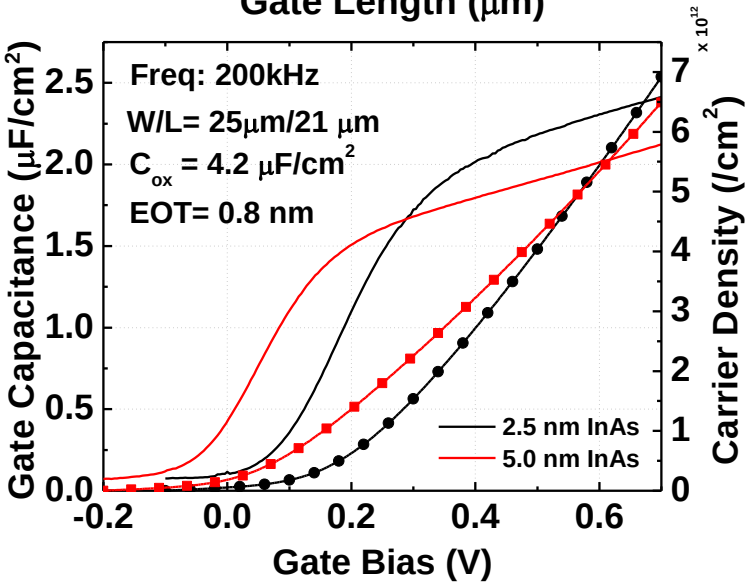
~10:1 reduction in minimum off-state leakage

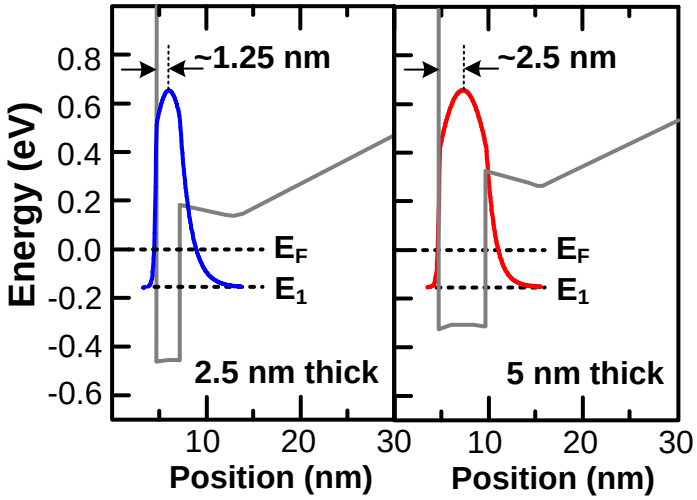
~5:1 increase in gate leakage 🡐 increased eigenstate

On-state comparison: 2.5 nm vs. 5.0 nm-thick InAs channel





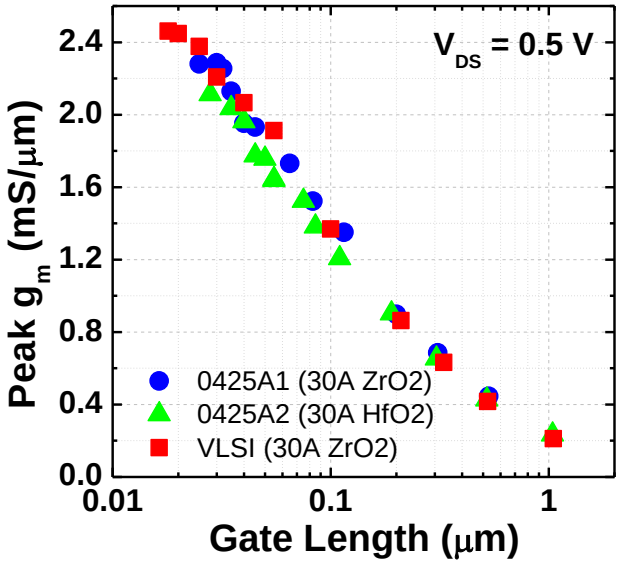


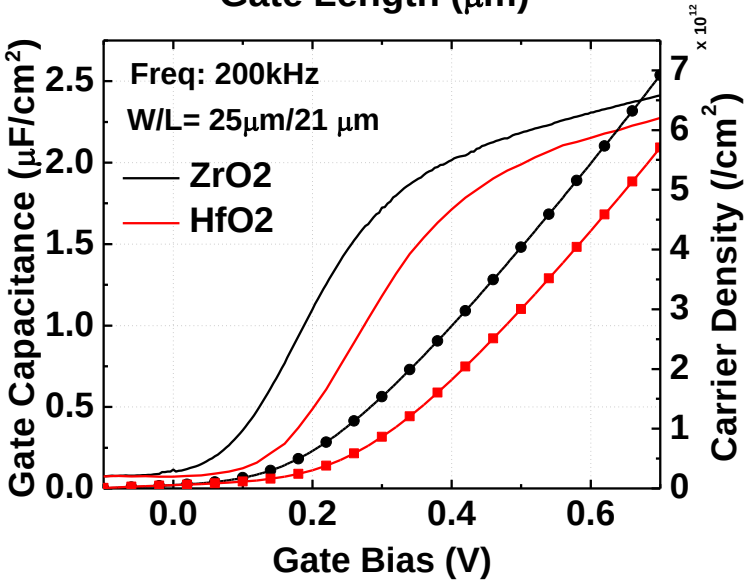


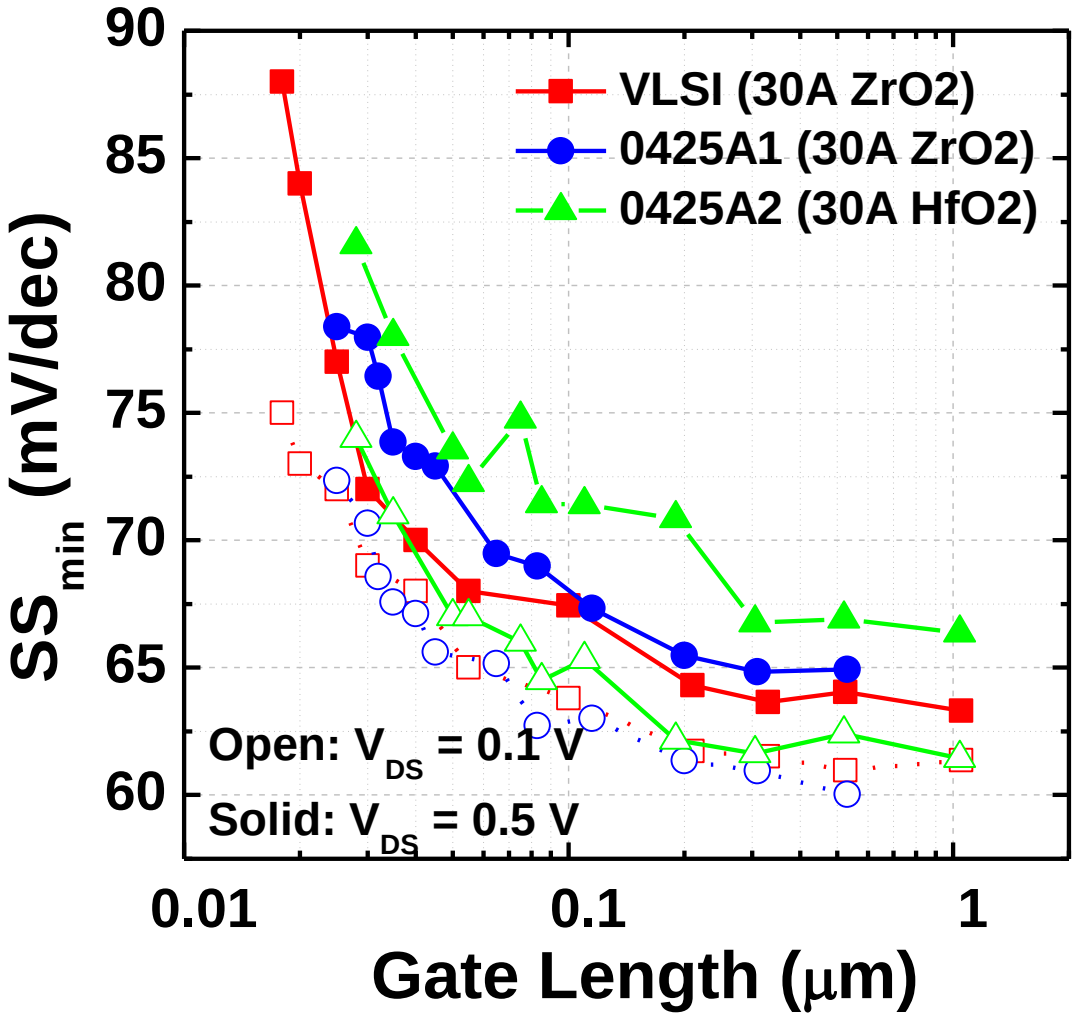
1D-Possion Schrodinger solver
(coded by W. Frensley, UT Dallas)

ZrO_2 vs. HfO_2: Peak g_m, SS, split-CV, and mobility

Comparison: two process runs ZrO_2, one run HfO_2, both 2nm (on 1nm Al_2O_3)

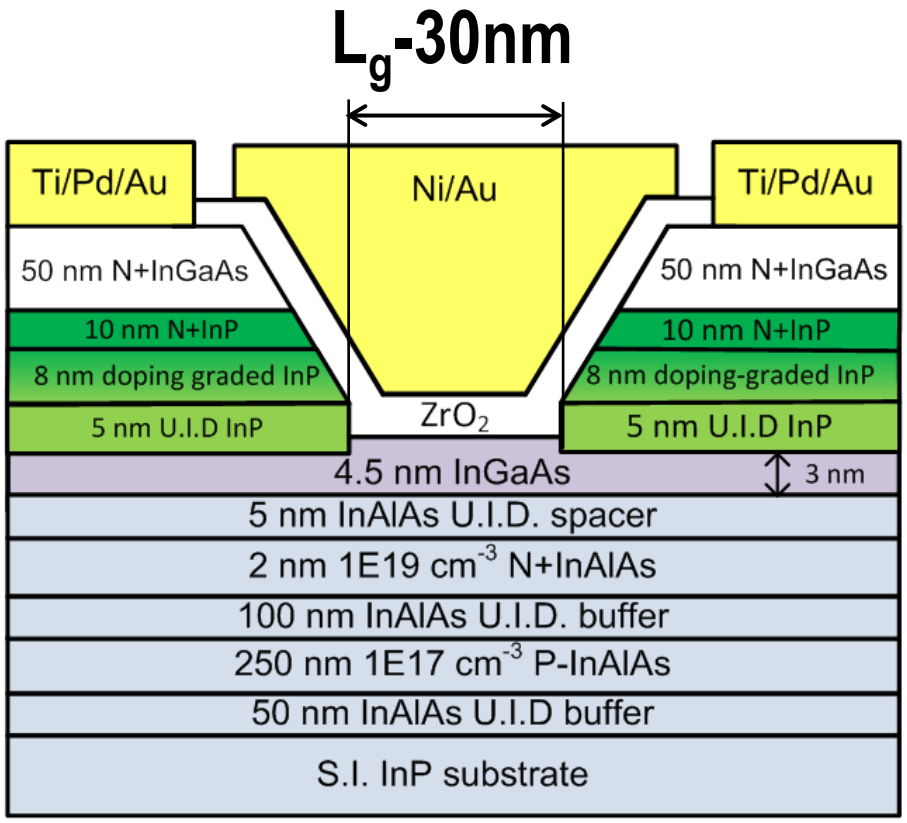




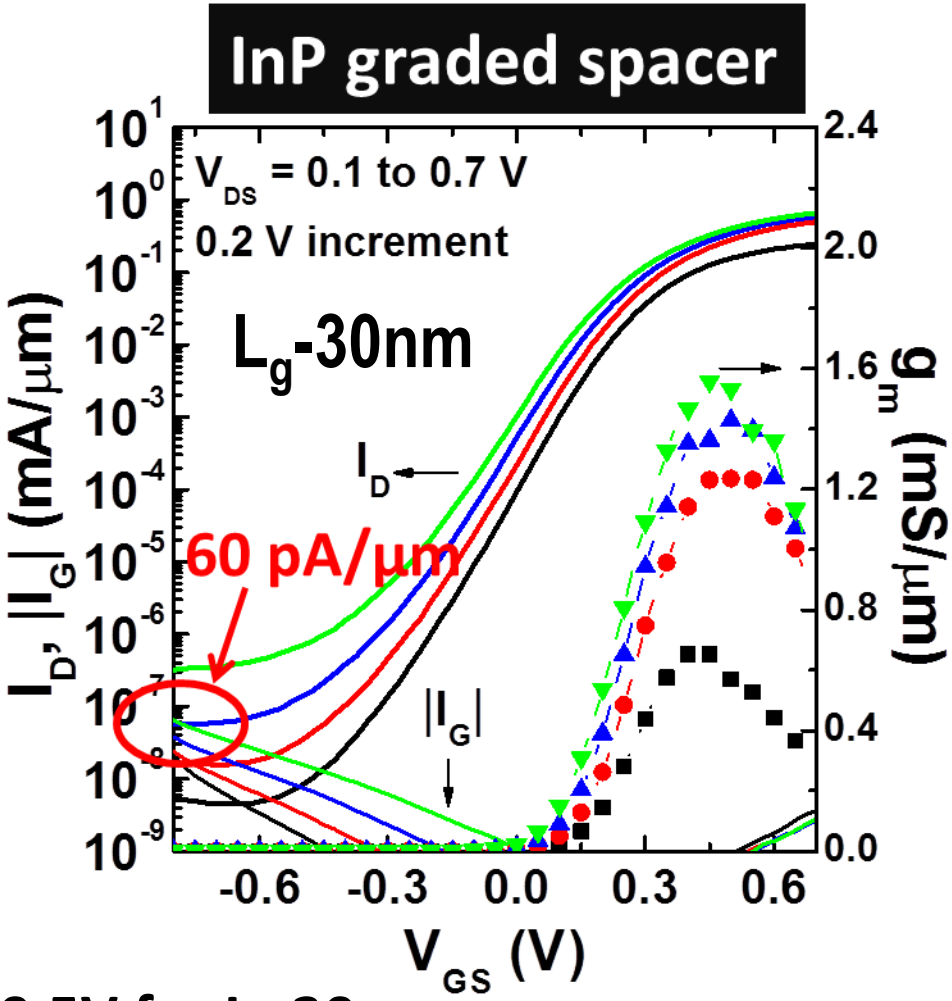


(1) ZrO_2 higher capacitance than HfO_2, (2) ZrO_2 results, low SS, are reproducible

Double-heterojunction MOS: 60 pA/μm leakage

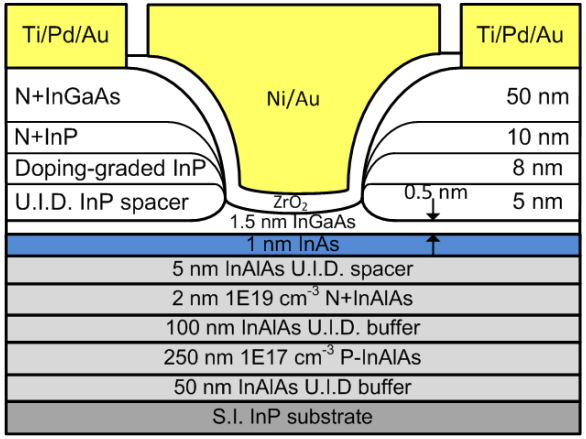


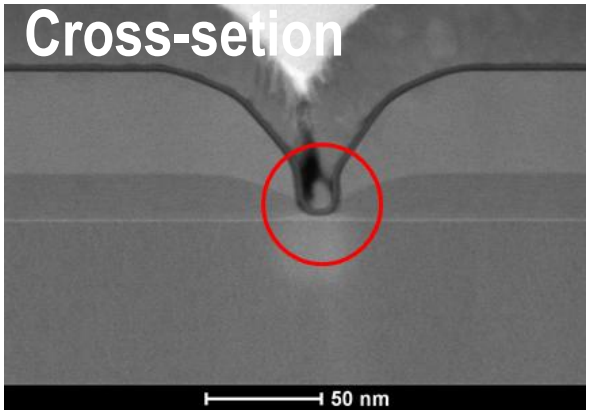
C. Y. Huang et al., IEDM 2014

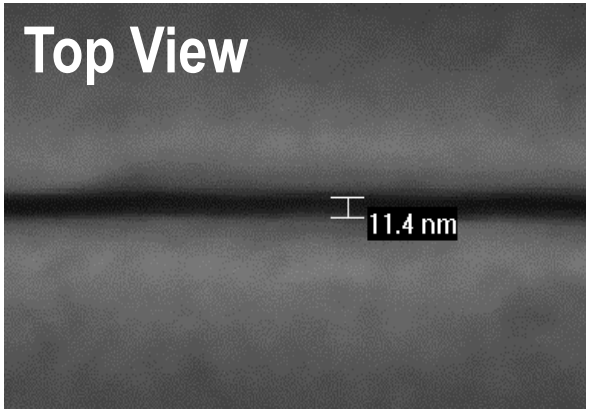


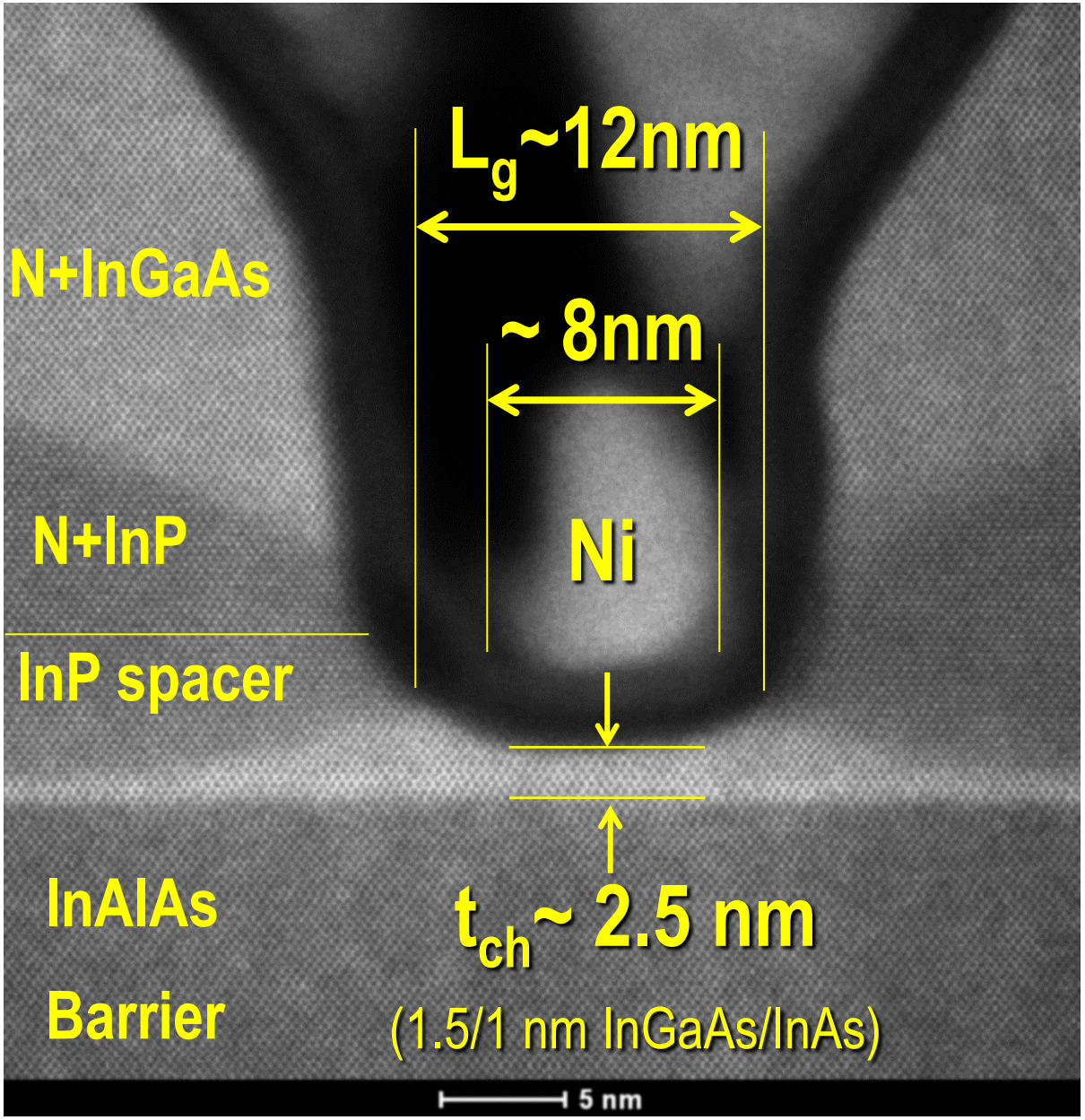
- **Minimum I_{off}~ 60 pA/μm at V_D=0.5V for L_g-30 nm**
- **100:1 smaller I_{off} compared to InGaAs spacer**
- **BTBT leakage suppressed→isolation leakage dominates**

12 nm L_g III-V MOS

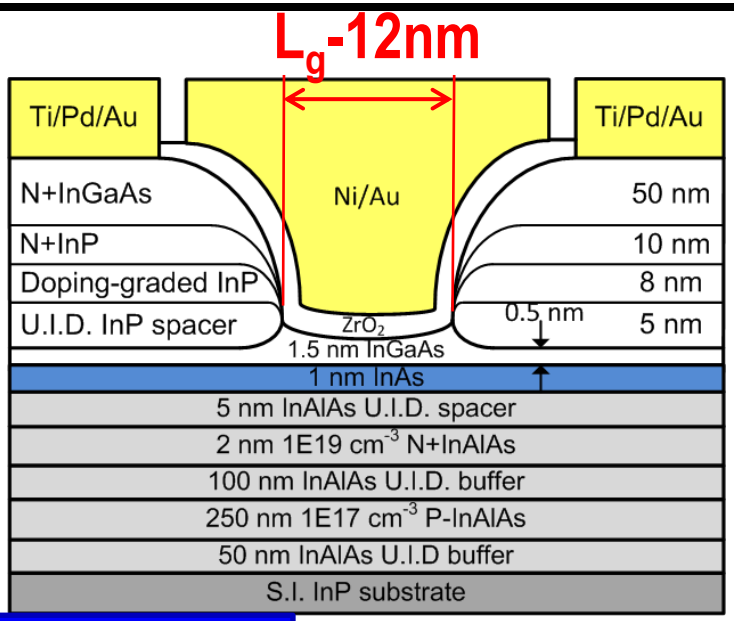


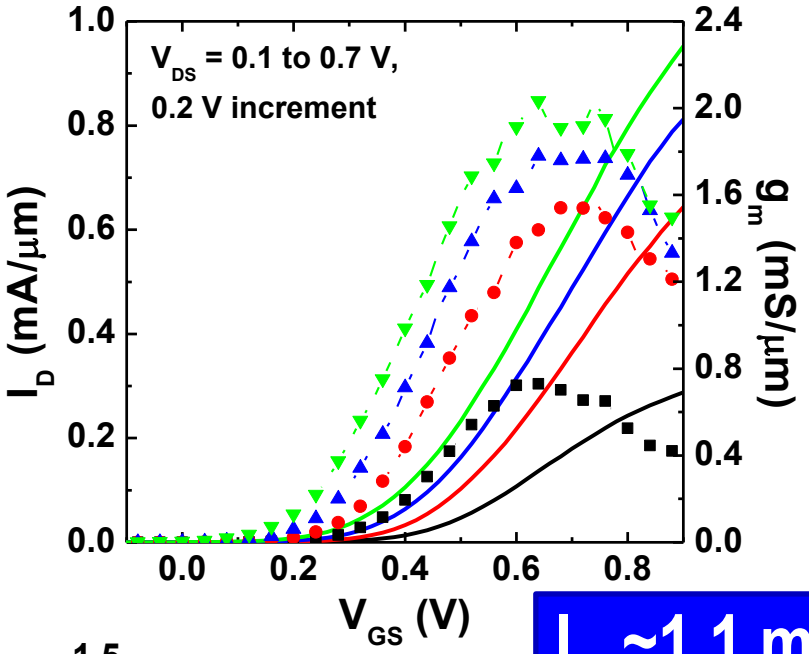




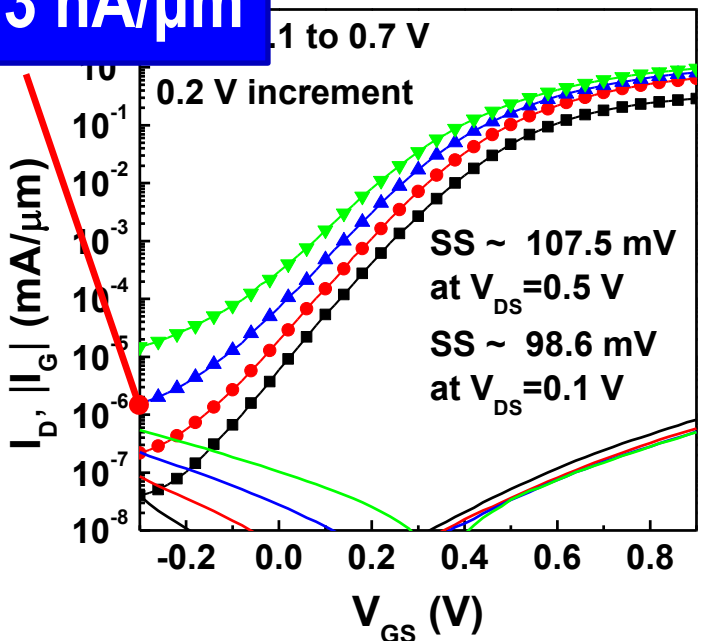


I_D-V_G and I_D-V_D curves of 12nm L_g FETs

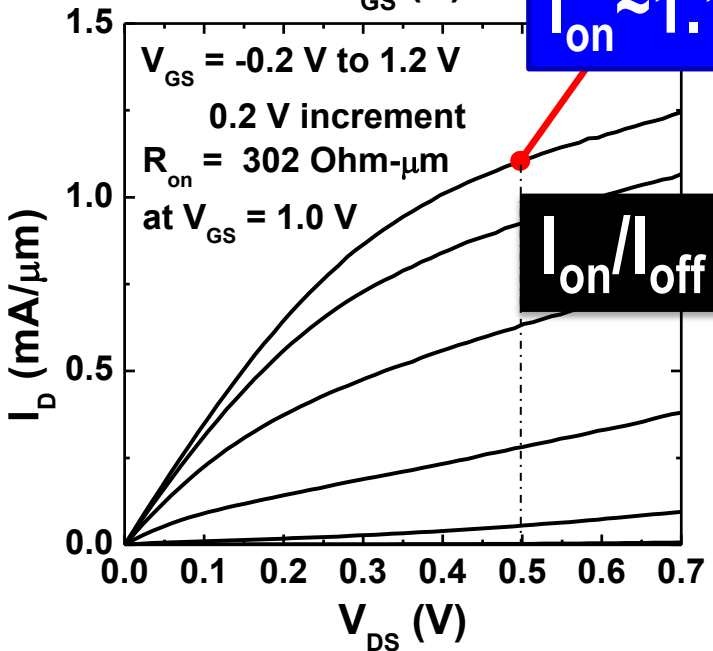




I_{off}~1.3 nA/μm

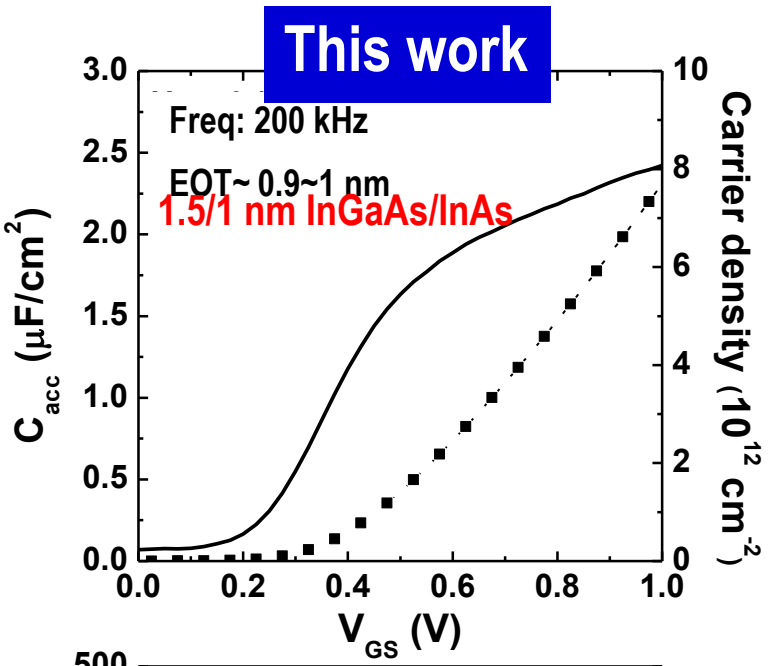


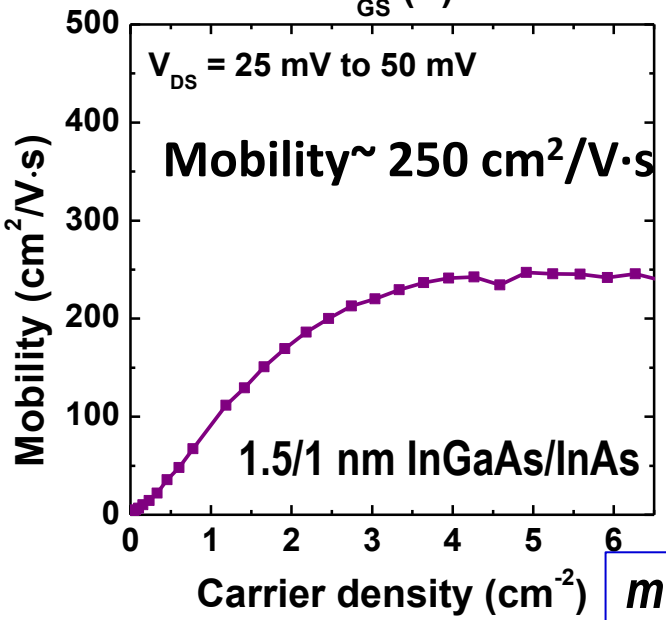
I_{on}~1.1 mA/μm

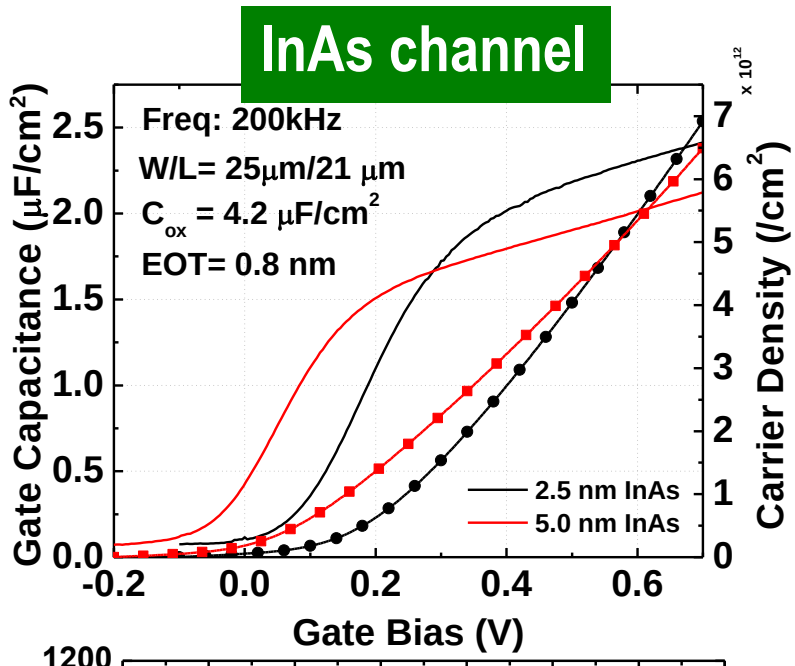


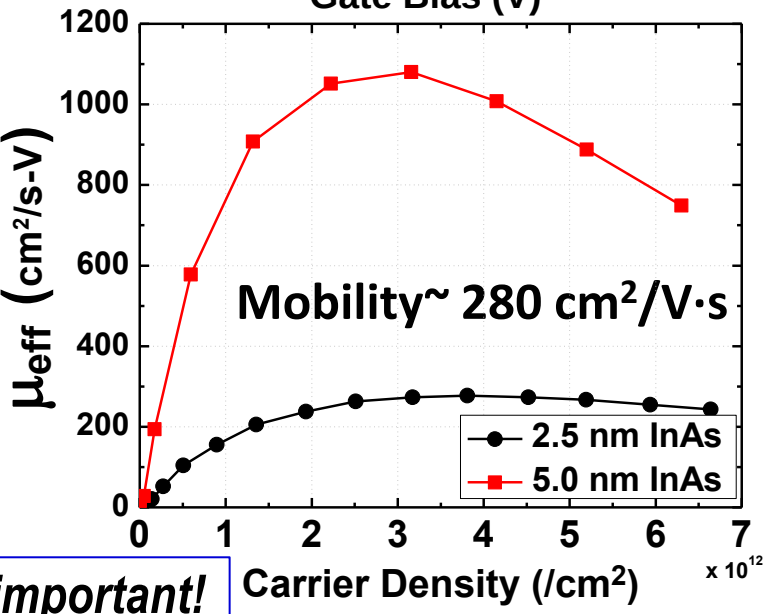
I_{on}/I_{off} > $8.3 \cdot 10^5$

Mobility extraction at L_g-25 µm long channel FETs







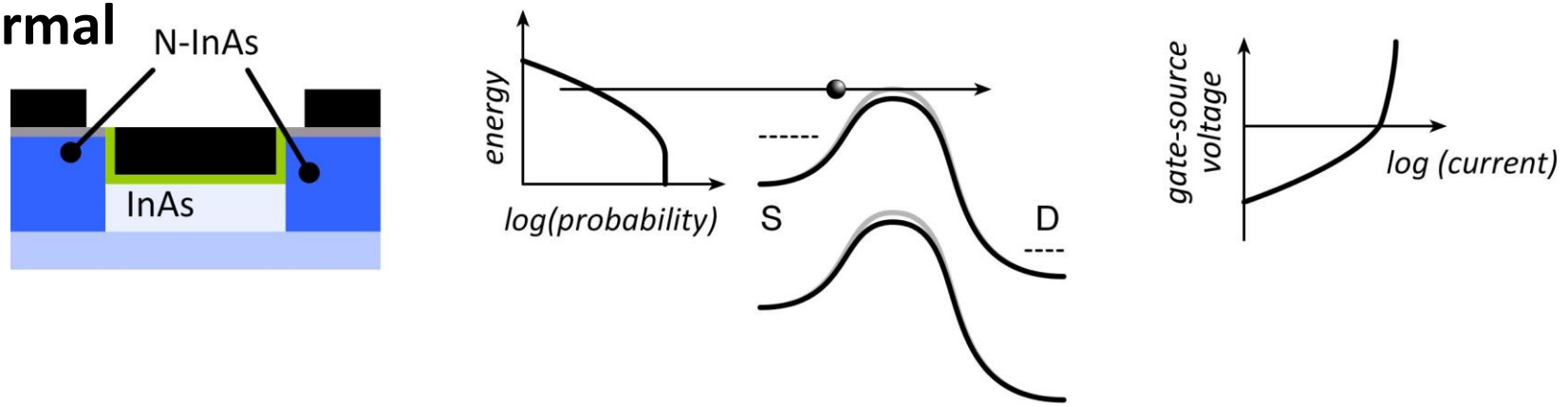


m, $R_{S/D}$ more important!*

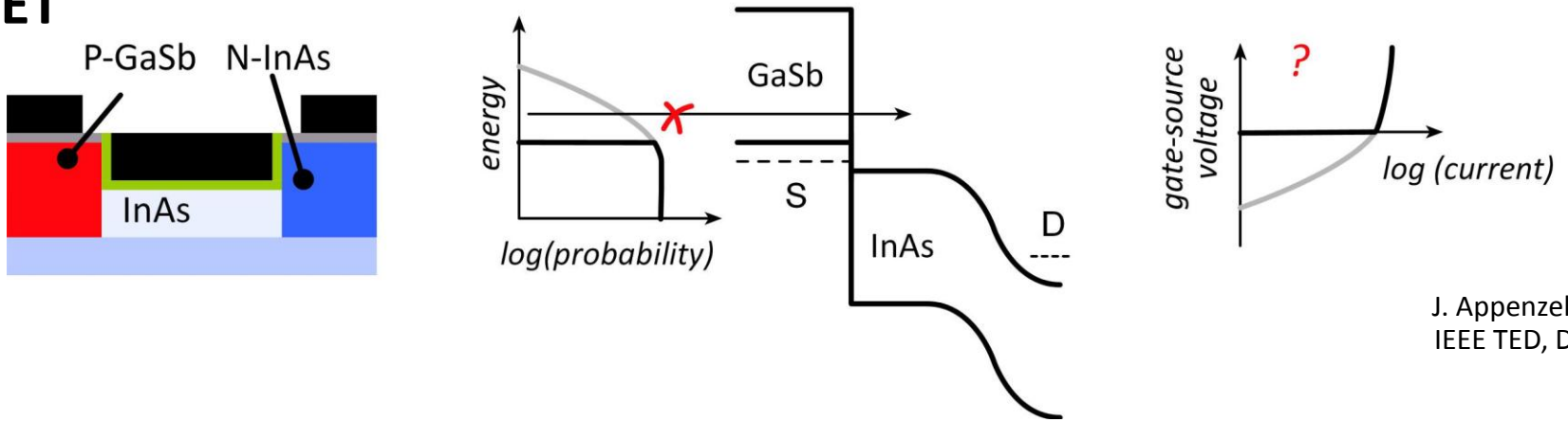
Steep FETs

Tunnel FETs: truncating the thermal distribution

Normal



T-FET



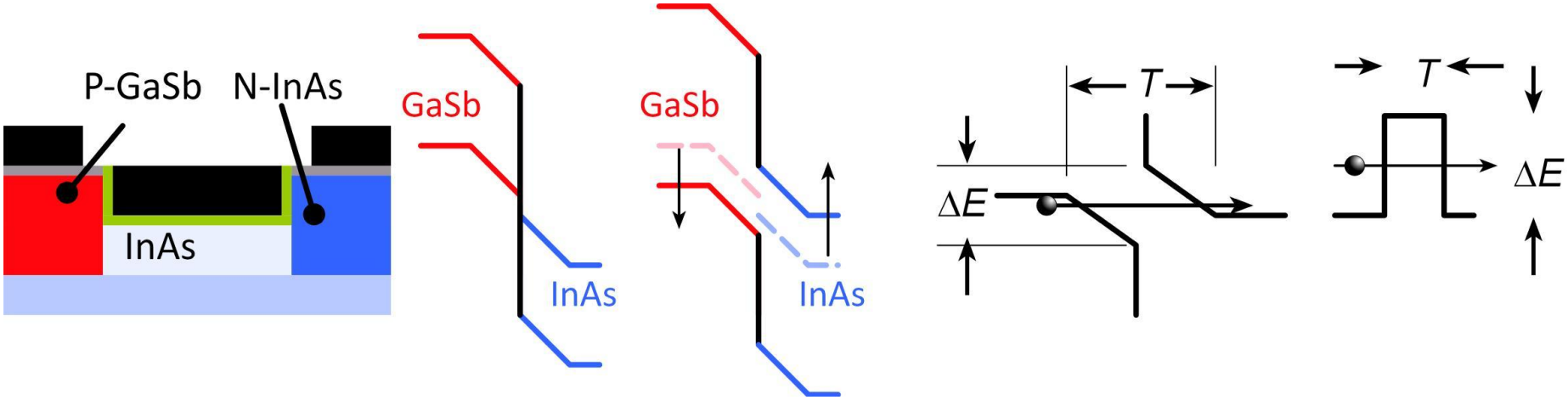
J. Appenzeller *et al.*, IEEE TED, Dec. 2005

Source bandgap truncates thermal distribution

Must cross bandgap: tunneling

Fix (?): broken-gap heterojunction

Tunnel FETs: are prospects good ?



Useful devices must be small

Quantization shifts band edges→ tunnel barrier

Band nonparabolicity increases carrier masses

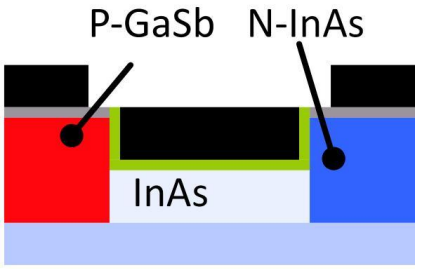
Electrostatics: bands bend in source & channel

What actual on-current might we expect ?

Tunneling Probability

Transmission Probability (WKB, square barrier)

$$P \cong \exp(-2\alpha T_{\text{barrier}}), \text{ where } \alpha \cong \frac{\sqrt{2m^* E_{\text{barrier}}}}{\hbar}$$



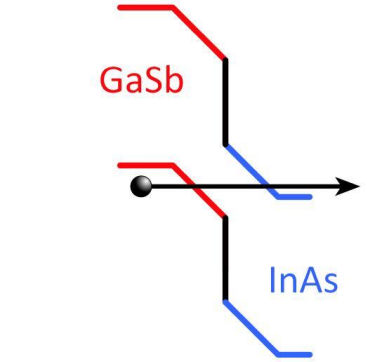
Assume: $m^* = 0.06 \cdot m_0$, $E_b = 0.2$ eV

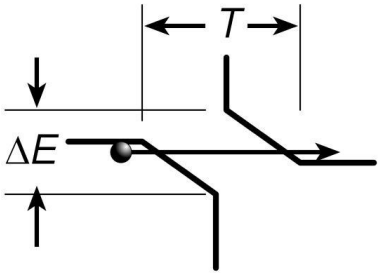
Then:

$P \cong 33\%$ for a 1nm thick barrier

$\cong 10\%$ for a 2nm thick barrier

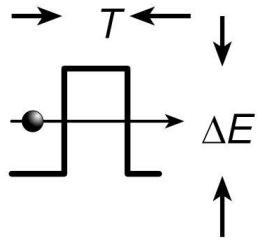
$\cong 1\%$ for a 4nm thick barrier





For high I_{on}, tunnel barrier must be *very* thin.

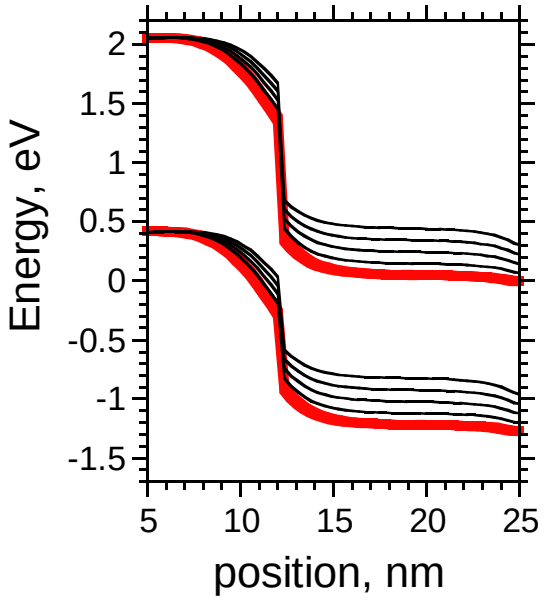
~3-4nm minimum barrier thickness:
P+ doping, body & dielectric thicknesses

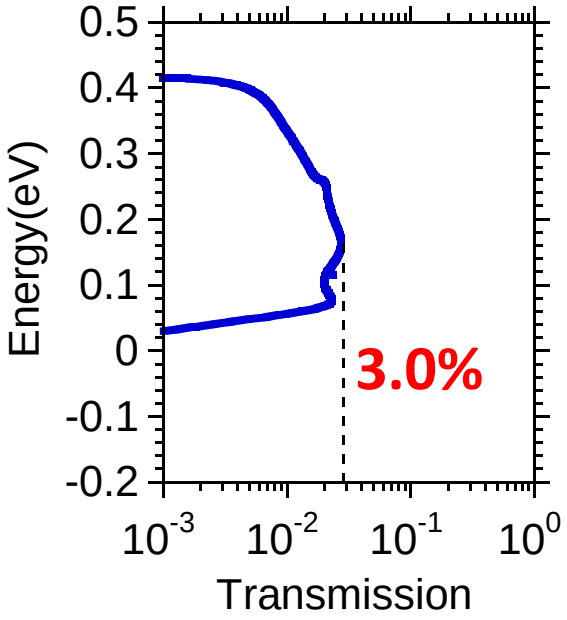


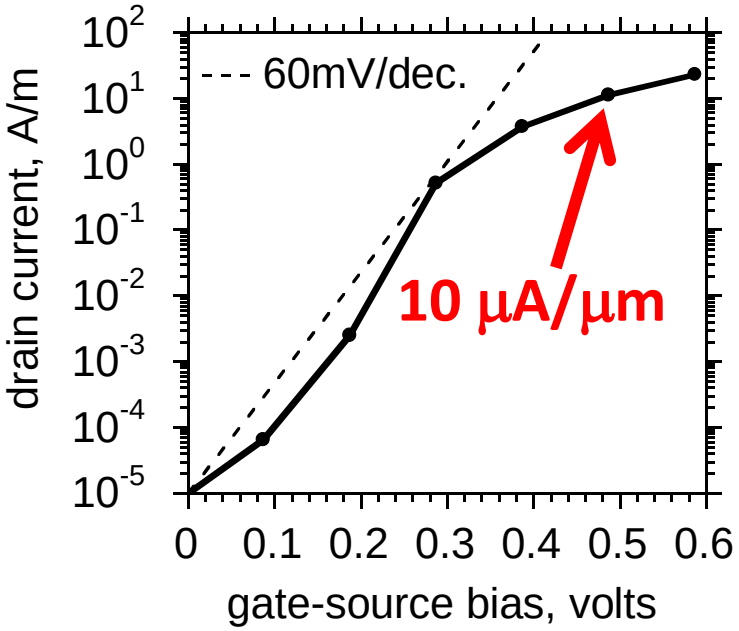
T-FET on-currents are low, T-FET logic is slow

NEMO simulation:

GaSb/InAs tunnel finFET: 2nm thick body, 1nm thick dielectric @ ε_r=12, 12nm L_g

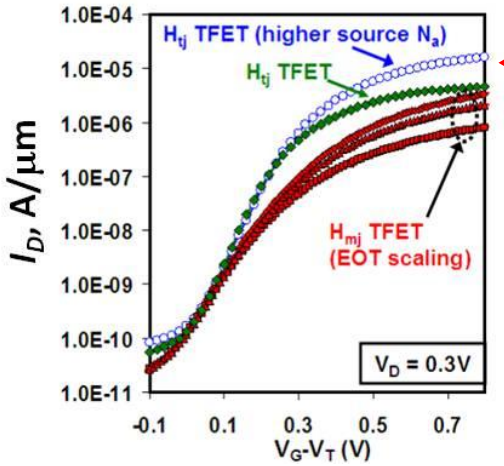






Experimental:

InGaAs heterojunction HFET,
Dewey et al,
2011 IEDM,
2012 VLSI Symp.



~15 μA/μm @0.7V

Low current → slow logic

Resonant-enhanced tunnel FET Avci & Young, (Intel) 2013 IEDM

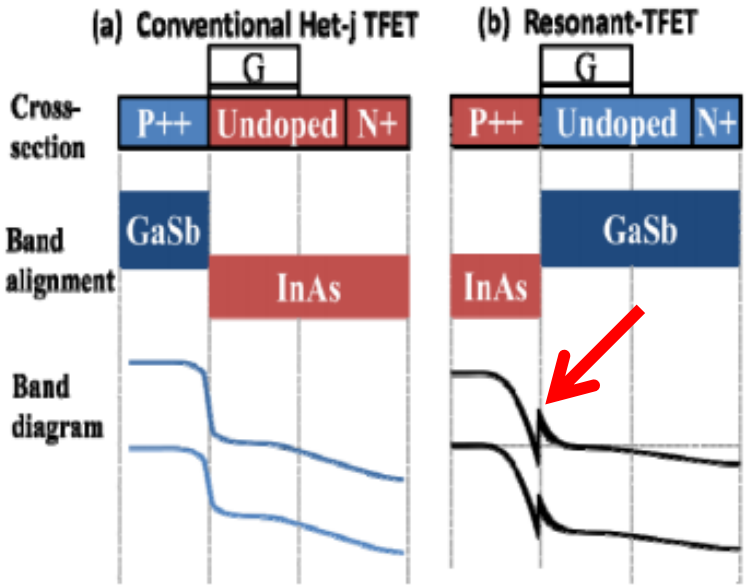


Figure 11 Device cross-section, band-alignments and band diagrams for (a) conventional Het-j TFET and (b) R-TFET. R-TFET uses the same materials but with reverse order.

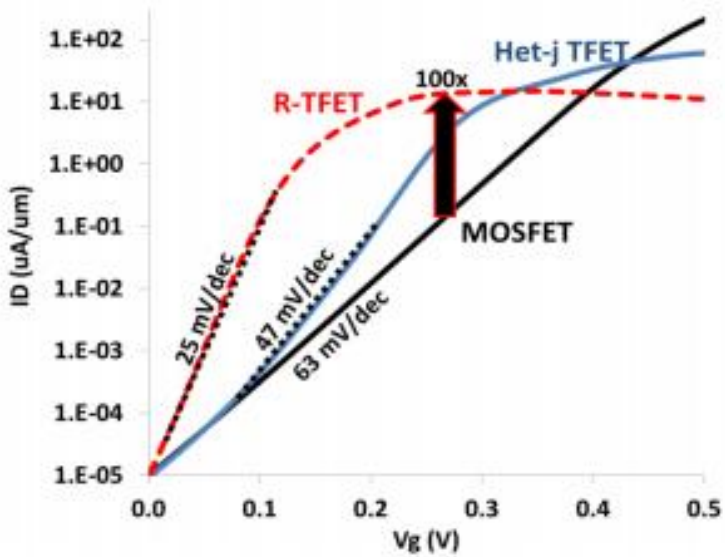


Figure 16 I-V curves for Lg=9nm NW R-TFET, Het-j TFET and MOSFET. R-TFET has 100x higher I_{on} than MOSFET at V_{DD}=0.27V. (I_{off}=10pA/um, V_{ds}=0.3V)

2nd barrier: bound state

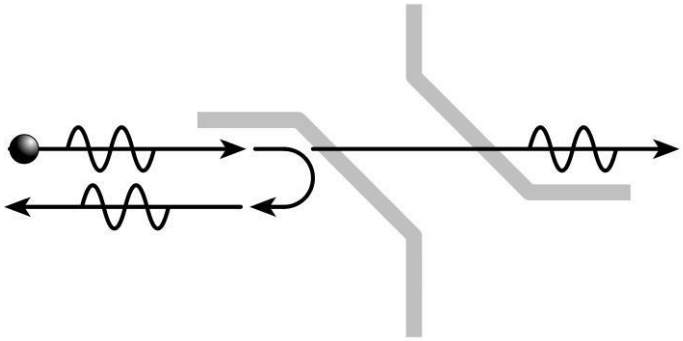
***dI/dV* peaks as state aligns with source**

improved subthreshold swing.

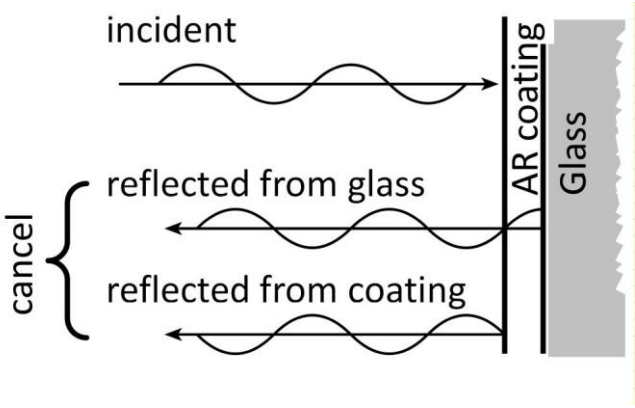
Can we also increase the on-current ?

Electron anti-reflection coatings

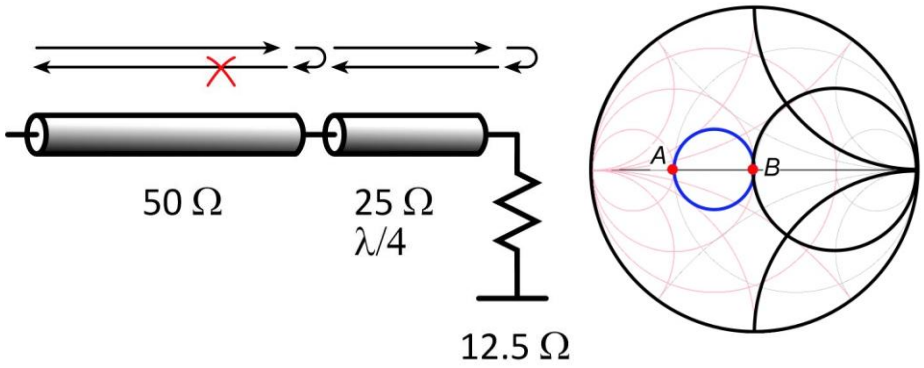
Tunnel barrier:
transmission coefficient < 100%
reflection coefficient > 0%
want: 100% transmission, zero reflection
familiar problem



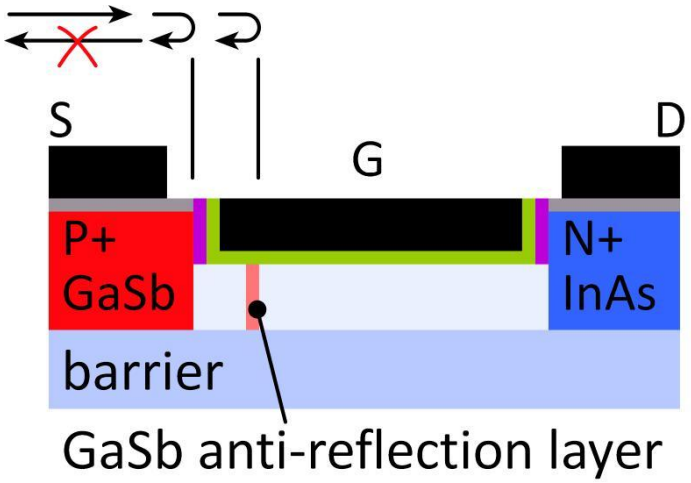
Optical coatings
reflection from lens surface
quarter-wave coating, appropriate *n*
reflections cancel

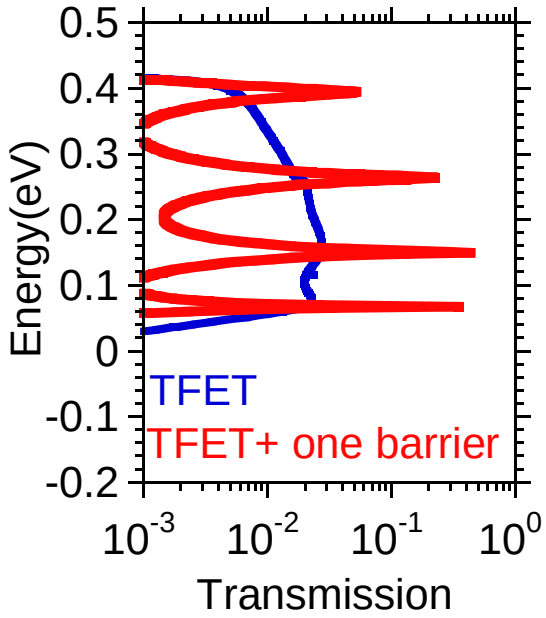


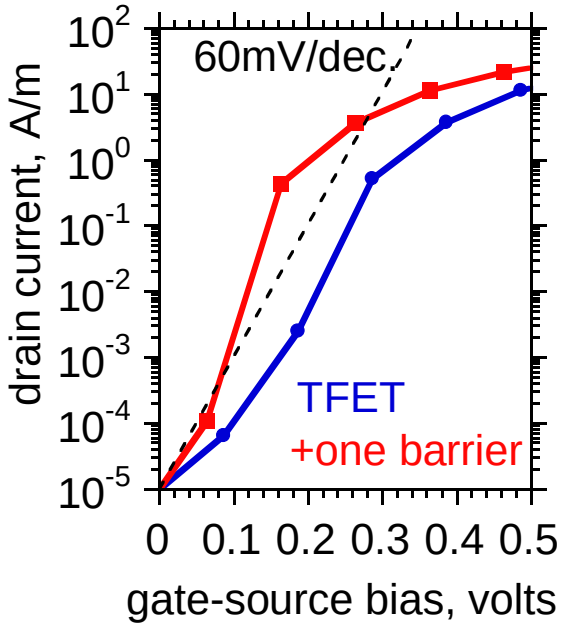
Microwave impedance-matching
reflection from load
quarter-wave impedance-match
no reflection
Smith chart.



T-FET: single-reflector AR coating







Peak transmission approaches 100%

Narrow transmission peak; limits on-current

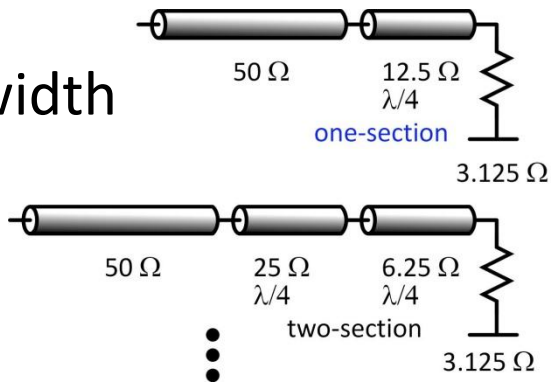
Can we do better ?

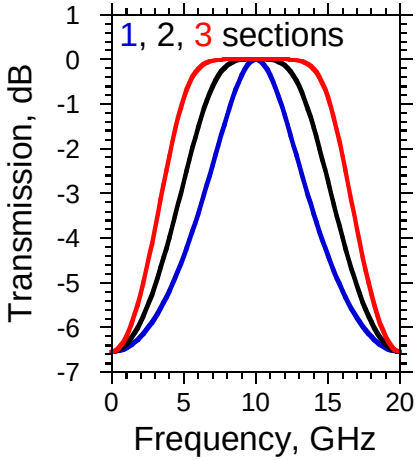
Limits to impedance-matching bandwidth

Microwave matching:

More sections→ more bandwidth

Is there a limit ?





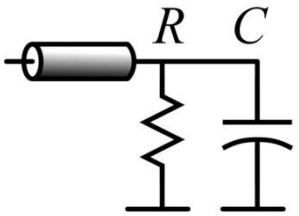
Bode-Fano limits

R. M. Fano, J. Franklin Inst., Jan. 1960

Bound bandwidth for high transmission

example: bound for RC parallel load→

$$\int_0^\infty \ln\left(\frac{1}{\|\Gamma\|^2}\right) d\omega \le \frac{\pi}{RC}$$



Do electron waves have similar limits ?

Yes ! Schrödinger's equation is isomorphic to E&M plane wave.

Khondker, Khan, Anwar, JAP, May 1988

T-FET design→ microwave impedance-matching problem

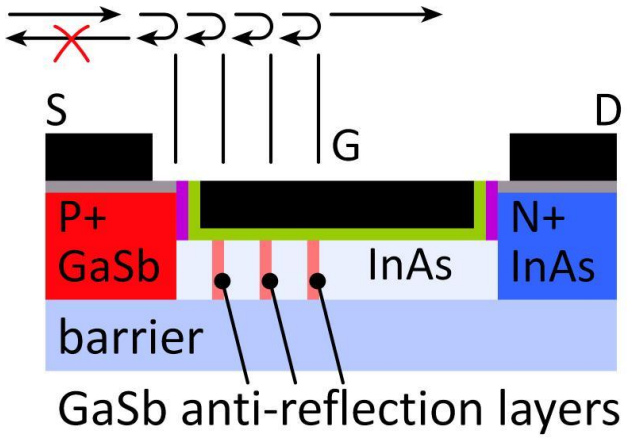
Fano: limits energy range of high transmission

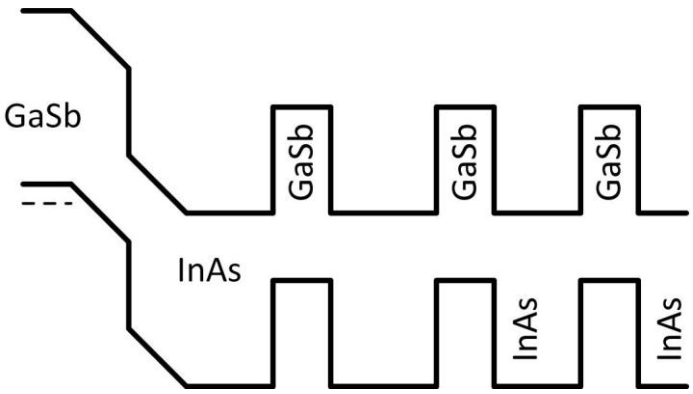
Design T-FETs using Smith chart, optimize using filter theory

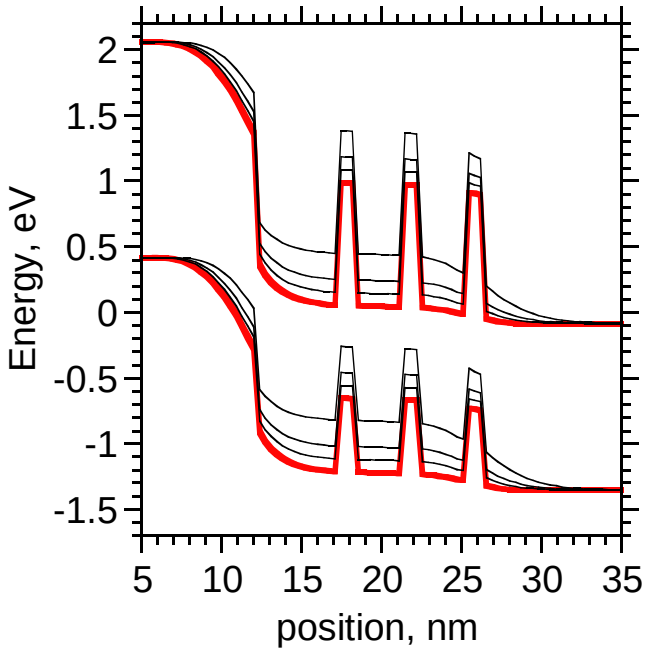
Working on this: for now design by random search

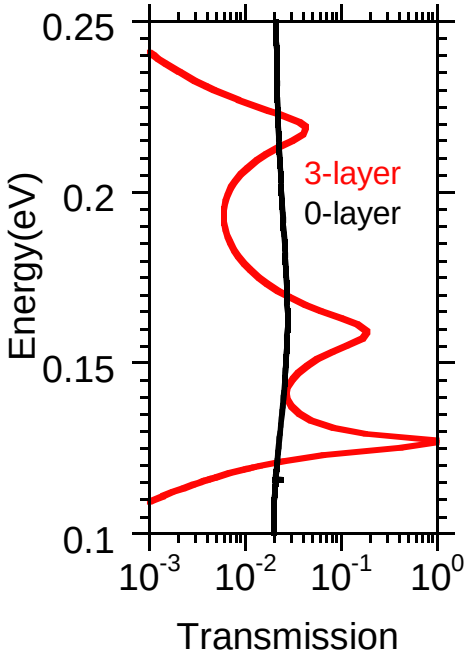
*$E/h \leftrightarrow f$, $\phi \leftrightarrow V$, $\psi \leftrightarrow I$, probability current $\leftrightarrow$ power, where $\phi(x) = (\hbar / jm^*)(\partial\psi / \partial x)$

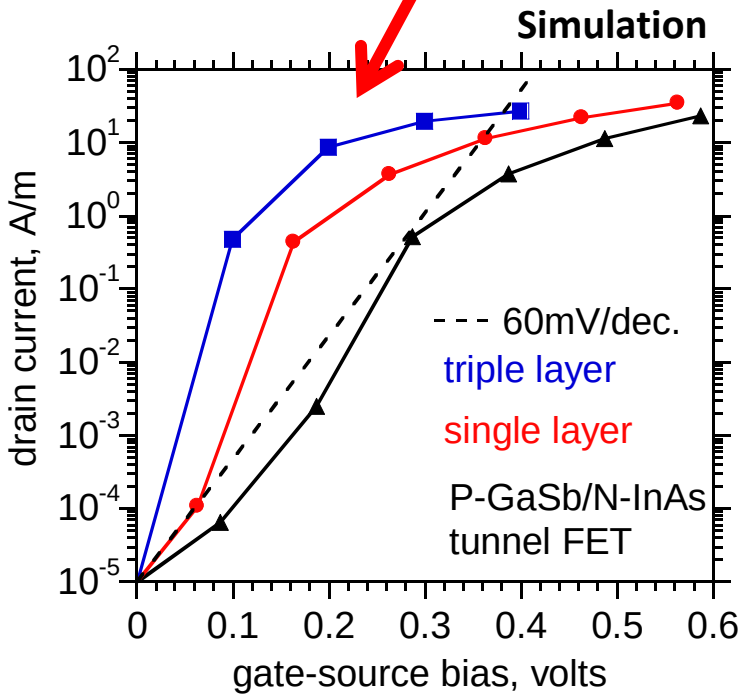
T-FET with 3-layer antireflection coating





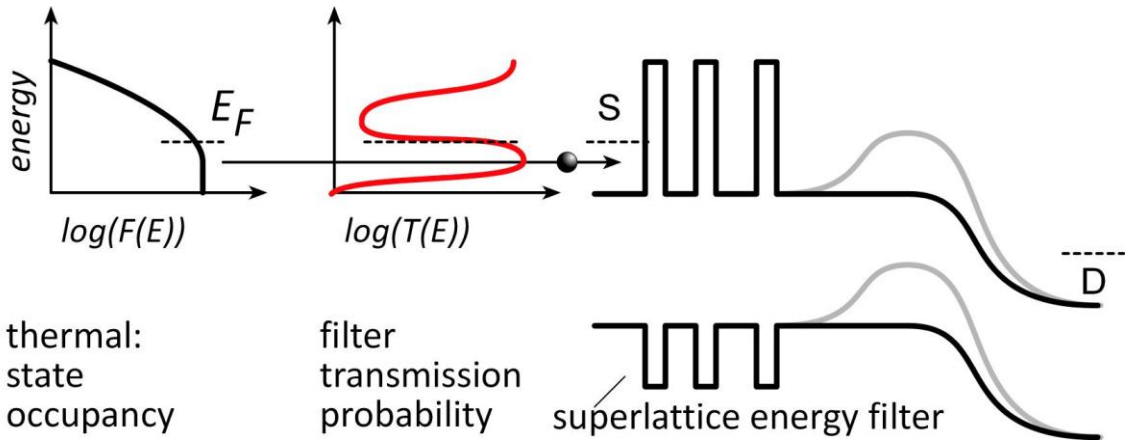






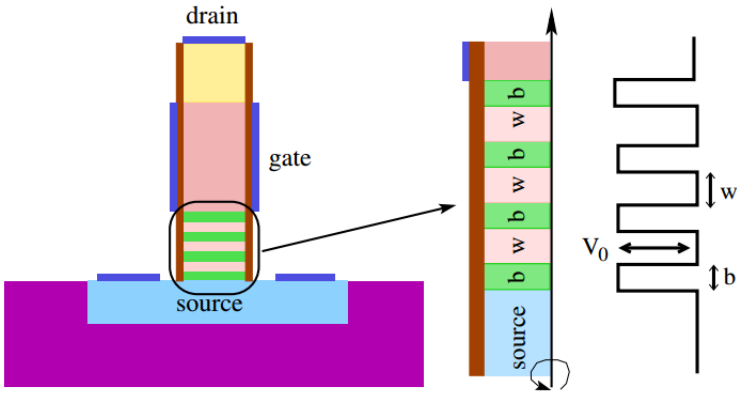
Interim result; still working on design

Source superlattice: truncates thermal distribution

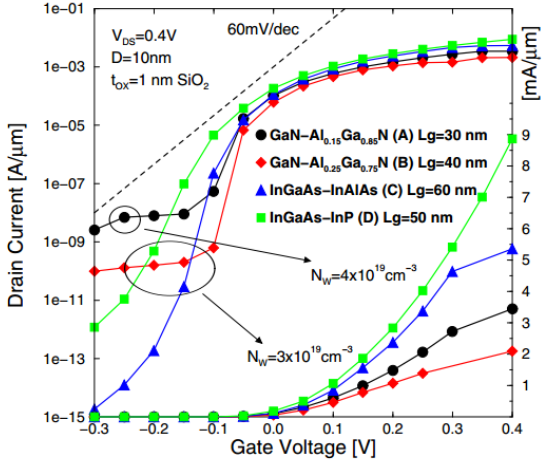


Proposed 1D/nanowire device:

M. Bjoerk *et al*., U.S. Patent 8,129,763, 2012. E. Gnani *et al*., 2010 ESSDERC



Gnani, 2010 ESSDERC



Gnani, 2010 ESSDERC:

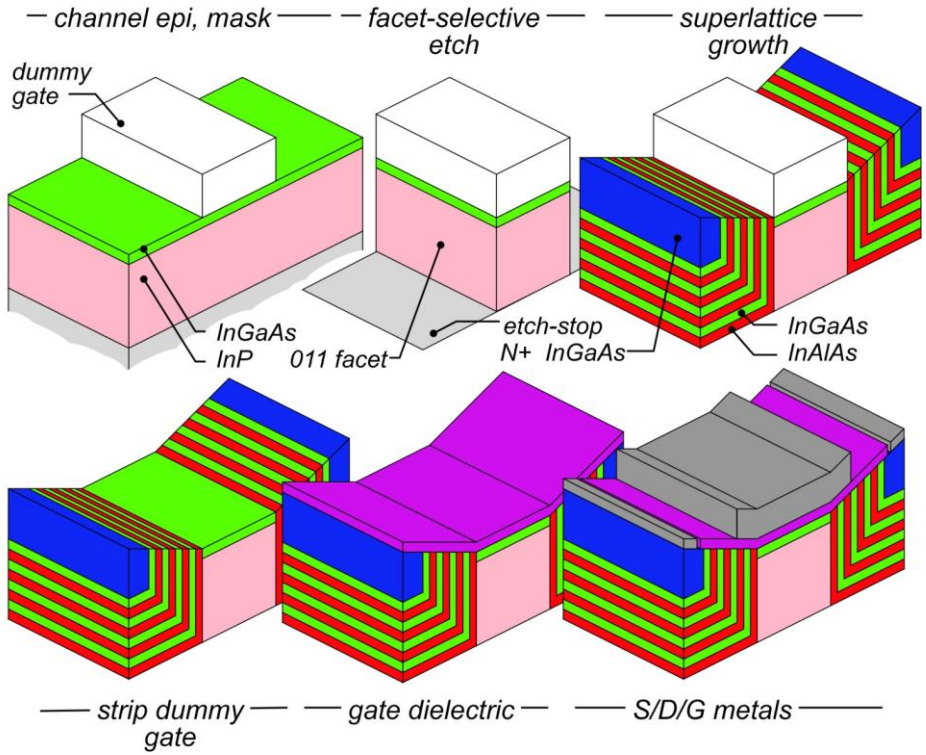
simulation

Planar (vs. nanowire) superlattice steep FET

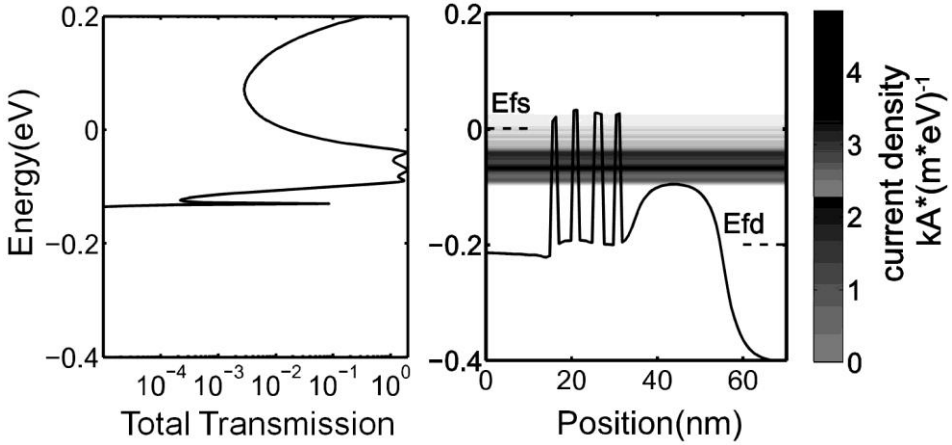
Planar superlattice FET
superlattice by ALE regrowth
easier to build than nanowire (?)

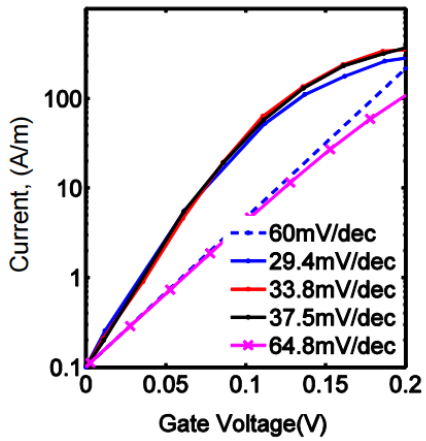
Performance (simulations):
~100% transmission in miniband.
0.4 mA/μm I_{on} , 0.1μA/μm I_{off} ,0.2V

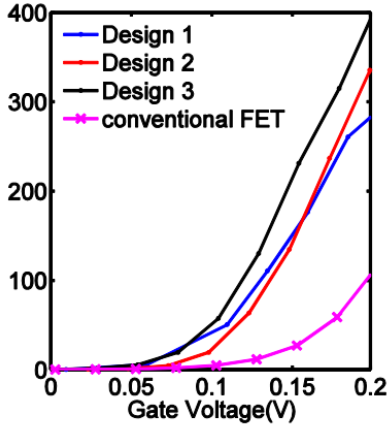
Ease of fabrication ?
Tolerances in SL growth ?
Effect of scattering ?



simulation







(backup slides follow)