Comparison of Ultra-Thin InAs and InGaAs Quantum Wells and Ultra-Thin-Body Surface-Channel MOSFETs

Cheng-Ying Huang[1], Sanghoon Lee[1], Evan Wilson[3], Pengyu Long[3], Michael Povolotskyi[3], Varistha Chobpattana[2], Susanne Stemmer[2], Arthur Gossard[1,2], Gerhard Klimeck[3], and Mark Rodwell[1]

[1]ECE, University of California, Santa Barbara
[2]Materials Department, University of California, Santa Barbara
[3]Network for Computational Nanotechnology, Purdue University, West Lafayette, IN

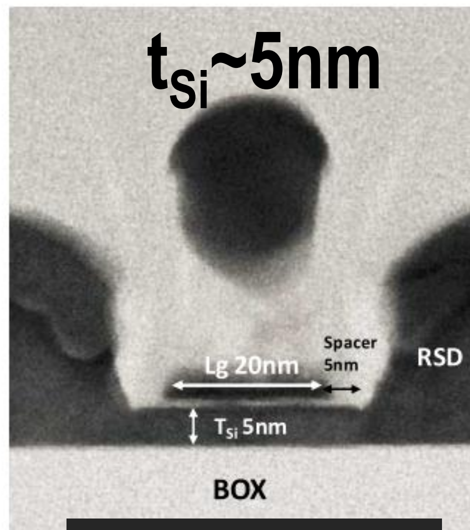
CSW/IPRM 2015
Santa Barbara, CA

Why III-V FETs? Why Ultra-thin channel?

- III-V channel: low electron effective mass→ high velocity, high mobility→ higher current at lower V_{DD}→ reducing switching power
- Channel thickness (T_{ch}) must be scaled in proportional to gate length (L_g) to maintain electrostatic integrity.
- For ultra-thin body (UTB) MOSFETs T_{ch}~1/4 L_g, and for FinFETs T_{ch}~1/2 L_g.
- At 7 or 5 nm nodes, channel thickness should be around 2-4 nm.
- Goal: Carefully examine *InGaAs* and *InAs* channels. The best design??

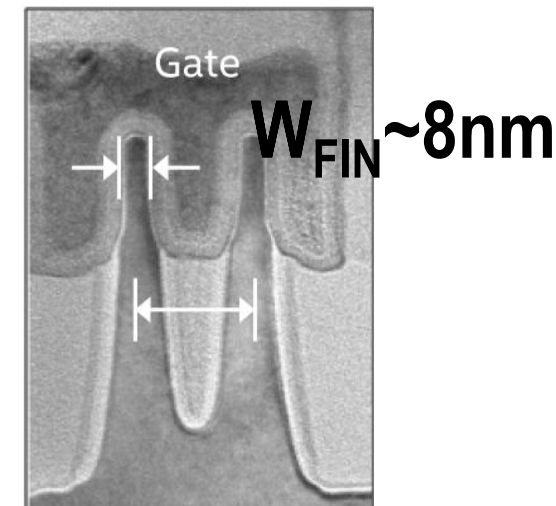
300K	Si	InAs	InGaAs
m_e^*	0.19	0.023	0.041
μ_e(cm²/V·s)	1450	33000	12000
μ_h(cm²/V·s)	370	450	<300
Eg(eV)	1.12	0.354	0.75
ε_r	11.7	15.2	13.9
a(Å)	5.43	6.0583	(InP)

Quantum confinement effects!!



STM-Leti-IBM 14nm UTBSOI

IEDM2014

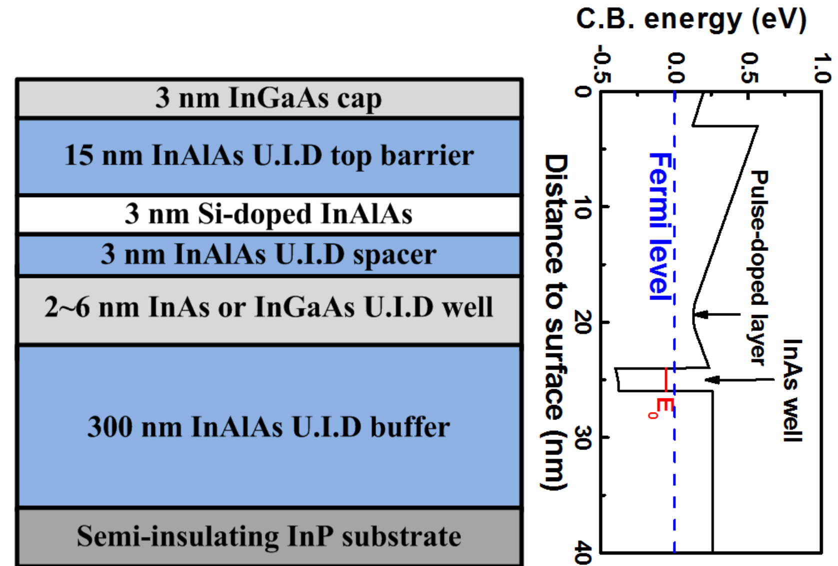


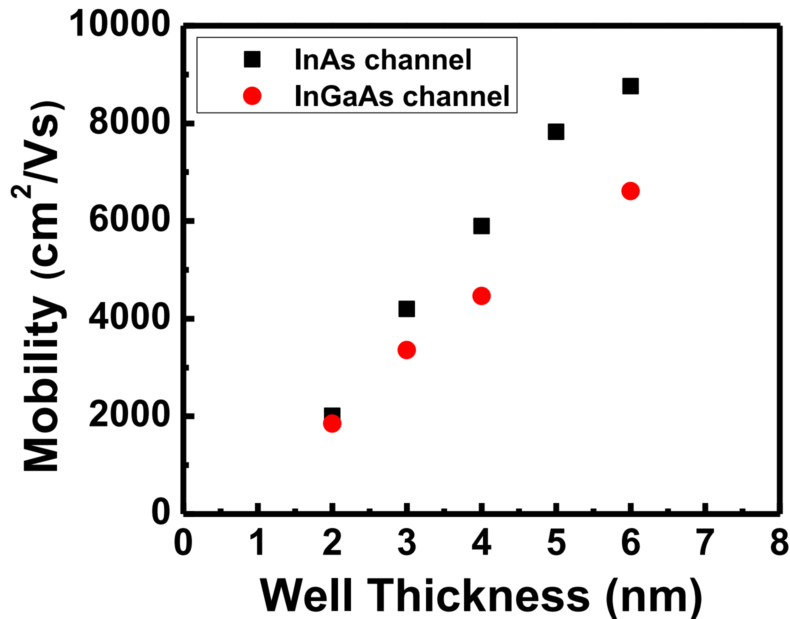
Intel 14nm FinFET

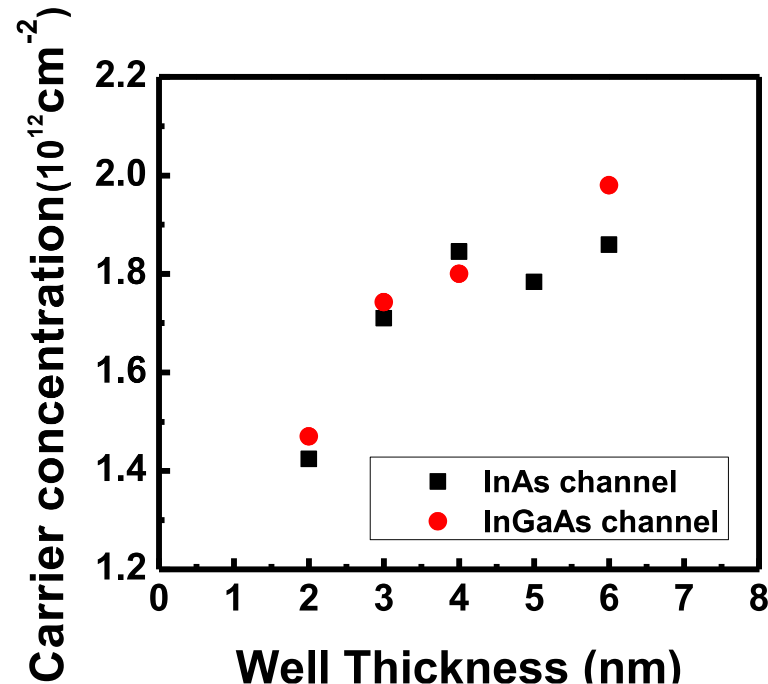
Makr Bohr, IDF2014

Ultra-thin channel 2DEG: Hall results

- Quantum well (QW) 2DEGs were grown by solid source MBE.
- For wide wells: $\mu_{InAs} > \mu_{InGaAs}$
- For narrow wells (~2 nm): $\mu_{InAs} \approx \mu_{InGaAs}$
- Carrier concentration decreases due to increased E_0.

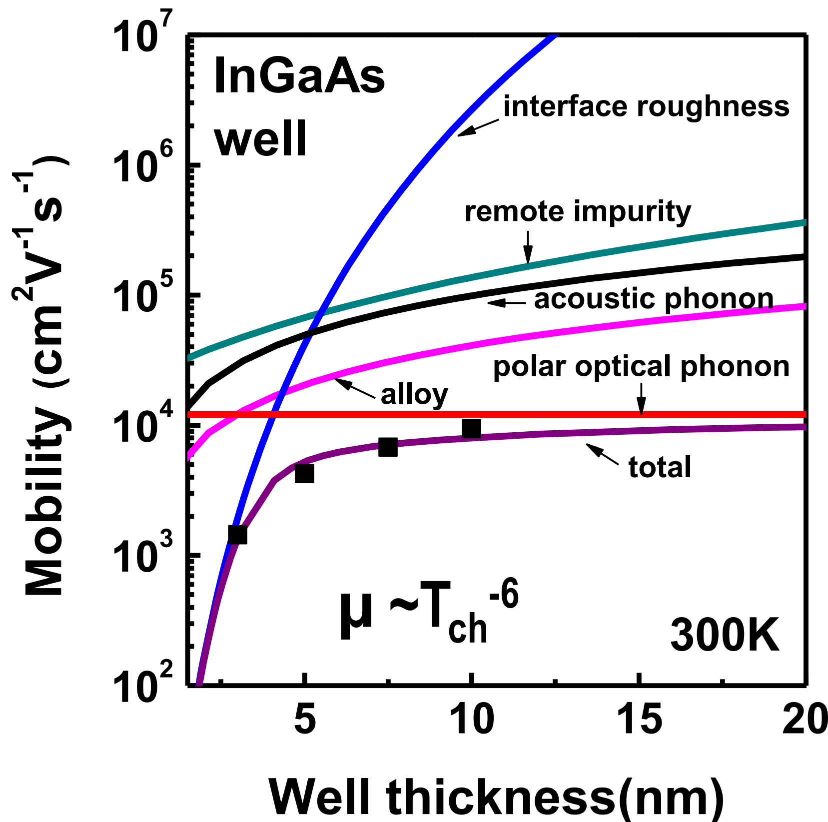




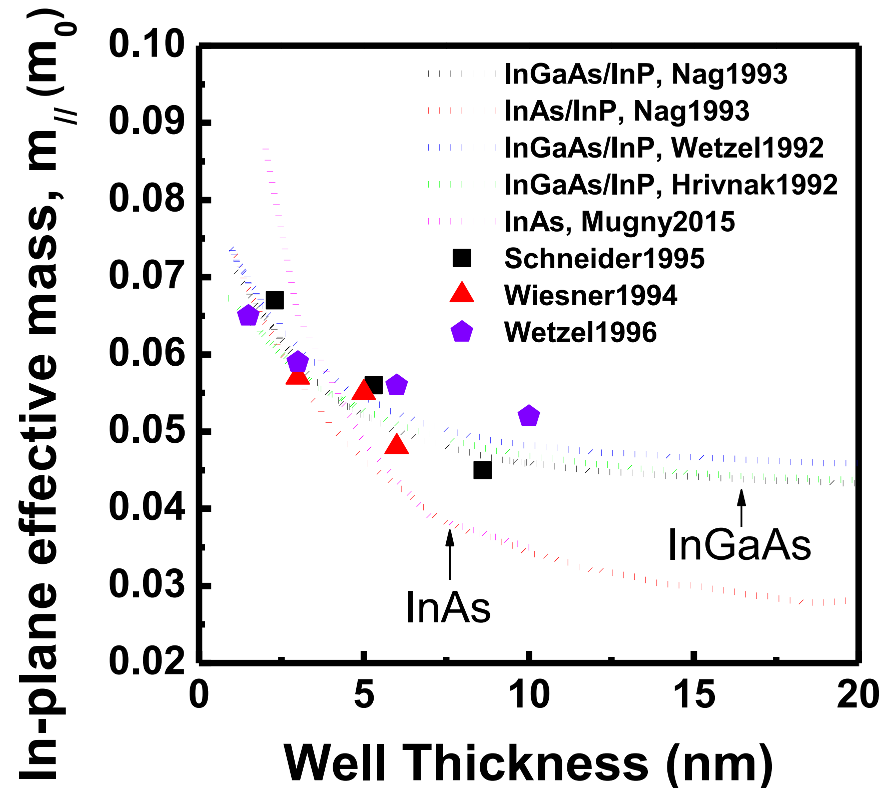


What happens in thin wells?

- Mobility is limited by interface roughness scattering. Strained InAs growth (S-K mode) might induce higher interface roughness.
- Electron effective mass are similar for ~2-3 nm InAs and InGaAs wells because of non-parabolic band effects.

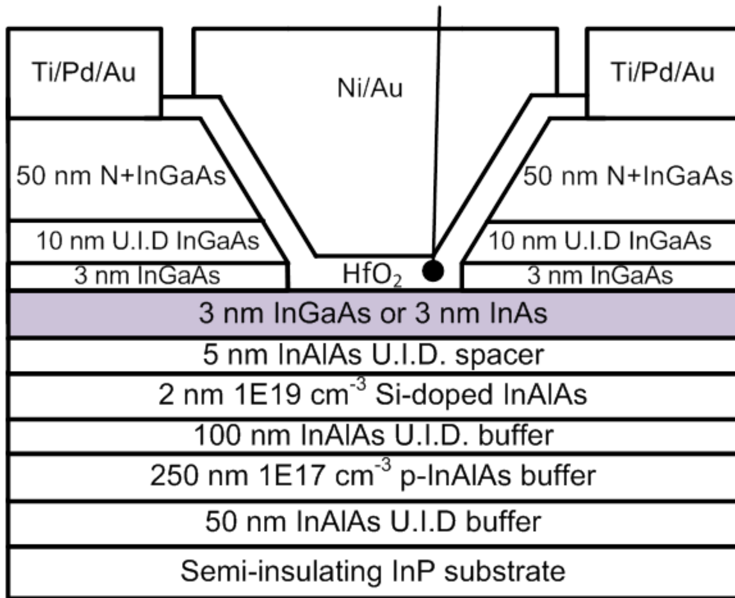


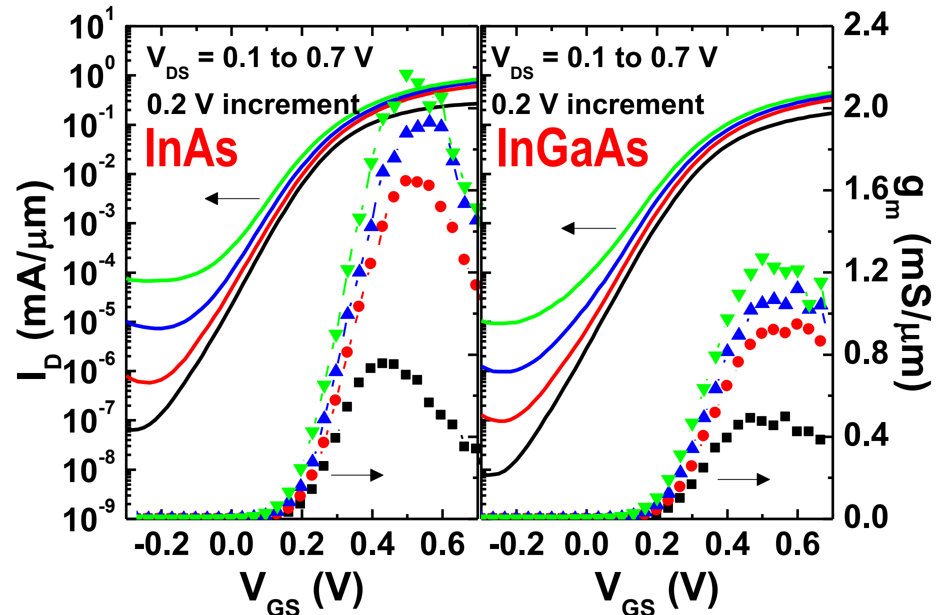
C. Y. Huang et al., J. Appl. Phys. 115, 123711 (2013)

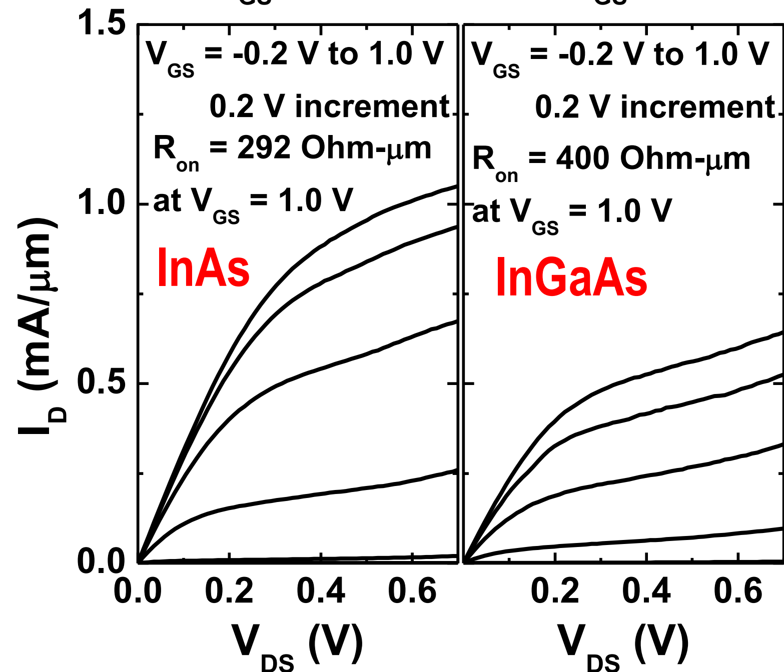


J. Appl. Phys. 77, 2828 (1995), Phys. Rev. B, 52, 1038 (1996), Appl. Phys. Lett 64, 2520 (1994), Appl. Phys. Lett 62, 2416 (1993), G. Mugny et al., EUROSOI-ULSI conference 2015.

Ultra-thin body III-V FETs: L_g~40 nm

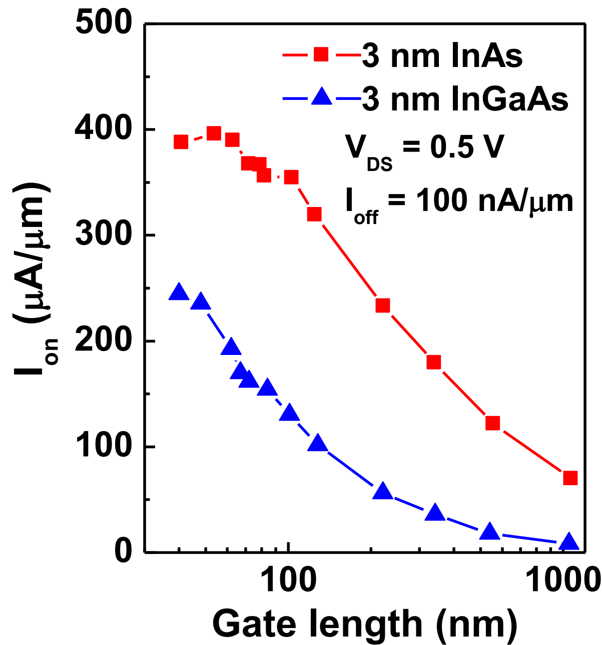


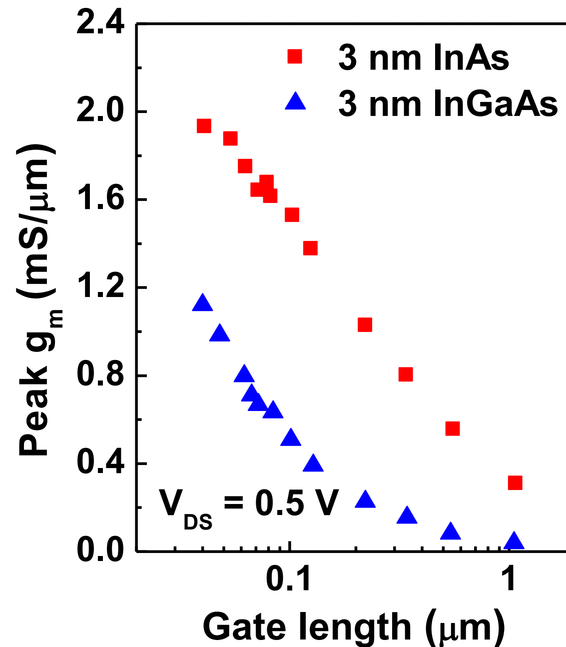


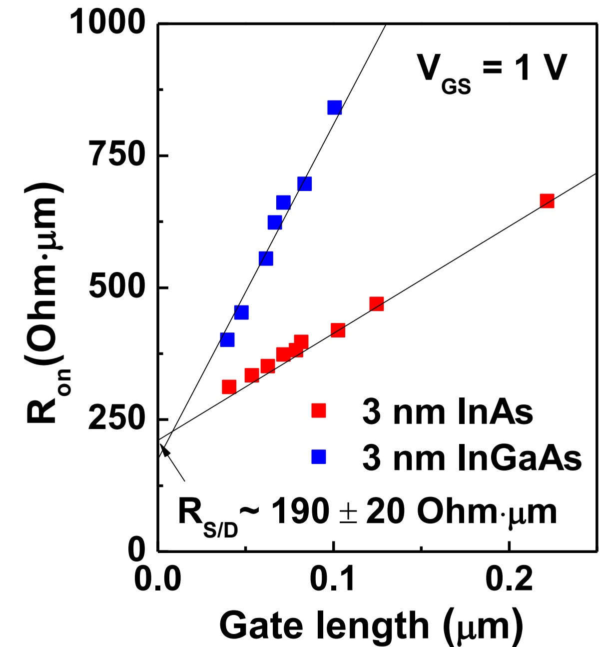


- **UTB FETs with 3 nm channels were fabricated to compare InAs and InGaAs channels.**
- **1.6:1 I_{on} and transcoaductance for InAs channels.**
- **10:1 lower I_{off} for InGaAs channels.**

On-state performance

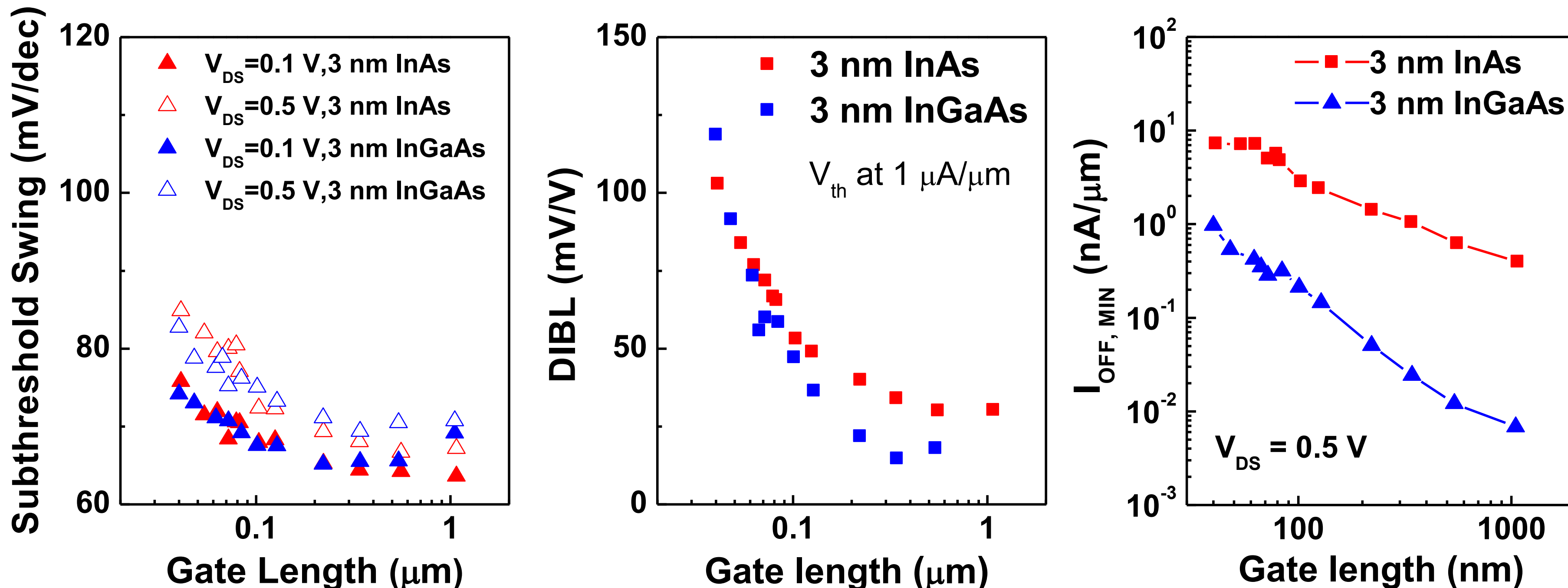






- Higher I_{on} and higher g_m for UTB InAs FETs than InGaAs UTB FETs.
- InAs FETs achieve g_m=2 mS/μm, and I_{on}=400 μA/μm at V_{DS}=0.5V and I_{off}=100 nA/μm.
- Similar source/drain resistance ($R_{S/D}$) ensures that the performance degradation of InGaAs is not from source/drain, but from channel itself (slope).

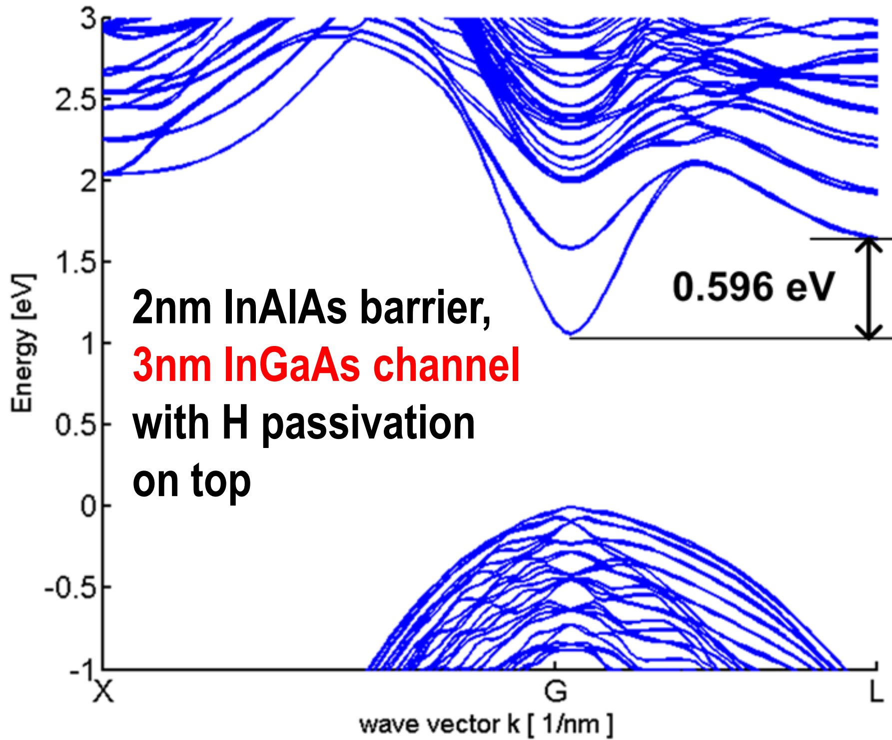
Subthreshold swing and off-state current

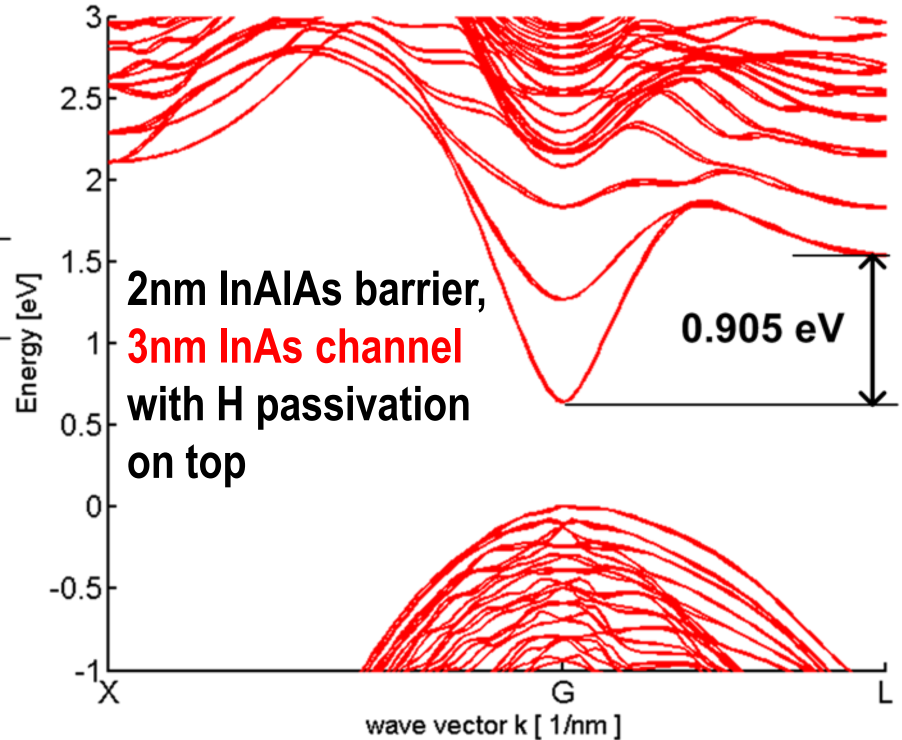


- Superior SS~83 mV/dec. and DIBL~110 mV/V because of ultra-thin channels and improved electrostatics.
- Minimum I_{off} is 10:1 lower for InGaAs channel at short L_g, where leakage current limited by band-to-band tunneling.
- InGaAs FETs are limited by gate leakage at long L_g.

Why QW-2DEGs and UTB-FETs show different results?

- 1st possible cause: Electron population in L valley due to strong quantum confinement → Unlikely.





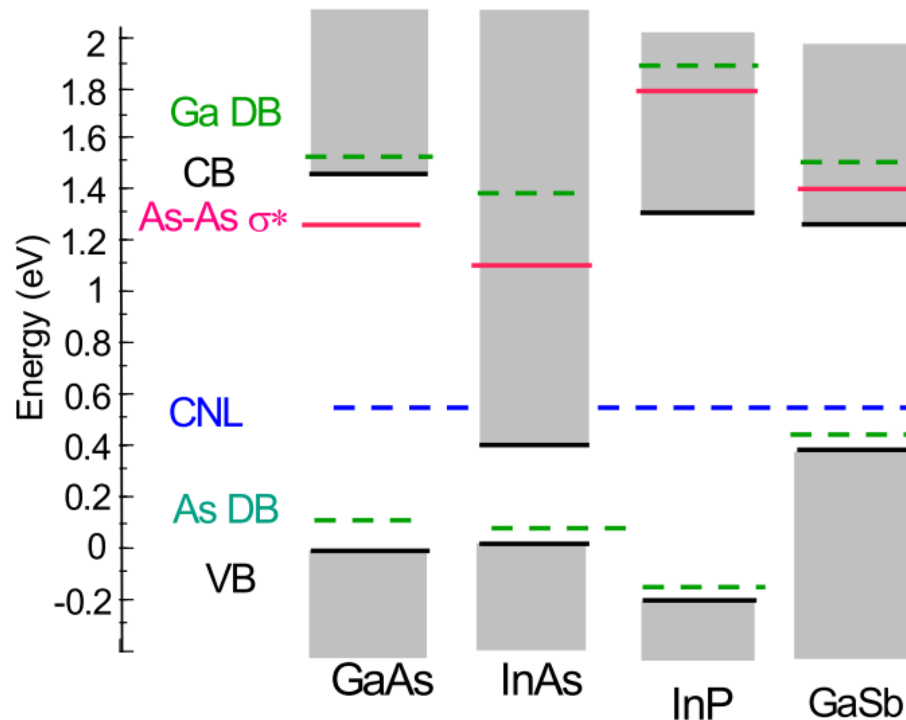
Courtesy of Evan Wilson, Pengyu Long, Michael Povolotskyi, and Gerhard Klimeck.

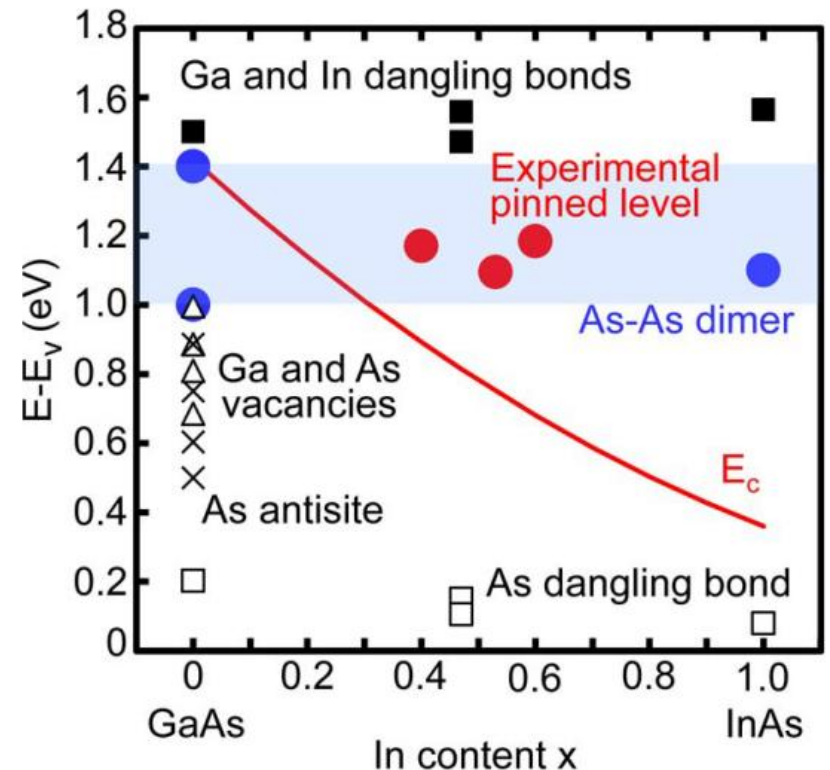
	$In_{0.53}Ga_{0.47}As$	InAs
m_e^* at Γ [m_0]	0.080	0.063
Γ – L separation [eV]	0.596	0.905
E_g at Γ [eV]	1.06	0.639

PURDUE UNIVERSITY

Why QW-2DEGs and UTB-FETs show different results?

- 2nd possible cause: Electron interaction with oxide traps inside conduction band → **Likely**.
- Electrons in high In% content channels have less scattering and less electron capture by the oxide traps.





J. Robertson et al., J. Appl. Phys. 117, 112806 (2015)
J. Robertson, Appl. Phys. Lett. 94, 152104 (2009)

N. Taoka et al., Trans. Electron Devices. 13, 456 (2011)
N. Taoka et al., IEEE IEDM 2011, 610.

UCSB L_g~12 nm III-V MOSFETs (DRC 2015)

N+InGaAs

N+InP

InP spacer

InAlAs Barrier

L_g~12nm

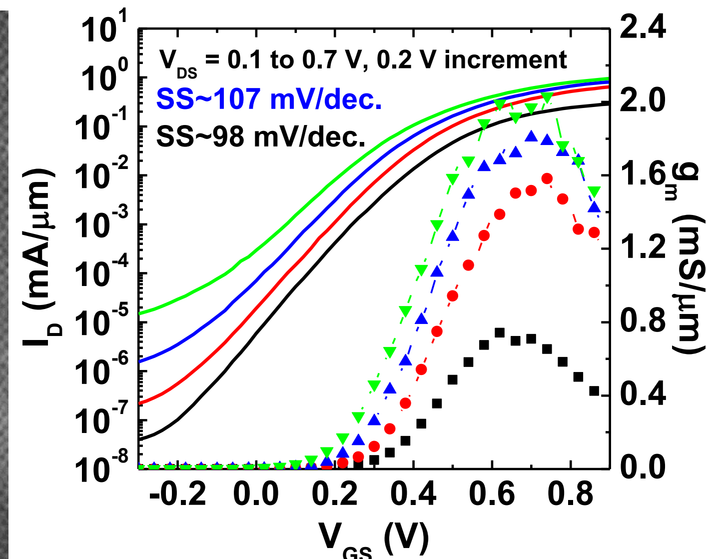
~ 8nm

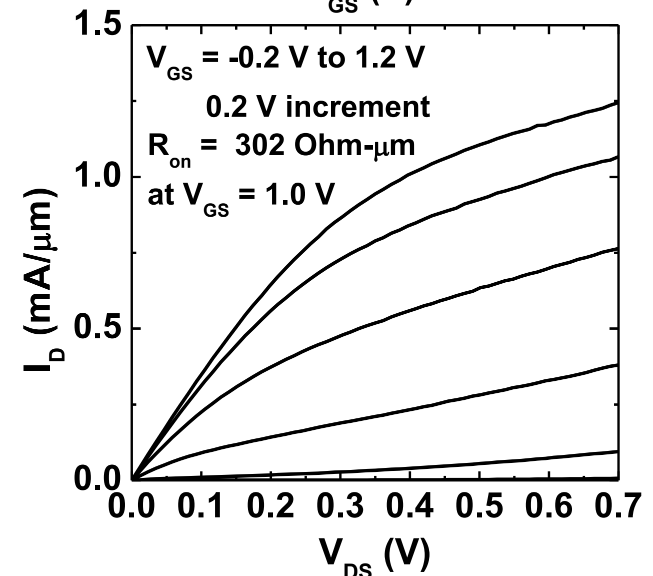
Ni

t_{ch}~ 2.5 nm

(1.5/1 nm InGaAs/InAs)

5 nm





I_{on}/I_{off}>8.3·10^5

Summary

- **Below 10 nm logic nodes, ultrathin channels are required.**
- **In QW 2DEGs, the electron Hall mobility are similar for InGaAs and InAs wells as the wells thinned to 2~3nm.**
- **In UTB MOSFETs, 3 nm InAs channels significantly improve on-state current and transconductance (~1.6:1), and reduce channel resistance as compared to 3 nm InGaAs channel.**
- **Purdue's tight-binding calculations show large ~0.6 eV Γ–L splitting in 3 nm InGaAs channels, ruling out the possibility of electron population in L-valley.**
- **UCSB C-V measurements show large dispersion in 3 nm InGaAs channels, possibly indicating the significant electron interactions with oxide traps. (As-As anti-bonding may be the culprit)**

Acknowledgment

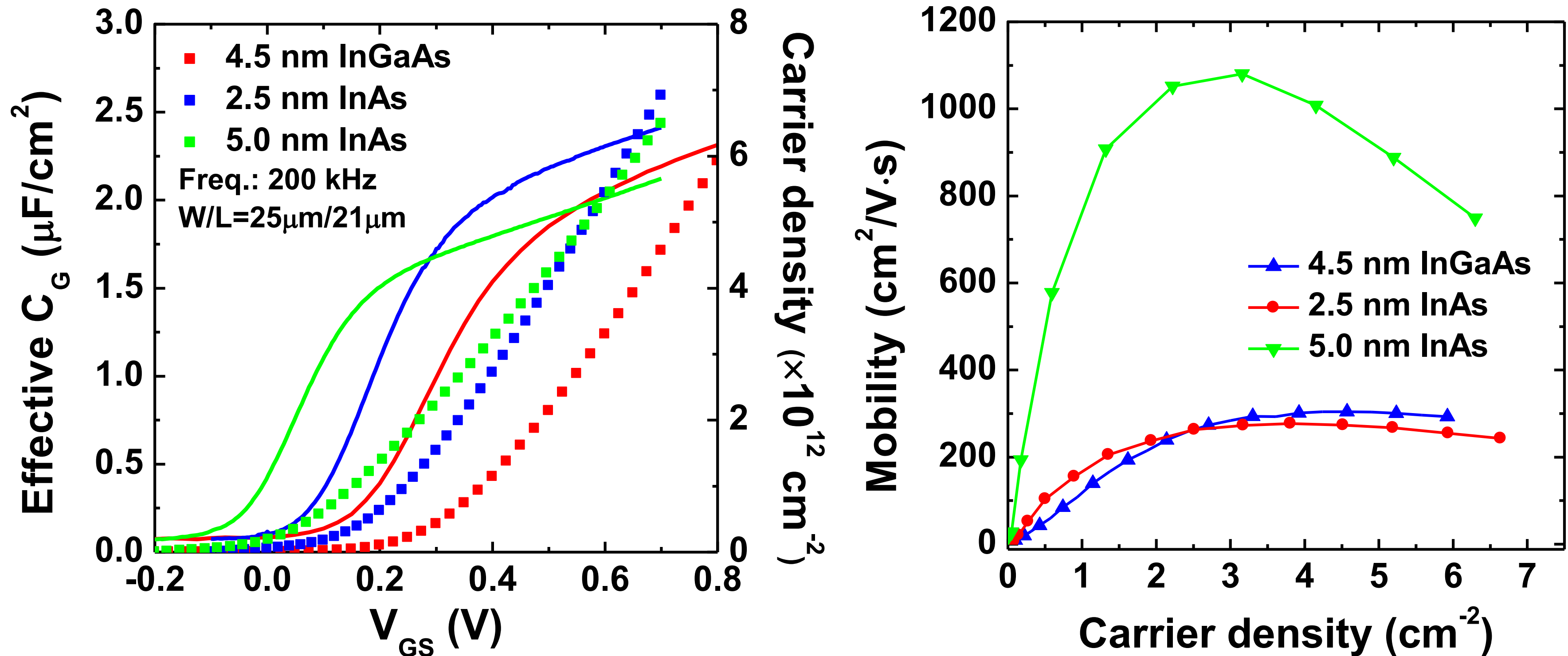
Thanks for your attention!
Questions?

- *This research was supported by the SRC Non-classical CMOS Research Center (Task 1437.009) and GLOBALFOUNDRIES(Task 2540.001).*
- *A portion of this work was done in the UCSB nanofabrication facility, part of NSF funded NNIN network.*
- *This work was partially supported by the MRSEC Program of the National Science Foundation under Award No. DMR 1121053.*

cyhuang@ece.ucsb.edu

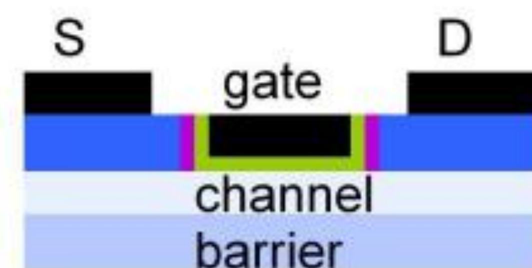
(backup slides follow)

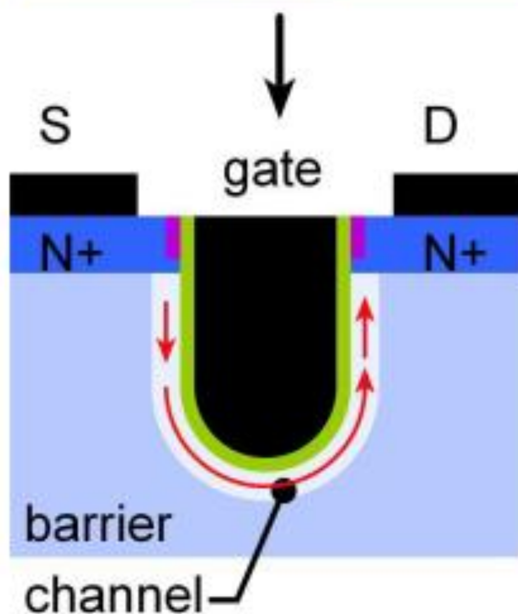
Mobility in different channel design: 25 µm-L_g

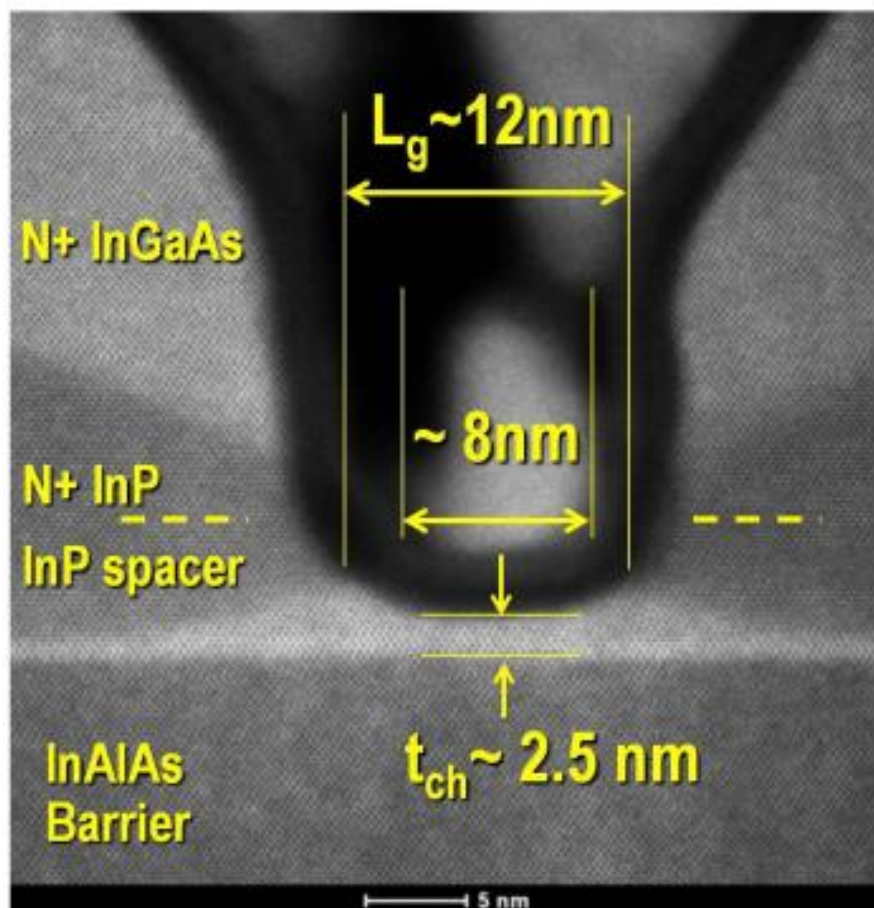


m*, $C_{g\text{-}ch}$, $R_{S/D}$ more important for ballistic FETs

Fixing source-drain tunneling by corrugation







Transport distance > gate footprint length
Only small capacitance increase

In(Ga)As: low m*→ high velocity → high current (?)

Ballistic on-current:

Natori, Lundstrom, Antoniadis (Rodwell)

$$J = K_1 \cdot \left(84\frac{\text{mA}}{\mu\text{m}}\right)\cdot\left(\frac{V_{gs}-V_{th}}{1\,\text{V}}\right)^{3/2},$$

$$\frac{1}{c_{equiv}} = \frac{T_{ox}}{\varepsilon_{ox}} + \frac{T_{\text{channel}}}{2\varepsilon_{\text{semiconductor}}}$$

$g = \#\,\text{valleys}$

$$K_1 = \frac{g\cdot(m^*/m_o)^{1/2}}{\left(1+(c_{dos,o}/c_{equiv})\cdot g\cdot(m^*/m_o)\right)^{3/2}}$$

More current unless dielectric, and body, are extremely thin.