Ultra-Low-Power Components for a 94 GHz Transceiver

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***Abstract*—We present a fully-integrated 94 GHz transceiver front-end in a 130 nm / 1.1 THz f_{max} InP HBT process. Low power is obtained through low-voltage design and high transistor gain. The IC is designed for multi-function, dual-polarization phased arrays. At 1.5 V collector bias, in dual-polarization simultaneous receiving mode, the IC has 21 dB gain, < 9.3 dB noise figure, and consumes 39 mW, while in transmitting mode with time-duplexed vertical and horizontal outputs, the transceiver achieves 5 dBm output power, 22 dB gain, and consumes 40 mW. At 1.0 V bias, in dual-polarization simultaneous receiving mode, the IC has 22.7 dB gain, < 8.9 dB noise figure, and consumes 26 mW.**

***Index Terms*—InP HBT, Millimeter wave integrated circuits, Phased arrays, Receivers, Transceivers, Transmitters**

I. INTRODUCTION

Millimeter-wave systems are used for high speed wireless communications and high resolution radar/imaging. There are key design tradeoffs, in particular performance (gain and radiated power) versus DC power consumption and die area. Many mm-wave systems are designed in SiGe and CMOS RF integrated circuit (RFICs) technologies. They require large DC power consumption to achieve the required system performance [1][2]. In the targeted application, a phased array with ~10,000 elements, large DC power consumption per element would require extremely large, heavy, and expensive power-supplies and heat-sinks.

We present (Fig. 1) an ultra-low power 94 GHz transceiver and the low-power techniques used to design it. The transceiver was designed for multi-function, dual-polarization phased array systems.

II. ULTRA-LOW POWER MM-WAVE DESIGN

The low power 94 GHz design was obtained through low-power IC design techniques (Fig. 2) and transistors with very high gain. Fig. 3 show the full IC block diagram. For low power, RF stages are biased as current mirrors (Fig. 2a), with 1.5 V or 1.0 V collector bias (the latter for lower power), and with a 1.5 V mirror reference supply. When feasible, smaller HBTs are used in the mirror references than in the main circuit to minimize bias circuit current. The mirror reference is shared between several blocks to minimize

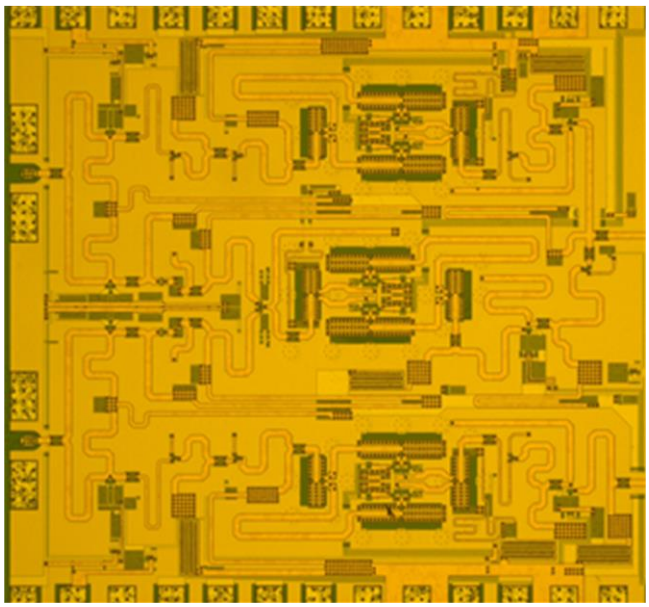


Fig. 1. 94 GHz transceiver (chip size: 1770 × 1550 μm^2).

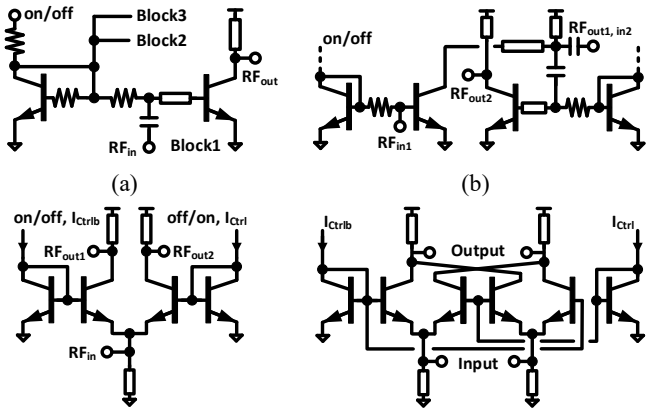


Fig. 2. Low power design: (a) RF stage current-mirror biasing for permitting 1.0 V collector bias and stage on/off switching, (b) transmit/receive switching at low-power points by stage DC power switching, (c) mirror as switch or variable-gain amplifier, and (d) multiplier for mixers, modulators, and phase shifters.

power consumption, and is also the on/off switch for Tx/Rx modes and V/H polarizations. At the RF backplane (Fig. 3), the IC is switched between transmit and receive simply by

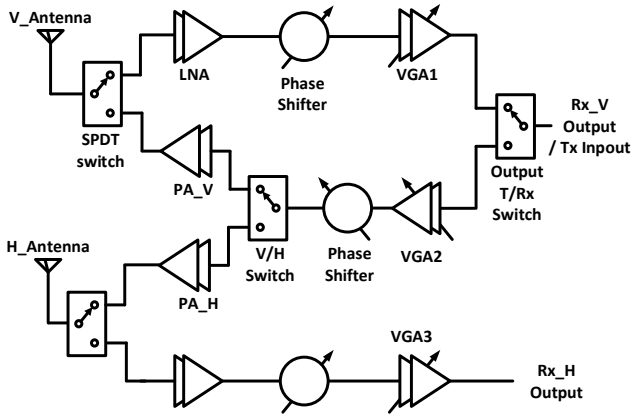


Fig. 3. Block diagram of the 94 GHz transceiver.

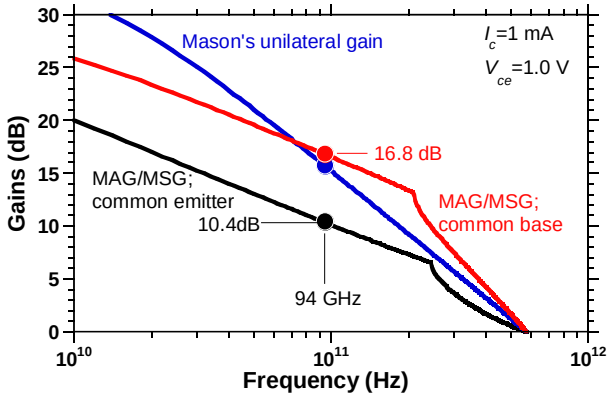


Fig. 4. Gains of common-emitter (CE) and common-base (CB) configurations (0.13 × 3 μm² HBT at I_C = 1 mA and V_{CE} = 1.0 V).

switching off gain stages (Fig. 2b) while ensuring that the RF port impedance remains 50 Ω. Common-base stages biased by current mirrors provide variable gain and switch signal paths (Fig. 2c), while mirror-based analog multipliers (Fig. 2d) form mixers which are then used as I/Q modulators within the analog phase-shifters.

III. INP HBT TECHNOLOGY

The ICs were designed into a 130 nm InP HBT process providing 50 Ω/square thin film resistors, 0.3 fF/μm² MIM capacitors, and three levels of gold interconnects (M1-M3). At a high-power bias, I_C = 6.9 mA and V_{CE} = 1.6 V, a 0.13 × 2 μm² HBT exhibits a current gain cutoff frequency f_τ = 520 GHz and a maximum frequency oscillation f_{max} = 1.1 THz [3]. Critically, at a low-power bias, I_C = 1 mA and V_{CE} = 1.0 V (Fig. 4), at 94 GHz the same HBT provides 10 dB (10 dB/mW) common-emitter (CE) and 17 dB (17 dB/mW) common-base (CB) maximum stable gain. With high gain and low power per stage, the IC power can be kept low. We used the CE configuration for low-noise amplifiers (LNAs) and low-gain stages. Since it has higher gain and better

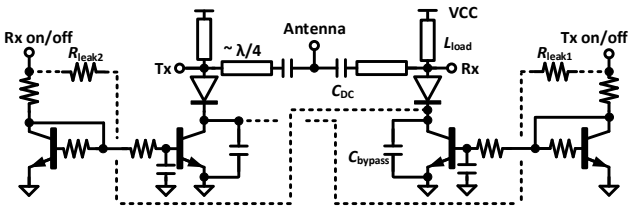


Fig. 5. Schematic of the antenna SPDT switch.

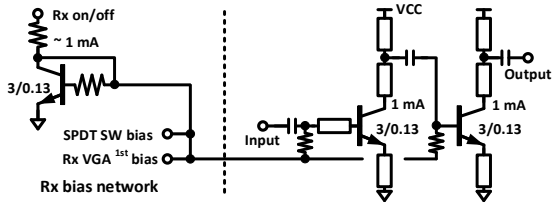


Fig. 6. Schematic of the LNA and its bias network.

input/output isolation, the CB configuration is used for high-gain stages, phase shifters, variable gain amplifiers (VGAs) and active switches.

The IC photograph and block diagram are shown in Fig. 1 and Fig. 3. The base architecture will transmit on vertical or horizontal polarizations, while receiving simultaneously both vertical (V) and horizontal (H) polarizations [4].

A. SPDT switch

The single-pole double-throw (SPDT) switch connects the antenna to either the transmitter or receiver (Fig. 5). The switch uses current-switched base-collector diodes and λ/4 isolation lines. A large resistance $R_{leak1,2}$ keeps the diodes in reverse bias when off. L_{load} resonates with diode parasitic capacitance.

B. LNA and bias network

The LNA is composed of two CE stages with inductive emitter degeneration for simultaneous input and noise matching, and is biased by a current mirror (Fig. 6). The current mirror also works as an on/off switch for selecting Rx and Tx modes. The SPDT switch and the first stage of the VGA are also biased by the same current mirror in the transceiver to reduce bias network power consumption.

C. Phase shifter

The phase shifter uses an active vector modulator (Fig. 7). A sub-(λ/4) balun [5] and λ/4 line generate I/Q signals; two further such baluns generate differential I/Q input signals to the Gilbert cell mixer/modulator core, and a final balun converts the differential output signal to single-ended format. Current mirrors are control the I/Q signal amplitudes. The sum of I_{Ctrl} and I_{Ctrlb} is set to 0.4 mA (= Q_{Ctrl}+Q_{Ctrlb}). The emitter area ratio between the current mirror and the main circuit is 1:3 to reduce the bias current.

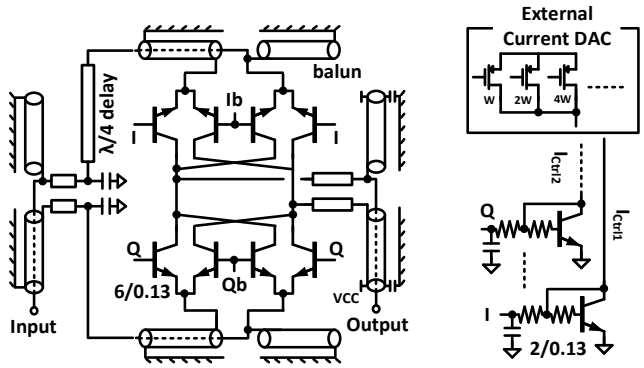
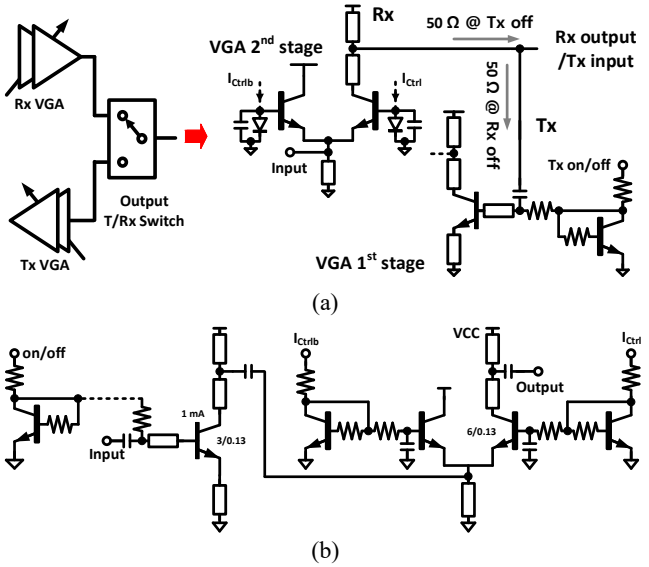


Fig. 7. Schematic of the phase shifter (left) and control circuits (right).



(a)

(b)

Fig. 8. T/Rx VGAs 1 and 2: (a) block diagram and matching condition of T/Rx on/off states, and (b) schematic of VGA 3 and its control network.

In the target system, the bias currents would be controlled by simple external -bit PMOS current digital-to-analog converters on a separate CMOS die.

D. T/Rx VGAs

Fig. 8 shows the T/Rx VGAs and their switching function. The VGA first stage has the same topology as the LNA; the second stage uses current steering to control the gain [5]. The gain is controlled by control currents I_{Ctrl} and I_{Ctrlb}, which are controlled complementarily, with their sum set to 1 mA. The Rx VGA output is matched to 50 Ω including the input capacitance of the Tx VGA in the off-state. Similarly, the Tx VGA input matching network includes the output capacitance of the Rx VGA in the off-state. Tx or Rx modes are selected by tuning the appropriate stages on and off. As no additional switch is needed, power consumption and chip area are both saved.

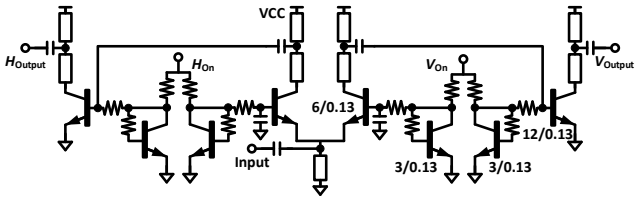


Fig. 9. Schematic of the PA and its bias network.

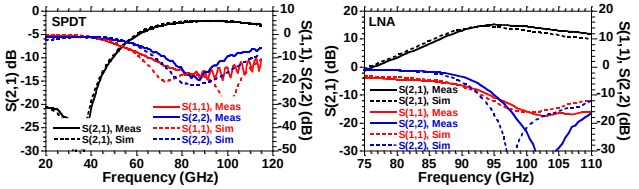


Fig. 10. Measured and simulated S-parameters of the SPDT switch (left) and LNA (right).

E. PA

The PA is composed of a class-A CE stage output stage and of a CB preamplifier with V and H polarization outputs, which are switched by current mirrors (Fig. 9). The preamplifier provides high isolation between V and H polarization outputs by using a CB configuration and the second stage was designed for > 7 dBm saturated output power.

IV. Measurement Results

The fabricated chips were characterized on wafer and biased at 1.5 V for both the current mirror reference and the supply voltage. The receiver was also tested with a 1.0 V collector supply voltage. Both the full IC and circuit block test structures were tested. The circuit test structures each have an individual biasing current mirror, while the fully-integrated transceiver IC has only five current mirrors (Rx V/H, PA V/H, and Tx). Measured S-parameters of the SPDT switch show 2 dB insertion and 19 dB isolation with 4.8 mW power consumption (Fig. 10). The LNA has 15.1 dB gain at 94 GHz and consumes 3.5 mW (Fig. 10). The measured noise figure is less than 6 dB. Measured results of the phase shifter show it can provide 360° phase shift with over 4 dB gain variation (Fig. 11). The VGA has over 7 dB gain adjustment (control current: 0.3-0.8 mA) with an associated 2 degrees the phase shift; VGA can thus equalize the gain variation due to the phase shifter with small phase error (Fig. 12). The total power consumption of the phase shifter and the VGA, including the current mirror control circuits, are 6.5 mW and 7 mW respectively. The PA has 17 dB gain at 94 GHz. The saturated output power is 7 dBm with a power added efficiency (PAE) of 18 % at 94 GHz (Fig. 13). The PA consumes 22.5 mW including the bias circuit. The fully-integrated transceiver front-end has a gain

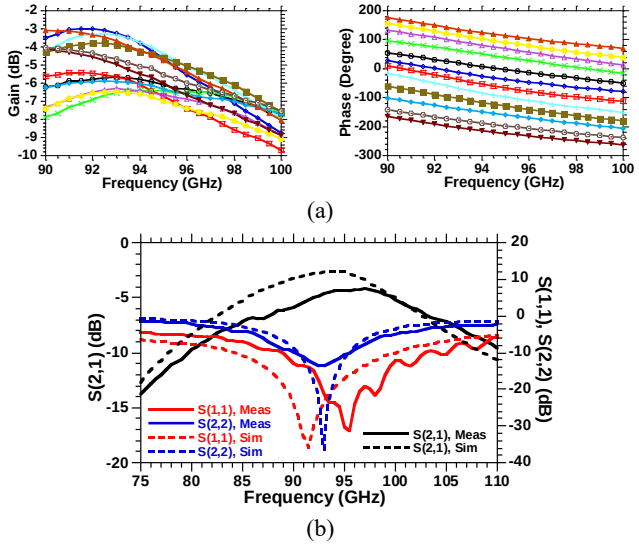


Fig. 11. Phase shifter: (a) measured phase shift and gain variation for different settings, and (b) measured and simulated S-parameters at the control bias current I_{Ctrl} = 0 mA and Q_{Ctrl} = 0 mA.

of 21 dB with power consumption of 39 mW for dual-polarization simultaneous reception and a noise figure is less than 9.3 dB in receiving mode. In transmitting mode, the transceiver achieves 5 dBm output power with a gain of 22 dB and a power consumption of 40 mW for time-duplexed V and H output. At a reduced 1.0 V collector bias (but with 1.5 V on the mirror reference) in dual-polarization simultaneous receiving mode, the IC has 22.7 dB gain, < 8.9 dB noise figure, and consumes 26 mW.

V. Conclusion

Ultra-low power components for a 94 GHz transceiver in a 130 nm InP HBT process are presented. The components are designed for multi-function, dual-polarization phased array. The fully-integrated transceiver front-end in the receiving and transmitting modes has power consumption of 39 mW @ 1.5 V (26 mW @ 1.0 V) and 40 mW, respectively. To the best of the authors' knowledge, this work presents the lowest power consumption transceiver front-end with competitive performance so far achieved at W-band frequencies.

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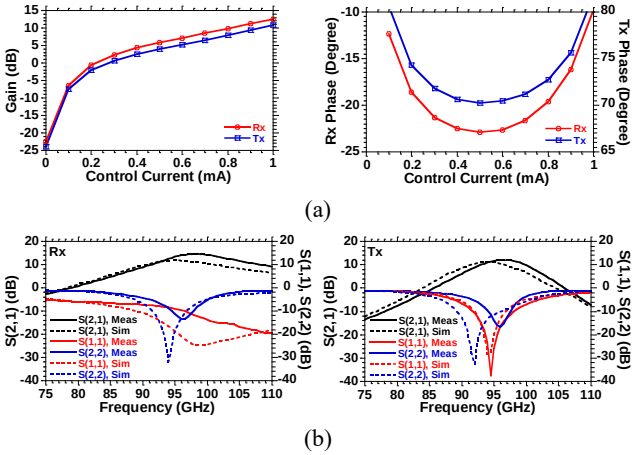

Fig. 12. T/Rx VGAs: (a) measured gain and phase variation for different control current settings, and (b) measured and simulated S-parameters at the highest gain setting.

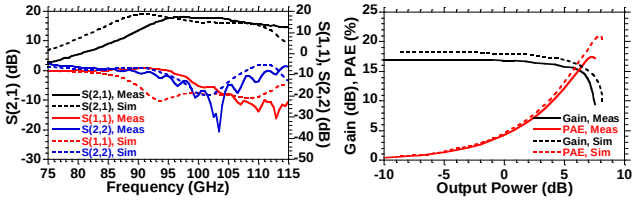

Fig. 13. PA: measured and simulated S-parameters (left), and output power and PAE (right).

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