High-linearity W-band Amplifiers in 130 nm InP HBT Technology

Robert Maurer[1], Seong-Kyun Kim[1], Miguel Urteaga[2], and Mark. J.W. Rodwell[1]

[1]ECE Department, University of California at Santa Barbara, Santa Barbara, CA, 93106, USA
[2]Teledyne Scientific and Imaging, 1049 Camino Dos Rios, Thousand Oaks, CA, 91360, USA

***Abstract*— We present a high-linearity pseudo-differential W-band amplifier IC, implemented in a 130 nm InP HBT process in a 1.1×0.72 mm^2 die. Correcting for test structure losses, the amplifier has a measured 21.9 dBm output-referred 3rd order intercept point (OIP3) and a single-stage gain of 6.4 dB at 100 GHz. The amplifier has a noise figure of 6.8 dB +/- 1dB at 95 GHz. The OIP3/Pdc ratio is 0.79 at 100 GHz. To the author's knowledge, these are among the first reported dynamic range measurements for W-band amplifiers.**

***Index Terms*—High IP3 Amplifier, InP HBT, W-band**

I. INTRODUCTION

High-linearity mm-wave amplifiers are needed for high-dynamic range receivers, in communications, radar, and electronic warfare. The IC reported here was designed as the 1st IF amplifier for a broadly-tunable high-dynamic range dual-conversion receiver (1-25 GHz) which achieves a wide tuning bandwidth by upconverting to a fixed 1st IF of 100 GHz. The amplifier can also serve as the post-LNA gain stage in high-dynamic-range W-band receivers. The primary goal for this amplifier was to achieve a high IIP3 so that the receiver is resistant to distortion generated from jammers lying within the receiver's IF bandwidth. The secondary goal was to achieve as low a noise figure as possible without sacrificing linearity or gain to maximize the dynamic range of the system. The ICs were fabricated in a 130 nm InP HBT process.

The common emitter amplifiers were designed in a pseudo-differential topology. Inductive emitter degeneration was used to increase amplifier IP3 and to simultaneously achieve an input match and low noise figure. Full receiver designs would use multiple cascaded pseudo-differential stages; the ICs reported here are single-stage test structures, and use sub-quarter-wavelength baluns [1] on input and output to interface to single-ended W-band wafer probes. The measured amplifier gain, noise, and OIP3 must be corrected for the balun insertion losses.

The 100 GHz amplifier MMICs have a gain of 6.4 dB at 100 GHz, a noise figure of 6.8 dB at 95 GHz, and an IIP3 / OIP3 of 15.52 dBm / 21.92 dBm. We will review the 130 nm InP HBT IC process in section II. Section III will outline the amplifier design, and section IV will detail the measurement procedures and experimental results.

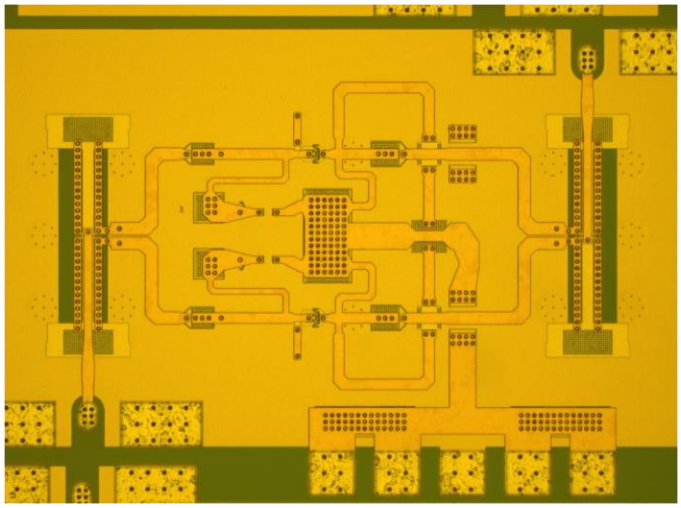

Fig. 1. Single-stage IF amplifier with input and output baluns to permit on-wafer testing. The full IC size is 1.1 mm × 0.72 mm, while the core differential amplifier is 0.46 mm × 0.47 mm.

II. INDIUM PHOSPHIDE HBT PROCESS

Teledyne Scientific Company's 130 nm InP HBT process with a ~3.5 V breakdown voltage was used to design this amplifier. The peak bandwidth of a single HBT in this process is f_{max} = 1150 GHz and f_τ = 520 GHz [2]. The HBT cells used in the amplifiers were composed of 4 emitter fingers, each with L_e = 5 μm. The emitter fingers within the cell are spaced at a large 8.7 μm for reduced thermal resistance. The quiescent HBT bias was I_c = 100 mA (2 mA per μm of L_e) and V_{ce} = 2 V.

A 3-metal layer gold interconnect is used with microstrip ground planes in metal 1 and lines in metal 3. The inter-metal interconnect separation dielectric material is BCB (ε_r = 2.7). The separation between the first and second level interconnect is 1.0 μm and the separation between the second and third level interconnect is 5.0 μm. MIM capacitors (SiNx, 0.3 fF/μm^2) are formed between the first and second level interconnect metal, and 50-Ω/square thin-film resistors are also available.

III. HIGH-LINEARITY AMPLIFIER IC DESIGN

The amplifier IC design was simulated using Advanced Design System (ADS) and an HBT model provided by Teledyne. All transmission line structures, baluns, MIM capacitors, device feed structures and probe pads were simulated using ADS Momentum 2.5-D electromagnetic simulator. Thin-film microstrip transmission lines were formed

using the top metal layer (MET3) for signal and using the first metal layer (MET1) for a ground-plane (separation of 7.0 μm).

The common emitter amplifiers were designed in a pseudo-differential topology, as this minimizes, in a receiver with multiple gain stages, interstage coupling through the power supply. Further, in a pseudo-differential structure, the impedance of the on-wafer MIM power supply bypass capacitors does not detune the output impedance-matching network.

A microstrip transmission line is used to terminate the emitter port of the cell to add inductive degeneration. At the cost of reduced gain, this increases the OIP3 and permits simultaneous matching for low noise and low input reflection coefficient. At the collector port of the cell, a λ/4 transmission line short-circuits any locally-generated 200 GHz second harmonic, as this mixes with the fundamental to produce additional 3rd-order intermodulation. The base port of each HBT cell is biased using a simple current mirror. A circuit diagram can be seen in Figure 2.

Input and output baluns were added to permit on-wafer testing of single-stage amplifier test structures. The baluns are sub-quarter-wavelength with a shunt matching capacitor to bring them into resonance at 100 GHz. The insertion loss of the baluns and corresponding matching capacitors were measured to be 1.2 dB using a separate test structure. The measured insertion losses of the baluns were used to de-embed the gain, noise, and IP3 of the core differential amplifier. Both the breakout performance and the de-embedded amplifier performance will be presented in the following section.

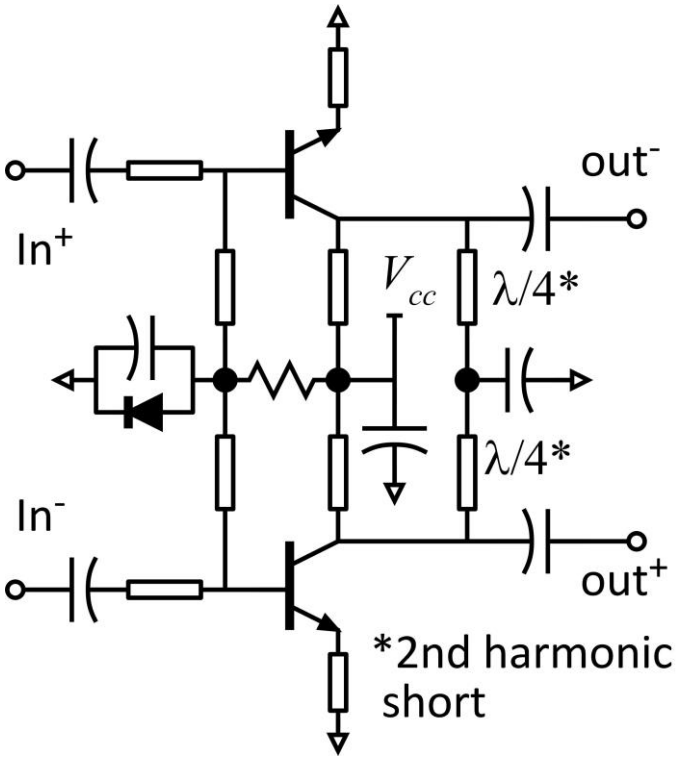

Fig. 2. Circuit block diagram

IV. Experimental Results

The IC was tested for small signal gain using an Agilent N5242A PNA-X with Oleson W-band frequency extender modules. Probe tip LRRM calibration was performed with WinCal XE on a Cascade Microtech calibration substrate. The reference plane was set at the probe pads of the IC.

The small signal gain of the amplifier is shown in Figure 3. For these measurements, I_c = 100 mA and V_{cc} = 2.0 V. The de-embedded small signal gain of the pseudo-differential amplifier is 6.2 dB at 100 GHz.

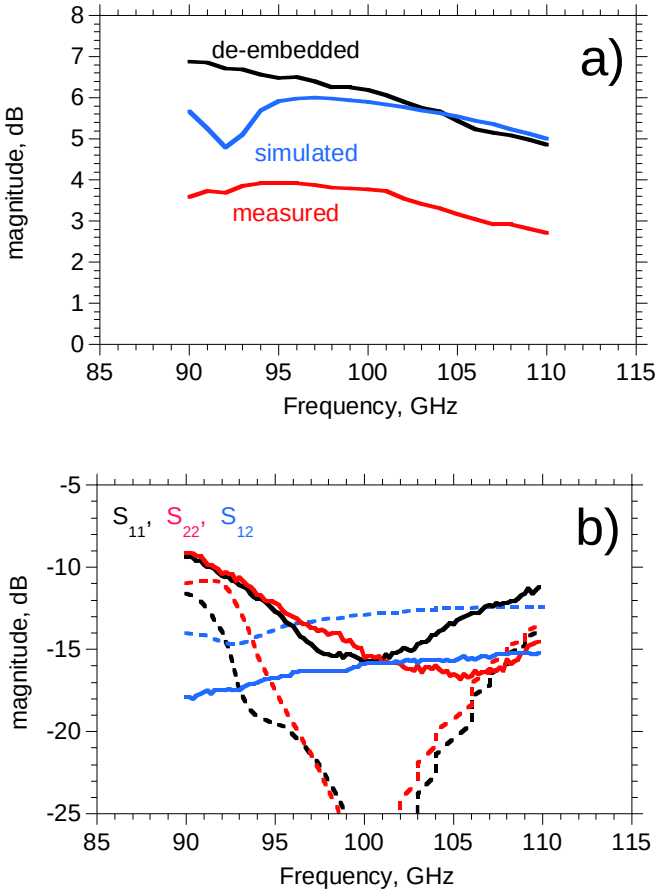

Fig. 3. a) Measured, simulated, and de-embedded amplifier S_{21}, b) Measured (solid) and simulated (dashed) S_{11}, S_{22}, and S_{12}

Noise measurements were performed using a Micronetics Inc. 90-95 GHz noise source and an Agilent N8972A Noise Figure Analyzer (NFA). The NFA was limited to a maximum input frequency of 1.5 GHz, therefore a QuinStar Technology W-band balanced mixer was used to downconvert the output to a compatible frequency. The LO was supplied by a QuinStar 94 GHz Gunn Oscillator. Because of the narrow bandwidth of the noise source and the NFA, noise measurements were limited to a frequency range from 94 GHz to 95 GHz. The measured and simulated noise figures of the amplifier can be seen in Figure 4.

The two-tone IP3 measurement system was constructed using WR-10 waveguide components. A block diagram of the setup can be seen in Figure 5. One fundamental tone was

produced with an Agilent N5242A PNA-X network analyzer with an OML W-band VNA Extender head. A second fundamental tone spaced 100 MHz above the first was produced by an Agilent N5247A PNA-X network analyzer with a W-band active frequency tripler. A variable attenuator was used to adjust the input power of each fundamental tone. The two fundamental tones were combined with a Quinstar WR-10 matched hybrid tee (magic tee) and coupled to the amplifier with a pair of Picoprobe W-band GSG probes.

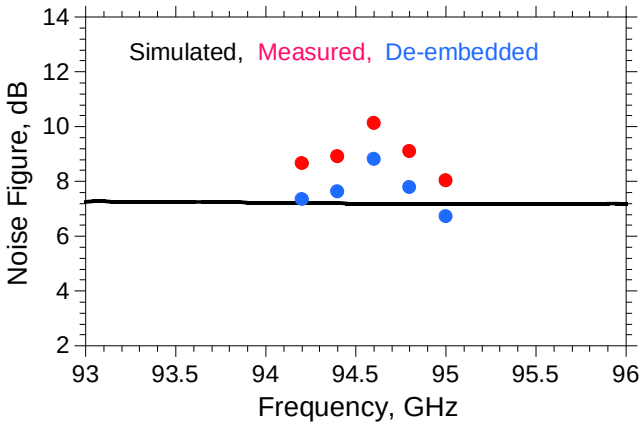

Fig. 4. Measured, simulated, and de-embedded noise figure.

The output was connected to a -20 dB directional coupler, with the through port was connected to a power sensor, to monitor power, and the 20 dB coupled port was connected to the RF port of a Quinstar W-band balanced mixer. The LO supplied to the downconversion mixer was kept 1 GHz below the first fundamental tone. The IF output was detected using a Rohde and Schwarz Spectrum Analyzer. The power of the fundamental tones displayed at 1 GHz and 1.1 GHz and the power of the third-order IM products displayed at 0.9 GHz and 1.2 GHz were recorded for various input powers and used to determine the IP3. The insertion loss of each waveguide component and directional coupler, the conversion loss of the mixer, and the IP3 of the mixer were all measured and used to extract the OIP3 of the amplifier. These measurements were performed at 4 different frequencies at a bias condition of V_{cc} = 2 V & I_c = 100 mA.

The measured S_{21} of the amplifier with baluns and the measured insertion loss of the baluns were then used to de-embed the IIP3 and OIP3 of the core differential amplifier. The IIP3 and OIP3 of the breakout and the de-embedded amplifier can be seen in figure 6 and figure 7, respectively. The simulation results shown in these plots correspond to those of the core differential amplifier.

To our knowledge, these are among the first reported intermodulation results for W-band amplifiers. One commonly-used benchmark for a high-linearity amplifier is the ratio of OIP3 to DC power consumption. Figure 8 places our work in context with other previously published high-linearity mm-wave amplifiers. The outliers here are the results of Kobayashi [3], which used InP HBT technology collector designed explicitly for reduced IM3, and the results of Kwon [4], which used a common-base configuration with AlGaAs/GaAs HBT.

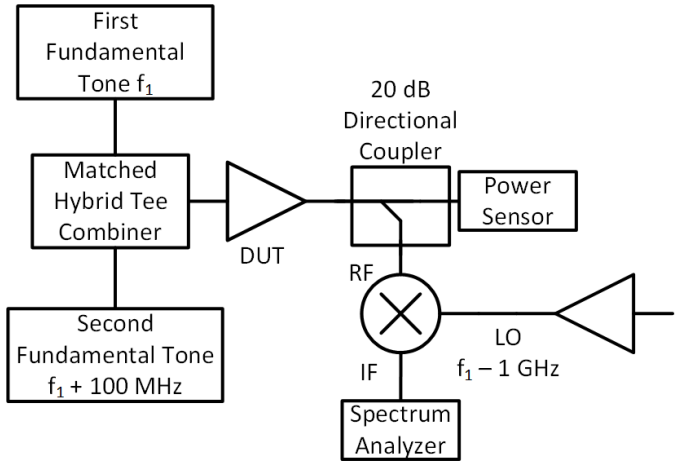

Fig. 5. Two-tone IP3 measurement configuration

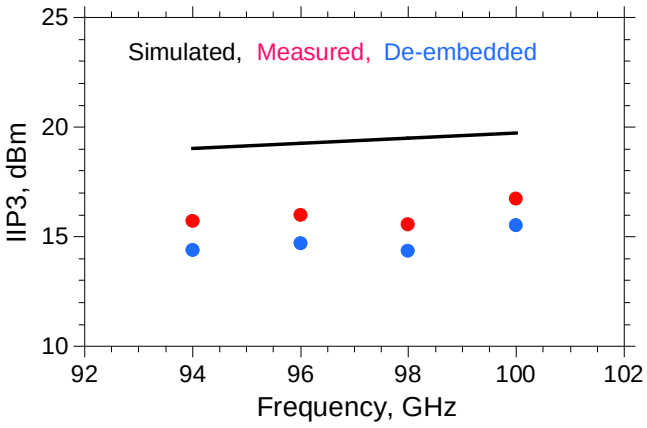

Fig. 6. Comparison of measured and simulated input-referred third-order intercept

V. Conclusion

A High-linearity amplifier MMIC in a 130 nm InP HBT process is presented with an OIP3 of 21.9 dBm and a gain of 6.4 dB at 100 GHz and a noise figure of 6.8 dB at 95 GHz. We report an OIP3/Pdc ratio of 0.79. To our knowledge these are among the first reported results for high-linearity W-band amplifiers.

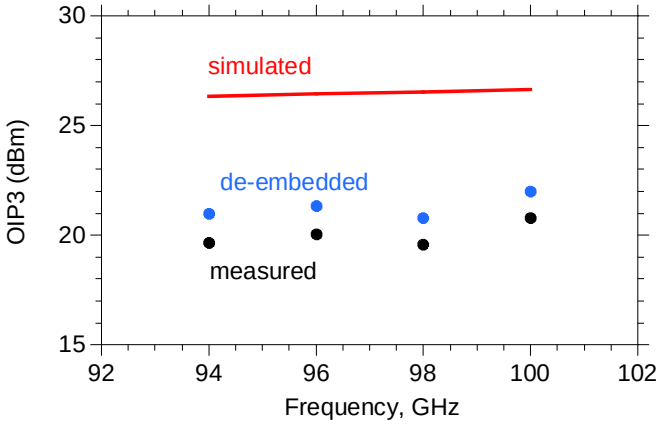

Fig. 7. Comparison of measured and simulated output-referred third-order intercept

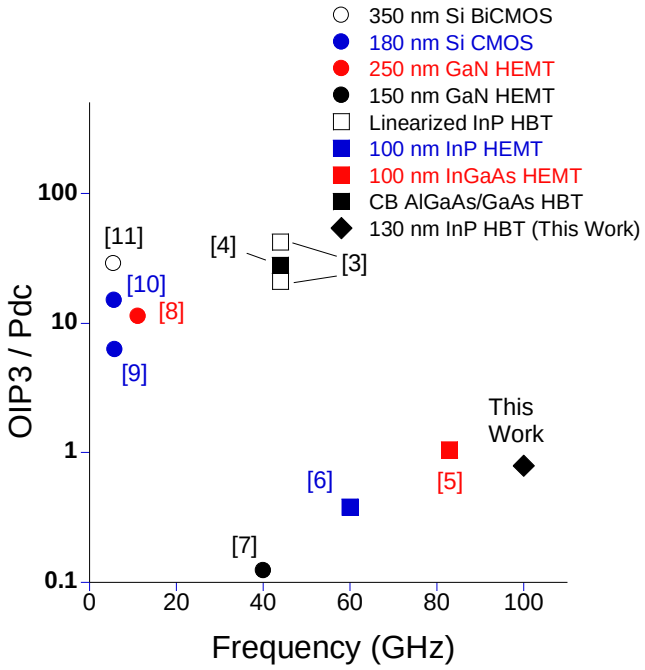

Fig. 8. Comparison of the performance of high-IP3 mm-wave amplifiers.

VI. Acknowledgment

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