A Tunnel FET Design for High-Current, 120 mV Operation

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***Abstract*—** We report simulations of logic transistor operation at supply voltages V_{DD} between 0.08-0.18V. Tunnel FETs (TFETs) can operate at low voltage with low off-currents I_{OFF}, but on-currents I_{ON} are greatly reduced by low tunneling probability. The minimum feasible V_{DD} is constrained not only by the transistor subthreshold swing (*SS*) given a target I_{ON}/I_{OFF} ratio, but also by the reduction of the drain current as the drain Fermi level approaches the channel conduction-band energy. This output conductance reduces the TFET voltage gain and impairs the logic gate noise margin; increasing the TFET threshold voltage V_{th} increases the noise margin while reducing both I_{ON} and I_{OFF}. In ballistic simulations with 10^{-3}A/m I_{OFF}, triple-heterojunction tunnel FETs (3HJ-TFETs) show >50% tunneling probability and a high 265A/m I_{ON} at V_{DD}= 0.18V and 195A/m at V_{DD}=0.12V. In simulations with an optical deformation constant (proportional to scattering strength) of 220meV/nm, consistent with μ=1.1x10^5 cm^{2}V^{-1}s^{-1}, reduces I_{ON} by 31% given fixed I_{OFF} and V_{DD}. In ballistic simulations, increasing V_{th} by 0.02V above that required for 10^{-3}A/m I_{OFF}, a noise margin of 24% of V_{DD} is obtained at V_{DD}=0.12V.

I. Introduction

CV_{DD}^2 power dissipation constrains VLSI circuit performance [1]; low dissipation implies low V_{DD}. MOSFETs have, at best, 60mV/dec. subthreshold swing, hence the I_{ON}/I_{OFF} ratio becomes small as V_{DD} is reduced. Fig. 1 shows ballistic simulations; a Si MOSFET with 30nm gate length L_g exhibits ~60 mV/dec. *SS*, but with 10^{-3}A/m I_{OFF}, the I_{ON} is ~100A/m at V_{GS}=0.3V and a small ~2A/m at V_{GS}=0.18V. TFETs can have small *SS* [2], but I_{ON} is limited by low tunneling probability. In ballistic simulations (Fig. 1), a GaSb/InAs double-gated ultra-thin-body (UTB) TFET with (001) confinement [3] and an 1.8nm thick channel shows ~30A/m I_{ON} at V_{DD}=0.3V and ~8A/m at V_{DD}=0.18V. The low I_{ON} will result in slow logic operation.

We had recently proposed a triple heterojunction TFET (3HJ-TFET), in which, in ballistic simulations, the tunneling probability and I_{ON}, at V_{DD}=0.3V, was substantially enhanced by $(1\bar{1}0)$ confinement and by the addition of source and channel heterojunctions (HJs) [4, 5]. Reducing V_{DD} from 0.7V to 0.3V would reduce switching energy by 1:5.4, but a 0.12V supply would save 1:34 in energy. Here we consider the design of 3HJ-TFETs for V_{DD}=0.08-0.18V operation. Such low-voltage design involves not only the SS but also the TFET I_D-V_{DS} characteristics and their effect on logic noise margin. As the 3HJ-TFET design reduces the tunnel barrier thickness, high leakage currents due to phonon-assisted tunneling are a potential concern; we also examine the effect of phonon scattering on I_{OFF}. We will examine these constraints using self-consistent transport simulations with ballistic [6] and inelastic non-coherent [7] quantum transport with a sp3d5s* tight binding basis with spin orbit coupling [8].

II. High I_{ON}

In a 3HJ-TFET (Fig. 2), $(1\bar{1}0)$ confinement improves the tunneling probability through reduced transport effective mass and tunnel barrier energy [4]. Additional InAs/InAlAsSb channel and AlSb/GaSb source [9,10] HJ increase the junction built-in potential and field, reducing the tunneling distance. The HJ introduce two resonant states, further enhancing transmission. The design, modified from [5] for 0.12-0.18V operation, includes an AlSb source (N_A=3×10^{19}cm^{-3}), a 1.7 nm $Ga_{0.5}Al_{0.5}Sb$ (N_A=6×10^{19}cm^{-3}) grade, a 2.7 nm GaSb (N_A=5×10^{19}cm^{-3}) P-junction layer, a 1.75 nm InAs undoped N-junction layer, an undoped $In_{0.9}Al_{0.1}As_{0.9}Sb_{0.1}$ grade and an undoped $In_{0.79}Al_{0.21}As_{0.79}Sb_{0.21}$ channel. The GaSb resonant state is placed immediately below the source valence band and the InAs resonant state immediately above the channel conduction band to maximize I_{ON}. In ballistic simulations, the on-state tunneling probability is >50% over the conduction window between the source Fermi level and the conduction-band edge (Fig. 3); the GaSb/InAs TFET shows ~1% tunneling probability. At V_{DD}=0.18V, the 3HJ-TFET shows ~270A/m I_{ON}, while the GaSb/InAs TFET shows ~8A/m I_{ON}. While the 3HJ-TFET surpasses the GaSb/InAs TFET in 300mV operation [5], the advantage is more pronounced at V_{DD}= 0.18V, where the 3HJ-TFET has a 1.8nm tunneling distance, compared to 5nm for the GaSb/InAs TFET.

Similar high-I_{ON} P-channel 3HJ-TFET designs are feasible [11], as are designs using (InAs/InP) channel materials having low semiconductor-dielectric interface trap density [12].

III. Low I_{OFF}

Although the resonant states associated with the source and channel HJ (Fig. 4a) are well separated in energy, they may increase I_{OFF} through phonon scattering. To explore this, we modeled acoustic and optical phonon scattering using the self-consistent Born approximation [11] method with 30meV phonon energy and the optical deformation potential varied from 0-220meV/nm, the latter corresponding to μ=1.1x10^5 cm^{2}V^{-1}s^{-1}. For a device with 30nm L_g, almost free from source-drain (S/D) tunneling, increasing the phonon scattering strength increases I_{OFF} (Fig. 5b) and degrades the *SS* (Fig. 5a, c). With

fixed I_{OFF}=10^{-3}A/m and V_{DD}=0.3V, I_{ON} at V_{DD}=0.3V degraded from 780A/m to 540A/m using a 220meV/nm deformation potential constant. At 15nm L_g, below 10^{-1} A/m, I_{OFF} is dominated by S/D tunneling [12], as in this bias range the energy separation between the resonant states (Fig. 7a) is too large for phonon scattering to dominate. For I_{OFF} between 10^{-1}A/m to 10^{2}A/m, I_{OFF} is dominated by phonon scattering (Fig. 7b), as the resonant states become closer in energy as V_{GS} increases. I_{OFF} from S/D tunneling dominates over phonon scattering for 3HJ-TFETs at <15nm L_g.

IV. Logic Gate Noise Margin

Noise margin refers not to thermal fluctuations but to the margin between the gate output logic levels and the allowable input voltage levels for the cascaded gate; this margin accommodates FET and supply variations and electromagnetic interference. High noise margin requires high inverter voltage gain at the V_{GS}=V_{DS}=V_{DD}/2 logic switching point (SP), implying a large ratio of transconductance $g_m = \partial I_D / \partial V_{GS}$ to output conductance $G_{DS} = \partial I_D / \partial V_{DS}$. Fig. 8 shows 3HJ-TFET common-source characteristics, from which (Fig. 9) the TFET inverter V_{in}-V_{out} characteristics are computed. At V_{DD}=0.18V, at the logic switching point, V_{DS} is below that necessary to saturate the drain current, giving large G_{DS} (Fig. 8) and low inverter voltage gain and noise margin (Fig. 9). At V_{DD}=0.12V (Fig. 8), at the switching point, the TFETs operate even further below saturation. By increasing (fig. 10) the TFET V_{th} by 0.02V, the switching point shifts (SP2), and the TFET operates with V_{DS} at the threshold of saturation. The inverter V_{in}-V_{out} characteristics (fig. 11) show increased noise margin even with V_{DD} as low as 0.08V. Under this shift in bias, the (ballistic) I_{ON} is decreased from (106A/m at V_{DD}=0.08V, 195A/m at 0.12V, 301A/m at 0.18V) to (60A/m at 0.08V, 155A/m at 0.12V, 265A/m at 0.18V). The increased V_{th}, of course, also decreases I_{OFF}, partially offsetting any increase in I_{OFF} from scattering.

The output conductance results from the drain electron energy distribution. Focusing on V_{DD}=0.18V, at SP1 (Fig. 12a), the switching point with V_{th} set to give 10^{-3} A/m I_{OFF}, the drain Fermi level lies only 24meV below the conduction-band energy. *Even at zero Kelvin*, reducing V_{DS} by more than 24mV causes reverse electron transport from drain to source, causing the observed $\partial I_D / \partial V_{DS}$; at 300K the output conductance is made yet worse by the drain thermal distribution. In contrast, at SP2 (Fig. 12b), V_{th} has been increased by 0.02V, increasing the channel conduction-band energy. At the V_{GS}=V_{DS}=V_{DD}/2=0.09V switching point (SP2) the drain Fermi level lies 40meV above the conduction-band energy. G_{DS} , and the logic gate voltage gain and noise margin, are thus improved. While V_{DS} switches between 0V and V_{DD}, modulation of the channel potential by V_{GS} is smaller because of the gate oxide. Further, V_{GS}, V_{DS}, and V_{th} are all very low. These effects, present in both TFETs and 3HJ-TFETs, together bring the drain potential close to that of the channel, with consequent loss of saturation.

V. Conclusions

We have proposed a device technology providing high simulated on-currents at 0.12-0.18V supply voltages. CV_{DD}^2 switching energy is greatly reduced, and, with high I_{ON}, the CV_{DD} / I_{ON} gate delay will be much smaller than GaSb/InAs TFETs. Simulations suggest that phonon scattering will not catastrophically degrade the 3HJ-TFET. Both subthreshold swing and noise margin determine the minimum V_{DD}.

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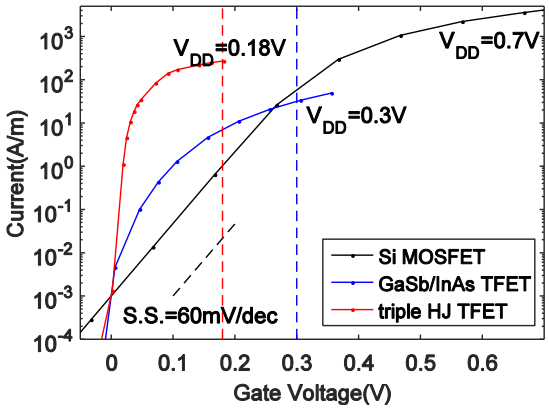

Fig. 1: I_D-V_{GS} transfer characteristics, from ballistic simulations, of a Si MOSFET, a GaSb/InAs TFET and triple HJ TFET. All devices have double gates, a 1.8nm thick channel, a 2.56nm thick gate dielectric with ε_R=9, and 30nm gate length.

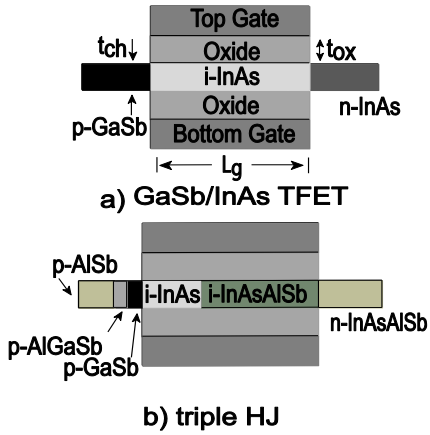

Fig. 2: Cross-sectional schematics of (a) a conventional single-heterojunction (HJ) GaSb/InAs TFET and, (b) a triple-HJ TFET. Both have planar channels and double gates (e.g. are finFETs).

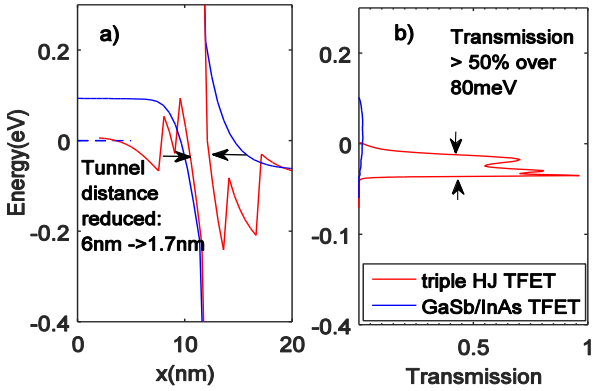

Fig. 3: Band diagram (a) and transmission probability (b) of a (110)-confined GaSb/InAs TFET and a triple-HJ TFET with step-graded source and channel heterojunctions. V_{GS}=V_{DS}=V_{DD}=0.18V. Transport is along [110]. The triple-HJ TFET shows 50% transmission probability over the full conduction window between the source Fermi energy and channel conduction-band energy.

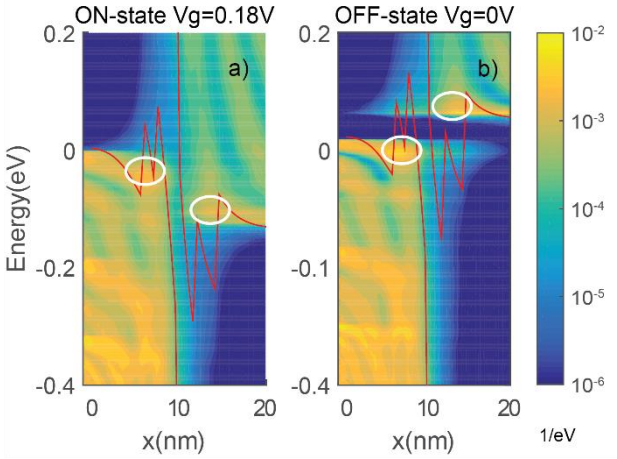

Fig. 4: Ballistic local density of states in ON-state (a) and OFF-state bias (b) of a (110)-confined triple-HJ TFET. Resonant states are circled. While the two resonant states are clearly separated in ballistic simulations, inelastic scattering will increase I_{OFF} due to coupling between two states.

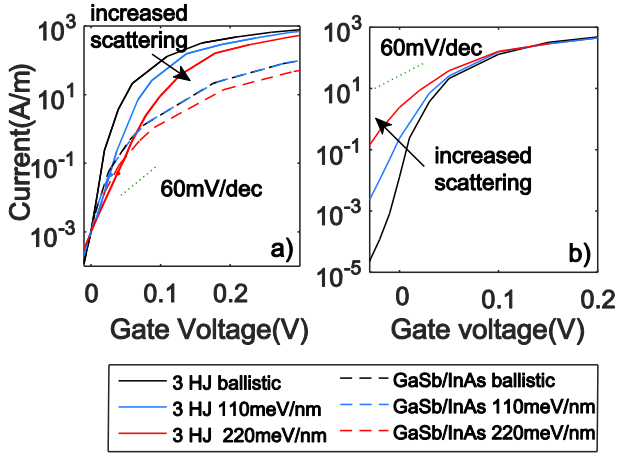

Fig. 5: I_D-V_{GS} transfer characteristics for triple HJ and GaSb/InAs TFETs of L_g=30nm as a function of inelastic phonon scattering strength. In (a), V_{th} for each curve is shifted to set I_{OFF}=10^{-3}A/m, while in (b) V_{th} is held constant.

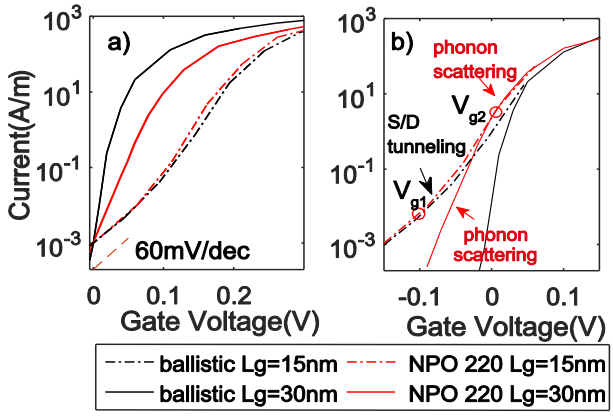

Fig. 6: I_D-V_{GS} transfer characteristics, at 15nm and 30nm L_g, for triple HJ TFETs, simulated with zero and with 220 meV/nm inelastic phonon scattering strength. In (a), V_{th} for each curve is shifted to set I_{OFF}=10^{-3}A/m, while in (b) V_{th} is held constant to facilitate comparison of leakage mechanisms.

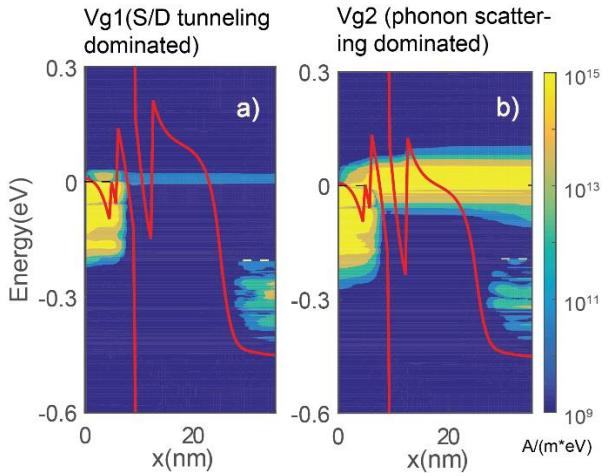

Fig. 7: Energy-resolved current density, simulated at zero transverse wave vector k_t and with a 220meV/nm deformation potential constant, for a 15nm L_g triple HJ TFET. The bias conditions (a) V_{g1} and (b) V_{g2} are those indicated in Fig. 6(b)

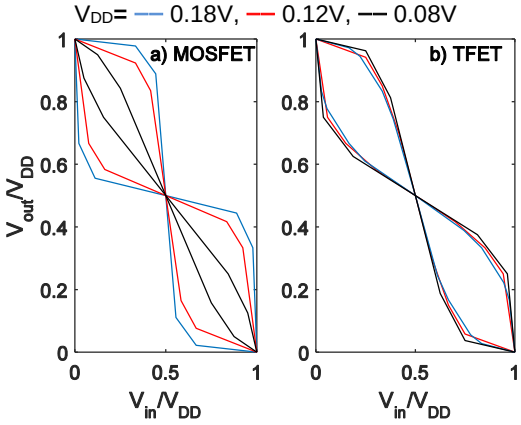

Fig. 9: Simulated V_{in}-V_{out} voltage transfer characteristics, as a function of supply voltage, of CMOS inverters using (a) standard Si MOSFETs and (b) triple HJ TFETs.

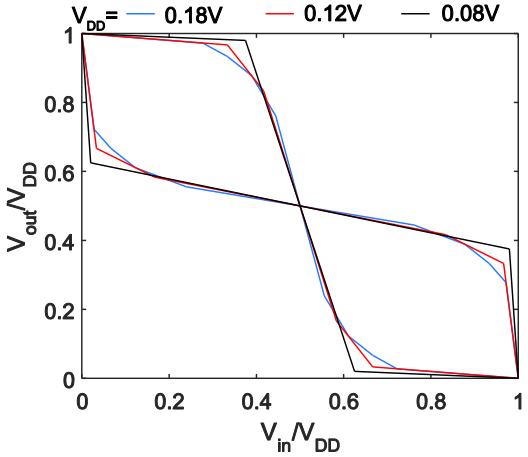

Fig. 11: Simulated V_{in}-V_{out} voltage transfer characteristics, as a function of supply voltage, of CMOS inverters using triple HJ TFETs, but with V_{th} increased 0.02V beyond that necessary to set I_{OFF} to 10^{-3}A/m. The V_{th} shift increases the noise margin, but decreases both I_{OFF} and I_{ON} .

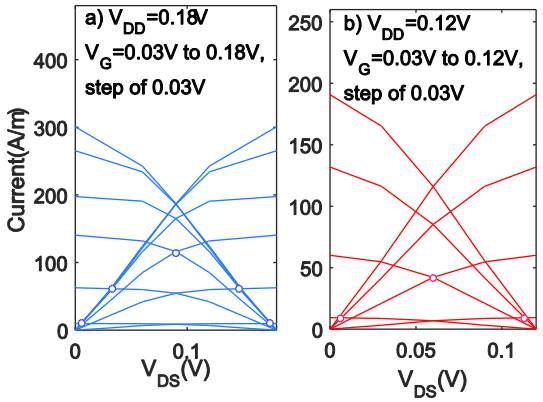

Fig. 8: Output characteristics for V_{DD}=0.18V (a) and (b) 0.12V, assuming pTFET characteristics symmetric to the nTFET. V_{th} is adjusted to set I_{OFF} to 10^{-3}A/m. At V_{DD} =0.18V, the FETs are closer to current saturation at the V_{GS}=V_{DS}=V_{DD}/2 switching point. The inverter voltage gain is consequently larger.

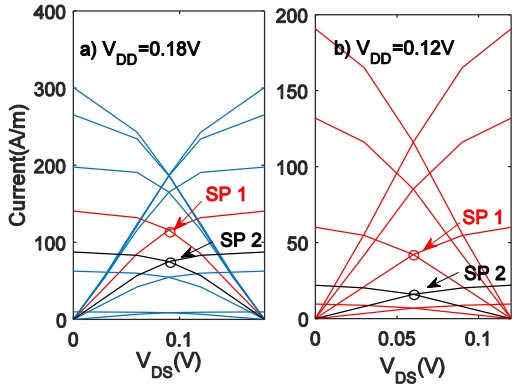

Fig. 10: Output characteristics, at V_{DD}=0.18V (a), with V_{GS} varying between 0.03V and 0.09V in 0.03V increments (without SP2) . SP1 indicates the V_{GS}=V_{DS}= V_{DD}/2 logic switching point. Increasing V_{th} by 0.02V moves the switching point to SP2, improving the current saturation at the switching point and thereby increasing the voltage gain. (b) shows a similar analysis at V_{DD}=0.12V.

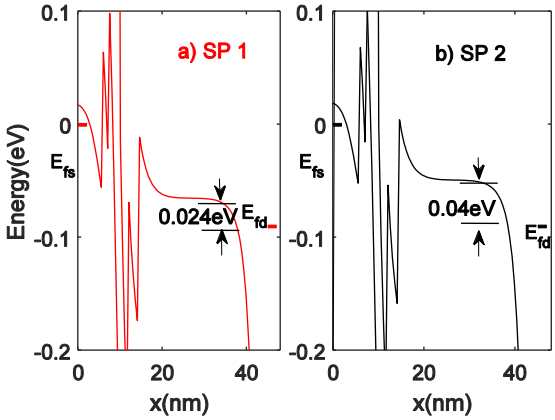

Fig. 12: Band diagram, for V_{DD}=0.18V, at the V_{GS}=V_{DS}= V_{DD}/2 switching point for (a) SP1 and (b) SP 2, bias conditions indicated in Fig. 10(a). The source E_{fs} and drain E_{fd} Fermi levels are indicated. Increasing V_{th} (SP2 vs. SP1) increases the separation between the channel conduction-band energy and E_{fd}. The TFET output conductance is decreased, and the inverter voltage gain and noise margin are thereby increased.