A Tunnel FET Design for High-Current, 120 mV Operation

P. Long, J. Z. Huang, M. Povolotskyi, J. Charles, T. Kubis, G. Klimeck, ***Purdue University***

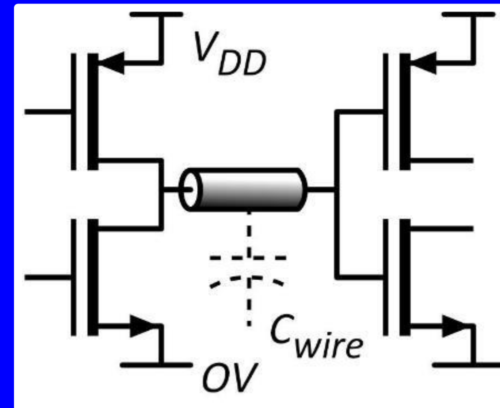
D. Verreck, **Imec, KU Leuven**

M. J.W. Rodwell, **University of California, Santa Barbara**

B. H. Calhoun, **University of Virginia, Charlottesville**

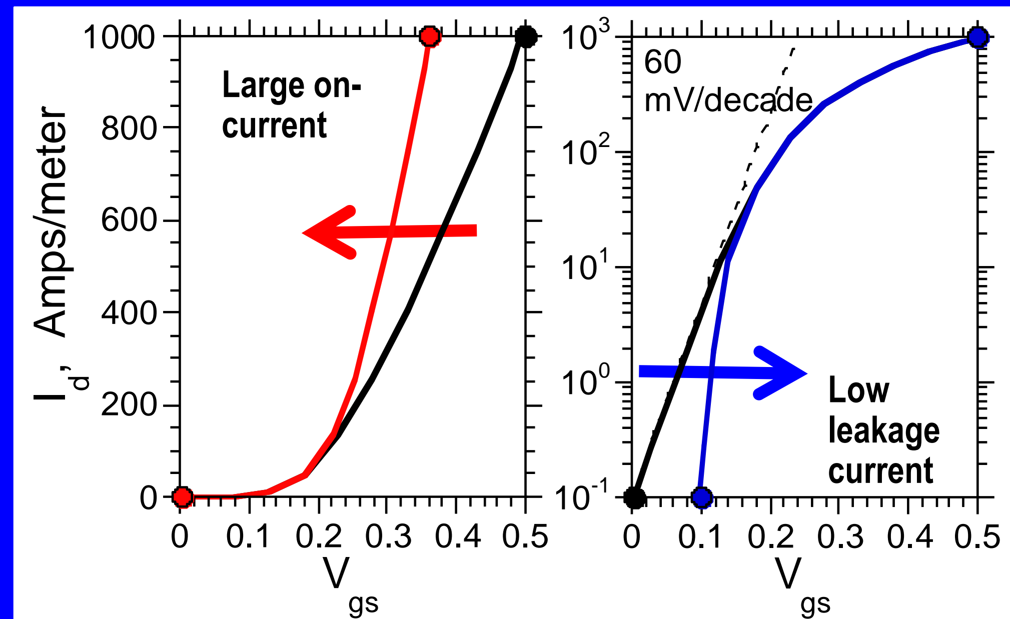
What does VLSI need ?

Low voltage
low switching energy $CV_{DD}^2/2$.



Large on-current
small delay CV_{DD}/I .

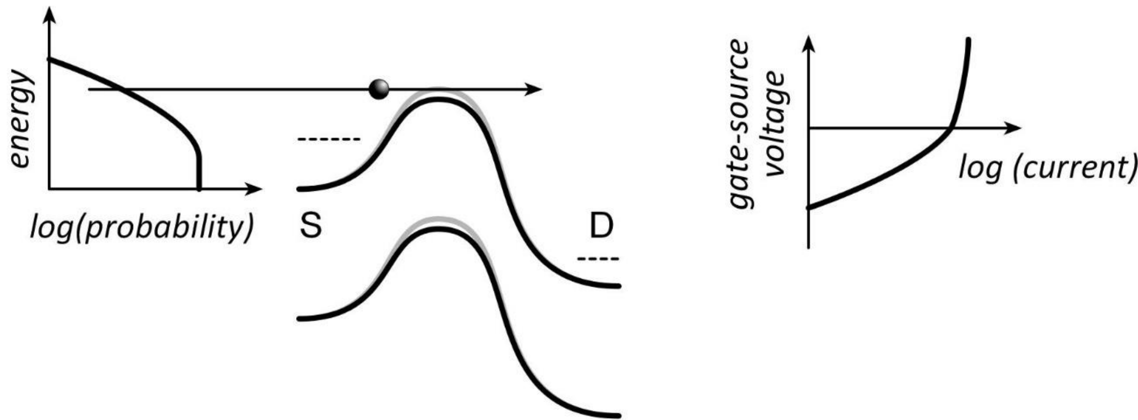
Low leakage current
thermal: $I_{off} \propto \exp(-qV_{DD}/kT)$
want low V_{DD} yet low I_{off} .



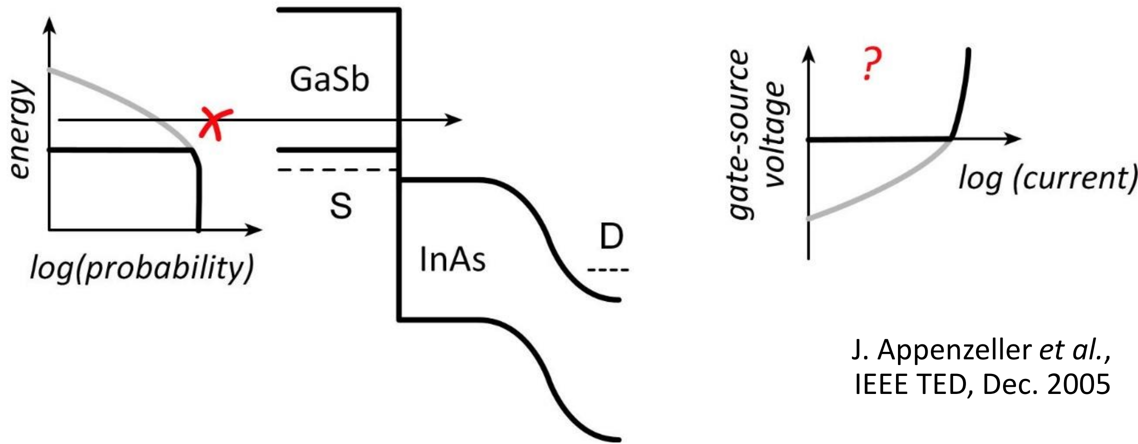
Want:
low supply voltage
→ Steeper than 60mV/dec below threshold
→ Large *dI/dV* above threshold

Tunnel FETs: truncating the thermal distribution

MOSFET



T-FET

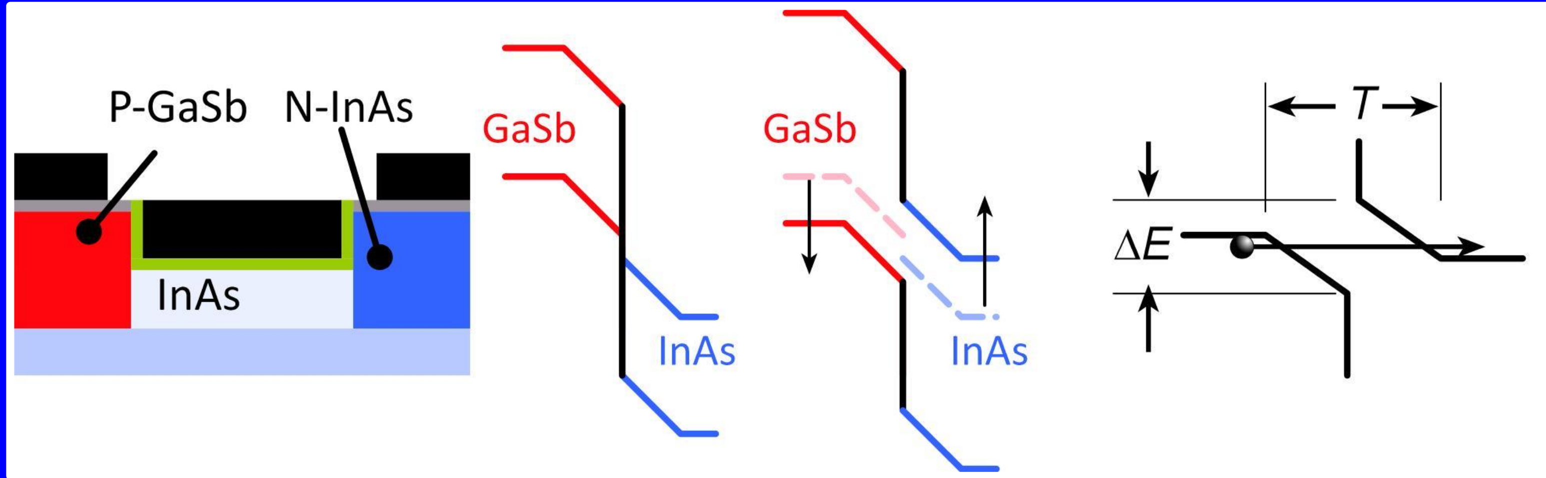


Source bandgap truncates thermal distribution→ steep S.S. ✓

Must cross bandgap: tunneling→ low I_{ON} ✗

Fix (??): GaSb/InAs broken-gap heterojunction

Tunnel FETs: are prospects good ?



Useful devices must be small: short gate→ thin channel

Quantization shifts band edges→ tunnel barrier

Confinement also increases effective masses

Transmission $\cong exp(-2\alpha T_{barrier})$**, where** $\alpha \cong \frac{(2m^* E_{barrier})^{1/2}}{\hbar}$

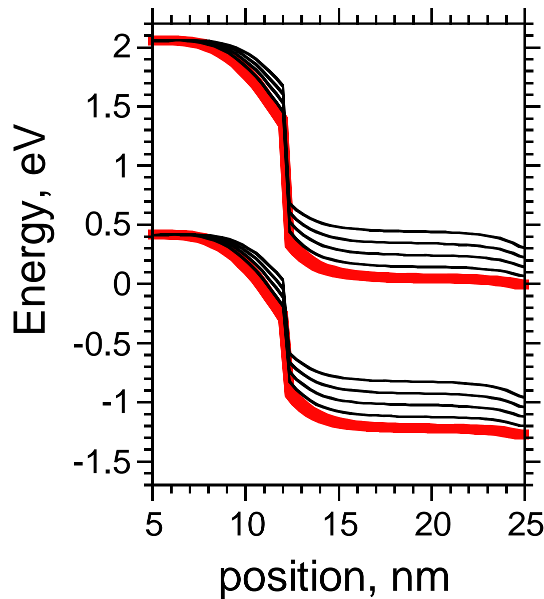
~10% for a 2nm barrier, 1% for a 4nm barrier

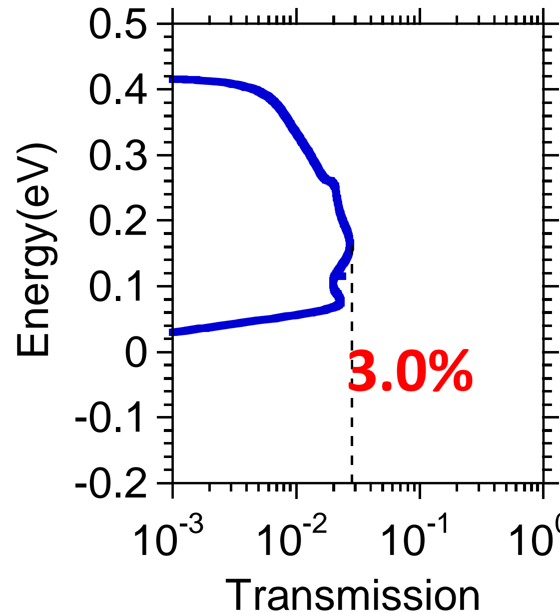
What actual on-current might we expect ?

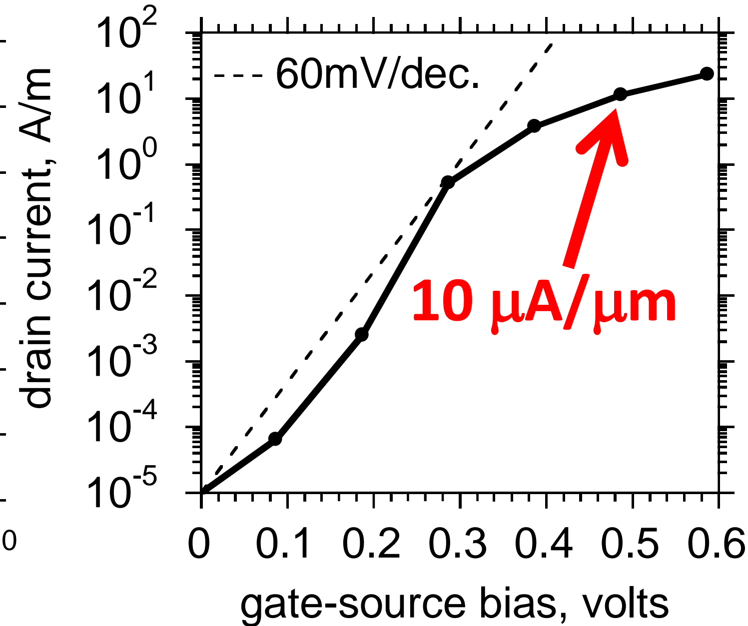
T-FET on-currents are low, T-FET logic is slow

NEMO simulation:

GaSb/InAs tunnel finFET: 2nm thick body, 1nm thick dielectric @ ε_r=12, 12nm L_g

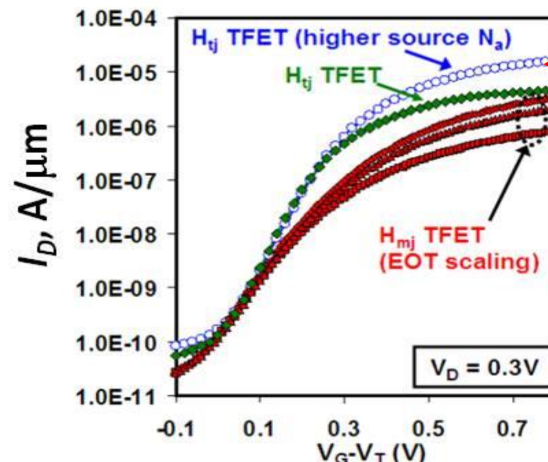






Experimental:

InGaAs heterojunction HFET;
Dewey et al,
2011 IEDM,
2012 VLSI Symp.



~15 μA/μm @0.7V

Low current → slow logic

How to increase on-current?

Increasing the on-current

$\text{Trick \#1: (110) confinement, } [1\bar{1}0] \text{ transport}$ P. Long *et al.*, EDL 3/2016

Reduces tunnel barrier height

Reduces hole mass

$\text{Trick \#2: channel heterojunction}$ P. Long *et al.*, EDL 3/2016

Reduces tunnel barrier thickness

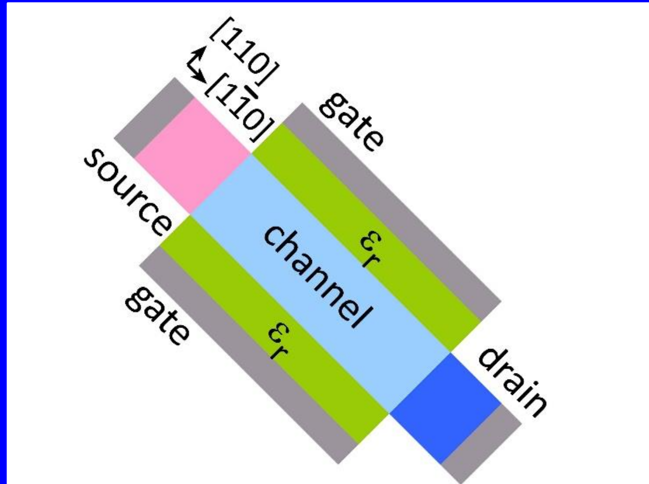
Adds resonant state Avci & Young, (Intel) 2013 IEDM

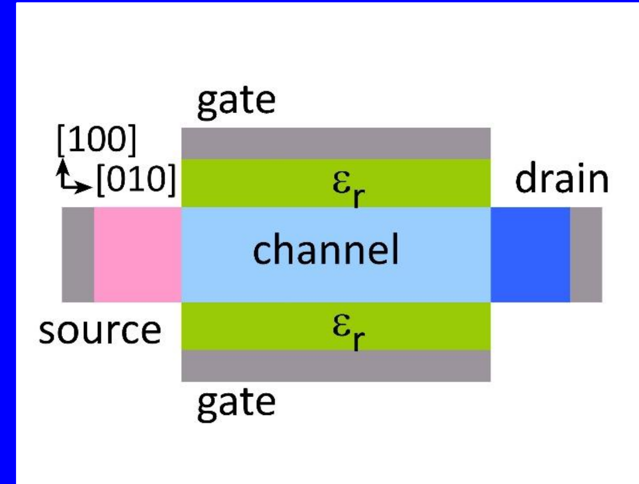
$\text{Trick \#3: source heterojunction}$ S. Brocard, *et al.*, EDL, 2/2014

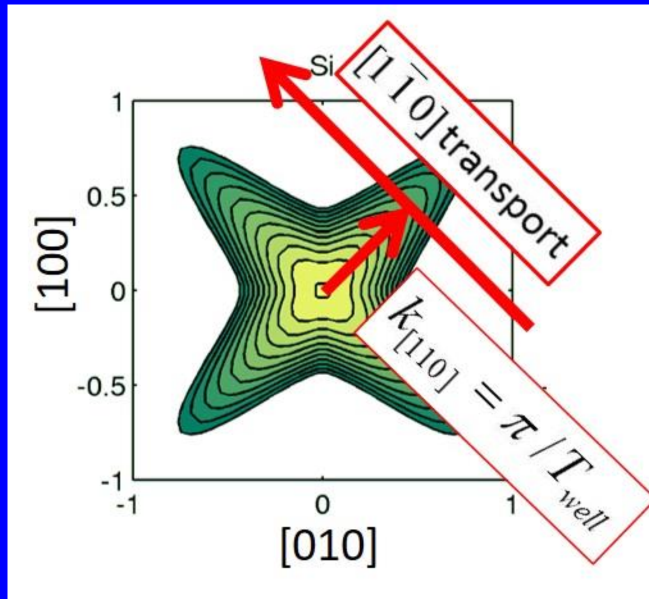
Reduces tunnel barrier thickness

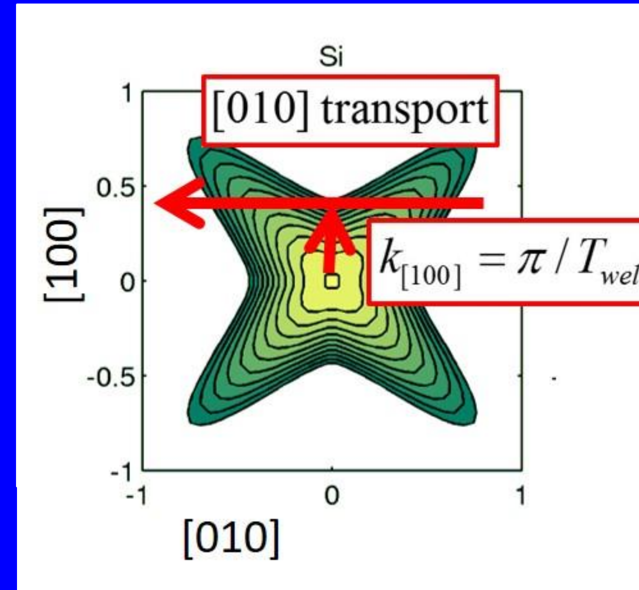
Adds resonant state

[110] gives more on-current than [100]







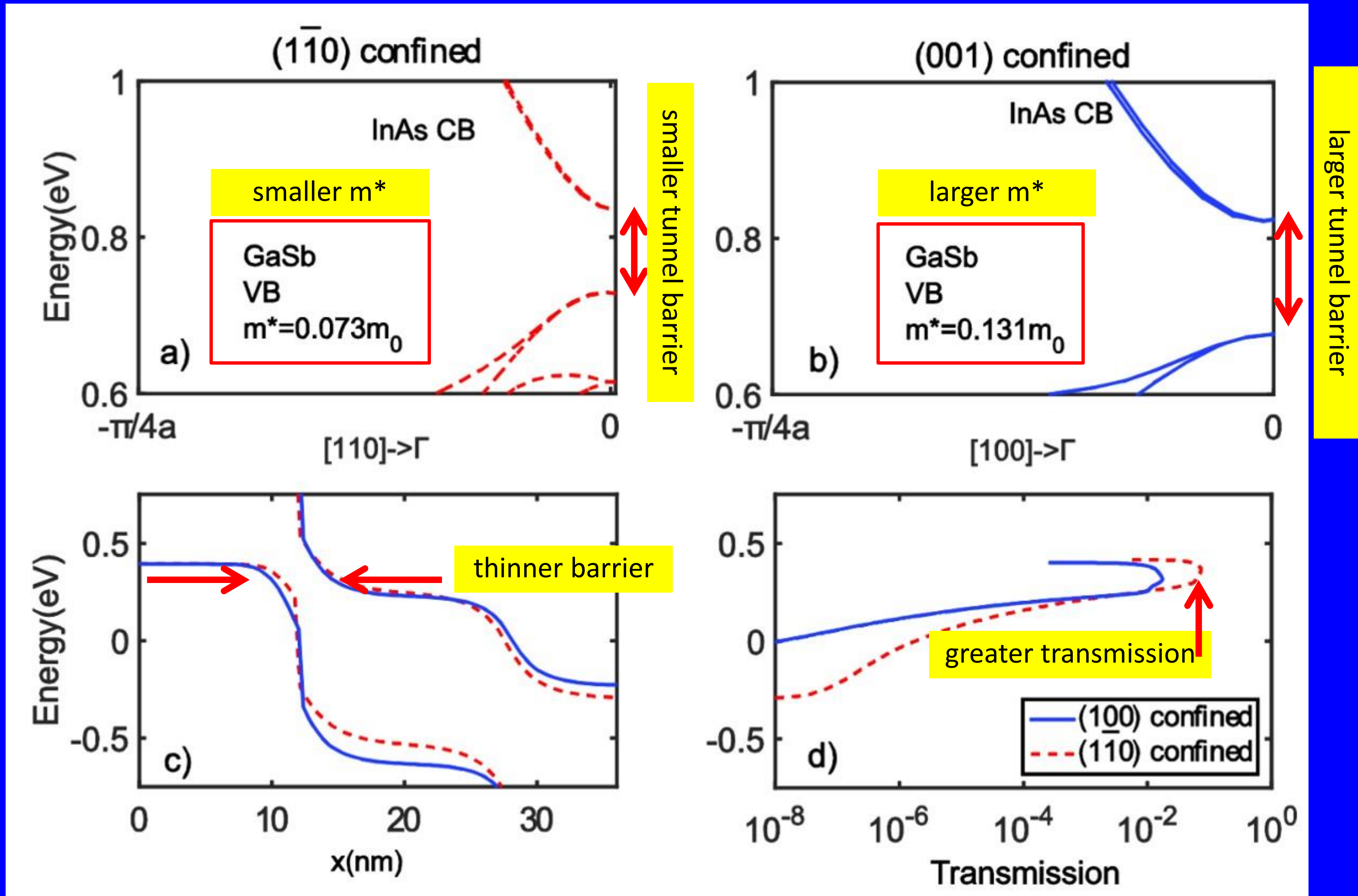


Valence Band

high confinement mass
low transport mass

low confinement mass
high transport mass

[110] gives more on-current than [100]



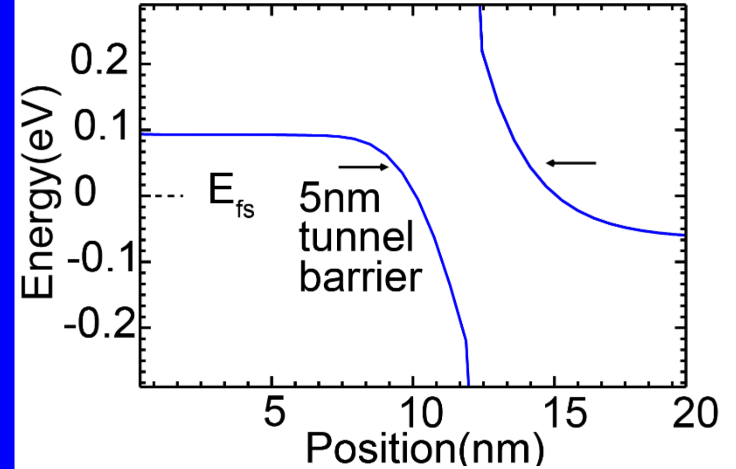
larger hole confinement mass→ smaller barrier→ more current
smaller hole transport mass→ more current

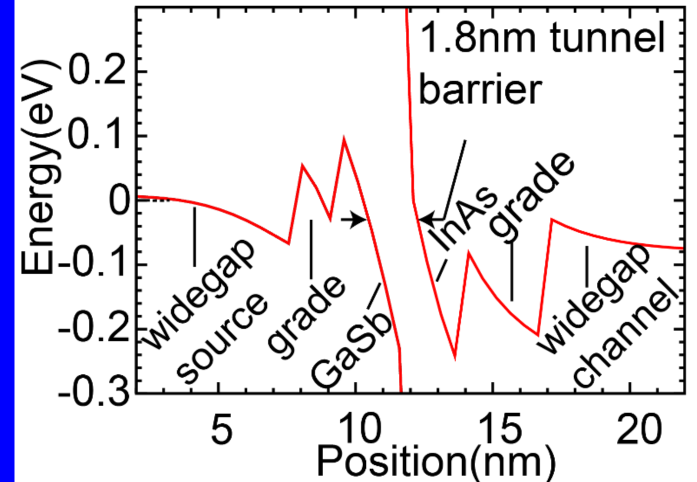
Heterojunctions increase the junction field

Source heterojunction: S. Brocard, *et al*., EDL, 2/2014; Channel heterojunction: P. Long *et al*., EDL 3/2016

P+ GaSb
InAs channel
N+ drain
ε_r
ε_r
[001]
[010]
gates
TFET

P+ widegap source
GaSb
InAs
widegap channel
grades
[011]
[01$\bar{1}$]
Triple-HJ TFET





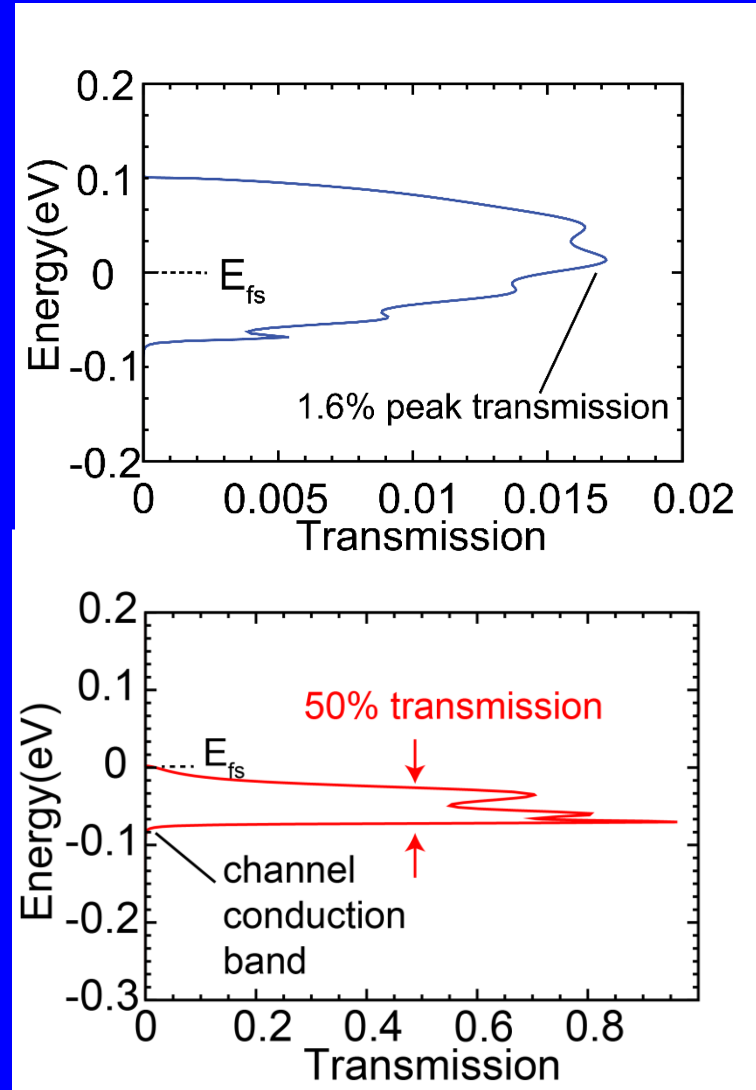
Added heterojunctions→ greater built-in potential→greater field→ thinner barrier

Heterojunctions increase the tunneling probability

Source heterojunction: S. Brocard, *et al*., EDL, 2/2014; Channel heterojunction: P. Long *et al*., EDL 3/2016

P+ GaSb
InAs channel
N+ drain
ε_r
ε_r
[001]
[010]
gates
TFET

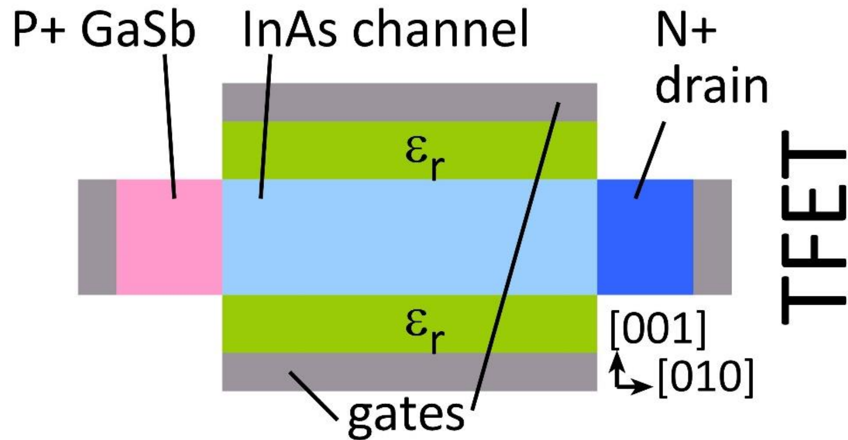
P+ widegap source
GaSb
InAs
widegap channel
grades
[011]
[01$\bar{1}$]
Triple-HJ TFET

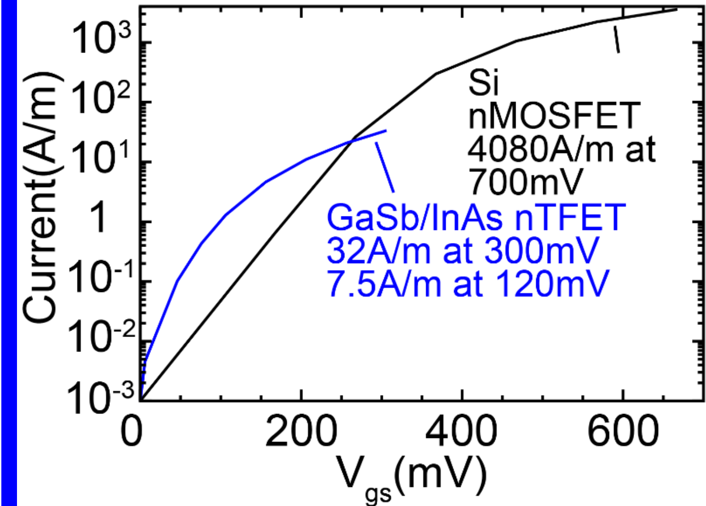


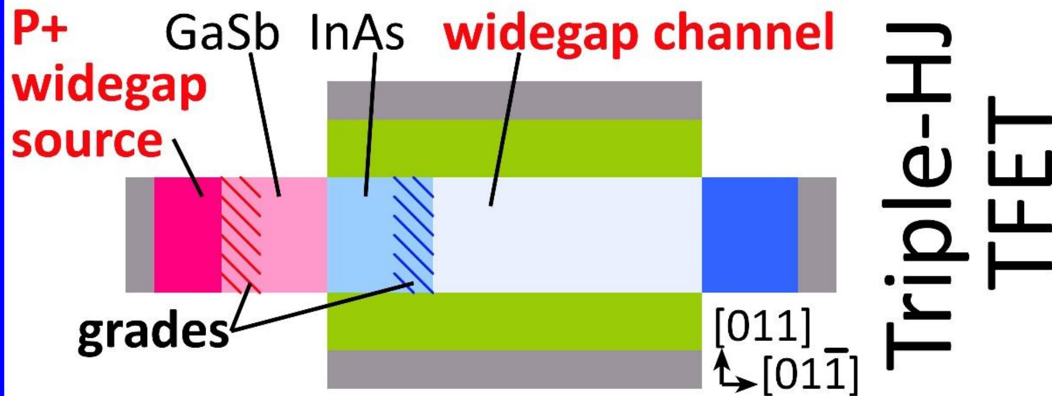
Added heterojunctions→ greater built-in potential→greater field→ thinner barrier

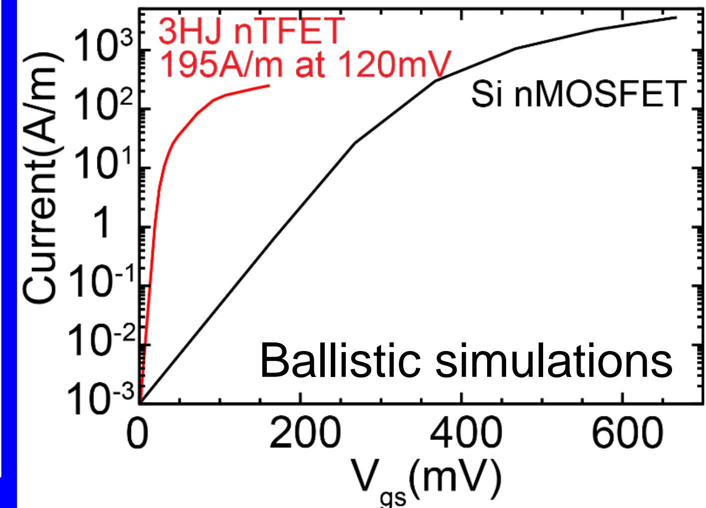
Heterojunctions increase the on-current

Source heterojunction: S. Brocard, *et al*., EDL, 2/2014; Channel heterojunction: P. Long *et al*., EDL 3/2016





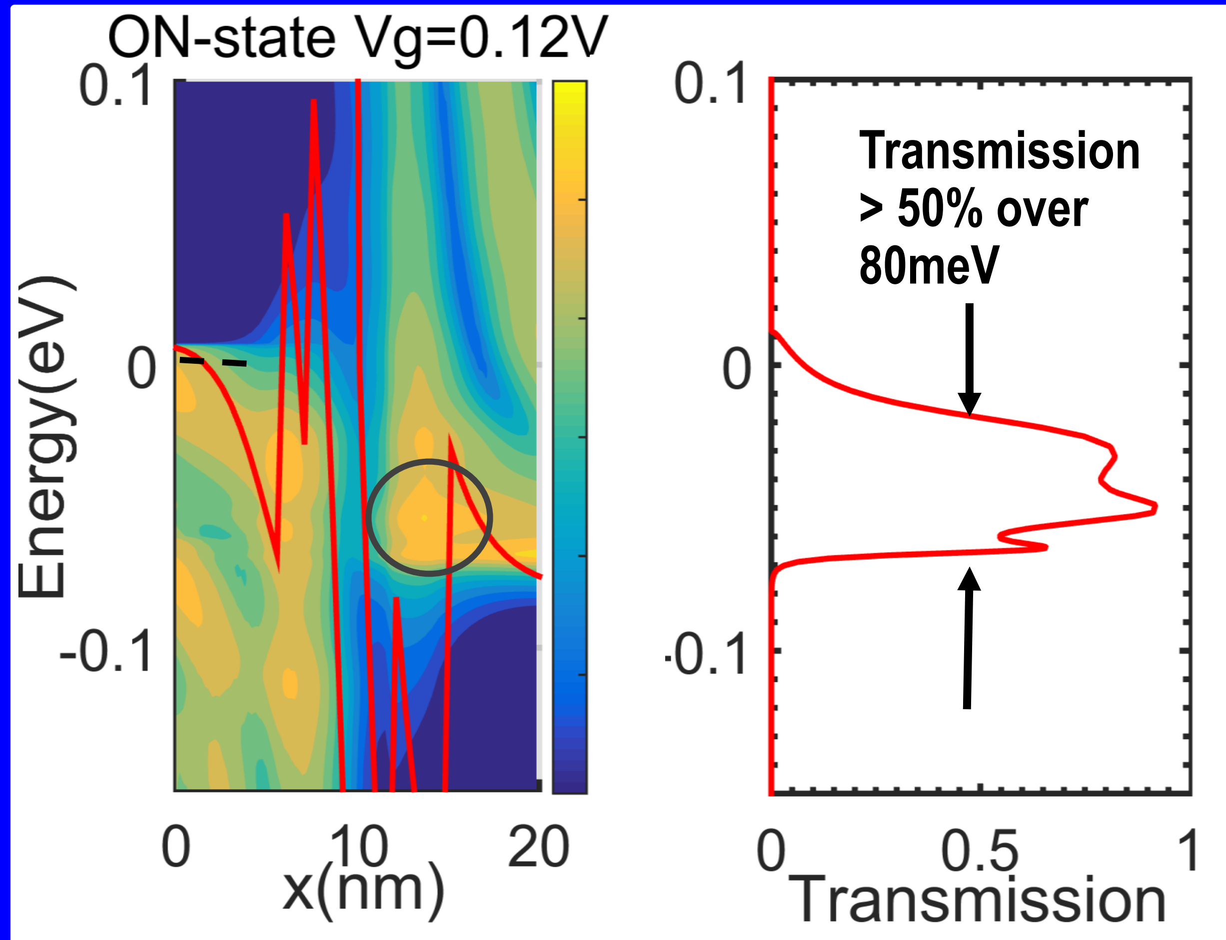




Added heterojunctions→ greater built-in potential→greater field→ thinner barrier

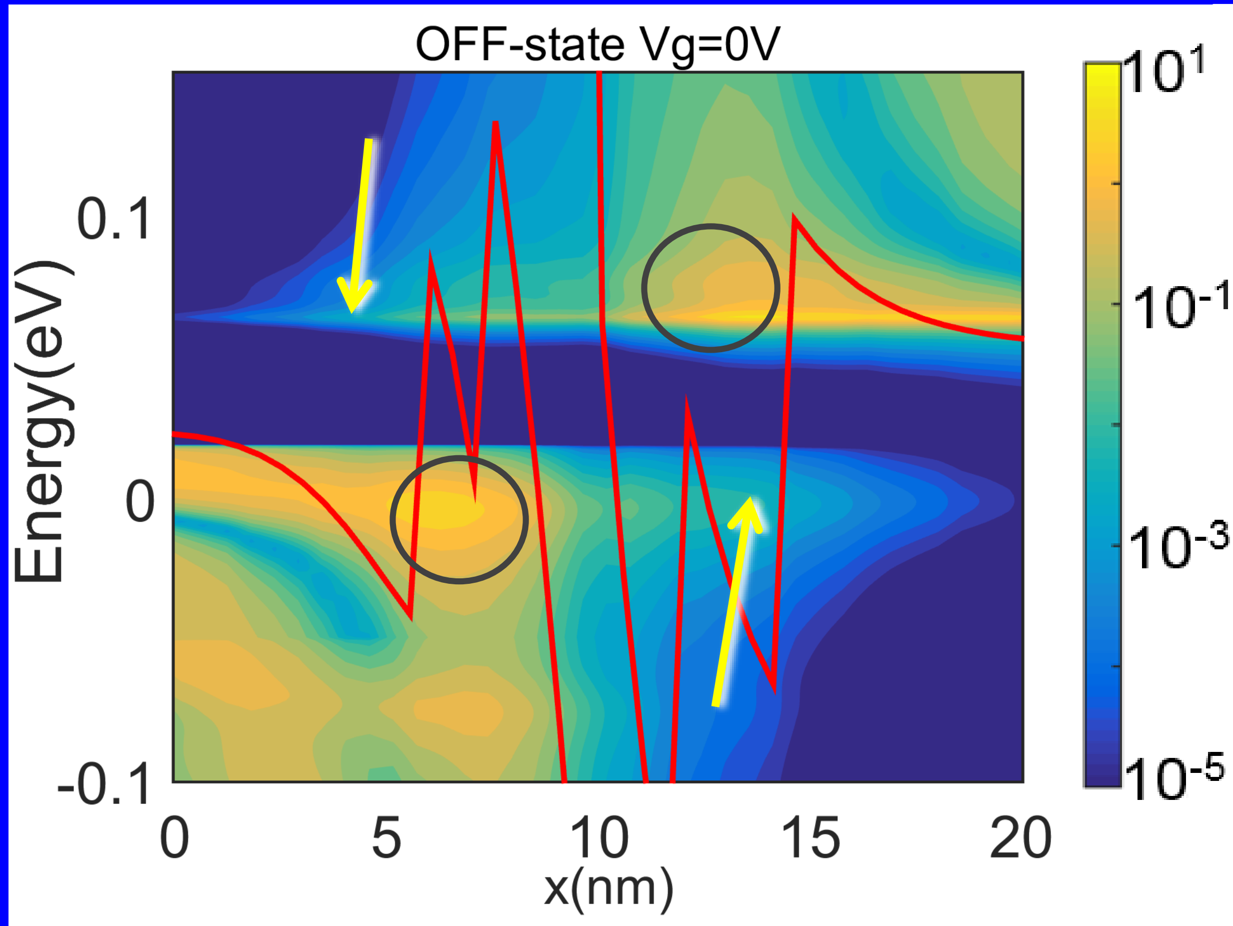
Role of the resonant bound states: ON-state

local density of states, 1/eV



On-state: bound states increase transmission

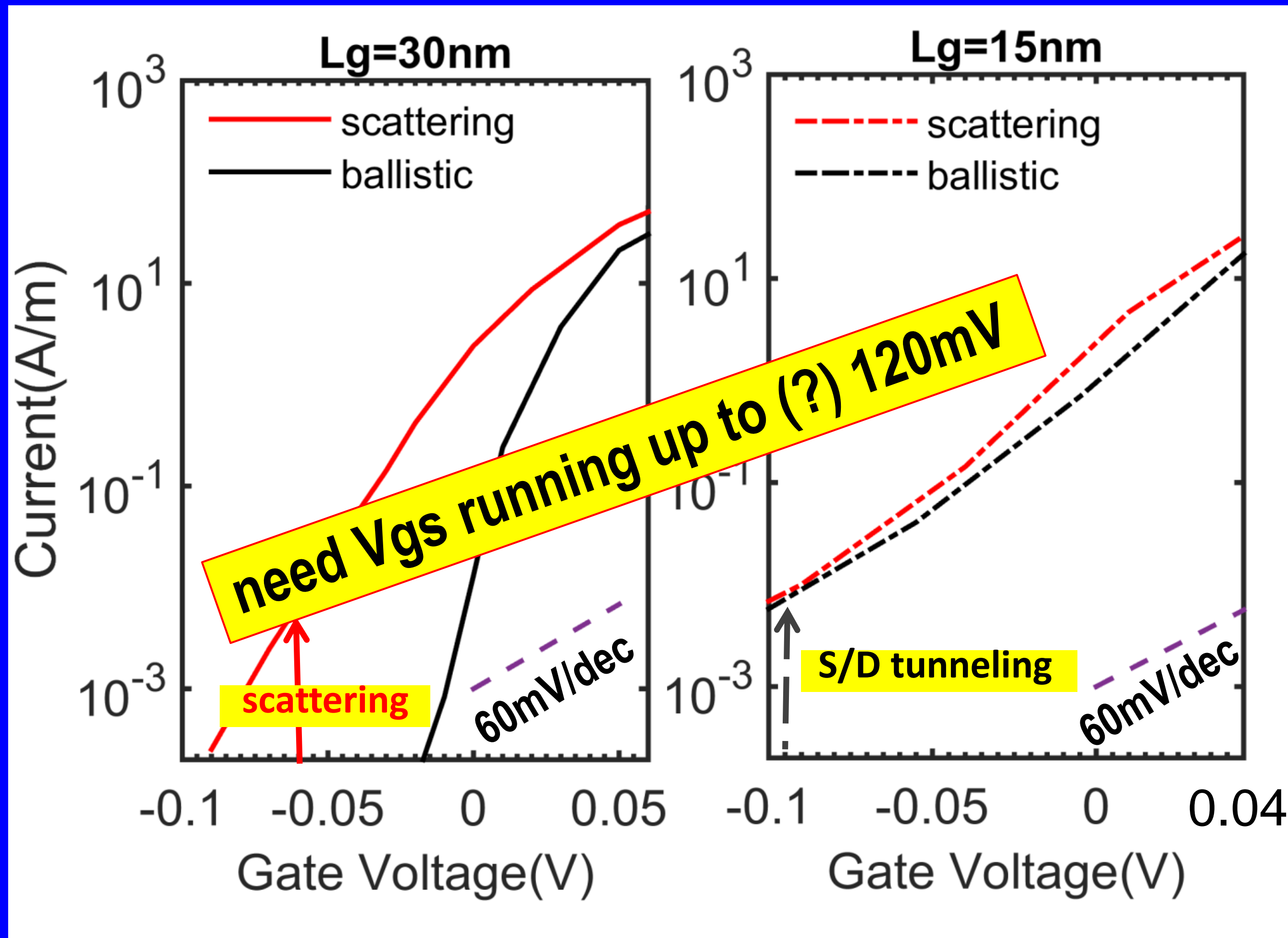
Role of the resonant bound states: OFF-state



- **Phonon scattering:**
  - ***Off-sate: evanescent tails of bound states → leakage between two states → Keep the bound state energies near the well edge energies***

L_g=30nm: I_{off} limited by scattering

L_g=15nm: I_{off} limited by S/D tunneling



At 30nm L_g, V_{DD} must be increased ~0.07V to maintain on/off ratio

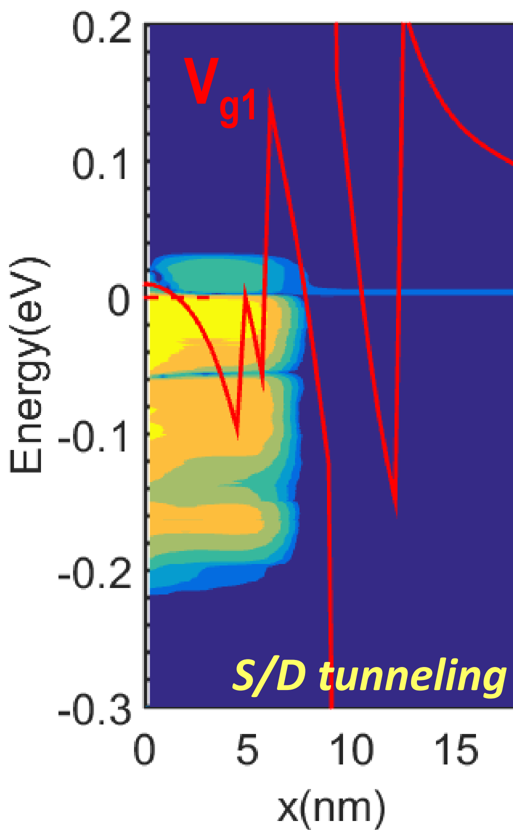
At 15nm L_g, on/off ratio limited by S/D tunneling

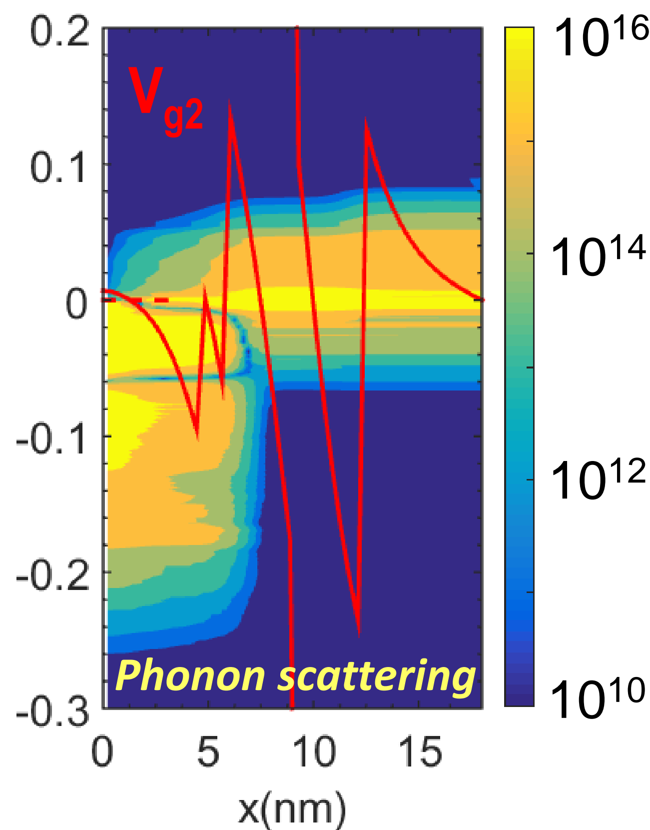
Simulations use 220meV/nm optical deformation constant , consistent with μ=1.1x10^5 cm^{2}V^{-1}s^{-1}.

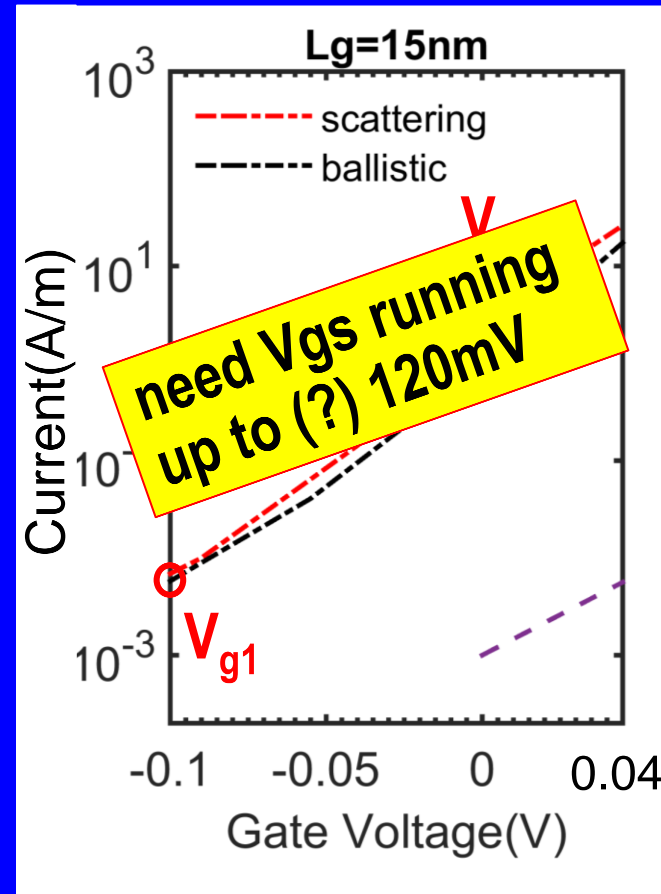
Leakage at L_g=15nm

Local current density

(absolute value of current)



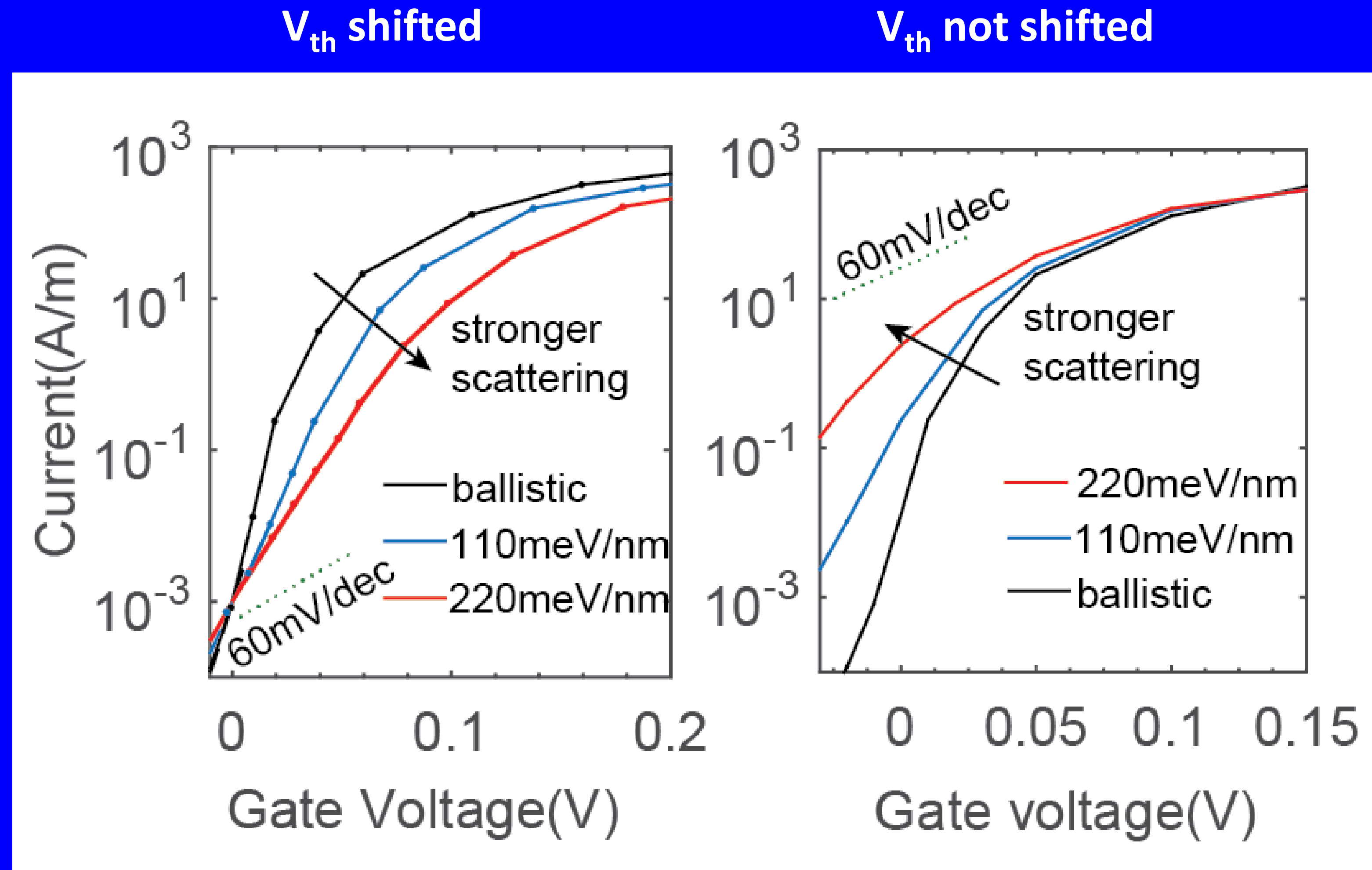




V_{g1} (close to off): current limited by S/D tunneling

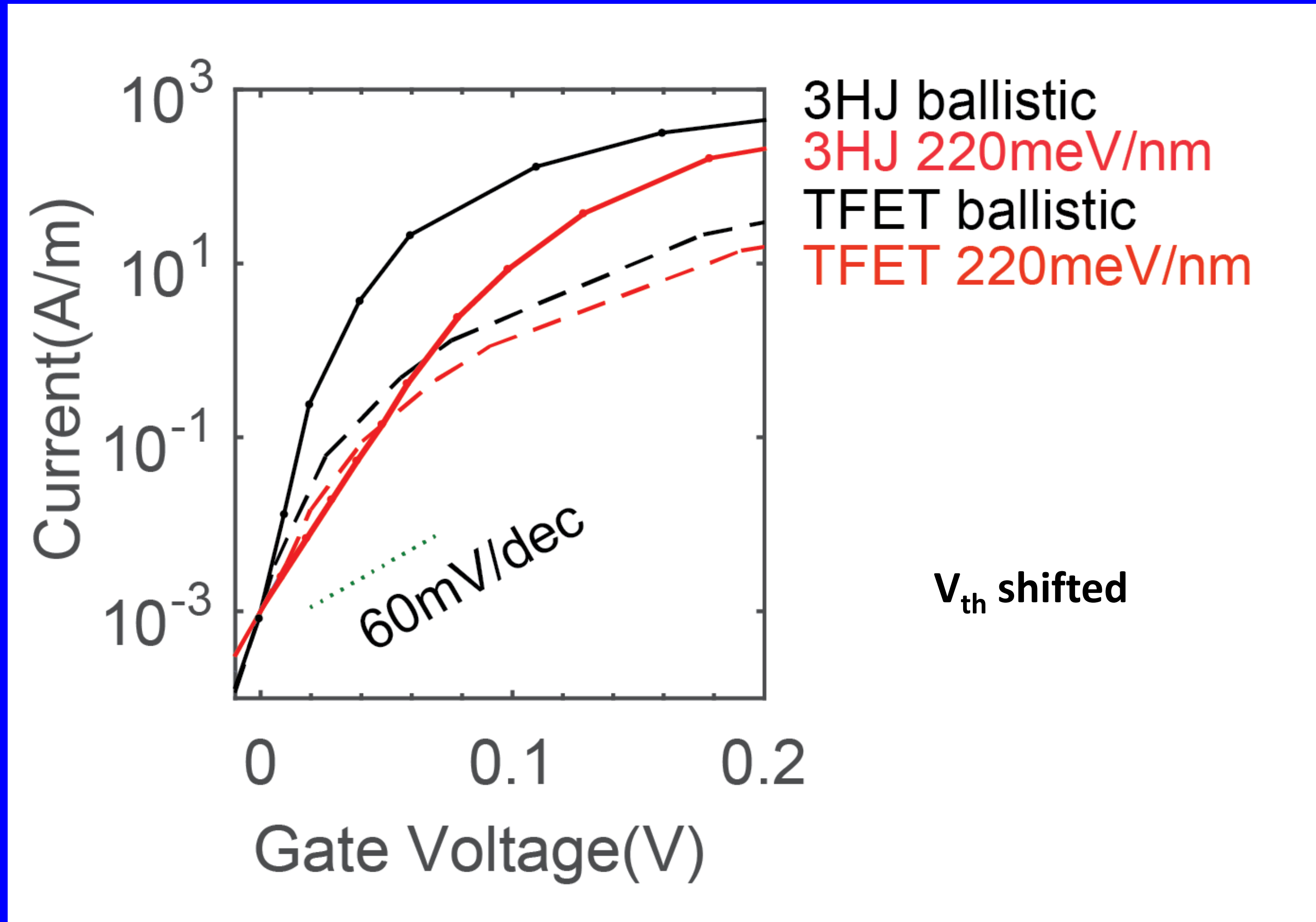
V_{g2}: current limited by phonon scattering

Phonon-Assisted Tunneling: 3HJ-TFET



S.S. and I_{off} increased with intensity of phonon scattering

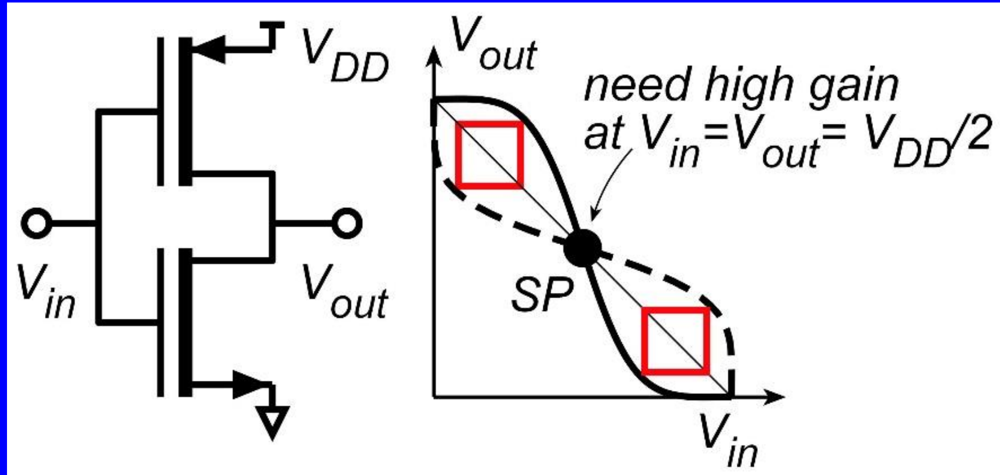
Phonon-Assisted Tunneling: TFET vs. 3HJ-TFET



Even with P.A.T., 3HJ design provides much larger I_{ON} than TFET

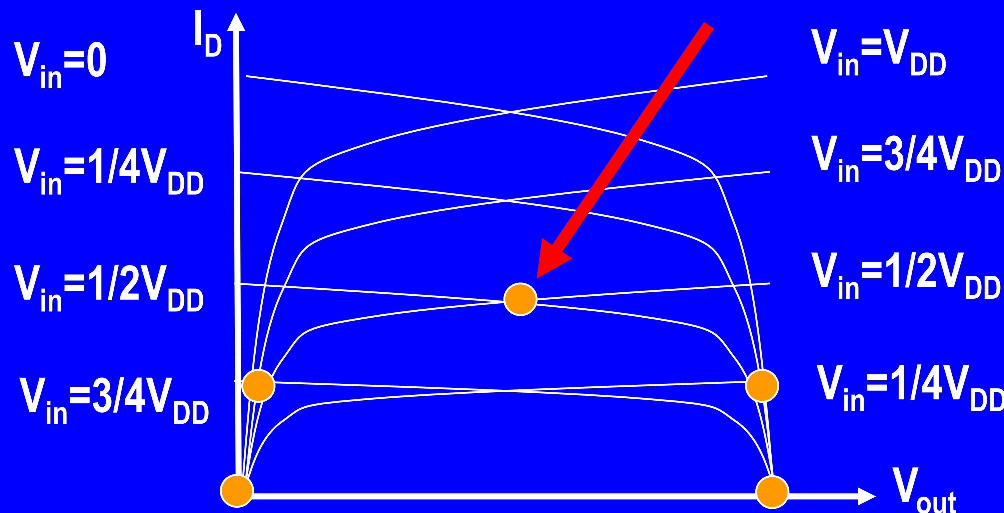
Noise margin sets a minimum threshold voltage

Need high voltage gain dV_{out}/dV_{in} at switching point



$$Gain = dV_{out}/dV_{in} = \frac{dI_D/dV_{GS}}{dI_D/dV_{DS}}$$

→ *FET I_D-V_{DS} curve should be saturated (flat) at the switching point*



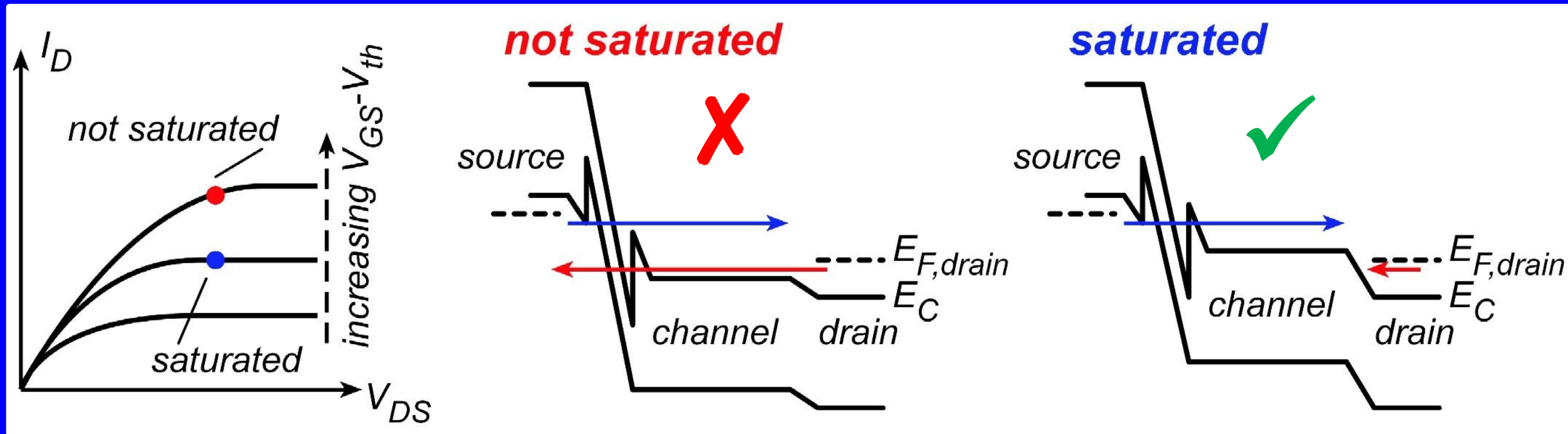
$E_{F,drain}$ should be below E_c at switching point

Need low output conductance when biased at switching point

output conductance: from drain-source reverse injection

to avoid : need drain Fermi level below channel conduction band

must decrease (V_{gs}-V_{th}) → increase V_{th}



Increasing the threshold voltage:

Improves the noise margin

Reduces I_{ON}. Also reduces I_{OFF}

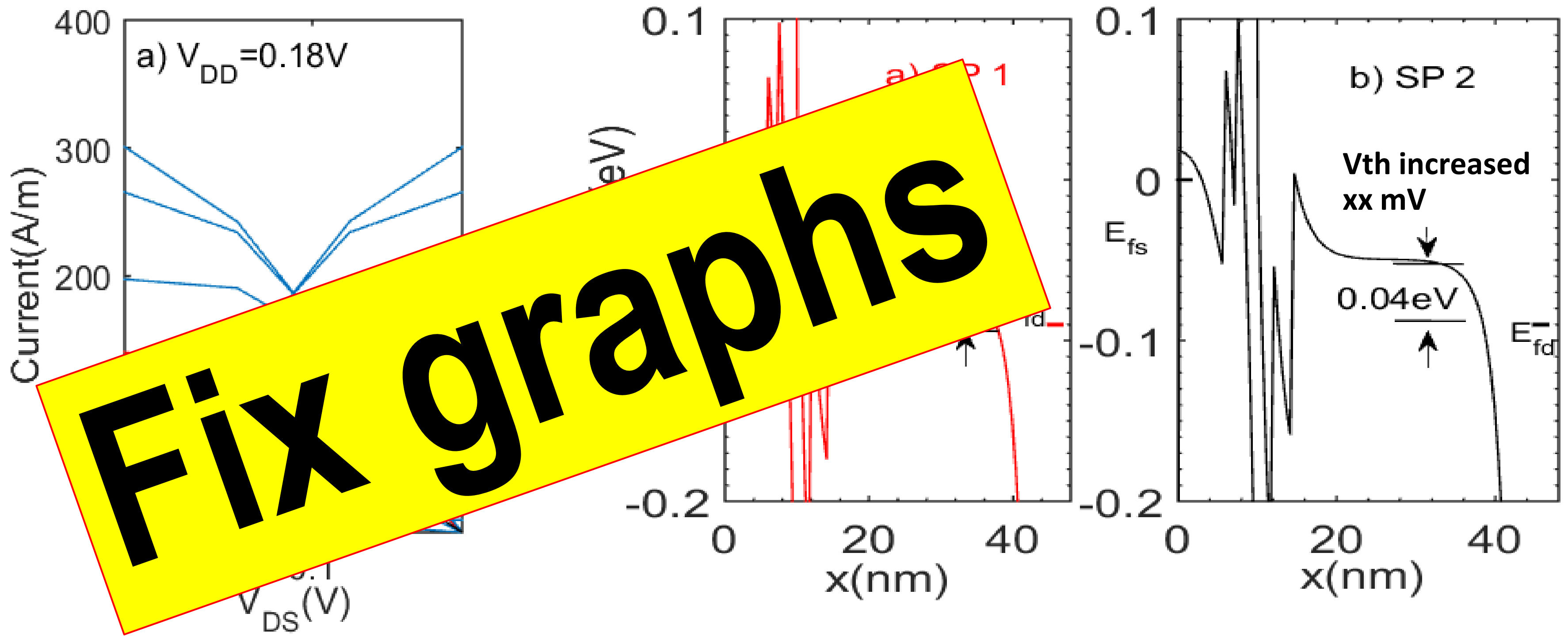
$E_{F,drain}$ should be below E_c at switching point

Need low output conductance when biased at switching point

output conductance: from drain-source reverse injection

to avoid : need drain Fermi level below channel conduction band

must decrease (V_{gs}-V_{th}) → increase V_{th}

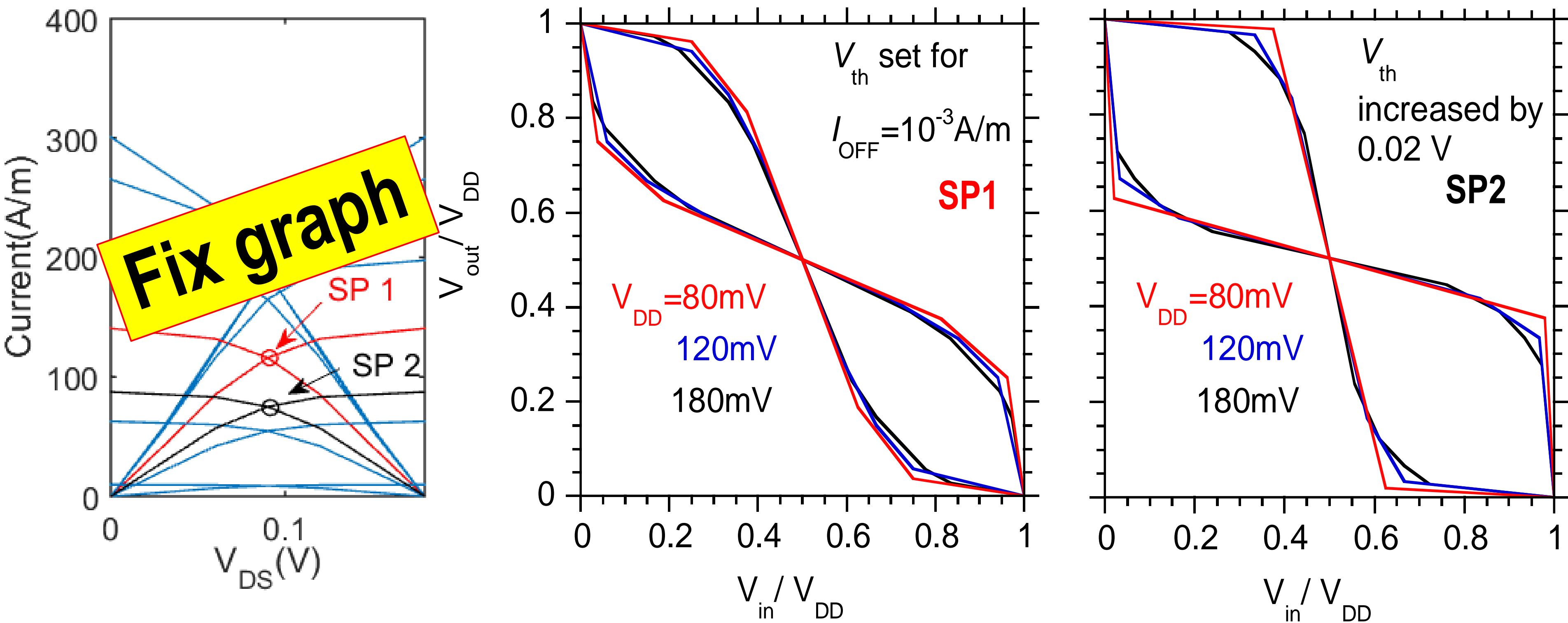


Increasing the threshold voltage:

Improves the noise margin

Reduces I_{ON}. Also reduces I_{OFF}

Increasing V_{th} increases noise margin



SP1:
FET not saturated → large dI_D/dV_{DS} → low gain, small noise margin

SP2:
V_{th} increased 20 mV → FET ***is*** just saturated.
Small dI_D/dV_{DS} → large gain, large noise margin

Increasing V_{th} deceases I_{on} from 106 A/m to 60A/m at V_{DD}=0.08V

Tunnel FET Design for High-Current, 120 mV Operation

you have all the wrong words here

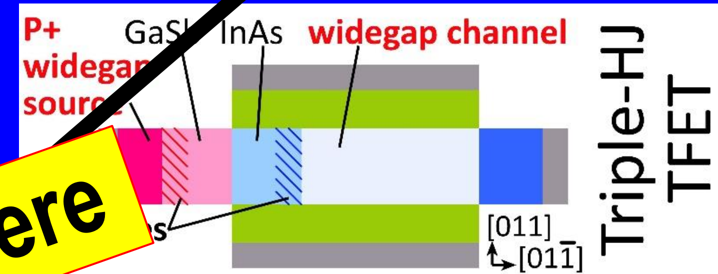
Low-energy computing
is low-voltage computing

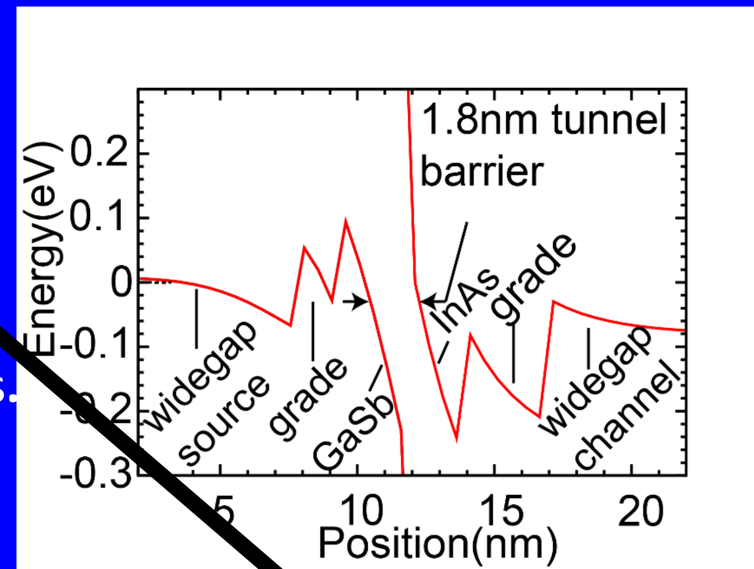
MOSFETs:
60 mV/dec.
set minimum ~500 mV operation.

Tunnel FETs:
subthreshold swin...
small on-cu... ...ogic
~12... → extremely slow logic

...heterojunction FETs:
increased junction field, resonant states.
>50% tunneling probability; full energy range
N-TFET & PTFET designs.
Designs using semiconductors with good high-K's.

Future work:
modeling leakage: scattering, defects.

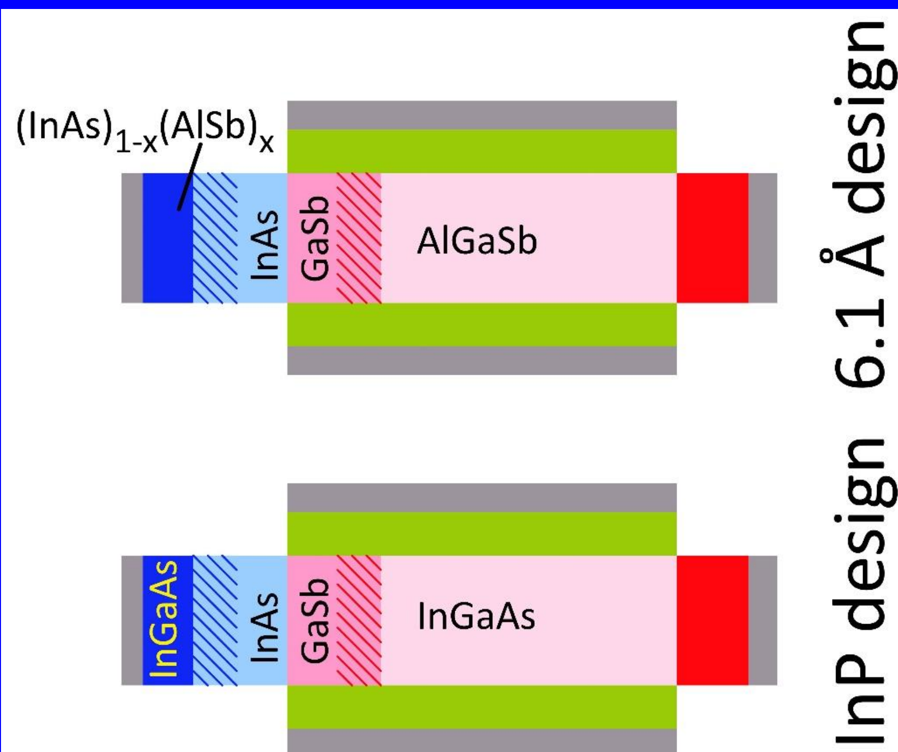




(end)

P-Channel designs

J. Huang *et al.*, in review (also arXiv preprint 1605.07166)



6.1 Å design:
No demonstrated high-quality dielectrics

InP-based design:
channel is InAs/InGaAs/InP
Some unpublished UCSB data
suggesting good high-K interfaces
on p-type InGaAs
(Chobpattana, Stemmer)
working to verify now

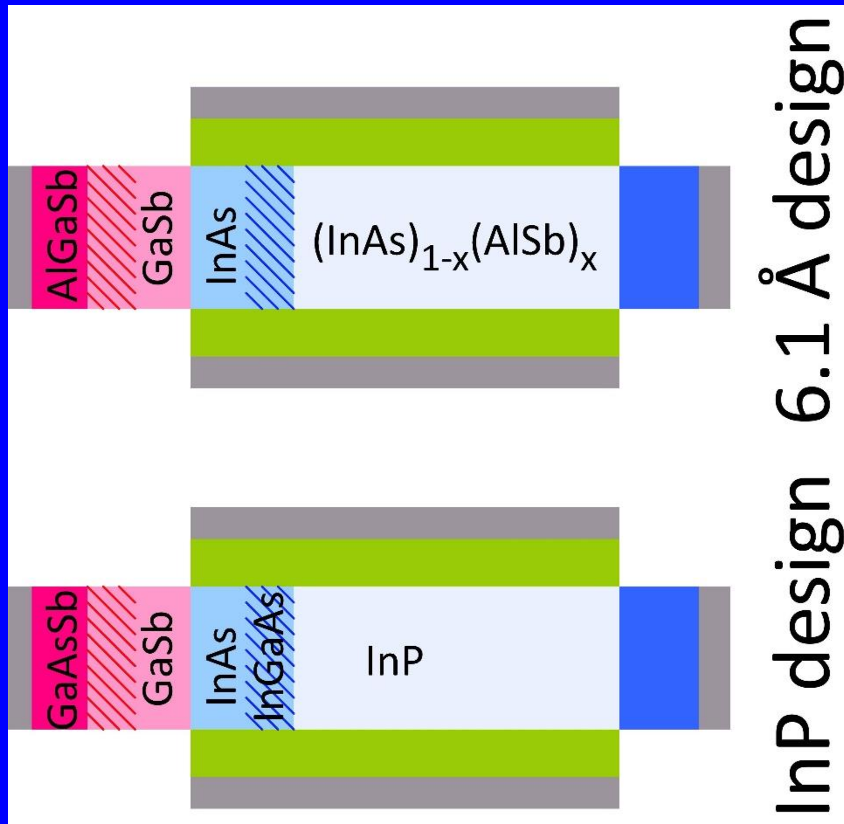
Simulations: (10^{-3} A/m I_{OFF}, 300 mV V_{DD})
6.1 Å design: 580 A/m I_{on}.
comparable to N-TFET
InP design: not yet simulated.

P-TFET performance is similar to that of the N-TFET

J.Z. Huang, et al, J-EDS, Vol 4, No.6, Nov 2016

Designs compatible with high-quality dielectrics

P. Long *et al.*, 2016 IEEE IPRM conference



6.1 Å design:
No demonstrated high-quality dielectrics

InP-based design:
channel is InAs/InGaAs/InP
high-quality dielectrics for all of these
Chobpattana, Stemmer, APL, 2014.
MOSFETs: 61 mV/dec. InAs,
65mV/dec. InGaAs
67mV/dec. InP

Simulations: (10^{-3} A/m I_{OFF}, 300 mV V_{DD})
InP design: 380 A/m I_{on}.
6.1 Å design: 800 A/m I_{on}.
(need to improve design)

Triple-heterojunction design can be realized with high-quality dielectrics.

Present designs can be further improved.

Performance comparisons (ideal ballistic case)

L_g=30nm

Design	V_{DD}	relative switching energy $\propto V_{DD}^2$	I_{on}@ 10^{-3} A/m I_{off}	speed F.O.M. I_{on}/V_{DD}
Si NMOS (experimental)	700 mV	1	~1000 A/m	~1400 S/m
Si NMOS (simulated)	700 mV	1	4080 A/m	5830 S/m
GaSb/InAs TFET	300 mV	0.18	32 A/m	107 S/m
GaSb/InAs TFET	70 mV	0.01	0.34 A/m	4.86 S/m
3HJ-TFET; 0.3V design	300 mV	0.18	800 A/m	2670 S/m
3HJ-TFET; 70mV design	70 mV	0.01	61 A/m	871 S/m

70 mV operation→ 100:1 less switching energy than 700 mV CMOS
3HJ TFET @ 70 mV: 6.7:1 slower than CMOS
GaSb TFET @70 mV: 1200:1 slower than CMOS

Caveats:
Simulations ignore scattering: with it, what performance will we then obtain ?
Structure is complex: can we make it ?
Can we reduce threshold variations, or at least compensate for them ?