

# High-Current Tunneling FETs With $(1\bar{1}0)$ Orientation and a Channel Heterojunction

Pengyu Long, Jun Z. Huang, Michael Povolotskyi, Gerhard Klimeck, *Fellow, IEEE*,  
and Mark J. W. Rodwell, *Fellow, IEEE*

**Abstract**—We propose InAs/GaSb ultrathin-body tunneling field-effect transistors (TFETs) using confinement in the  $(1\bar{1}0)$  plane and transport in the  $[110]$  direction to increase the tunneling probability by reducing the tunnel barrier energy and hole effective mass. To reduce the OFF-state leakage current, we add an InAs/ $In_{1-n}Al_nAs_{1-n}Sb_n$  heterojunction to the channel, which increases the valence band barrier. The heterojunction also increases the tunneling probability and ON-current by reducing the tunneling distance through the p-n junction and introducing a resonant state. A fully atomistic non-equilibrium Green function quantum transport approach in NEMO5 is used to explore the design space. While choosing  $10^{-3}$  A/m OFF-current ( $I_{OFF}$ ) and a 0.3 V power supply, we simulate 270 A/m ON-current ( $I_{ON}$ ) for a 30-nm gate length and 170 A/m for a 15-nm gate length ( $L_g$ ), while a conventional 15-nm  $L_g$  GaSb/InAs TFET under  $(001)$  confinement shows only 24 A/m  $I_{ON}$ .

**Index Terms**—Tunnel FETs, crystal orientation, band structure engineering, resonant tunneling.

## I. INTRODUCTION

FUTURE VLSI performance is constrained by power dissipation [1]. Low switching power calls for a low supply voltage, yet decreased standby power calls for either increased voltages or reduced transistor subthreshold swing (*S.S.*). In conventional MOSFETs, the *S.S.* is limited to 60mV/dec by thermal injection [1]. Though tunnel FETs (TFETs) [2]–[4] can obtain smaller *S.S.*, their ON current ( $I_{ON}$ ) is limited by the PN junction tunneling probability [3], which is determined by the carrier effective mass and tunneling distance. In nanoscale TFETs confinement quantizes subbands and

Manuscript received January 11, 2016; revised January 26, 2016; accepted January 27, 2016. Date of publication January 28, 2016; date of current version February 23, 2016. This work uses nanoHUB.org computational resources operated by the Network for Computational Nanotechnology funded by the U.S. National Science Foundation under Grant EEC-0228390, Grant EEC-1227110, Grant EEC-0634750, Grant OCI-0438246, Grant OCI-0832623, and Grant OCI-0721680. This material is based upon work supported by the National Science Foundation under Grant 1125017. NEMO5 developments were critically supported by an NSF Peta-Apps award OCI-0749140 and by Intel Corp. The review of this letter was arranged by Editor S. J. Koester.

P. Long, J. Z. Huang, M. Povolotskyi, and G. Klimeck are with the Network for Computational Nanotechnology and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: davidlong180@gmail.com).

M. J. W. Rodwell is with the Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA 93106-9560 USA.

Color versions of one or more of the figures in this letter are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/LED.2016.2523269

therefore increases the barrier energy and non-parabolic dispersions increase the carrier effective masses; both effects result in a decreased tunneling probability and reduced  $I_{ON}$ . The use of InAs/GaSb PN tunnel barriers reduces the tunneling barrier energy and tunneling distance, however at the desired layer thicknesses of a few nm, strong confinement and non-parabolic effects still reduce  $I_{ON}$  significantly. Alternative methods are needed to further increase  $I_{ON}$ .

Here we propose the concept to *increase* the confinement effective mass (to lower the confinement energy) and to *decrease* the transport effective mass (to increase the tunneling current). This can be achieved in the InAs material system by choosing the  $(1\bar{1}0)$  plane for confinement and the  $[110]$  direction for transport. We also introduce an InAs/ $In_{1-n}Al_nAs_{1-n}Sb_n$  heterojunction into the channel, and therefore resonantly enhance the tunneling probability in the ON-state and reduce the OFF-state source-drain tunneling leakage current.

## II. CONFINEMENT AND TRANSPORT DIRECTIONS

III-V materials have strongly anisotropic heavy-hole bands [5], [6] hence 2-D hole subband structure is a strong function [5]–[7] of the confinement plane.  $(1\bar{1}0)$  confinement provides subbands with low effective mass [8], particularly given  $[110]$  transport [9], [10]. For a  $t_{ch} = 2$  nm thick channel, the hole effective mass reduces from  $0.131m_0$  given  $(001)$  confinement and  $[100]$  transport, or  $0.19m_0$  given  $[110]$  transport, to  $0.073m_0$  given  $(1\bar{1}0)$  confinement and  $[110]$  transport. Further, because the heavy hole mass is larger in  $\langle 110 \rangle$  than in  $\langle 100 \rangle$ , the heavy hole subband energy shifts more slowly under  $(1\bar{1}0)$  confinement than under  $(100)$ . Compared to  $(100)$  confinement, at 2 nm  $t_{ch}$ ,  $(1\bar{1}0)$ -confined TFETs have lower hole effective mass and a smaller tunnel barrier energy (0.11eV vs. 0.15eV) between the GaSb source valence band and the InAs channel conduction band (Fig. 1a, b). The tunnel barrier is consequently thinner (Fig. 1c) and the tunneling probability higher (Fig. 1d).

The designs are based on a p-GaSb/n-InAs double-gate TFET (Fig. 2a). The gate oxide thickness is labeled  $t_{ox}$  and dielectric constant  $\varepsilon_r$ . The gate length is  $L_g$ , and source and drain doping densities are labeled  $N_S$  and  $N_D$ . The channel width extends in the  $z$  direction (perpendicular to the page). Table I lists the various design parameters. For  $(001)$ -confined

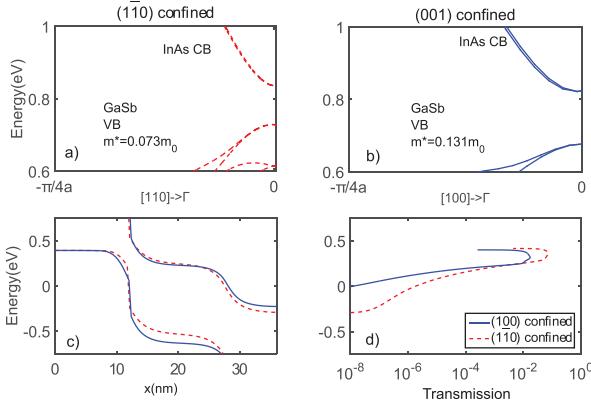


Fig. 1. Conduction band structure of InAs and valence band structure of GaSb for a)  $(\bar{1}\bar{1}0)$  confined, and b)  $(001)$  confined UTBs. c) Band diagram under ON-state bias and d) transmission probability of  $(\bar{1}\bar{1}0)$  confined and  $(001)$  confined UTB GaSb/InAs TFETs. The channels are 2 nm thick, and  $L_g = 15$  nm.

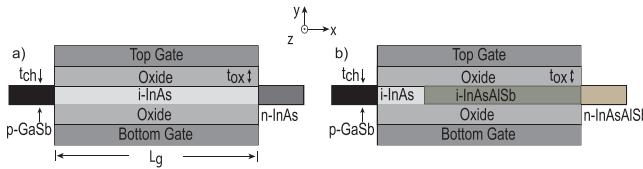


Fig. 2. Cross-section of a) a conventional GaSb/InAs TFET. b) Newly design heterostructure GaSb/InAs TFET with an InAs/  $In_{1-n}Al_nAs_{1-n}Sb_{1-n}$  heterojunction in the channel.

TFETs, the transport direction is  $[100]$ , and the GaSb/InAs heterointerface is InSb-like. For  $(\bar{1}\bar{1}0)$ -confined TFETs, the transport direction is  $[110]$ . The channel is 2 nm thick; at 15 nm  $L_g$ , thicker channels suffer large source-drain tunneling leakage current. III-V MOSFETs with  $T_{ch} = 2.5$  nm have been reported [11], [12].

Devices are simulated using the atomistic nanoelectronic modeling tool NEMO5 [13], which solves self-consistently the Poisson equation and the open boundary Schrödinger equation (quantum transmitting boundary method [14], [15]), using the 300K tight binding parameters of [16] and [17]; these give, in bulk, a 0.197 eV offset between the GaSb valence band and the InAs conduction band [18]. The InAlAsSb parameters are linearly interpolated using the virtual crystal approximation and are benchmarked against [19]. We integrate over the 1D Brillouin zone using a high order Gauss quadrature with 20 points. The simulations do not model carrier scattering. In [20]–[22], it is shown that phonon scattering slightly reduces TFET  $I_{on}$ , but does not significantly increase  $I_{off}$ . In the on-state, if carrier scattering is strong, the degree of resonant enhancement of the transmission will be decreased, and will degrade  $I_{on}$ . Trap-assisted tunneling and Shockley-Read-Hall thermal generation may also increase  $I_{off}$  and degrade S.S. [23]–[26]. Increasing the alloy fraction  $n$  within the  $In_{1-n}Al_nAs_{1-n}Sb_{1-n}$  channel will increase the channel bandgap and hence reduce thermal generation leakage currents.

Figure 1d demonstrates that in the energy range between the GaSb valence band and InAs conduction band, the TFET has a higher transmission probability with  $(\bar{1}\bar{1}0)$  compared to  $(001)$  confinement. At 30 nm  $L_g$ ,  $I_{ON}$  increases from

TABLE I  
PARAMETERS FOR GaSb/InAs TUNNELING FETs

$t_{ox}$	2.56 nm	$N_S$	$5 \cdot 10^{19} \text{ cm}^{-3}$
$t_{ch}$	2 nm	$N_D$	$2 \cdot 10^{19} \text{ cm}^{-3}$
$L_g$	30 nm, 15 nm	$\epsilon_{r,ox}$	9

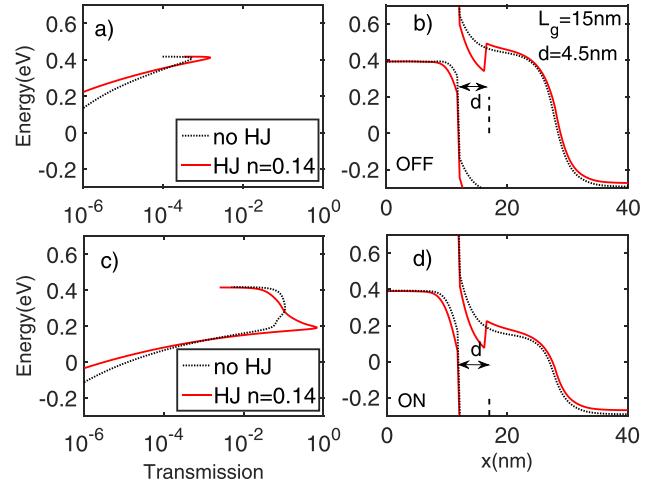


Fig. 3. Off-state transmission probability a) and band diagram b) of  $(\bar{1}\bar{1}0)$ -confined GaSb/InAs TFETs with and without an InAs/  $In_{1-n}Al_nAs_{1-n}Sb_{1-n}$  channel heterojunction. The transmission probability c) and band diagram d) are also shown in the ON state.  $x$  is the alloy fraction.

30A/m to 80A/m ( $V_{DD} = 0.3$ V,  $I_{OFF} = 10^{-3}$ A/m) comparing to a  $(001)$  confined TFET. However, undesired source-drain transmission at energies below the InAs conduction band edge is *increased* in the  $(\bar{1}\bar{1}0)$ -confined case (Fig. 1d) because InAs then has a smaller quantized bandgap (Fig. 1c) and smaller hole effective mass. The two-band S/D tunneling probability increases, and, at 15 nm  $L_g$ , the S.S. is degraded and, at fixed  $I_{OFF}$ ,  $I_{ON}$  reduced.

### III. CHANNEL HETEROJUNCTION

The introduction of an InAs/  $In_{1-x}Al_xAs_{1-x}Sb_x$  channel heterojunction (Fig. 2b) can improve both ON- and OFF-state performance, as reported in [27] and [28]. In the OFF-state, the heterojunction increases the valence-band barrier at the channel-source interface. This reduces the (two-band) S/D tunneling probability (Fig. 3a) in part because, under off-state bias (Fig. 3b), the energy separation between the InAs valence band and S/D tunneling evanescent states is increased, and in part because  $In_{1-n}Al_nAs_{1-n}Sb_{1-n}$  has slightly larger electron effective mass ( $0.067m_0$ ) than InAs ( $0.052m_0$ ). The width of the InAs well is adjusted so that the single resonant state is aligned with InAlAsSb conduction band; in the InAs layer, there are no states at energies below the InAlAsSb conduction band. The lower edge of the transmission characteristics (Fig. 3a) becomes sharper, resulting in a steeper S.S., as will be seen subsequently. InAs is retained at the PN junction to maintain a small tunnel barrier energy for high  $I_{ON}$ .

Under ON-state bias (Fig. 3d), i.e. with the channel conduction band  $\sim 0.2$ eV below the source valence band, inserting the

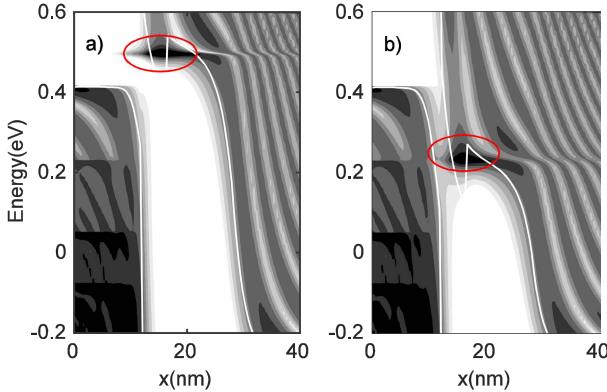


Fig. 4. Local density of states in the a) OFF state and b) ON state of a GaSb/InAs TFET with an InAs/In<sub>1-n</sub>Al<sub>n</sub>As<sub>1-n</sub>Sb<sub>n</sub> ( $n = 0.14$ ) channel heterojunction. The circled area indicates the resonant state.

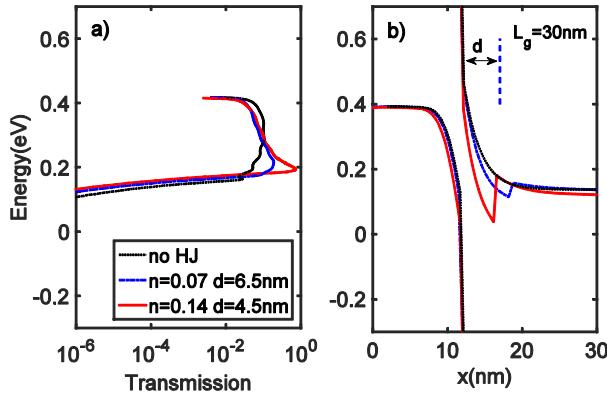


Fig. 5. a) Transmission probability and b) band diagram of the GaSb/InAs tunneling junction for different InAs/In<sub>1-n</sub>Al<sub>n</sub>As<sub>1-n</sub>Sb<sub>n</sub> heterojunctions. In all designs, the resonant state energy lies immediately above the In<sub>1-n</sub>Al<sub>n</sub>As<sub>1-n</sub>Sb<sub>n</sub> conduction band. The TFETs have (1̄10) confinement.

channel heterojunction increases the field in the PN tunnel barrier, reducing the PN junction tunneling distance hence increasing the tunneling probability (Fig. 3c). Inserting the channel heterojunction also introduces a resonant state in the InAs layer between the PN junction and the channel heterojunction (Fig. 4b). The tunneling probability is further increased by adjusting the In<sub>1-n</sub>Al<sub>n</sub>As<sub>1-n</sub>Sb<sub>n</sub> alloy fraction to align the resonant state energy to the channel conduction-band energy (Fig. 3c). This further improves  $I_{ON}$ .

To investigate the effect of the channel heterojunction on  $I_{ON}$ , independent of its effect on S/D tunneling, we first consider the case of 30 nm  $L_g$ . We simulate (Fig. 5b) a series of designs with varying InAs channel length  $d$ , while varying the In<sub>1-n</sub>Al<sub>n</sub>As<sub>1-n</sub>Sb<sub>n</sub> alloy fraction  $x$  such that the lowest resonant state in the InAs layer always lies immediately above the In<sub>1-n</sub>Al<sub>n</sub>As<sub>1-n</sub>Sb<sub>n</sub> conduction band.

As the InAs layer is progressively thinned and the alloy fraction  $n$  simultaneously increased, the InAs/In<sub>1-n</sub>Al<sub>n</sub>As<sub>1-n</sub>Sb<sub>n</sub> conduction band offset increases, and the energy separation between the InAs resonant state (aligned with the In<sub>1-n</sub>Al<sub>n</sub>As<sub>1-n</sub>Sb<sub>n</sub> conduction band) and the InAs conduction band increases (Fig. 5b)). The PN junction tunneling distance therefore progressively decreases (Fig. 5b)), progressively increasing  $I_{ON}$  (Fig. 6a). With  $V_{DD} = 0.3V$  and

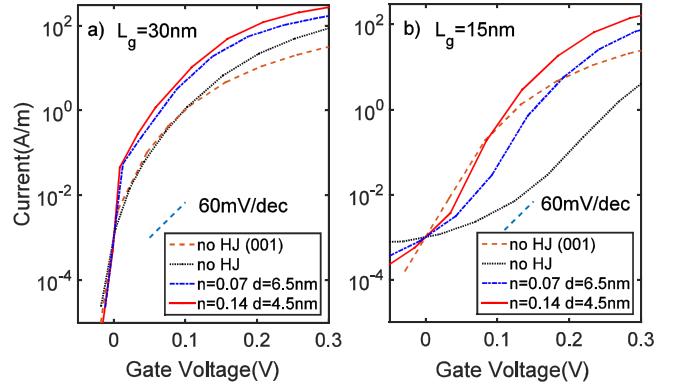


Fig. 6. Transfer characteristics of a) 30 nm  $L_g$  and b) 15 nm  $L_g$  (1̄10)-confined TFETs for different In<sub>1-n</sub>Al<sub>n</sub>As<sub>1-n</sub>Sb<sub>n</sub> heterojunction band profiles. Results are compared to (1̄10)- and (001)-confined TFETs with no channel heterojunction.

$I_{OFF} = 10^{-3}\text{ A/m}$ , and with (1̄10) confinement,  $I_{ON}$  increases from 80A/m ( $n=0$ ) to 270A/m ( $n = 0.14$ ,  $d = 4.5$  nm).

At 15 nm  $L_g$ , S/D tunneling is larger, and the InAs/In<sub>1-n</sub>Al<sub>n</sub>As<sub>1-n</sub>Sb<sub>n</sub> heterojunction provides a greater improvement in the ON/OFF current ratio. With  $V_{DD} = 0.3V$  and  $I_{OFF} = 10^{-3}\text{ A/m}$ , and with (1̄10) confinement, as the AlSb mole fraction  $n$  increases,  $I_{ON}$  increases from 5A/m ( $n = 0$ ) to 170A/m ( $n = 0.14$ ,  $d = 4.5$  nm). The (001)-confined TFET shows 24A/m  $I_{ON}$ .

A similar P-channel TFET design would use an N-InAs source, a channel containing a GaSb/AlGaSb heterojunction, a P+ AlGaSb drain, (1̄10) confinement, and [110] transport.

#### IV. SUMMARY

It is found that using the (1̄10) confinement plane and the [110] transport direction improves  $I_{ON}$  compared to (001)-confined TFETs. Introducing an InAs/In<sub>1-n</sub>Al<sub>n</sub>As<sub>1-n</sub>Sb<sub>n</sub> channel heterojunction reduces the S/D tunneling and improves the S.S. Further, the channel heterojunction greatly increases  $I_{ON}$ , both by decreasing the tunneling distance and by introducing a resonant state. Within this design space a 15 nm gate length TFET with 170A/m ON current can be obtained.

#### REFERENCES

- [1] T. N. Theis and P. M. Solomon, "In quest of the 'next switch': Prospects for greatly reduced power dissipation in a successor to the silicon field-effect transistor," *Proc. IEEE*, vol. 98, no. 12, pp. 2005–2014, Dec. 2010. DOI: 10.1109/JPROC.2010.2066531
- [2] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," *IEEE Electron Device Lett.*, vol. 27, no. 4, pp. 297–300, Apr. 2006. DOI: 10.1109/LED.2006.871855
- [3] S. O. Koswatta, M. S. Lundstrom, and D. E. Nikanov, "Performance comparison between p-i-n tunneling transistors and conventional MOSFETs," *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 456–465, Mar. 2009. DOI: 10.1109/TED.2008.2011934
- [4] G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetti, M. Radosavljevic, H. W. Then, and R. Chau, "Fabrication, characterization, and physics of III-V heterojunction tunneling field effect transistors (H-TFET) for steep sub-threshold swing," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2011, pp. 33.6.1–33.6.4. DOI: 10.1109/IEDM.2011.6131666
- [5] G. Klimeck, R. C. Bowen, and T. B. Boykin, "Strong wavevector dependence of hole transport in heterostructures," *Superlattices Microstruct.*, vol. 29, no. 3, pp. 187–216, Mar. 2001. DOI: 10.1006/spmi.2000.0973

- [6] N. Neophyto, A. Paul, and G. Klimeck, "Bandstructure effects in silicon nanowire hole transport," *IEEE Trans. Nanotechnol.*, vol. 7, no. 6, pp. 710–719, Nov. 2008. DOI: 10.1109/TNANO.2008.2006272
- [7] J. Z. Huang, L. Zhang, P. Long, M. Povolotskyi, and G. Klimeck, (2015). "Quantum transport simulation of III-V TFETs with reduced-order K.P method." [Online]. Available: <http://arxiv.org/abs/1511.02516>
- [8] N. Neophyto and G. Klimeck, "Design space for low sensitivity to size variations in [110] PMOS nanowire devices: The implications of anisotropy in the quantization mass," *Nano Lett.*, vol. 9, no. 2, pp. 623–630, 2009. DOI: 10.1021/nl802893m
- [9] J. Wang, P. M. Solomon, and M. Lundstrom, "A general approach for the performance assessment of nanoscale silicon FETs," *IEEE Trans. Electron Devices*, vol. 51, no. 9, pp. 1366–1370. DOI: 10.1109/TED.2004.833962
- [10] N. Neophyto, G. Klimeck, and H. Kosina, "Subband engineering for p-type silicon ultra-thin layers for increased carrier velocities: An atomistic analysis," *J. Appl. Phys.*, vol. 109, no. 5, p. 053721, 2011. DOI: 10.1063/1.3556435
- [11] S. Lee, V. Chobpattana, C.-Y. Huang, B. J. Thibeault, W. Mitchell, S. Stemmer, A. C. Gossard, and M. J. W. Rodwell, "Record  $I_{on}$  (0.50 mA/ $\mu$ m at  $V_{DD} = 0.5$  V and  $I_{off} = 100$  nA/ $\mu$ m) 25 nm-gate-length  $ZrO_2/InAs/InAlAs$  MOSFETs," in *IEEE Symp. VLSI Technol., Dig. Tech. Papers*, Jun. 2014, pp. 1–2.
- [12] C.-Y. Huang, P. Choudhary, S. Lee, S. Kraemer, V. Chobpattana, B. Thibeault, W. Mitchell, S. Stemmer, A. Gossard, and M. Rodwell, "12 nm-gate-length ultrathin-body InGaAs/InAs MOSFETs with  $8.3 \cdot 10^5$   $I_{on}/I_{off}$ ," in *Proc. 73rd Annu. Device Res. Conf. (DRC)*, Jun. 2015, p. 260. DOI: 10.1109/DRC.2015.7175669
- [13] J. E. Fonseca, T. Kubis, M. Povolotskyi, B. Novakovic, A. Ajoy, G. Hegde, H. Ilatikhameneh, Z. Jiang, P. Sengupta, Y. Tan, and G. Klimeck, "Efficient and realistic device modeling from atomic detail to the nanoscale," *J. Comput. Electron.*, vol. 12, no. 4, pp. 592–600, 2013. DOI: 10.1007/s10825-013-0509-0
- [14] C. S. Lent and D. J. Kirkner, "The quantum transmitting boundary method," *J. Appl. Phys.*, vol. 67, no. 10, pp. 6353–6359, 1990. DOI: 10.1063/1.345156
- [15] M. Luisier, A. Schenk, W. Fichtner, and G. Klimeck, "Atomistic simulation of nanowires in the  $sp^3d^5s^*$  tight-binding formalism: From boundary conditions to strain calculations," *Phys. Rev. B*, vol. 74, no. 20, p. 205323, Nov. 2006. DOI: 10.1103/PhysRevB.74.205323
- [16] Y. P. Tan, M. Povolotskyi, T. Kubis, T. B. Boykin, and G. Klimeck, "Tight-binding analysis of Si and GaAs ultrathin bodies with subatomic wave-function resolution," *Phys. Rev. B*, vol. 92, no. 8, p. 085301, 2015. DOI: 10.1103/PhysRevB.92.085301
- [17] Y. Tan *et al.* Tight Binding Parameters by DFT Mapping. <https://nanohub.org/resources/15173>, accessed Jan. 26, 2016.
- [18] I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, "Band parameters for III-V compound semiconductors and their alloys," *J. Appl. Phys.*, vol. 89, no. 11, pp. 5815–5875, 2001. DOI: 10.1063/1.1368156
- [19] T. H. Glisson, J. R. Hauser, M. A. Littlejohn, C. K. Williams, "Energy bandgap and lattice constant contours of III-V quaternary alloys," *J. Electron. Mater.*, vol. 7, no. 1, pp. 1–16, 1978. DOI: 10.1007/BF02656016
- [20] M. Luisier and G. Klimeck, "Simulation of nanowire tunneling transistors: From the Wentzel-Kramers-Brillouin approximation to full-band phonon-assisted tunneling," *J. Appl. Phys.*, vol. 107, no. 8, p. 084507, 2010. DOI: 10.1063/1.3386521
- [21] S. O. Koswatta, S. J. Koester, and W. Haensch, "On the possibility of obtaining MOSFET-like performance and sub-60-mV/dec swing in 1-D broken-gap tunnel transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 12, pp. 3222–3230, Dec. 2010. DOI: 10.1109/TED.2010.2079250
- [22] U. E. Avci, D. H. Morris, S. Hasan, R. Kotlyar, R. R. Kim, R. Rios, D. E. Nikonorov, and I. A. Young, "Energy efficiency comparison of nanowire heterojunction TFET and Si MOSFET at  $L_g=13$  nm, including P-TFET and variation considerations," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2013, pp. 33.4.1–33.4.4. DOI: 10.1109/IEDM.2013.6724744
- [23] U. E. Avci, B. Chu-Kung, A. Agrawal, G. Dewey, V. Le, R. Rios, D. H. Morris, S. Hasan, R. Kotlyar, J. Kavalieros, and I. A. Young, "Study of TFET non-ideality effects for determination of geometry and defect density requirements for sub-60 mV/dec Ge TFET," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2015, pp. 34.5.1–34.5.4. DOI: 10.1109/IEDM.2015.7175669
- [24] M. G. Pala and D. Esseni, "Interface traps in InAs nanowire tunnel-FETs and MOSFETs—Part I: Model description and single trap analysis in tunnel-FETs," *IEEE Trans. Electron Devices*, vol. 60, no. 9, pp. 2795–2801, Sep. 2013. DOI: 10.1109/TED.2013.2274196
- [25] D. Esseni and M. G. Pala, "Interface traps in InAs nanowire tunnel FETs and MOSFETs—Part II: Comparative analysis and trap-induced variability," *IEEE Trans. Electron Devices*, vol. 60, no. 9, pp. 2802–2807, Sep. 2013. DOI: 10.1109/TED.2013.2274197
- [26] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, "Temperature-dependent  $I-V$  characteristics of a vertical  $In_{0.53}Ga_{0.47}As$  tunnel FET," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 564–566, Jun. 2010. DOI: 10.1109/LED.2010.2045631
- [27] K. Ganapathi and S. Salahuddin, "Heterojunction vertical band-to-band tunneling transistors for steep subthreshold swing and high on current," *IEEE Electron Device Lett.*, vol. 32, no. 5, pp. 689–691, May 2011. DOI: 10.1109/LED.2011.2112753
- [28] M. G. Pala and S. Brocard, "Exploiting hetero-junctions to improve the performance of III-V nanowire tunnel-FETs," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 115–121, May 2015. DOI: 10.1109/JEDS.2015.2395719