Exploring Channel Doping Designs for High-Performance Tunneling FETs

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Introduction

Future high-performance low-power integrated circuits require compact logic devices with both steep subthreshold swing (SS) and large drive current (I_{ON}). Tunneling field-effect transistors (TFETs) can meet the first requirement but their I_{ON} is severely limited either by the low source-channel tunneling probability or by the high source-to-drain tunneling leakage. One of the methods that can be employed to boost I_{ON} is doping engineering. In particular, (1) lowering the drain doping density elongates the drain depletion region and thus suppresses the leakage leading to improved SS (and I_{ON}). This scheme, however, is not scalable as a long drain length is needed to reach charge neutrality [1]; (2) embedding an opposite N+ doping layer next to the P+ source, i.e., the source-pocket (SP) design [2], or inserting a δ doping layer [3], can enhance the electric field at the source-channel tunnel junction and improve I_{ON}. It can be shown that the improvement increases as the pocket doping density (N_p) increases, but in practice doping density has an upper limit. In this paper, we show that, (1) embedding a P+ drain pocket can also improve the SS (and I_{ON}) and it is more scalable than lowering the drain doping; (2) by resorting to P+ channel, we can further improve I_{ON} of the SP design without having to increase N_p.

Proposed Designs

As shown in Fig. 1, three designs are proposed to improve a double-gate ultra-thin-body (UTB) InAs TFET (D1). For the first design (D2), we insert a P+ pocket layer before the N+ drain. For the second design (D3), the P+ pocket layer of D2 is extended to the whole channel except a source pocket region, which remains intrinsic. For the third design (D4), we replace the intrinsic pocket of D3 with an N+ pocket. The body and oxide thicknesses are 3nm and 1nm, with oxide permittivity 3.8. Source, channel, and drain lengths are 10nm, 20nm, and 15nm. Source (drain) doping density is -5 $(+2)$ $\times 10^{19} \mathrm{cm}^{-3}$. Pocket (channel) doping density N_p (N_{ch}) of D2 (D3) is fixed to $-5 \times 10^{19} \mathrm{cm}^{-3}$. The N_p (N_{ch}) of D4 is fixed to $+5$ (-5) $\times 10^{19} \mathrm{cm}^{-3}$. Then pocket length L_p is to be optimized.

Simulation Method and Results

The devices are simulated and optimized using NEMO5 tool [4] with Poisson equation and quantum transport equations (quantum transmitting boundary method with eight-band $k \cdot p$ Hamiltonian) solved self-consistently. The doping effect is modeled by putting (completely-) ionized charge density into the Poisson equation and thus discrete dopant induced scattering is neglected. Fig. 2 shows that all three designs (all with optimized L_p) can improve SS and I_{ON} of D1, with D4 delivers the largest I_{ON}. D4 delivers even larger I_{ON} than the SP design (for the same N_p and both with optimized L_p), while D3 is very similar to the SP design. Fig. 3 shows that longer L_p of D2 leads to better SS. At OFF state (Fig. 4), the pocket of D2 suppresses the source-to-drain tunneling by increasing the tunneling barrier height and distance; this effect is more pronounced for longer L_p. While at ON state (Fig. 5), the drain pocket does not appreciably affect I_{ON} although the pocket introduces a potential barrier. This barrier and the source tunneling barrier form a quantum well, resulting in several resonant tunneling peaks. Unlike the low drain doping design, this design does not need a long drain length and thus is more scalable. Fig. 6 shows that longer L_p of D3 leads to better I_{ON} (the threshold voltages of D3 are right shifted due to the P+ channel). As explained by Fig. 7 and 8, at ON state, in particular, the electric field at the tunnel junction is increased due to the potential drop at the intrinsic pocket. This potential drop is larger for longer L_p. When L_p reaches 4nm, a small potential well is formed, resulting in resonant tunneling above the well. Further increasing L_p leads to a wider (and deeper) potential well that creates resonant states inside the well, degrading the SS. Similar behavior is observed for the SP design [5] and the channel heterojunction design [6]. Fig. 9 shows that the longer L_p of D4 the larger I_{ON} and when $L_p = 2.8$nm it outperforms D3. As found in Fig. 10 and 11, D4 further enhances the electric field at the tunnel junction. This is due to the even larger and sharper potential drop from the P+ channel to the N+ pocket, pushing the tunneling barrier thinner.

Conclusion

A series of channel doping designs (D2∼D4) are proposed to enhance TFET performance. Quantum ballistic simulations show, that with $I_{OFF} = 10^{-3}$A/m and $V_{DD} = 0.3$V, D2, D3, and D4 improve the I_{ON} of D1 from 25A/m to 43A/m, 114A/m, and 170A/m, respectively. The designs can also apply to p-type as well as heterojunction TFETs.

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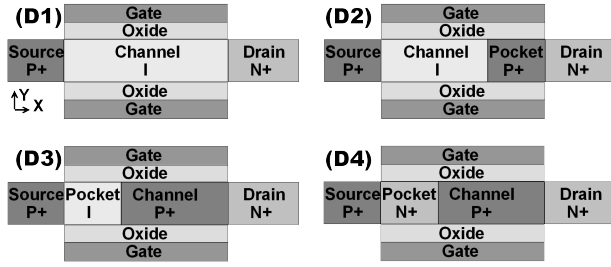[6] P. Long, et al., IEEE-EDL, vol. 37, p. 345, (2016).

Fig. 1: Geometries of n-type TFETs using intrinsic channel (D1), intrinsic channel with a P+ drain pocket (D2), P+ channel with an intrinsic source pocket (D3), and P+ channel with an N+ source pocket (D4).
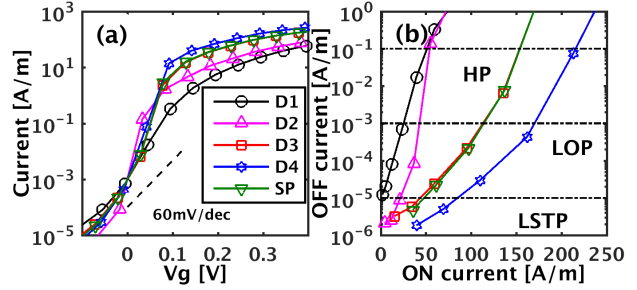
Fig. 2: (a) I_{DS}-V_{GS} and (b) I_{ON}-I_{OFF} ($V_{DD} = 0.3V$) of the four devices and the SP design, all with optimized pocket lengths. HP: high performance, LOP: low operating power, and LSTP: low standby power.
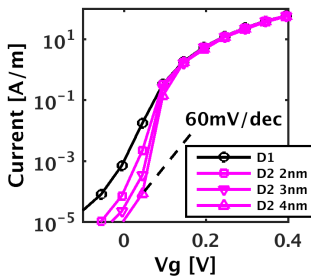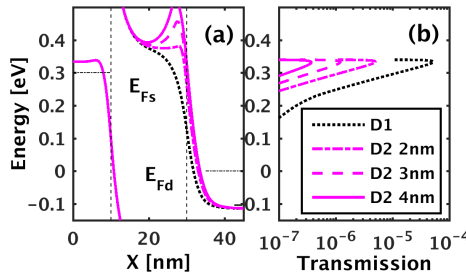
Fig. 3: I_{DS}-V_{GS} of D2 for three pocket lengths, in comparison with D1.

Fig. 4: (a) Band diagram and (b) transmission of D2 for three pocket lengths, in comparison with D1, at Vg=0V.
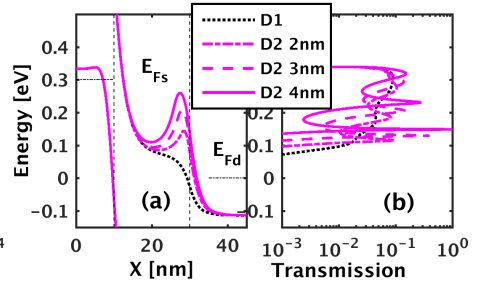
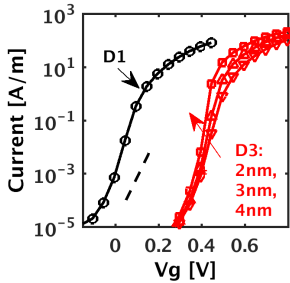Fig. 5: (a) Band diagram and (b) transmission of D2 for three pocket lengths, in comparison with D1, at Vg=0.3V.

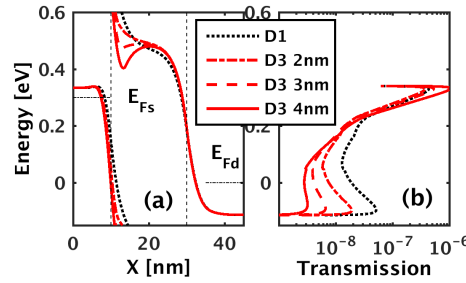Fig. 6: I_{DS}-V_{GS} of D3 for three pocket lengths, in comparison with D1.

Fig. 7: (a) Band diagram and (b) transmission of D3 for three pocket lengths, in comparison with D1, at Vg=0.3V/−0.1V.
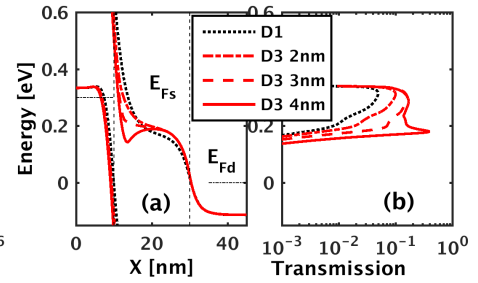
Fig. 8: (a) Band diagram and (b) transmission of D3 for three pocket lengths, in comparison with D1, at Vg=0.6V/0.2V.

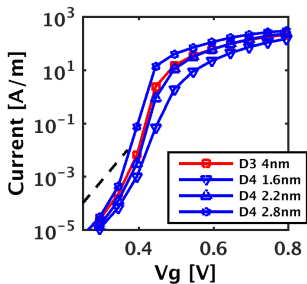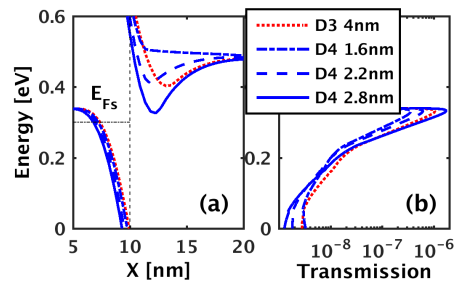Fig. 9: I_{DS}-V_{GS} of D4 for three pocket lengths, in comparison with D3.

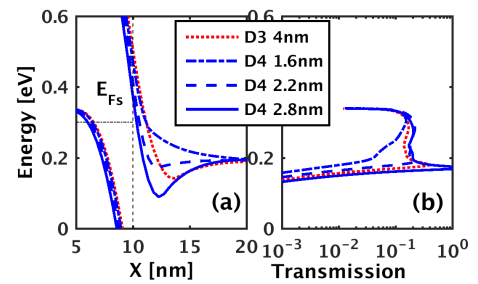Fig. 10: (a) Band diagram and (b) transmission of D4 for three pocket lengths, in comparison with D3, at Vg=0.3V.

Fig. 11: (a) Band diagram and (b) transmission of D4 for three pocket lengths, in comparison with D3, at Vg=0.6V.