Extremely high simulated ballistic currents in triple-heterojunction tunnel transistors

Pengyu Long[1,3], Michael Povolotskyi[1], Jun Z. Huang[1], Hesameddin Ilatikhameneh[1], Tarek Ameen[1], Rajib Rahman[1], Tillmann Kubis[1], Gerhard Klimeck[1], Mark. J.W. Rodwell[2]
[1]Network for computational nanotechnology, Purdue University, West Lafayette, IN 47906
[2]ECE Department, University of California, Santa Barbara, CA 93106-9560 [3]Email: davidlong180@gmail.com

Future VLSI devices will require low $CV_{DD}^2/2$ switching energy, large on-currents (I_{ON}), and small off-currents (I_{OFF}). Low switching energy requires a low supply voltage V_{DD}, yet reducing V_{DD} typically increases I_{OFF} and reduces the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio. Though tunnel FETs (TFETs) have steep subthreshold swings and can operate at a low V_{DD}, yet their I_{ON} is limited by low tunneling probability. Even with a GaSb/InAs heterojunction (HJ), given a 2nm-thick-channel (001)-confined TFET, [100] transport, and assuming V_{DD}=0.3V and $I_{\mathrm{OFF}}=10^{-3}$A/m, the peak tunneling probability is <3% (fig.1a) and I_{ON} is only 24 A/m (fig.1b) [1]. This low I_{ON} will result in large CV_{DD}/I delay and slow logic operation. Techniques to increase I_{ON} include graded AlSb/AlGaSb source HJs [2,3] and tunneling resonant states [4]. We had previously shown that tunneling probability is increased using ($1\bar{1}0$) confinement and channel heterojunctions [1], the latter increasing the junction built-in potential and junction field, hence reducing the tunneling distance. Here we propose a *triple heterojunction* TFET combining these techniques. The triple-HJ design further thins the tunnel barrier to 1.2 nm, and creates two closely aligned resonant states 57meV apart. The tunneling probability is very high, >50% over a 120meV range, and the ballistic I_{ON} is extremely high, 800A/m at 30nm L_{G} and 475 A/m at 15nm L_{G}, both with $I_{\mathrm{OFF}}=10^{-3}$ A/m and V_{DD}=0.3 V. Compared to a (001) GaSb/InAs TFET, the triple-HJ design increases the ballistic I_{ON} by 26:1 at 30nm L_{G} and 19:1 at 15nm L_{G}. The designs may, however, suffer from increased phonon-assisted tunneling.

The devices are simulated using the atomistic nanoelectronic modeling tool NEMO5 [5], which solves self-consistently the Poisson equation and the open boundary Schrödinger equation (quantum transmitting boundary method [6]), using the 300K tight binding parameters of [7, 8]. The TFETs have double gates (e.g. are finFETs) with 2.56nm thick gate dielectric ($\varepsilon_{r,ox}$=9), and 2nm thick channels.

In a channel-HJ TFET [1] (fig. 3b), an InAs/ $In_{1-n}Al_nAs_{1-n}Sb_n$ channel HJ increases the junction electric field and introduces a resonant state, both increasing I_{ON}. In the OFF-state, the increased valence band barrier (fig. 2) decreases I_{OFF}. As the channel Al mole fraction *n* is progressively increased and the InAs wells progressively thinned, at first the PN junction field increases, the tunnel barrier thins, and the tunneling transmission probability and I_{ON} increase. But, if the InAs layer is thinned below 3.5 nm and *n* increased above 0.21, the increased junction potential elongates the source depletion region, offsetting the decrease in PN tunnel barrier width on the channel side. Consequently, I_{ON} does not further improve. To further improve I_{ON}, source depletion must be suppressed.

The source HJ [2,3] (fig. 3c) suppresses source depletion; adding it to a channel-HJ TFET forms a triple-HJ TFET (fig. 3d) and allows the tunnel barrier to be further thinned. As the local density of states (fig. 4) shows, the wells formed by the source and channel HJ have resonant states aligned with the source valence band and channel conduction band respectively. These increase on-state transmission, hence I_{ON}.

Fig. 5 compares the band diagrams and transmission characteristics of a ($1\bar{1}0$)-confined GaSb/InAs HJ TFET to that of a triple-HJ TFET. In the ON-state, the GaSb/InAs HJ TFET has a 5.3nm thick tunnel barrier and 10% peak tunneling probability; the triple-HJ TFET has a 1.3nm thick barrier and >50% tunneling probability over a 120meV range. Fig. 6 compares the transfer characteristics of the four designs at 15nm and 30nm L_{G}, cases with large *vs*. small source-drain tunneling leakage. Table 1 lists I_{ON} and the corresponding tunneling distances. At 15nm L_{G}, the channel-HJ TFET has a better ON/OFF ratio and better subthreshold swing than the source-HJ TFET, in part due to smaller source/drain tunneling from a larger valence-band barrier and a larger channel electron effective mass. At both 15nm and 30nm L_{G}, the triple-HJ TFET has the highest I_{ON} of all designs, this due to the strongest junction electric field and smallest tunneling distance. A graded source HJ further increases the junction electric field and decreases the tunnel barrier width; its design includes an AlSb source ($N_{\mathrm{A}}=3\times10^{19}\mathrm{cm}^{-3}$), an 1.6 nm $Ga_{0.5}Al_{0.5}Sb$ ($N_{\mathrm{A}}=6\times10^{19}\mathrm{cm}^{-3}$) grade layer, an 2.8 nm GaSb ($N_{\mathrm{A}}=5\times10^{19}\mathrm{cm}^{-3}$) P-junction layer, an 3.3 nm InAs undoped N-junction layer, and an undoped $In_{0.79}Al_{0.21}As_{0.79}Sb_{0.21}$ channel. It achieves an 800A/m ballistic I_{ON} at 30nm L_{G} and 460A/m at 15 nm.

We avoid placing the source resonant state above the source valence band or the channel resonant state below the channel conduction band, as this would increase I_{OFF} by combined tunneling and thermionic emission. Nevertheless, in the off-state, evanescent states in the source and channel wells couple (fig. 4a) to states across the barrier; these states will increase I_{OFF} through phonon-assisted tunneling, an effect not modeled here, but modeled in [2]. Source thermalization with 5meV broadening reduces I_{ON} to 350A/m at 15nm L_{G}, but does not significantly reduce I_{ON} at 30nm L_{G}. We will report a more detailed analysis of the mechanisms controlling I_{OFF}.

[1] P. Long, *et al.*, EDL vol.37, no. 3 (2016), [2] M. G. Pala, *et al.*, IEEE EDS journal, vol.3, no.3 (2015) [3] W. Li *et al.* , IEEE Exploratory Solid-State Computational Devices and Circuits Journal, 2015, [4] U.E. Avci, *et al.*, IEDM (2013), [5] J.E. Fonseca, *et al.*, J. Comput. Electron, vol.12, no.4, [6] M. Luisier, *et al.* Phys. Rev. B, vol. 74, no. 20 (2006), [7] Y. P. Tan, *et al.*, IWCE (2015), [8] Y.P. Tan, et al., https://nanohub.org/resources/15173

Acknowledgements: The nanoHUB.org computational resources funded by the US NSF grant Nos. EEC-0228390, EEC-1227110, EEC-0634750, OCI-0438246, OCI-0832623 and OCI-0721680 are gratefully acknowledged. This work is supported by the NSF Grant No. 1125017. NEMO5 developments were critically supported by an NSF Peta-Apps award OCI-0749140 and by Intel Corp.

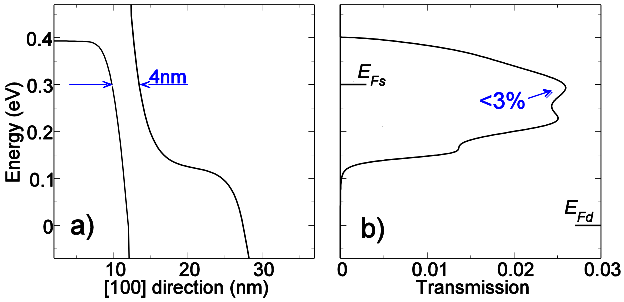

Fig. 1. Band diagram (a) and transmission probability (b) of a (001)-confined tunnel FET in ON-state bias. The transport is along [100]. The maximum transmission probability is 2.5%

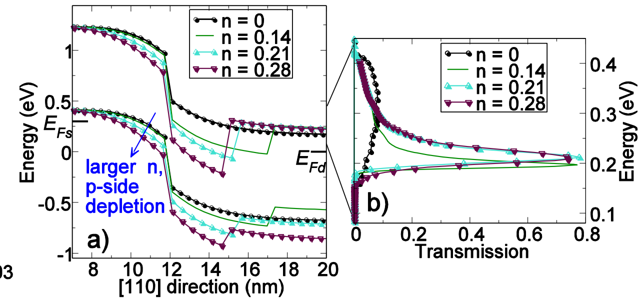

Fig. 2. Band diagram (a) and transmission probability (b) of a TFET with an $InAs/In_{1-n}Al_nAs_{1-n}Sb_n$ channel heterojunction and $(1\bar{1}0)$ confinement. Transport is along [110]. E_{Fs} and E_{Fd} refer to source and drain Fermi levels.

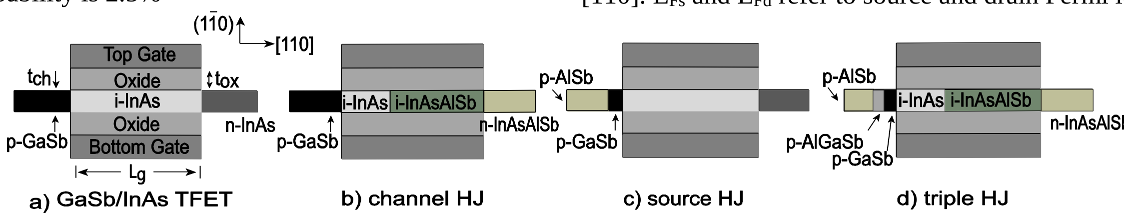

Fig. 3. Device cross-section of a TFET with a GaSb/InAs tunnel heterojunction (a), a InAs/InAlAsSb channel heterojunction (b), a AlSb/GaSb source heterojunction (c), and with both source and channel heterojunctions (d). In (d), the source heterojunction can be graded.

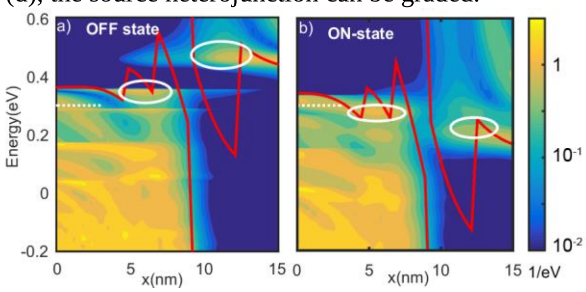

Fig. 4. Local density of states in OFF-state (a) and on-state bias (b) of a $(1\bar{1}0)$-confined triple-HJ TFET. Resonant states are circled.

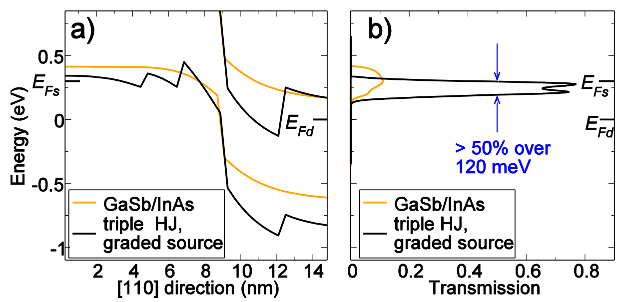

Fig. 5. Band diagram (a) and transmission probability (b) of a $(1\bar{1}0)$-confined GaSb/InAs TFET and a triple-HJ TFET with source grading. Transport is along [110].

	L_G=30nm		L_G=15nm	
	Tunnel barrier (nm)	I_{ON} (A/m)	Tunnel barrier (nm)	I_{ON} (A/m)
(001) GaSb/InAs	3.6	30	3.9	24
$(1\bar{1}0)$ GaSb/InAs	3.2	87	5.3	5
$(1\bar{1}0)$ Source HJ	2.6	145	3.3	29
$(1\bar{1}0)$ Channel HJ	1.9	300	2.1	225
$(1\bar{1}0)$ Triple HJ	1.2	800	1.3	460

Table 1: I_{ON} and tunneling distance for $(1\bar{1}0)$ GaSb/InAs HJ, source HJ, channel HJ, and triple-HJ TFETs. These are compared to a reference (001)-confined GaSb/InAs design.

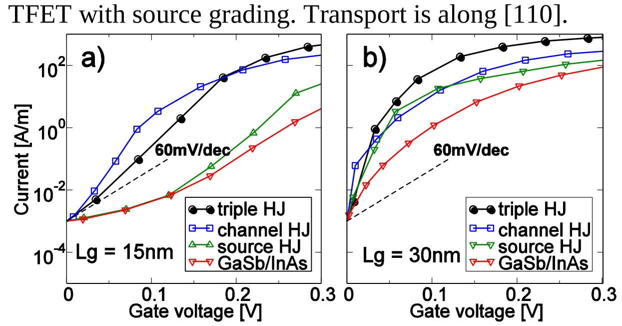

Fig. 6. Transfer characteristics of $(1\bar{1}0)$ confined TFETs for L_G=15nm (a) and L_G=30nm (b). Transport is along [110].