Transistor and IC design for 50GHz and above

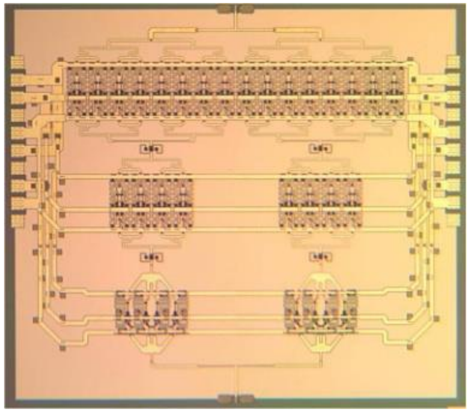
Mark Rodwell, UCSB

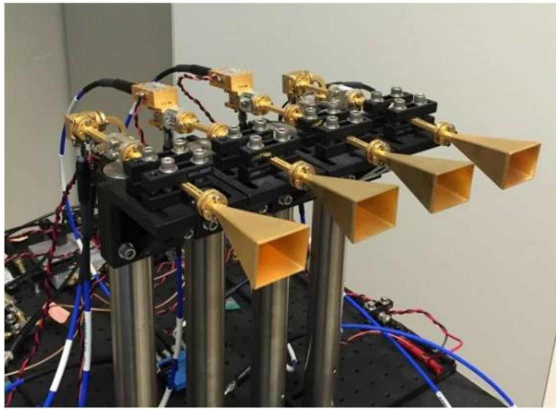
mm-wave systenms:
Prof. U. Madhow & group: ***UCSB***

mm-wave ICs
S-K Kim, R. Maurer, A. Ahmed, H. Yu, H-C. Park, T. Reed, ***UCSB***
Prof. J. Buckwalter & group, ***UCSB***
J. Hacker, Z. Griffith: ***Teledyne Scientific and Imaging***
M. Seo: ***Sungkyunkwan University***

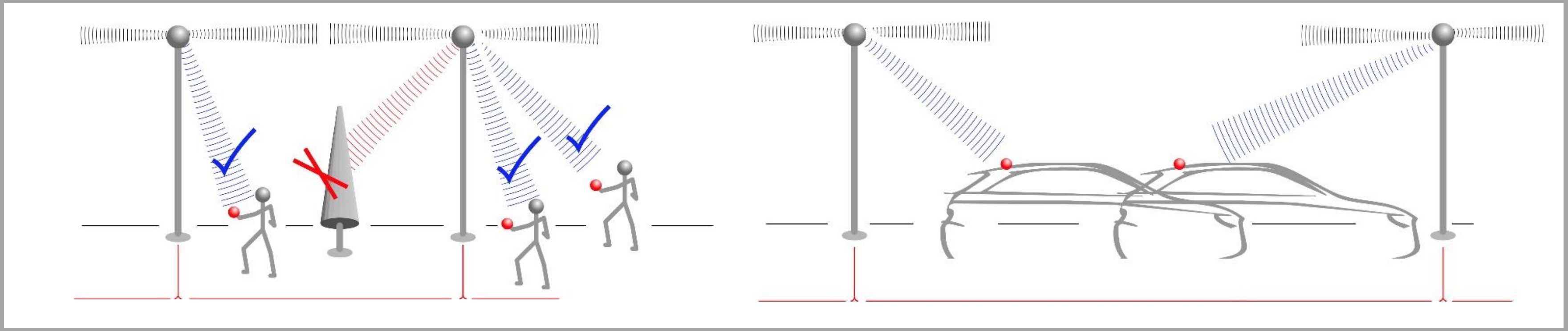
mm-Wave Transistors :
J. Rode, P. Choudhary, B. Markman, Y. Fang, J. Wu,
A.C. Gossard, B. Thibeault, W. Mitchell: ***UCSB***
M. Urteaga, B. Brar: ***Teledyne Scientific and Imaging***

Why mm-wave wireless ?

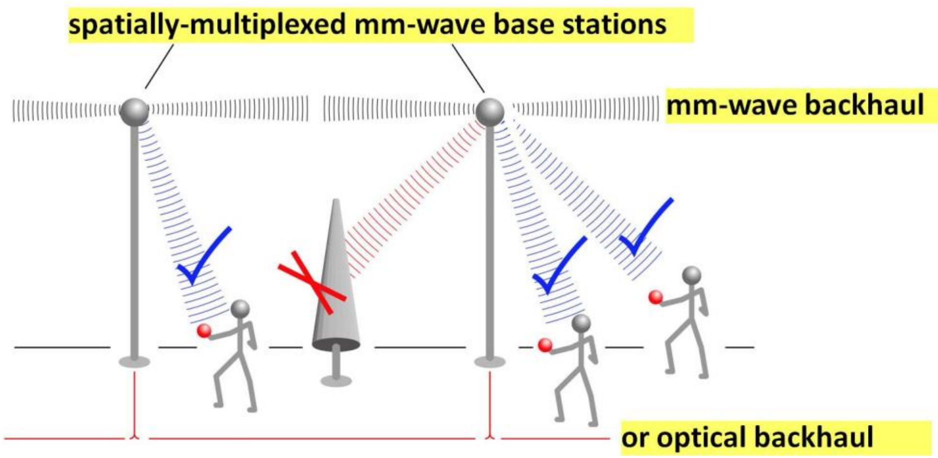


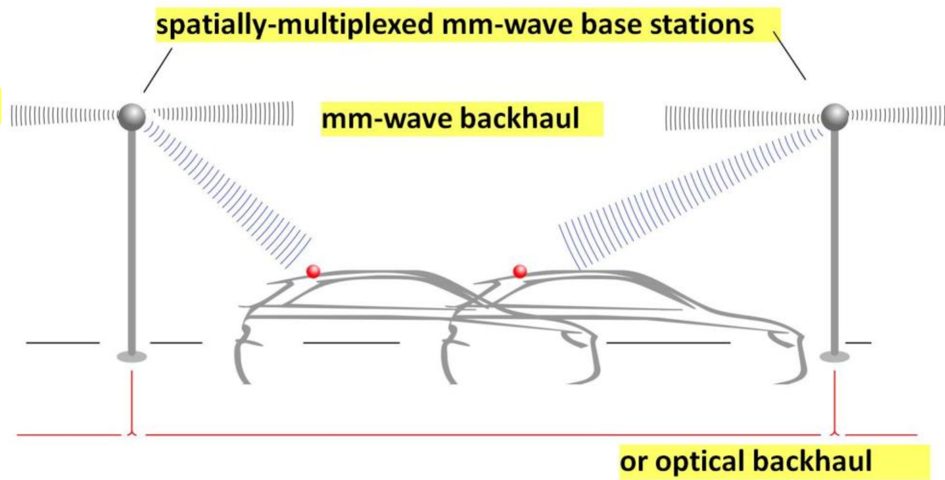


Overview

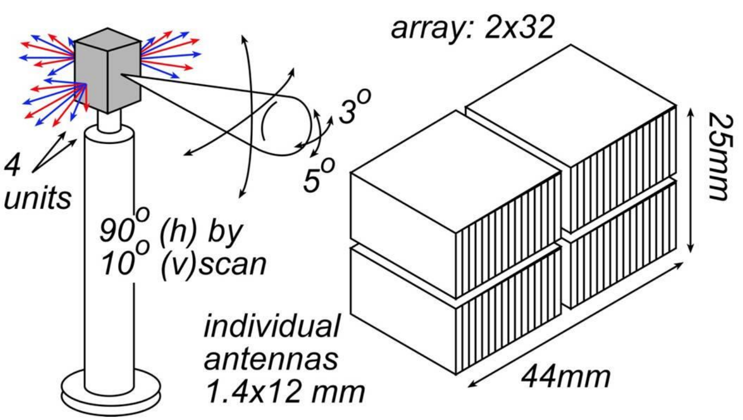


mm-Waves: high-capacity mobile communications

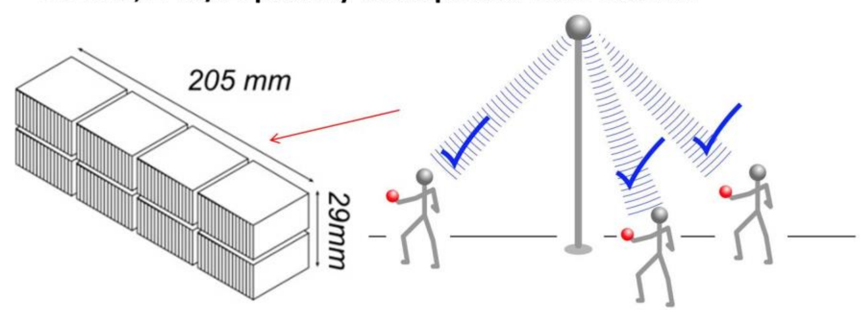




140 GHz, 10 Gb/s Adaptive Picocell Backhaul



60 GHz, 1 Tb/s Spatially-Multiplexed Base Station



128 users/face, 512 total users, each beam 2Gb/s

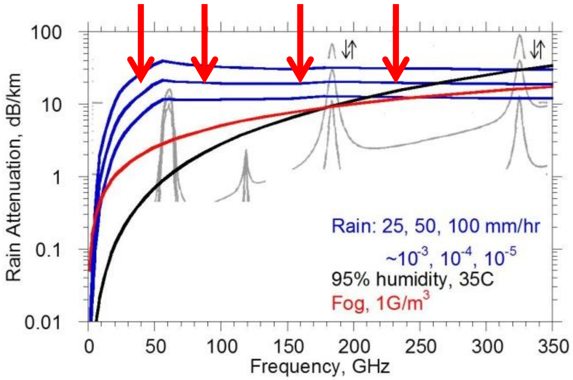
Needs→ research:

<u>RF front end:</u> phased array ICs, high-power transmitters, low-noise receivers

<u>IF/baseband:</u> ICs for multi-beam beamforming, for ISI/multipath suppression, ...

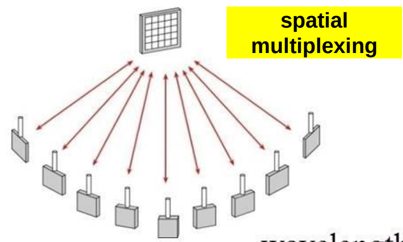
mm-Waves: benefits & challenges

Large available spectrum

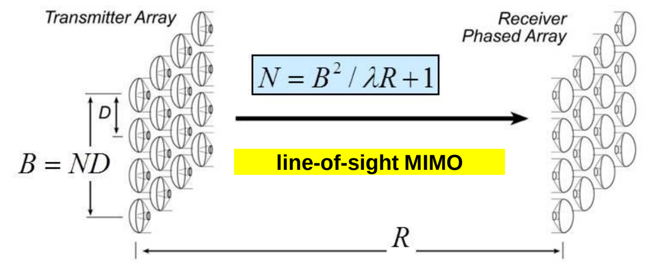


(note high attenuation in foul weather)

Massive # parallel channels

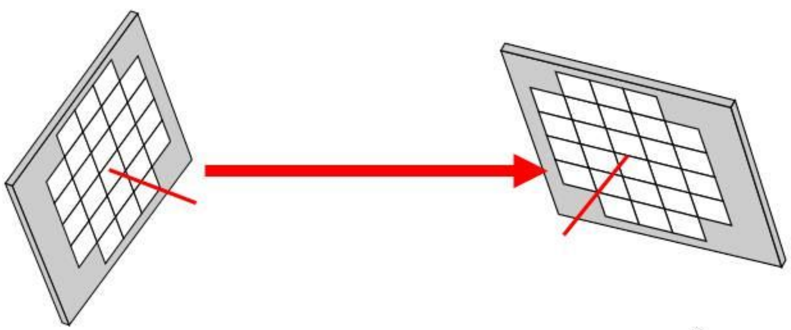


$$\text{angular resolution} \approx \frac{\text{wavelength}}{\text{array width}}$$



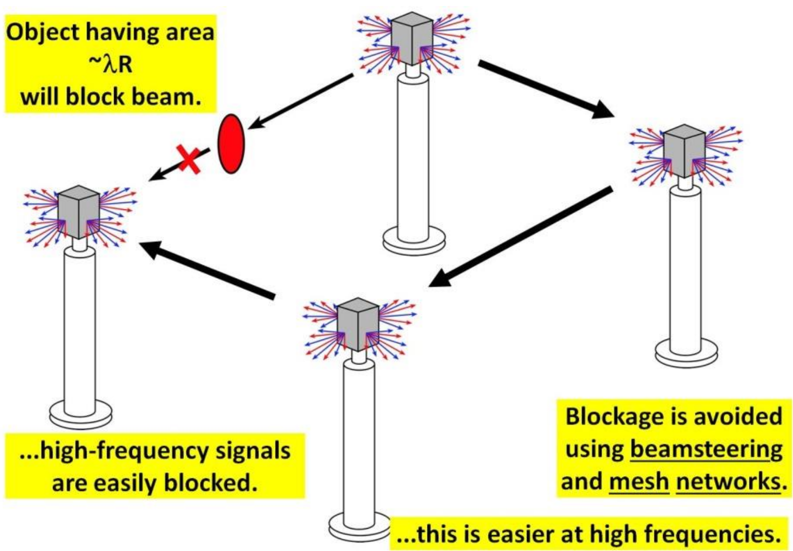
$$\#\text{channels} \propto (\text{aperture area})^2/(\text{wavelength} \cdot \text{distance})^2$$

Need phased arrays (overcome high attenuation)



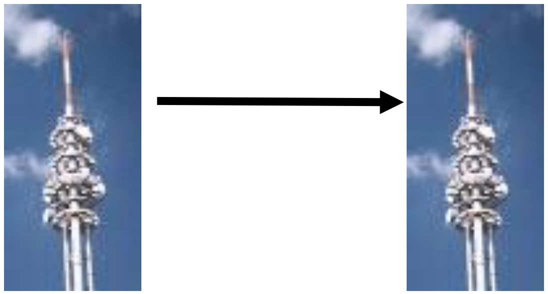
$$\frac{P_{received}}{P_{transmit}} \propto N_{receive} N_{transmit} \frac{\lambda^2}{R^2} e^{-\alpha R}$$

Need mesh networks



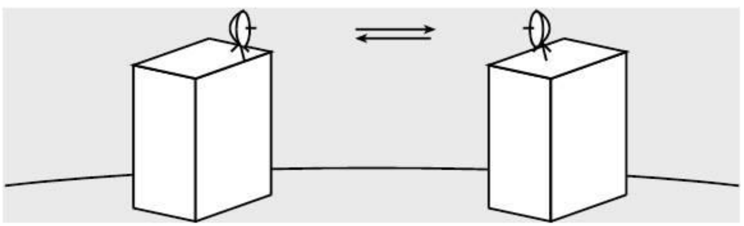
mm-Wave Wireless Needs Phased Arrays

isotropic antenna → weak signal → short range



$$\left(\frac{P_{received}}{P_{transmitted}}\right) \propto \left(\frac{\lambda^2}{R^2}\right) e^{-\alpha R}$$

highly directional antenna → strong signal, but must be aimed

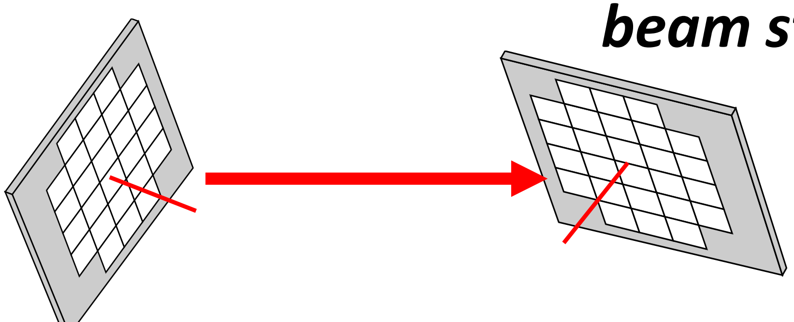


$$\left(\frac{P_{received}}{P_{transmitted}}\right) \propto D_t D_r \left(\frac{\lambda^2}{R^2}\right) e^{-\alpha R}$$

no good for mobile

must be precisely aimed → too expensive for telecom operators

beam steering arrays → strong signal, steerable

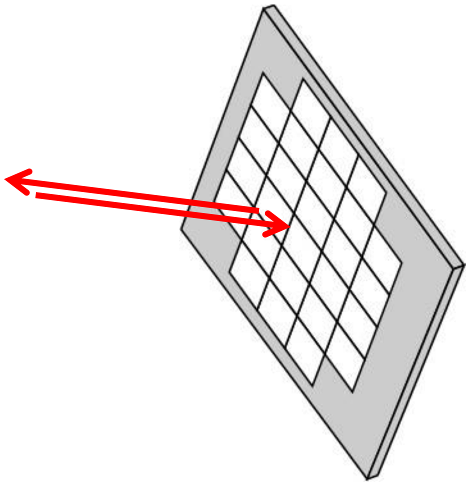


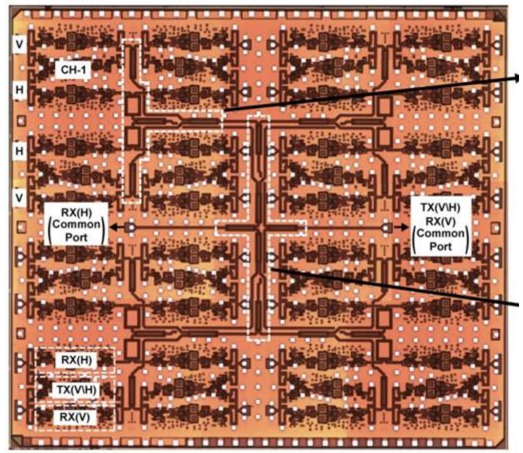
$$\frac{P_{received}}{P_{transmit}} \propto N_{receive} N_{transmit} \frac{\lambda^2}{R^2} e^{-\alpha R}$$

32-element array → 30 (45?) dB increased SNR

Millimeter-wave imaging

10,000-pixel, 94GHz imaging array→ 10,000 elements





Golcuk: Trans MTT, Aug 2014

Demonstrated:

SiGe (UCSD/Rebeiz)

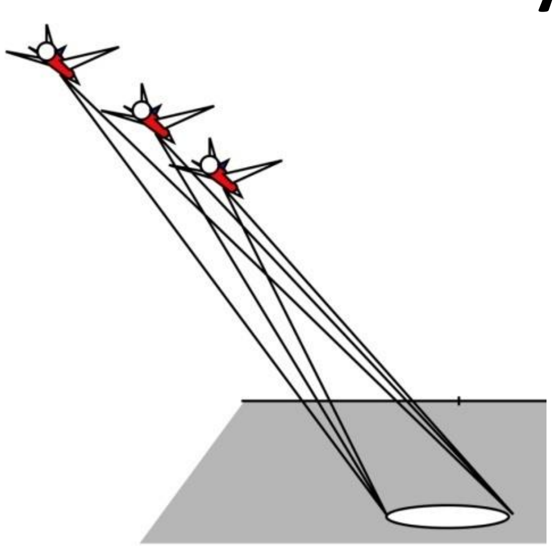
~1.3kW: 10,000 elements

Lower-power designs:

InP, CMOS, SiGe

(UCSB, UCSD, Virginia Poly.)

235 GHz video-rate synthetic aperture radar



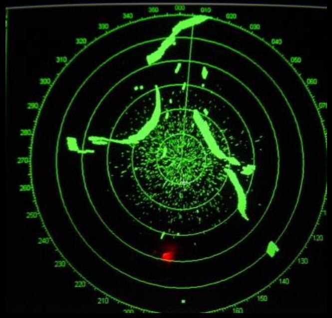
1 transmitter, 1 receiver
100,000 pixels
20 Hz refresh rate
5 cm resolution @ 1km
50 Watt transmitter
(tube, solid-state driver)

mm-wave imaging radar: TV-like resolution

mm-waves → high resolution from small apertures

What you see in fog

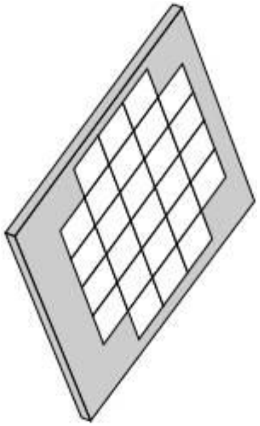
What 10GHz radar shows



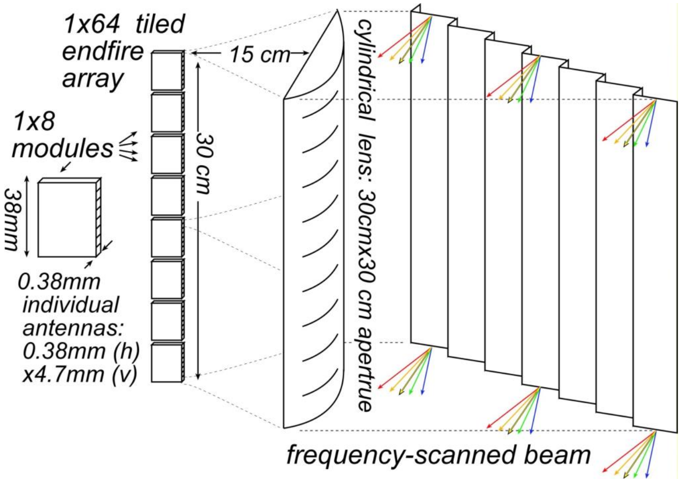
What you want to see

goal: ~0.2^o resolution, 10^3-10^6 pixels

Large NxN phased array

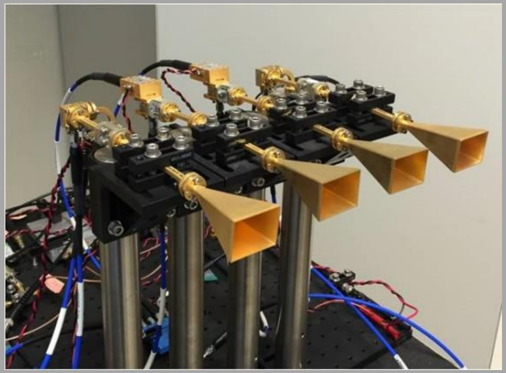


Frequency-scanned 1xN array

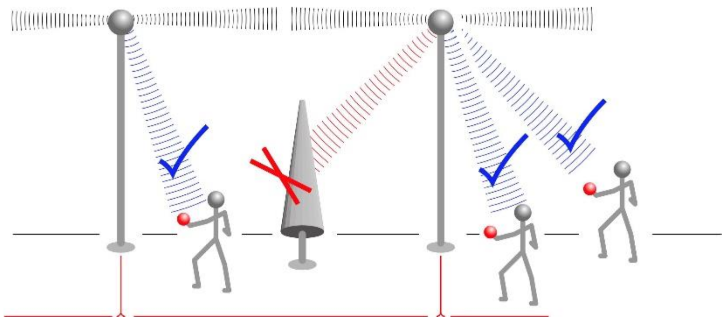


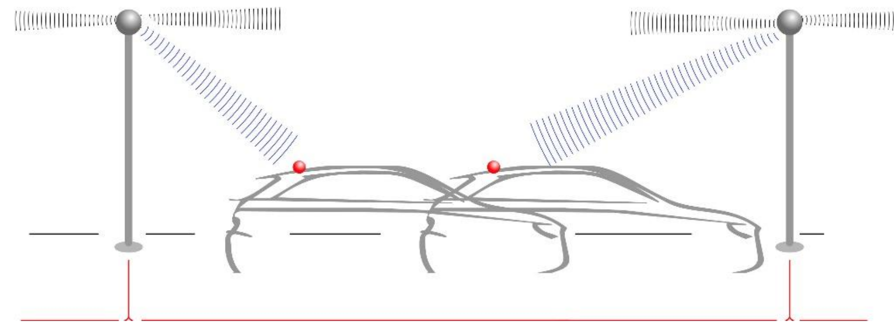
ultimate: ~400 GHz; intermediate: ~140 GHz

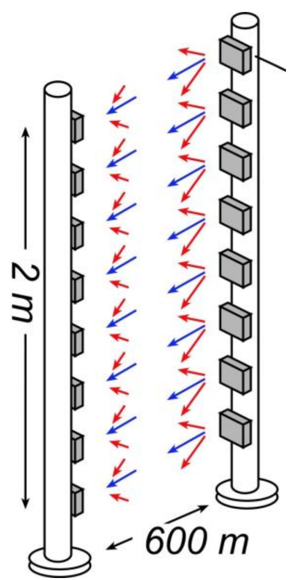
mm-wave systems

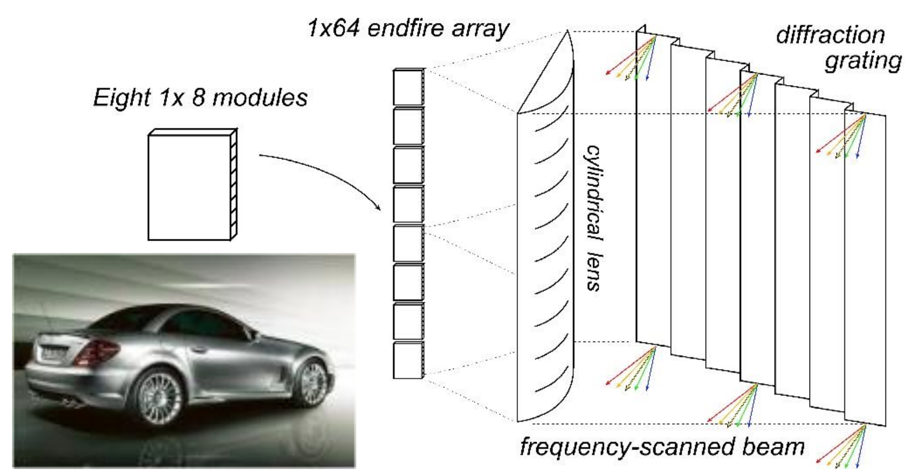


Target Systems









arrays

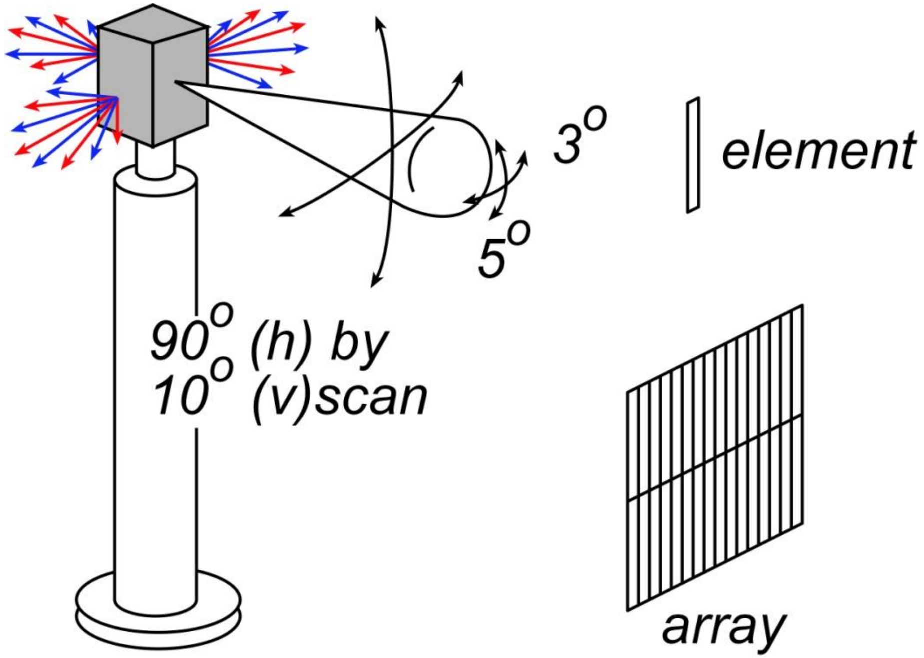
Antenna & array basics

Overall array sets beamwidth and gain

$$\text{horizontal beamwidth} \cong \frac{\lambda}{\text{array width}} \text{ (radians)}$$

$$\text{vertical beamwidth} \cong \frac{\lambda}{\text{array height}}$$

$$\text{Gain (directivity)} \cong \frac{4\pi \cdot \text{array area}}{\lambda^2}$$



Individual element sets maximum beamsteering range.

$$\text{horizontal steering} \cong \frac{\lambda}{\text{element width}} \text{ (radians)}$$

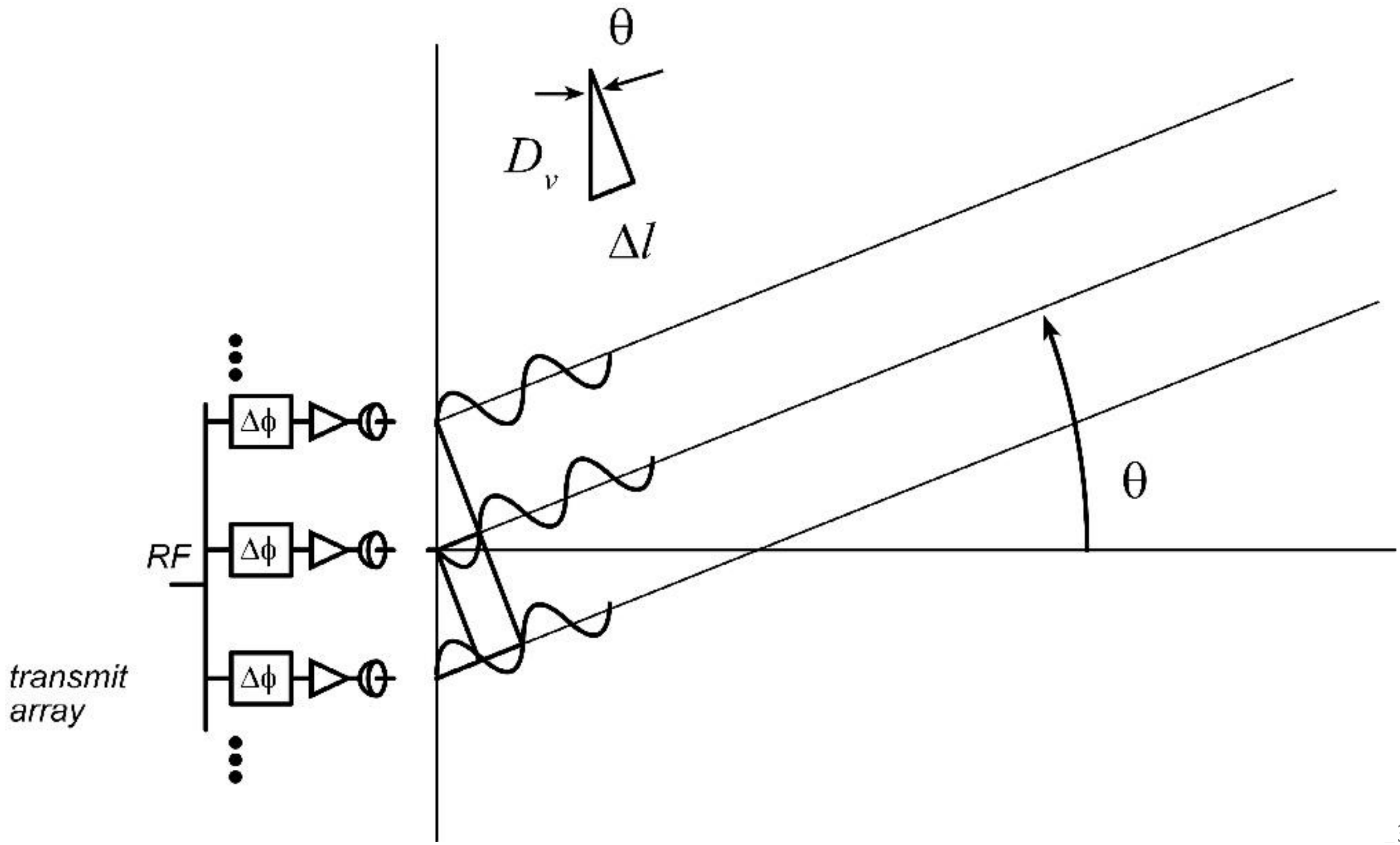
$$\text{vertical steering} \cong \frac{\lambda}{\text{element height}}$$

Electronic Beamsteering, a.k.a. phased array

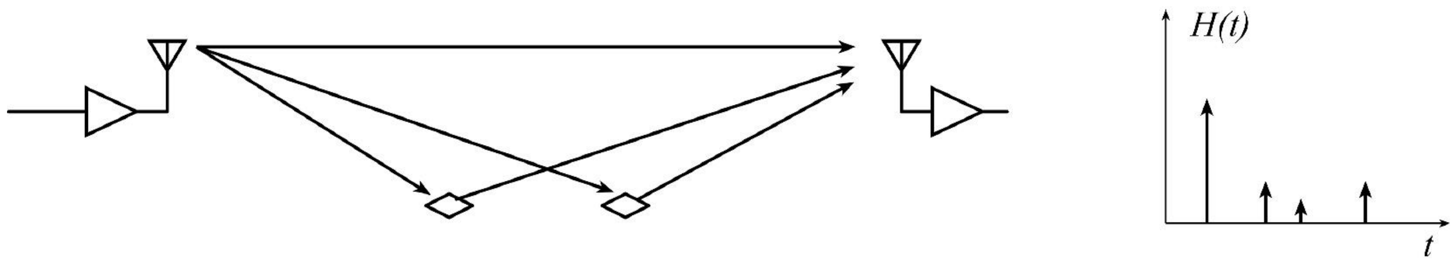
Phase - shifters bring signals back into phase at physical angle θ.

Path length difference $\Delta l = D_v \sin\theta$

Required electrical phase shift between adjacent elements $\Delta\phi = 2\pi \cdot \Delta l / \lambda$.



Reminder: Multipath Propagation



Given large angular beamwidth (low - directivity antennas)

Many objects in antenna beam pattern.

Many signal paths : multi - path propagation

Each path has different length, different delay.

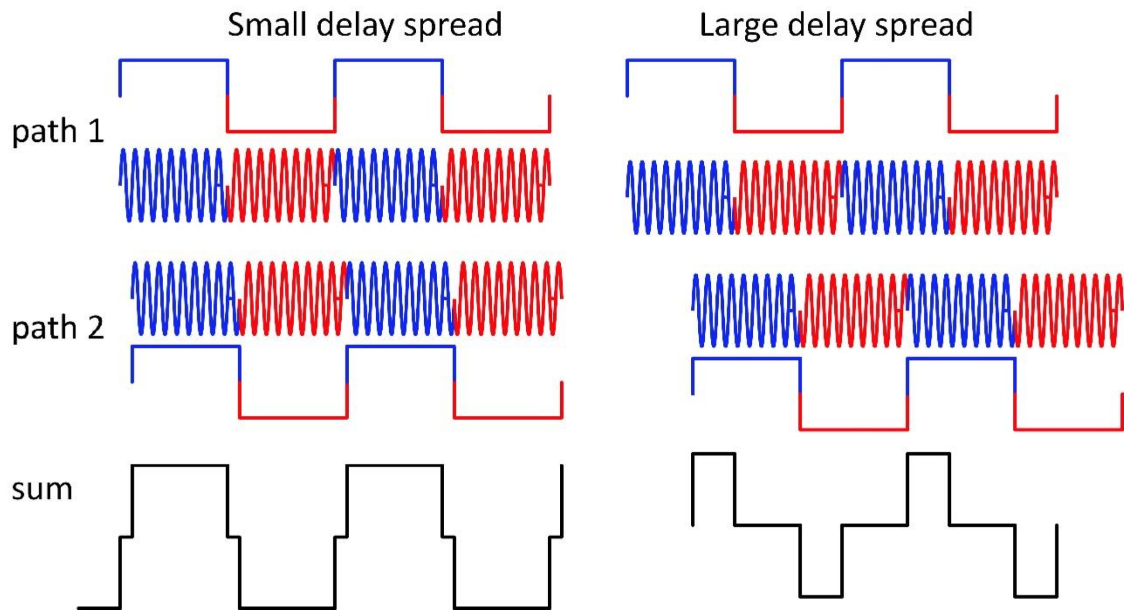
Reflecting surface boundary condition : possible phase shift.

Each path has different signal strenght

Directivity of antennas

Strenght of reflection

Fading vs Intersymbol interference



(Delay spread << Symbol period) $\rightarrow$ Fading

LOS and NLOS signals arrive with symbol periods ~ aligned

Carriers are out of phase $\rightarrow$ interference $\rightarrow$ possibly very weak signal

fix : two receiving antennas at appropriate separation

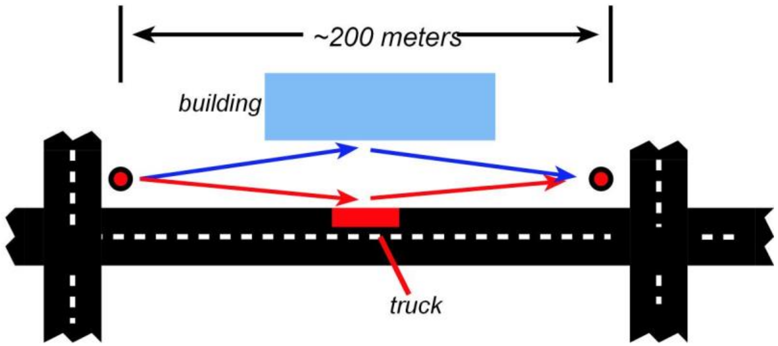
(Delay spread > Symbol period) $\rightarrow$ Intersymbol interference

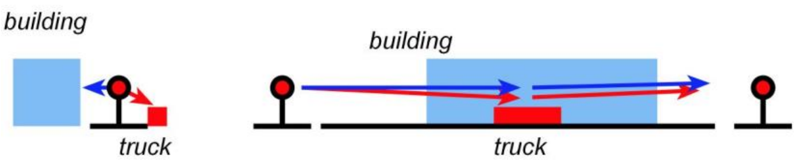
One bit period interfers with another

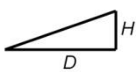
need adapitive equalizer in receiver

or use ODFM :longer symbol periods

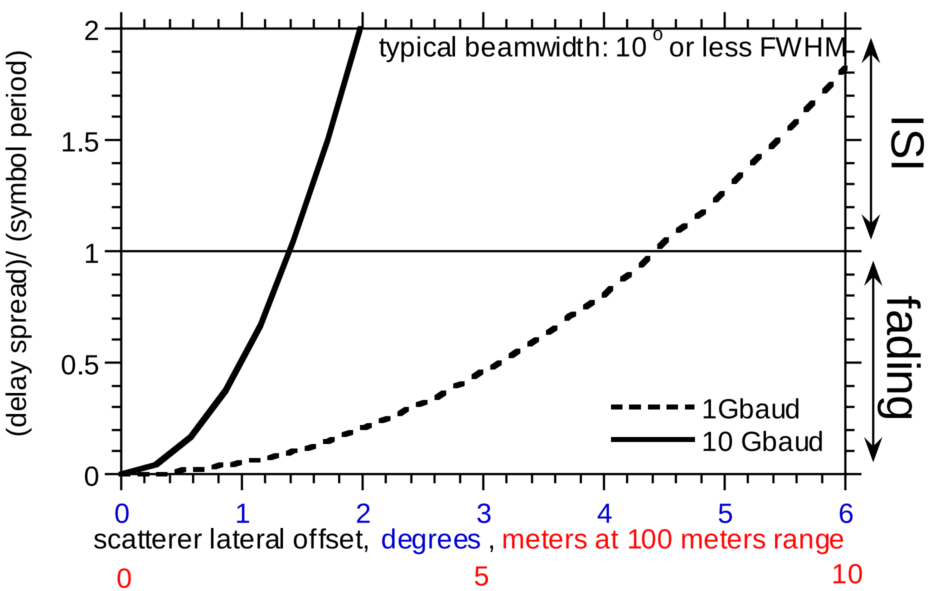
Beamforming can suppress ISI







$$\text{Delay spread} \cong \frac{H^2}{2Dc}$$

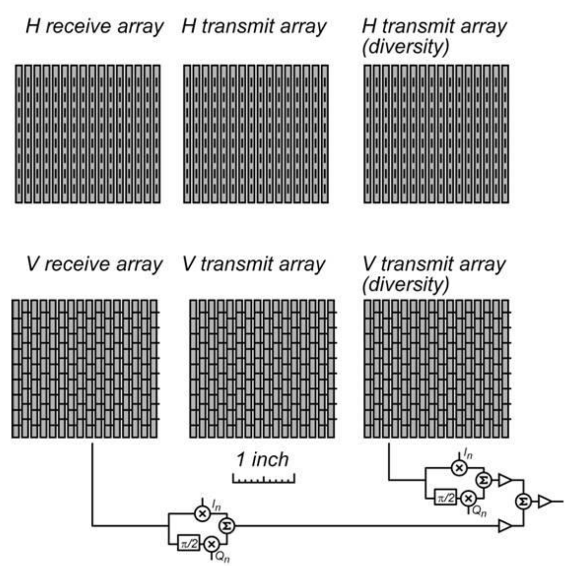


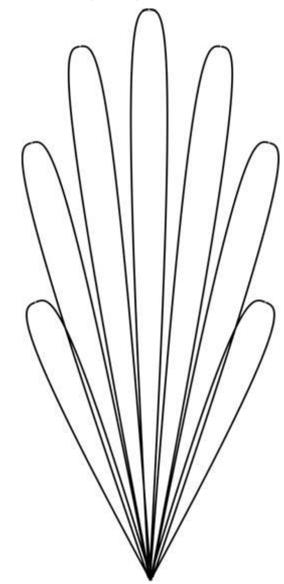
1 Gbaud with 10° array beamwidth :
multipath mostly causes fading
not much ISI

10 Gbaud with 10° array beamwidth :
significant fading and significant ISI

Solution 1: larger arrays
narrower beamwidth

Solution 2: multiple arrays
multiple receivers to handle fading ?
can sum these to form narrow nulls!
also handles fading and ISI



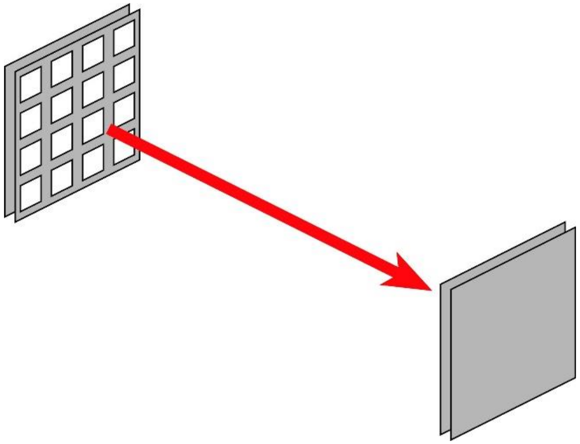


Optimum array size for low system power

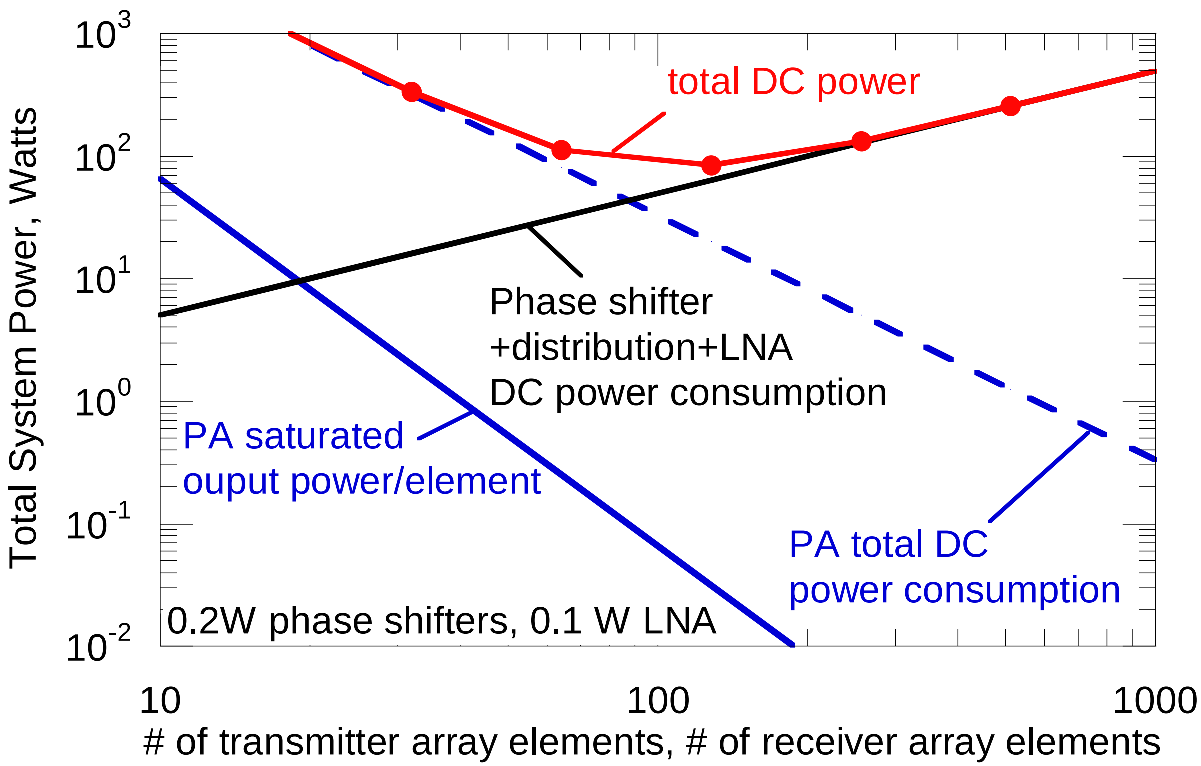
$$\frac{P_{receive}}{P_{transmit}} \propto N^2 \frac{\lambda^2}{R^2} \longrightarrow P_{transmit} \propto \frac{1}{N^2}$$

Do large arrays save power ?

$$\text{Total system power} = \frac{P_{transmit}}{\text{efficiency}} + N(\text{power of LNA, phase shifters...})$$

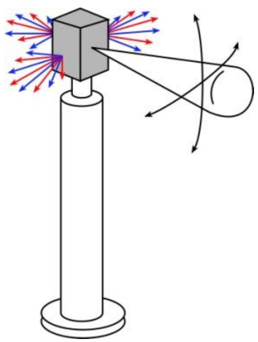


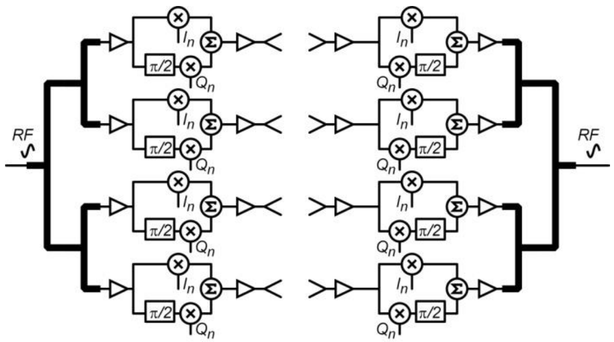
At optimum-size array, target PA output power is typically 10-200 mW

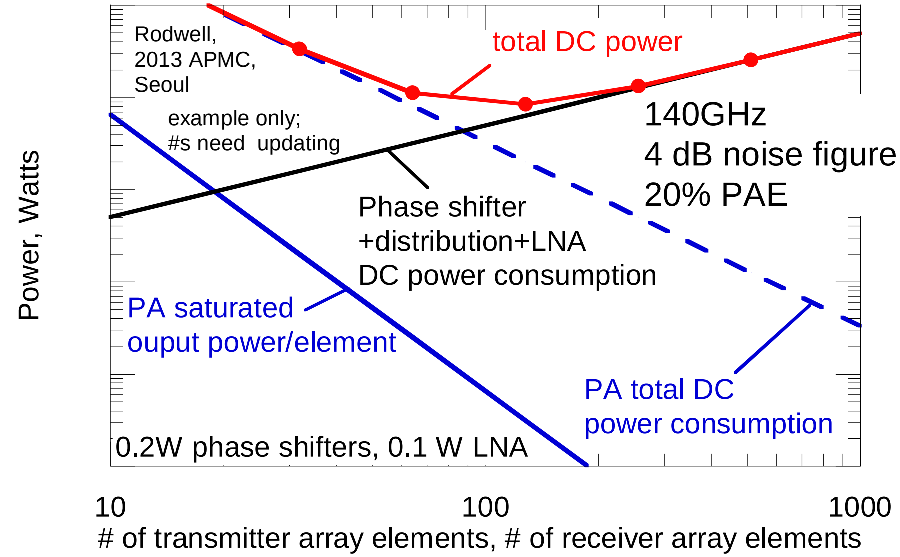


How big should be the array ?

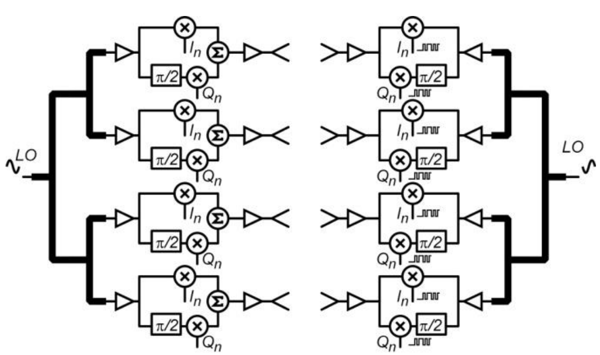
Large arrays:
more directive→ less PA power needed
more channels→ cost, DC power

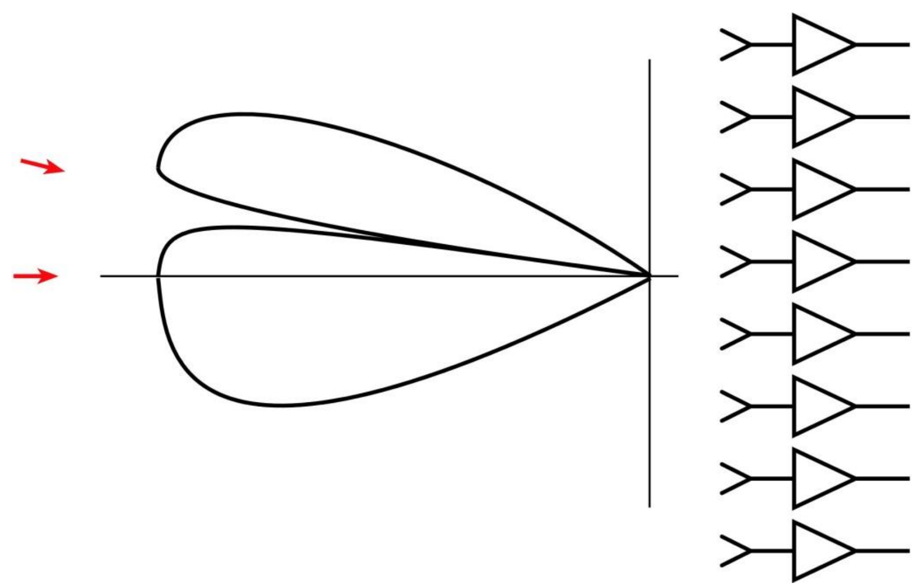






Large arrays:
more directive→
less SNR loss with NLOS nulling
eases multipath equalization



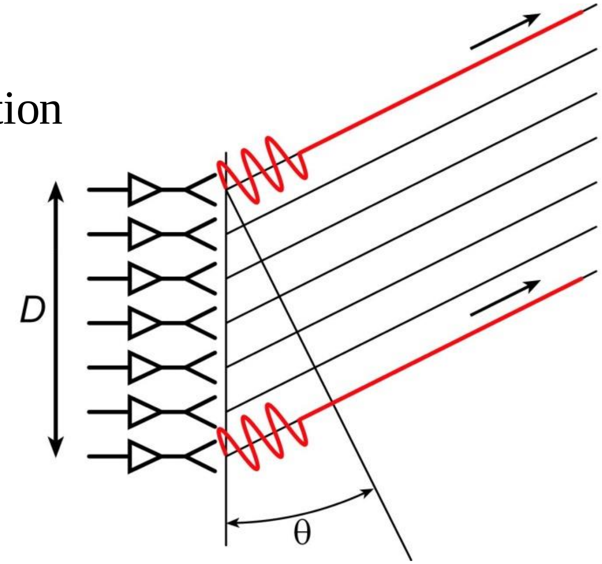


Data delay equalization in large arrays

Simple arrays retime the carrier but not the modulation

$$\text{timing skew} = \frac{D\sin\theta}{c}\text{; must be below} \sim T_{symbol}/2$$

$$\rightarrow \text{bandwidth} \approx \frac{c}{D\sin\theta}$$

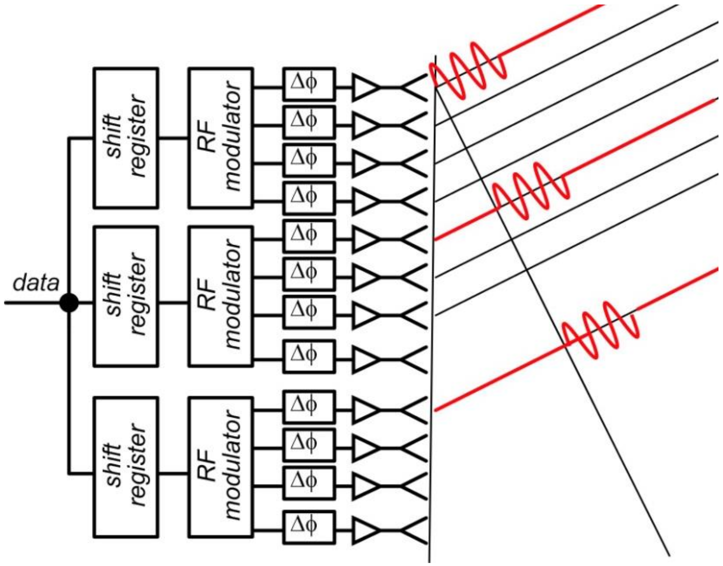


Very large arrays :

compensate by *array tiling*

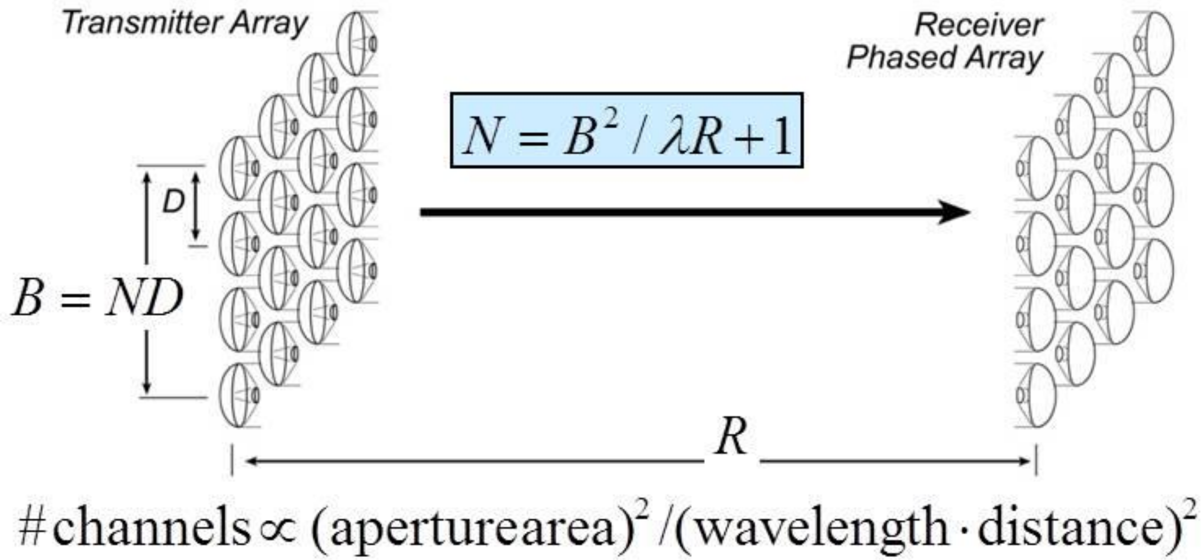
with modulation retimed

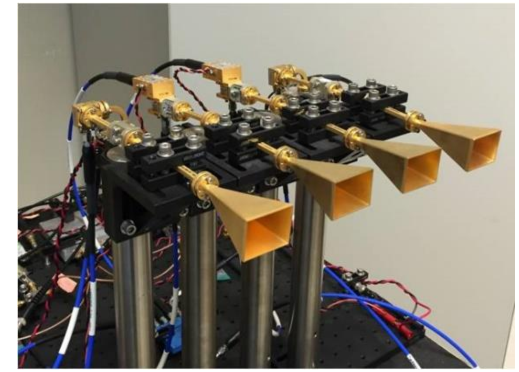
between tiles

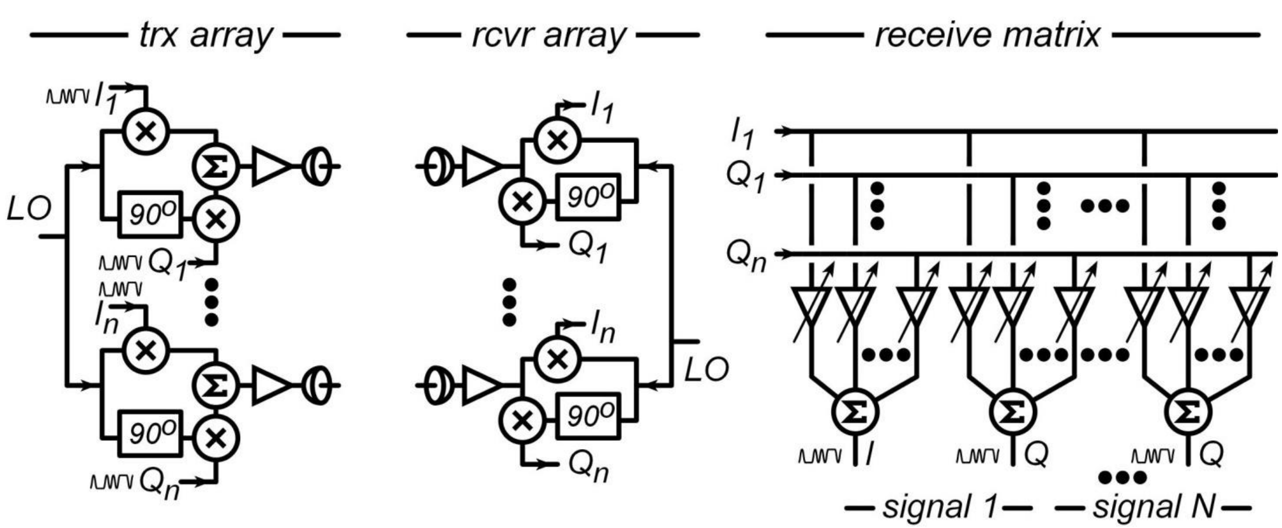


systems

mm-Wave LOS MIMO: multi-channel for high capacity





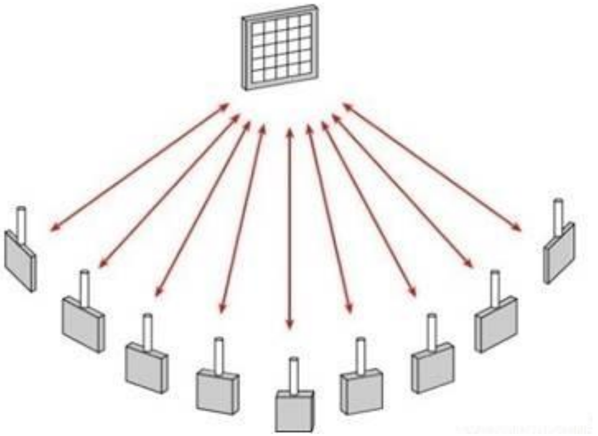


Torklinson : 2006 Allerton Conference
Sheldon : 2010 IEEE APS-URSI
Torklinson : 2011 IEEE Trans Wireless Comm.

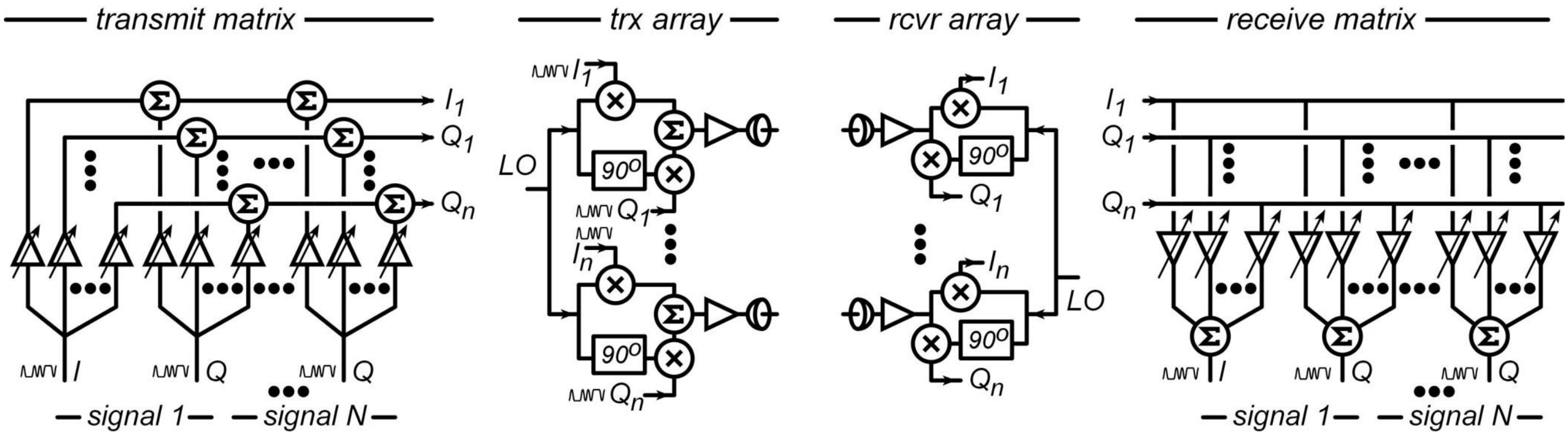
Spatial Multiplexing: massive capacity RF networks

multiple independent beams

each carrying different data
each independently aimed
beams = # array elements

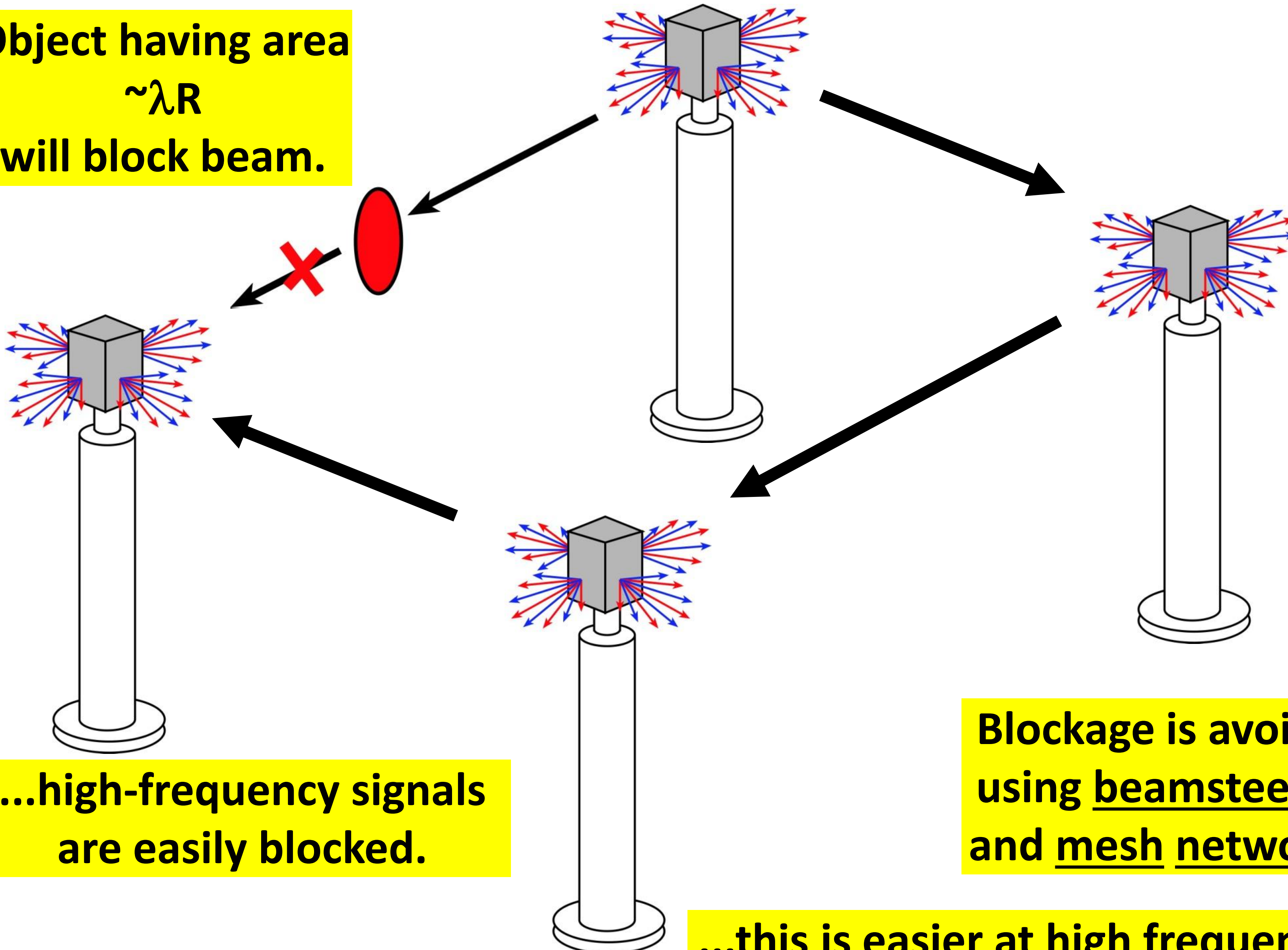


Hardware: multi-beam phased array ICs



100-1000 GHz Wireless Needs Mesh Networks

Object having area ~λR will block beam.



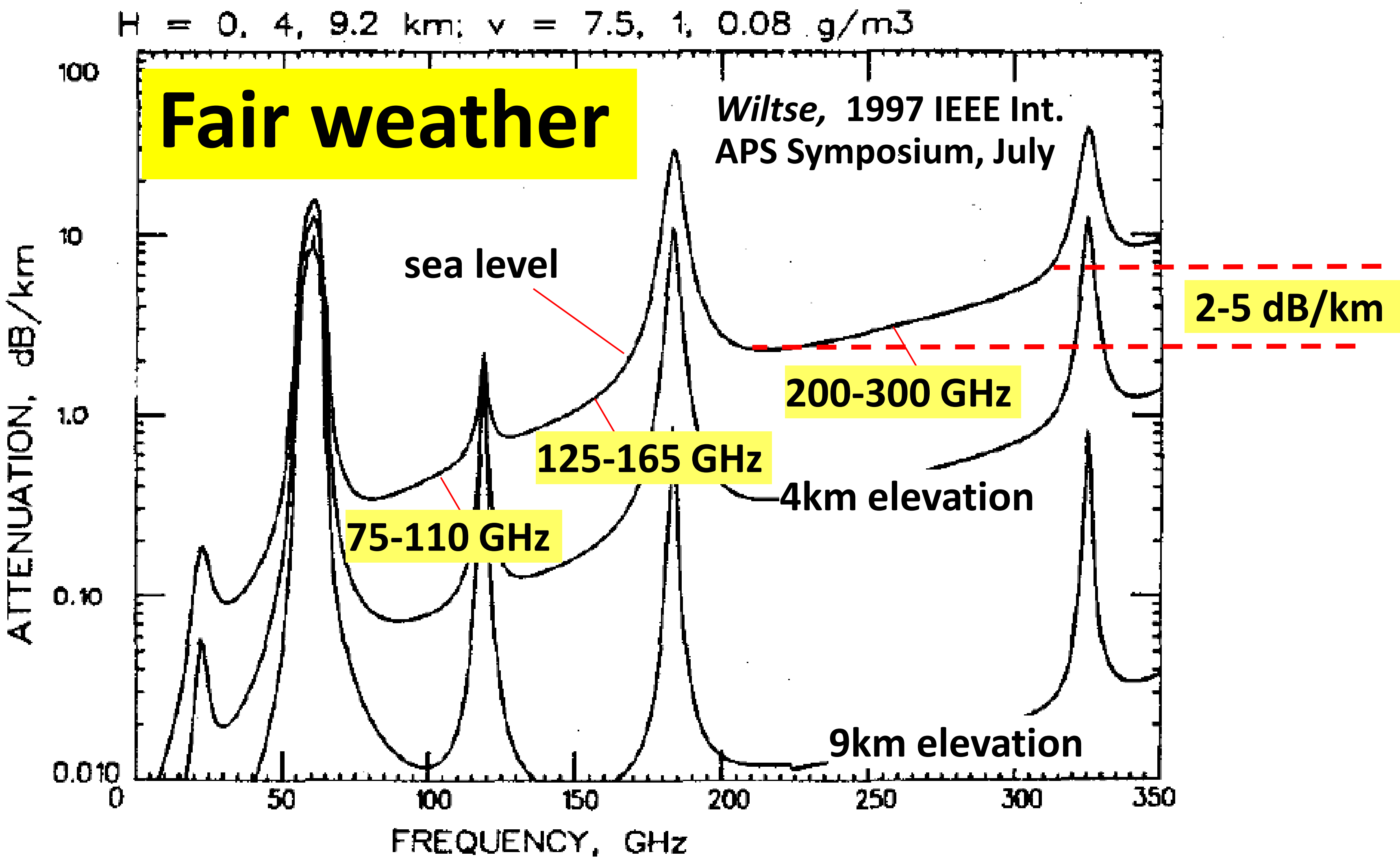
...high-frequency signals are easily blocked.

Blockage is avoided using <u>beamsteering</u> and <u>mesh</u> <u>networks</u>.

...this is easier at high frequencies.

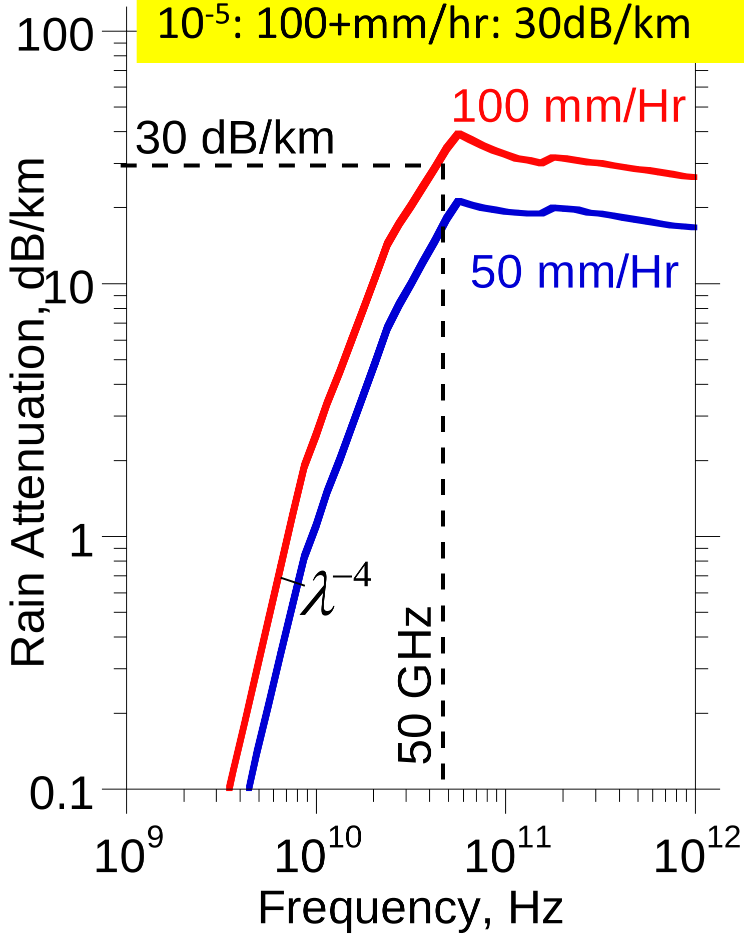
mm-wave propagation

Fair-Weather Propagation



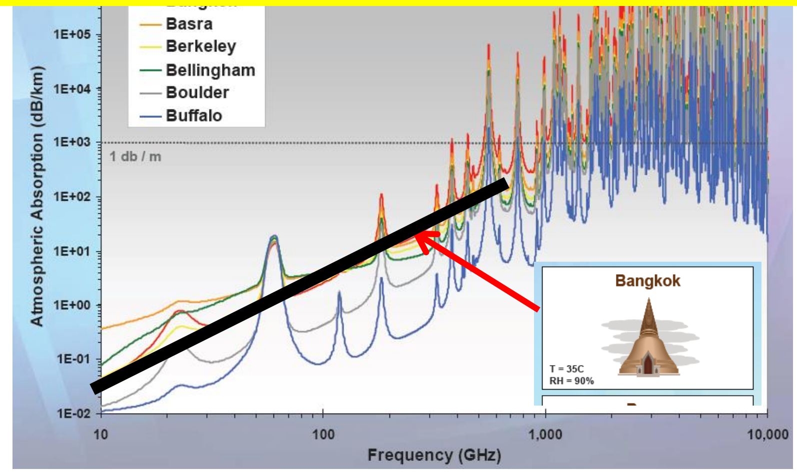
Foul Weather Propagation

Rain:
10^{-3}: 25mm/hr, 11dB/km
10^{-4}: 50-85mm/hr, 19dB/km
10^{-5}: 100+mm/hr: 30dB/km



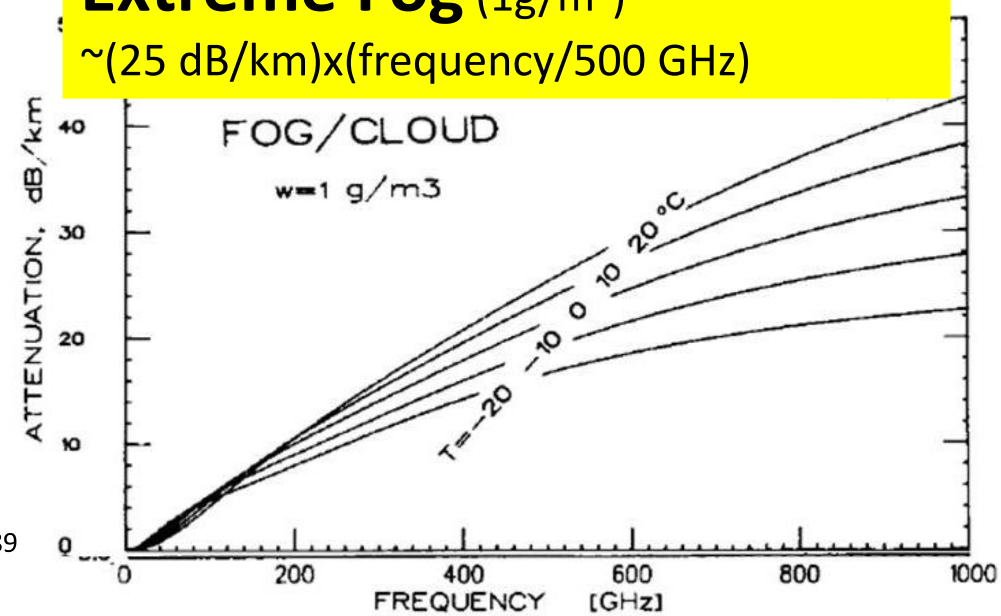
Olsen, Rogers, Hodge, IEEE Trans Antennas & Propagation Mar 1978
Liebe, Manabe, Hufford, IEEE Trans Antennas and Propagation, Dec. 1989
Liebe, IEEE Trans Ant and Pro, Vol 31, No. 1, Jan 1983
Karasawa, Maekawa, IEEE Proc, Vol 85 , #6 , June 1997

35°C, 95% Humidity
loss (dB/km)~(frequency/60GHz)^2
11 dB/km@200 GHz, 5.5dB/km@140GHz

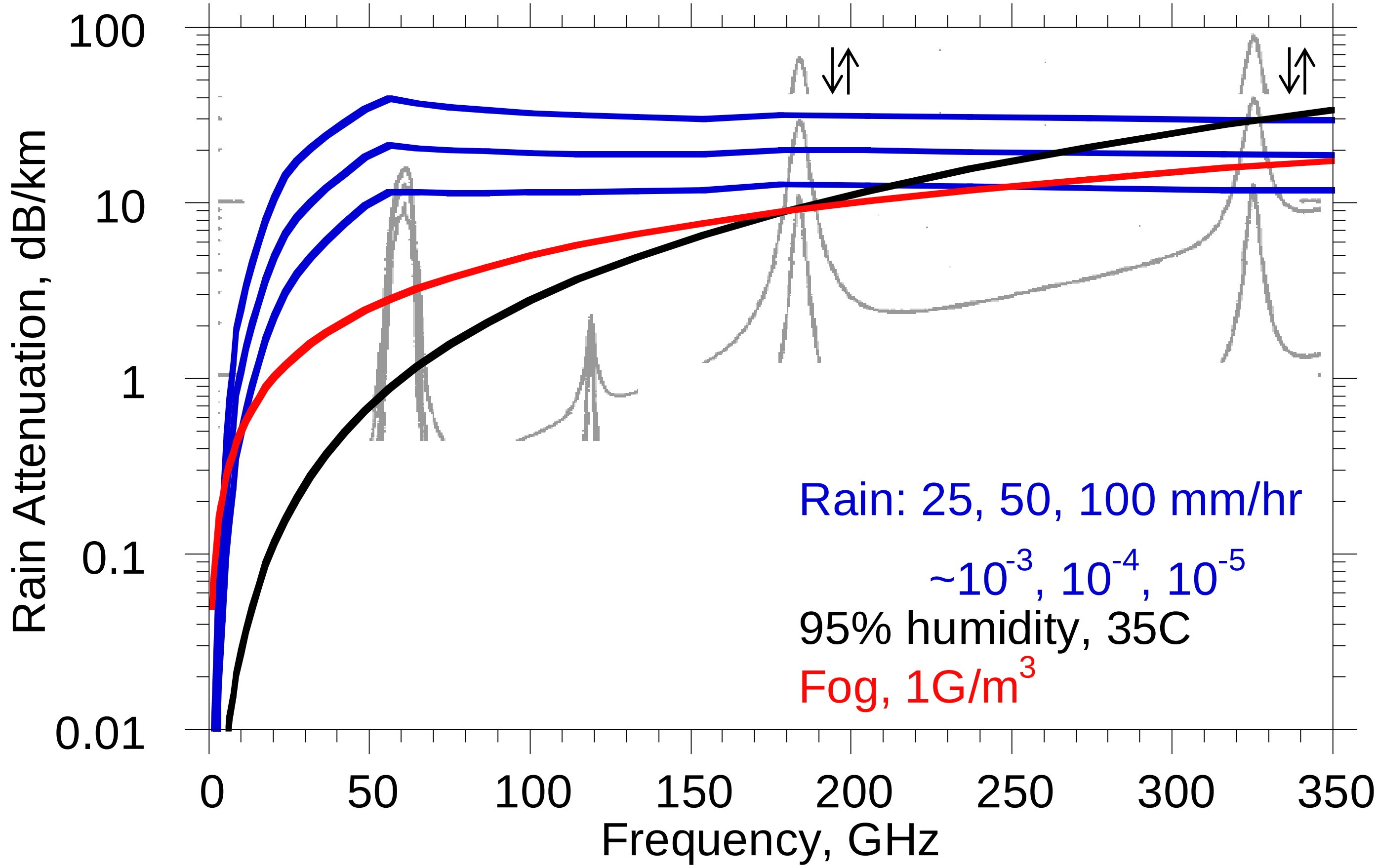


Rosker; Wallace, 2007 IEEE IMS

Extreme Fog (1g/m^3)
~(25 dB/km)x(frequency/500 GHz)



Atmospheric Attenuation: Implications



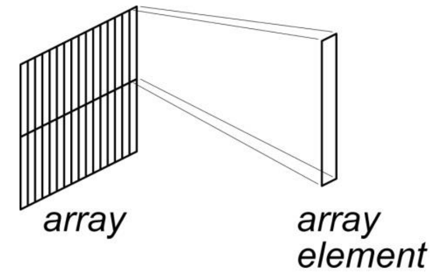
Worst-case attenuation roughly constant over 50-250 GHz.
10^{-5} outage rate: equal losses over 50-300 GHz
10^{-3} outage rate: equal losses over 50-200 GHz

target should be 50-250 GHz links.
Exclusive use of VLSI Si processes forces use of 50-180GHz

detailed
link analysis

Example Link budgets (60 GHz)

To calculate RANGE, vary the range until the transmit power (cell F4) is at the appropriate level				30			
B: Bit rate	1.00E+10	1/sec	4QAM required radiated power	-1.9	dBm	6.426E-04	W
carrier frequency	6.00E+10	Hz	output power per element	-12.0	dBm	6.37E-05	W
λ: wavelength	5.00E-03	m	PA backoff (Ppeak vs Psat)	3.0	dB		
Required SNR (measured as Eb/No)	6.3	dB	PA saturated output power	-9.0	dBm	1.27E-04	W
Receiver bandwidth	2.16E+09	Hz	EIRP	29.7	dBm		
SNR (measured as kTFB, B from above cell)	13.0	dB	dB EIRP below FCC limits	10.3	dB		
F: receiver noise figure	4.5	dB	Transmitter				
R: transmission range	50.0	m	A_effective	2.89E-03	meters^2	115.49	Wavelengths^2
atmospheric loss	2.653E-02	dB/m	Vertical beam angle, FWHM	2.5	deg	0.0436	radians
Dant, trans transmit antenna directivity	1.45E+03	none	Horizontal beam angle, FWHM	11.3	deg	0.1972	radians
Dant, rcvr receive antenna directivity	1.45E+03	none	array rows and columns	2	# rows	8	# columns
α: bandwidth factor (0.5<α<1)	0.80		total # array elements	16			
radiated channel bandwidth required	8000.0	MHz	vertical angle scanned, total	5.0	deg		
			horizontal angle scanned, total	90.4	deg		
			array height	22.9	wavelengths		
			array width	5.1	wavelengths		
			array height	1.15E-01	meters	4.51	inches
			array width	2.54E-02	meters	1.00	inches
kT	-173.83	dBm (1Hz)	Antenna directivity, dB	31.62	dB		
packaging loss (receiver)	2	dB	Receiver				
packaging loss (transmitter)	2	dB	A_effective	2.89E-03	meters^2	115.49	Wavelengths^2
end-of-life hardware degradation	3	dB	Vertical beam angle, FWHM	2.5	deg	0.0436	radians
hardware design margin	3	dB	Horizontal beam angle, FWHM	11.3	deg	0.1972	radians
beam aiming loss (edge of beam)	3	dB	array rows and columns	2	# rows	8	# columns
systems operating margin	6	dB	vertical angle scanned, total	5	deg		
Prec, received power at 1E-9 BER	-46.00	dBm	horizontal angle scanned, total	90.4	deg		
geometric path loss	1.33E-04		array height	2.3E+01	wavelengths		
geometric path loss, dB	-38.75	dB	array width	5.1E+00	wavelengths		
path obstruction loss (foliage, glass)	4.00	dB	array height	1.15E-01	meters	4.51	inches
atmospheric loss, dB	1.3265581	dB	array width	2.54E-02	meters	1.00	inches
atmospheric loss	26.53	dB/km	Antenna directivity, dB	31.62	dB		



array:
16 elements (2x8)
4.5 x 1.0 inches
11.5 x 2.54 cm

$$P_{received(4QPSK)} = Q^2 \cdot kTFB \quad \text{where } Q = \text{SNR}$$

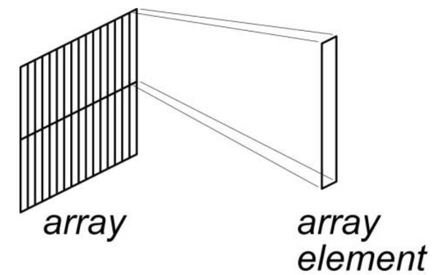
$$P_{received} / P_{trans} = (D_t D_r / 16\pi^2)(\lambda / R)^2$$

$$D = 4\pi A_{eff} / \lambda^2 \cong \frac{4\pi}{\theta_{FWHM}^{radians} \phi_{FHWM}^{radians}} \cong \frac{41{,}000}{\theta_{FWHM}^{o} \phi_{FHWM}^{o}}$$

Note various margins allocated.
Rain losses calculated from rain rate.

Example Link budgets (140 GHz)

This spreadsheet calculates power levels for 4QPSK point-point digital microwave radio links along the surface							
To calculate RANGE, vary the range until the transmit power (cell F4) is at the appropriate level				30			
B: Bit rate	1.00E+10	1/sec	4QAM required radiated power	6.1	dBm	4.087E-03	W
carrier frequency	1.40E+11	Hz	output power per element	-3.9	dBm	4.05E-04	W
λ: wavelength	2.14E-03	m	PA backoff (Ppeak vs Psat)	3.0	dB		
Required SNR (measured as Eb/No)	6.3	dB	PA saturated output power	-0.9	dBm	8.08E-04	W
Receiver bandwidth	5.00E+09	Hz	EIRP	37.7	dBm		
SNR (measured as kTFB, B from above cell)	9.3	dB	dB EIRP below FCC limits	2.3	dB		
F: receiver noise figure	6	dB	Transmitter				
R: transmission range	50.0	m	A_effective	5.30E-04	meters^2	115.49	Wavelengths^2
atmospheric loss	1.003E-02	dB/m	Vertical beam angle, FWHM	2.5	deg	0.0436	radians
Dant, trans transmit antenna directivity	1.45E+03	none	Horizontal beam angle, FWHM	11.3	deg	0.1972	radians
Dant, rcvr receive antenna directivity	1.45E+03	none	array rows and columns	2	# rows	8	# columns
α: bandwidth factor (0.5<α<1)	0.80		total # array elements	16			
radiated channel bandwidth required	8000.0	MHz	vertical angle scanned, total	5.0	deg		
			horizontal angle scanned, total	90.4	deg		
			array height	22.9	wavelengths		
			array width	5.1	wavelengths		
			array height	4.91E-02	meters	1.93	inches
			array width	1.09E-02	meters	0.43	inches
kT	-173.83	dBm (1Hz)	Antenna directivity, dB	31.62	dB		
packaging loss (receiver)	2	dB	Receiver				
packaging loss (transmitter)	2	dB	A_effective	5.30E-04	meters^2	115.49	Wavelengths^2
end-of-life hardware degradation	3	dB	Vertical beam angle, FWHM	2.5	deg	0.0436	radians
hardware design margin	3	dB	Horizontal beam angle, FWHM	11.3	deg	0.1972	radians
beam aiming loss (edge of beam)	3	dB	array rows and columns	2	# rows	8	# columns
systems operating margin	6	dB	vertical angle scanned, total	5	deg		
Prec, received power at 1E-9 BER	-44.50	dBm	horizontal angle scanned, total	90.4	deg		
geometric path loss	2.45E-05		array height	2.3E+01	wavelengths		
geometric path loss, dB	-46.11	dB	array width	5.1E+00	wavelengths		
path obstruction loss (foliage, glass)	4.00	dB	array height	4.91E-02	meters	1.93	inches
atmospheric loss, dB	0.5013679	dB	array width	1.09E-02	meters	0.43	inches
atmospheric loss	10.03	dB/km	Antenna directivity, dB	31.62	dB		



array:
16 elements (2x8)
1.9 x 0.43 inches
4.9 x 0.11 cm

$$P_{received(4QPSK)} = Q^2 \cdot kTFB \quad \text{where } Q = \text{SNR}$$

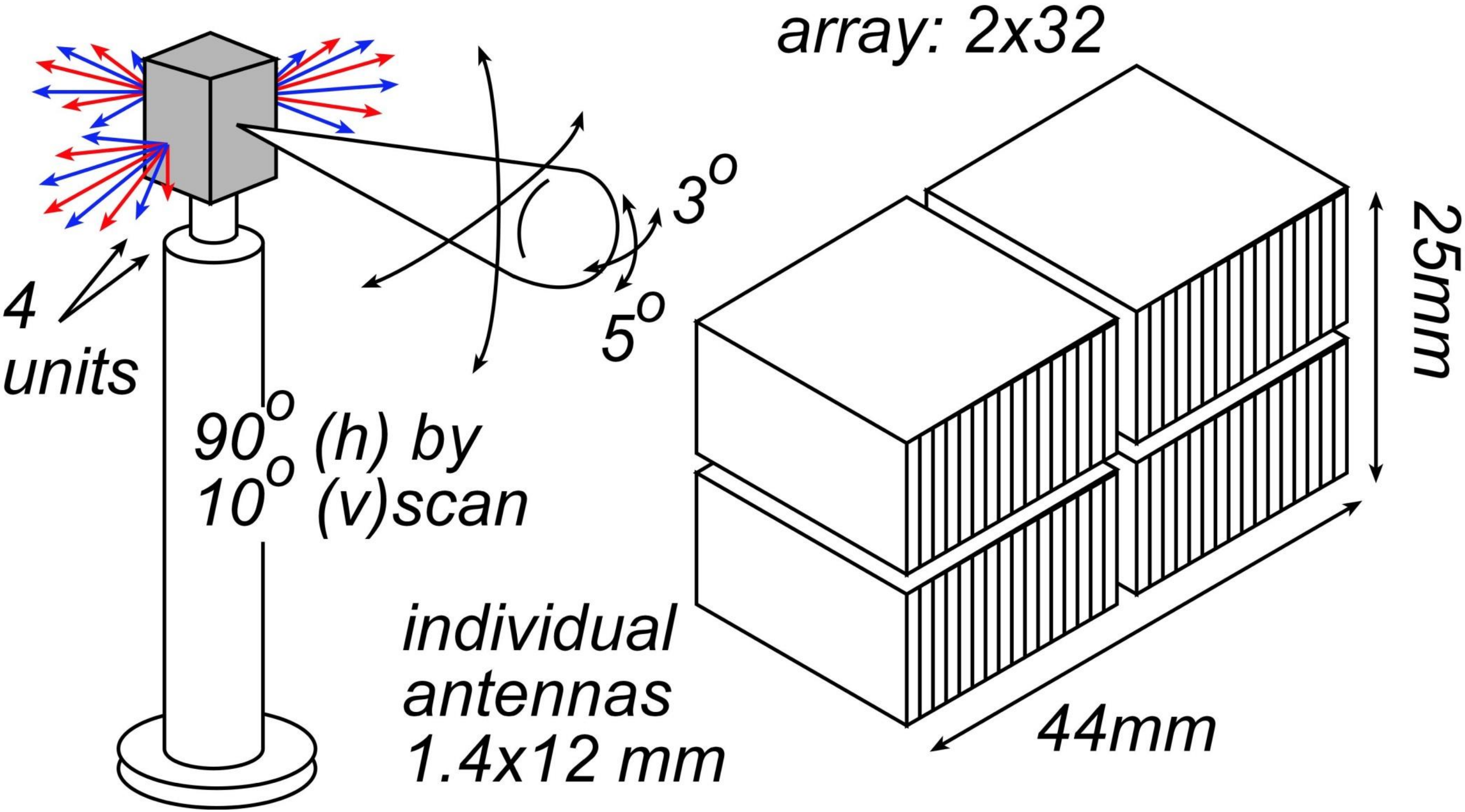
$$P_{received} / P_{trans} = (D_t D_r / 16\pi^2)(\lambda / R)^2$$

$$D = 4\pi A_{eff} / \lambda^2 \cong \frac{4\pi}{\theta_{FWHM}^{radians} \phi_{FHWM}^{radians}} \cong \frac{41{,}000}{\theta_{FWHM}^{o} \phi_{FHWM}^{o}}$$

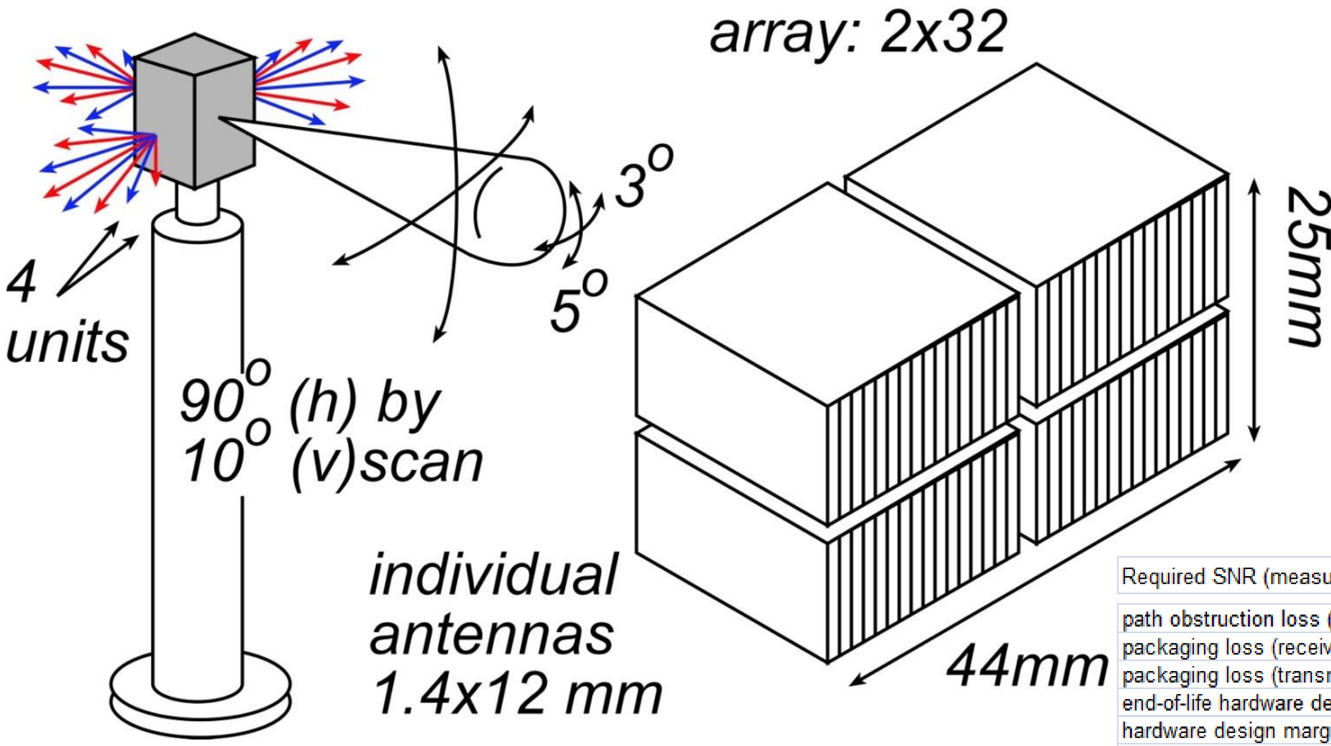
Note various margins allocated.
Rain losses calculated from rain rate.

hardware: rough numbers

140 GHz, 10 Gb/s Adaptive Picocell Backhaul



140 GHz, 10 Gb/s Adaptive Picocell Backhaul



Required SNR (measured as Eb/No)	6.8	dB
path obstruction loss (foliage, glass)	5.00	dB
packaging loss (receiver)	3	dB
packaging loss (transmitter)	3	dB
end-of-life hardware degradation	3	dB
hardware design margin	3	dB
beam aiming loss (edge of beam)	3	dB
systems operating margin	10	dB
PA backoff for OFDM	7.00E+00	dB

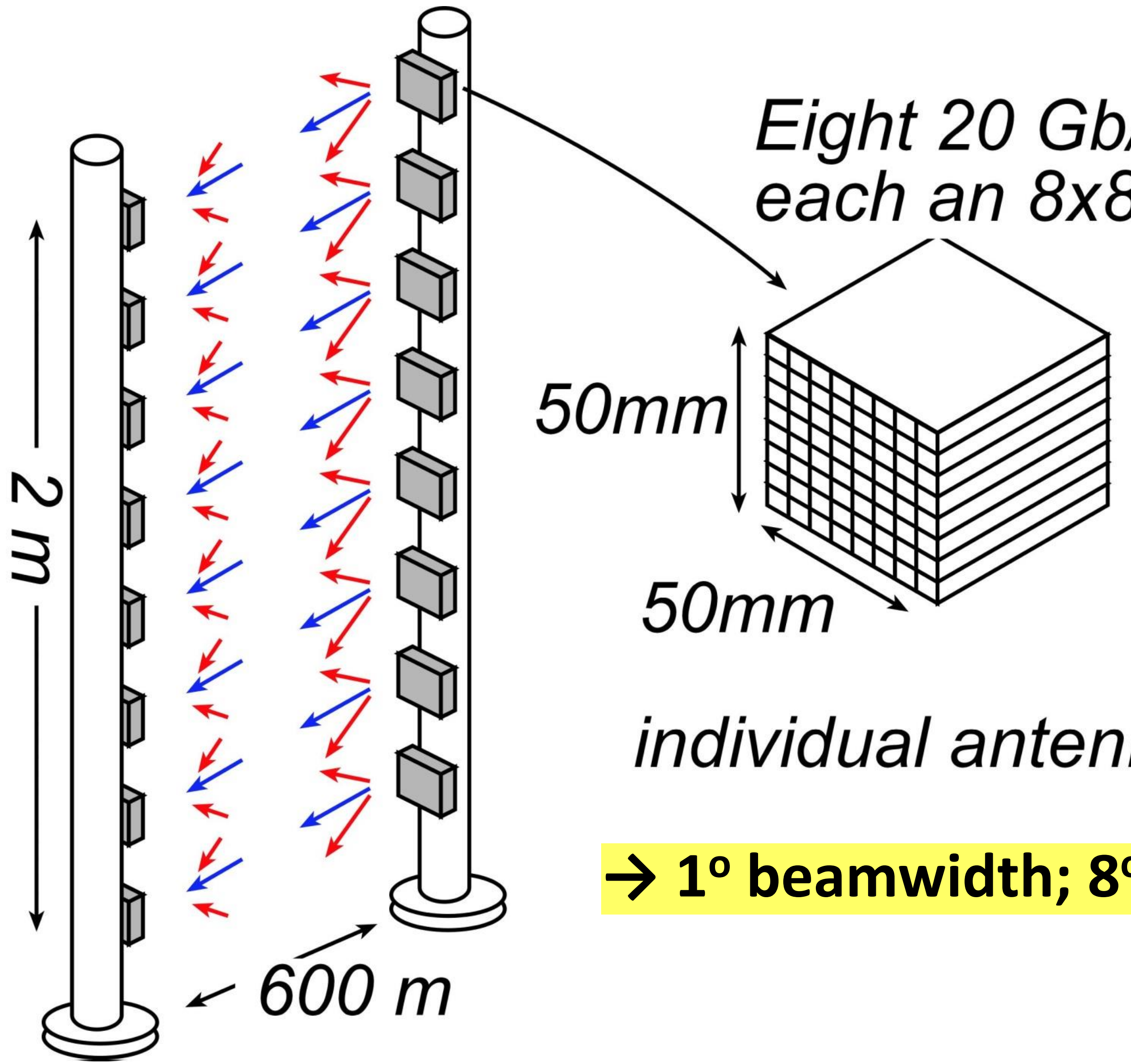
350 meters range in 50mm/hr rain

Realistic packaging loss, operating & design margins

PAs: 24 dBm P_{sat} (per element)

LNAs: 4 dB noise figure

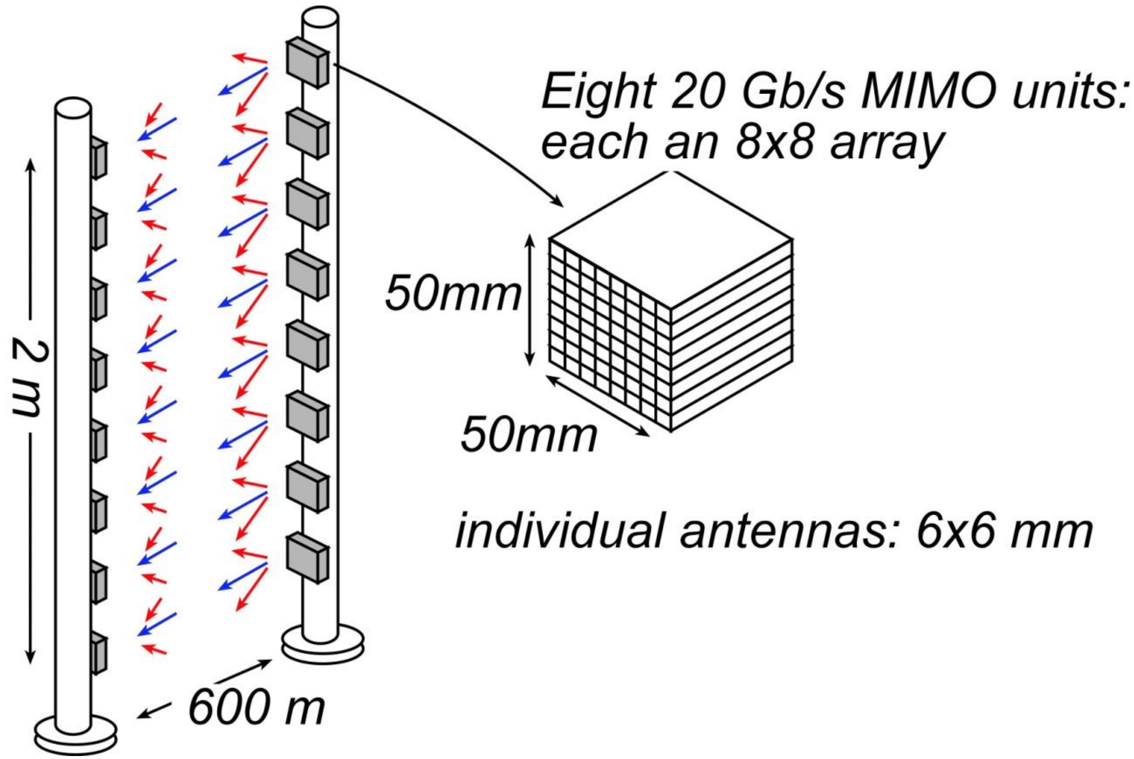
340 GHz, 160 Gb/s MIMO Backhaul Link



individual antennas: 6x6 mm

→ 1° beamwidth; 8° beamsteering

340 GHz, 160 Gb/s MIMO Backhaul Link



1° beamwidth; 8° beamsteering

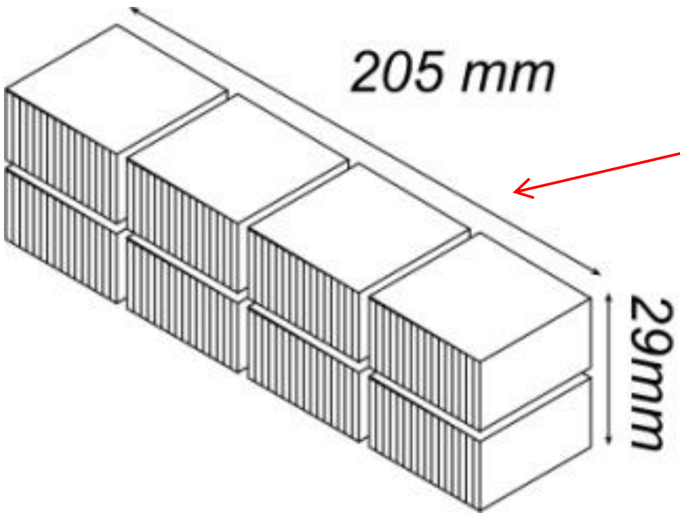
600 meters range in five-9's rain

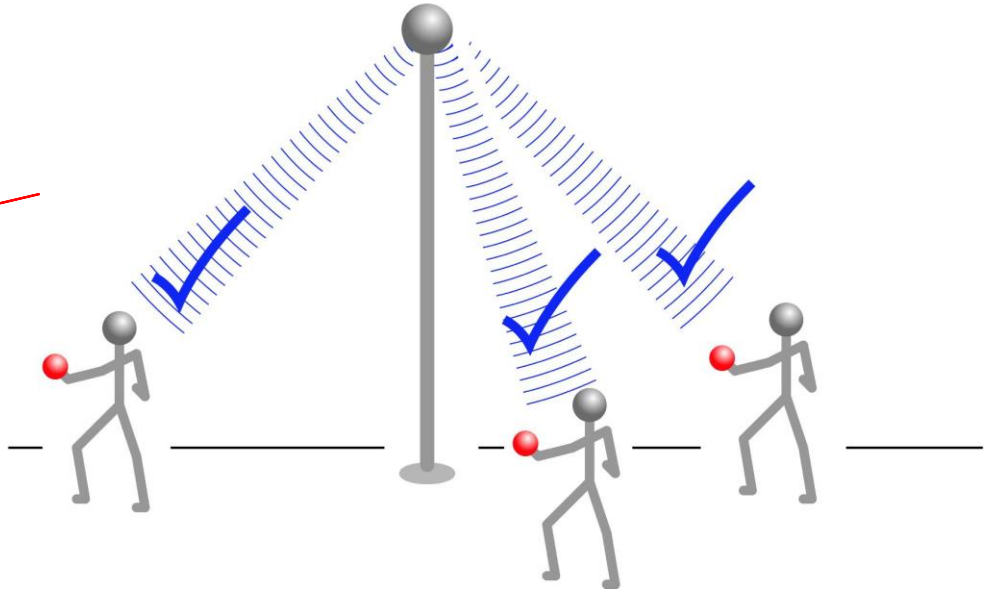
Realistic packaging loss, operating & design margins

PAs: 21 dBm P_{sat} (per element)

LNAs: 7 dB noise figure

60 GHz, 1 Tb/s Spatially-Multiplexed Base Station





2x64 array on each of four faces.

Each face supports 128 users, 128 beams: 512 total users.

Each beam: 2Gb/s.

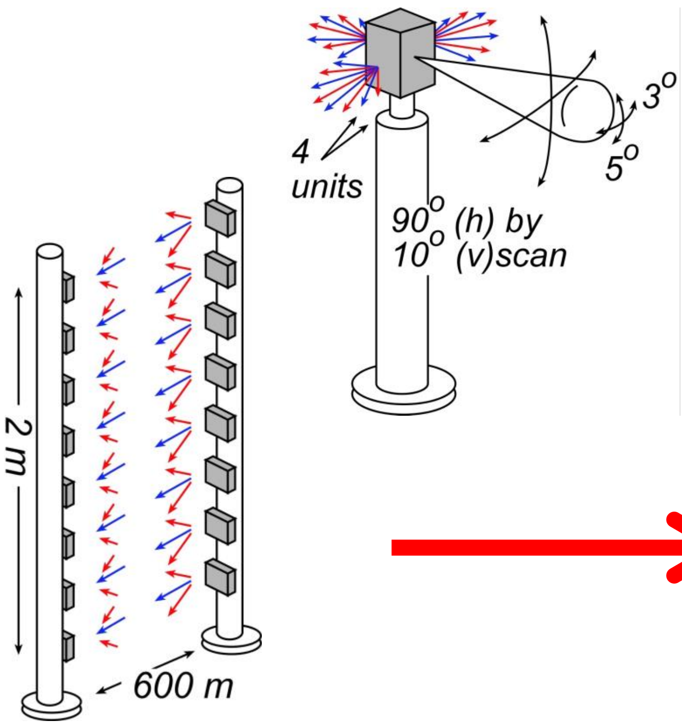
200 meters range in 50 mm/hr rain

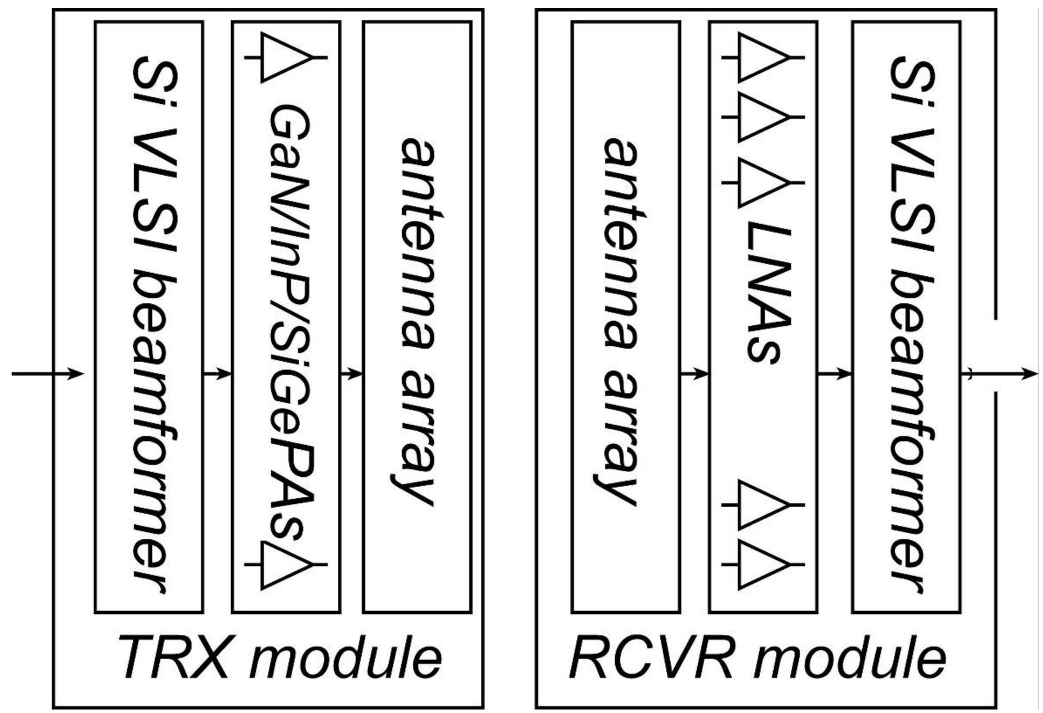
Realistic packaging loss, operating & design margins

PAs: 20 dBm P_{out} , 26 dBm P_{sat} (per element)

LNAs: 3 dB noise figure

mm-Wave Wireless Transceiver Architecture





custom PAs, LNAs → power, efficiency, noise
Si CMOS beamformer→ integration scale

...similar to today's cell phones.

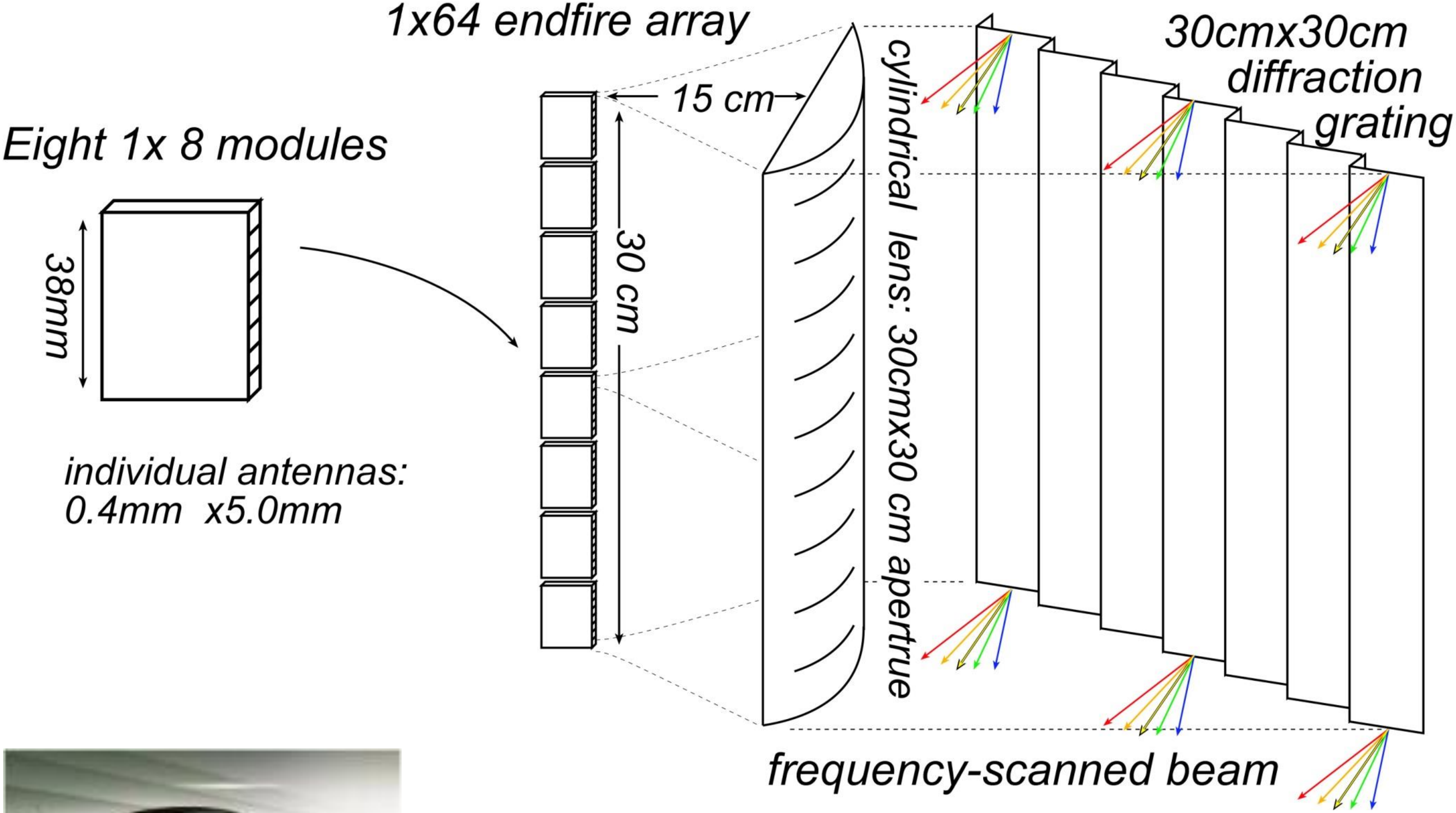
400 GHz frequency-scanned imaging radar

What your eyes see-- in fog

What you see with X-band radar

What you would like to see

400 GHz frequency-scanned imaging car radar



400 GHz frequency-scanned imaging car radar

Range: see a basketball at 300 meters (10 seconds warning) in heavy fog
(10 dB SNR, 28 dB/km, 1 foot diameter target, 65 MPH)

Image refresh rate: 60 Hz

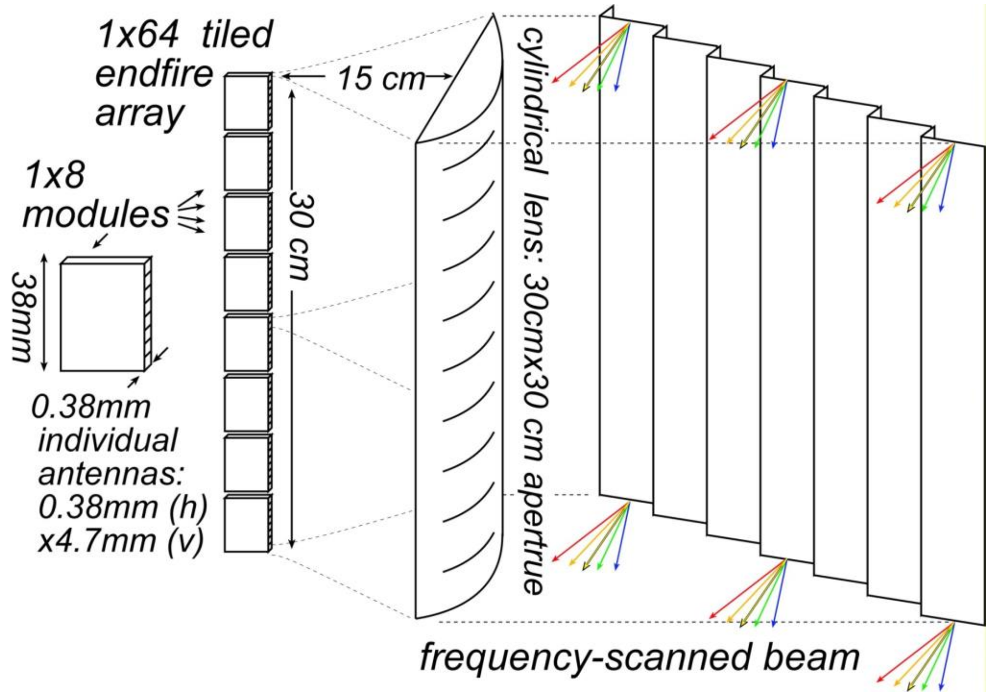
Resolution 64×512=32,800 pixels

Angular resolution: 0.10 degrees

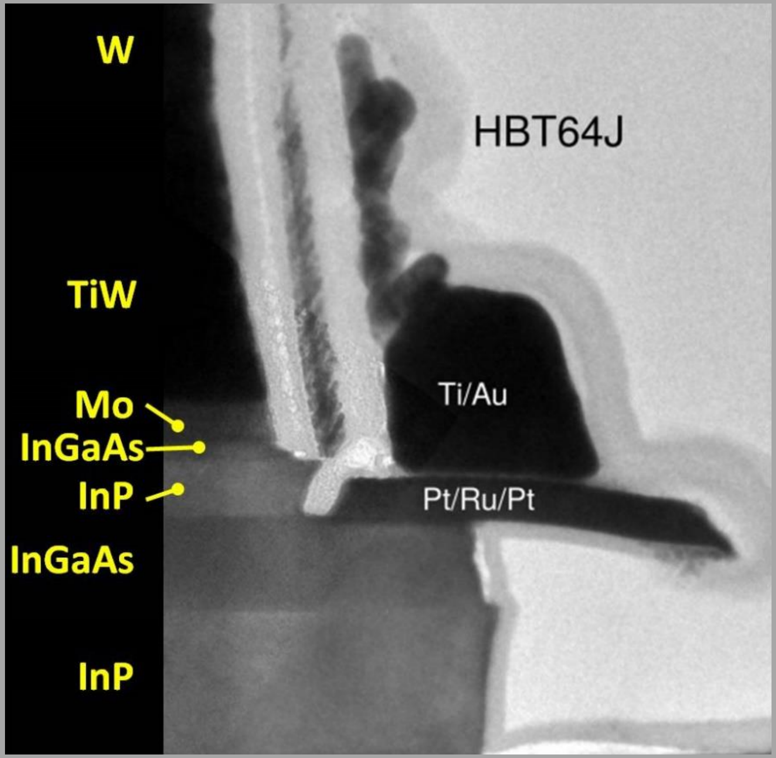
Angular field of view: 9 by 97 degrees

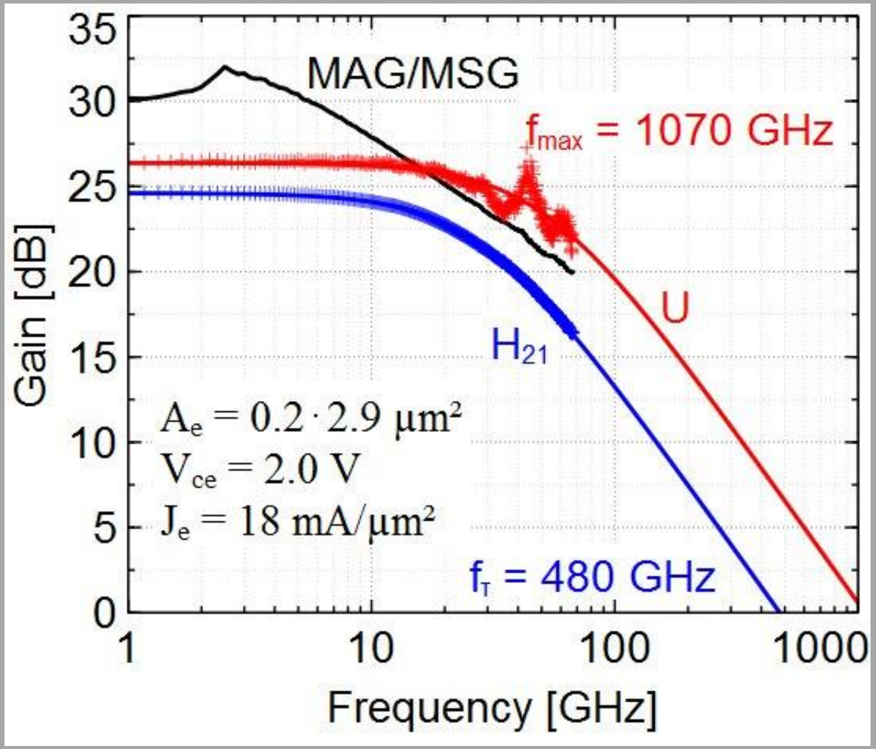
Aperture: 12" by 12"

Component requirements:
10 mW peak power/element,
3% pulse duty factor
6.5 dB noise figure,
5 dB package losses
5 dB manufacturing/aging margin



Transistors and IC technologies





Production Semiconductor Processes for mm-Wave

Silicon Germanium BiCMOS Processes			
foundry	process	nominal f_{max}	useful range
IBM (GF !)	9HP	320 GHz	~170 GHz
TowerJazz	SBC13H3	270 GHz	~140 GHz
TowerJazz	SBC18H4 (near release)	350 GHz	~180 GHz
ST Microelectronics	S9MW	270 GHz	~140 GHz
ST Microelectronics	SB55 (development)	340 GHz	~180 GHz

"Useful (frequency) range" means those frequencies at which acceptable-performance IC blocks can be realized, not the highest frequency of a published research result.

Production Semiconductor Processes for mm-Wave

VLSI CMOS Processes			
foundry	process	nominal f_{max}	useful range
various (IBM, GF, TSMC)	65nm bulk CMOS	~~250GHz	~130GHz
IBM (GF !)	45nm PD-SOI (high leakage power)	~~300 GHz	~150 GHz
IBM (GF !)	32 nm UTB-SOI	~~300 GHz	~150 GHz
ST Microelectronics	28 nm UTB-SOI	similar to above	
various	22nm, ~14nm UTB-SOI	poorer than above	
Intel, IBM/GF	22nm, ~14nm finFET	likely poorer than above,	

Generations beyond 28/32nm:

progressively poorer performance in 100+ GHz ICs

progressively lower transmitter power at all frequencies

Semiconductor Processes for mm-Wave

Production III-V foundries			
foundry	process	nominal f_{max}	useful range
Northrop-Grumman (low-volume)	600nm InP HBT: 4V: higher-power transmitters	>300GHz	~150 GHz
Northrop-Grumman (low-volume)	100nm InP HEMT (FET) for very low noise receivers	>350GHz	~200 GHz
Qorvo (Tri-Quint)	TQP13 HEMT power amps, low-noise -amps	~~150GHz	100 GHz

These processes are best for single-stage add-on power amps, low-noise amps; both to increase system range.

Research Semiconductor Processes

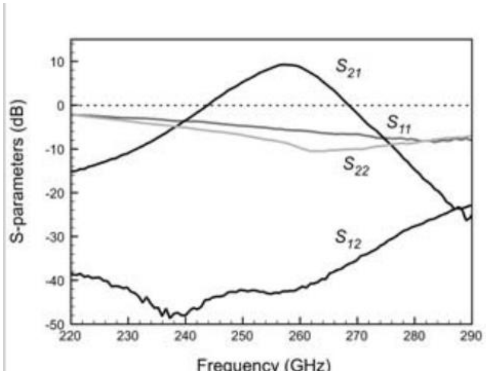
Research institutions with some "foundry-like" access			
foundry	process	nominal f_{max}	useful range
Teledyne	250nm InP HBT	700GHz	~250 GHz
Teledyne	130nm InP HBT	1100 GHz	~450 GHz
IHP	130nm SiGe BiCMOS	500GHz	~250 GHz

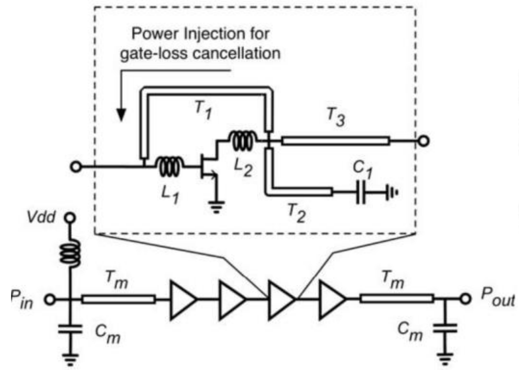
microwave GaN HEMT is a production technology
mm-wave GaN HEMT *may become* a production technology
mm-wave InP HBT may become a production technology

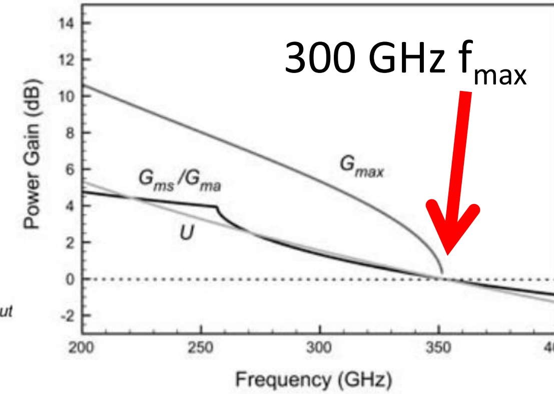
mm-wave CMOS (examples)

260 GHz amplifier:
65nm bulk CMOS, Over-neutralized to reach G_{max}, 9.2 dB, 4 stages

Momeni ISSCC, March 2013

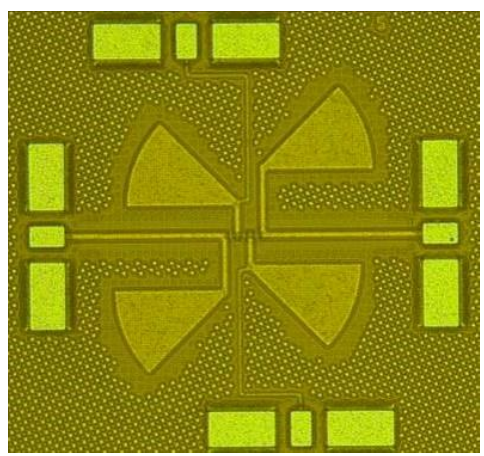


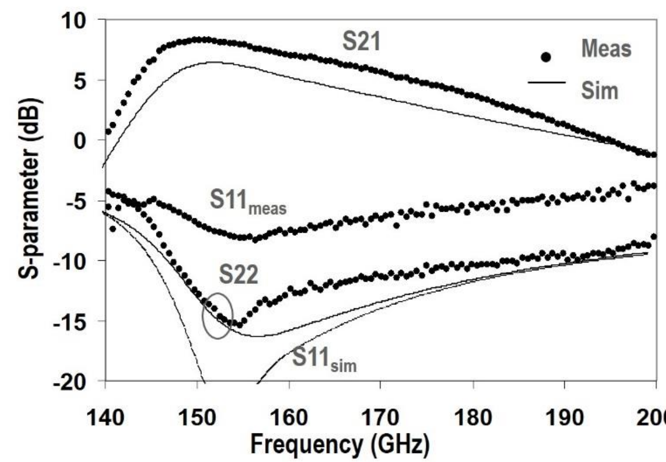




150 GHz amplifier: 65 nm bulk CMOS, 8.2 dB, 3 stages (250GHz f_{max})

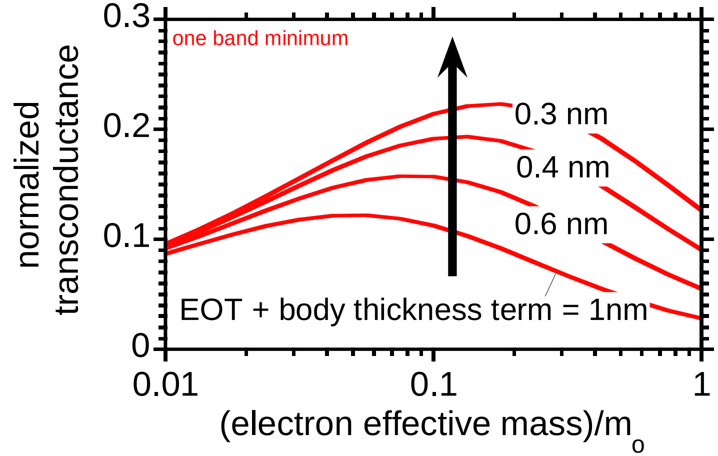
Seo et al. (UCSB), JSSC, December 2009



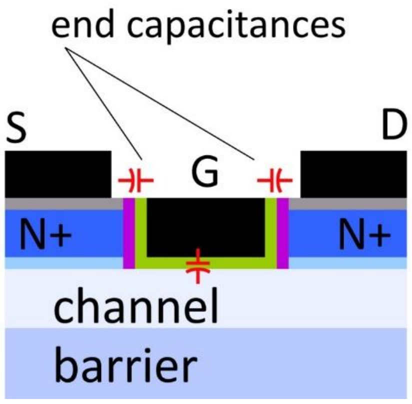


mm-Wave CMOS won't scale much further

Gate dielectric can't be thinned
→ on-current, g_m can't increase



Shorter gates give no less capacitance
dominated by ends; ~1fF/μm total

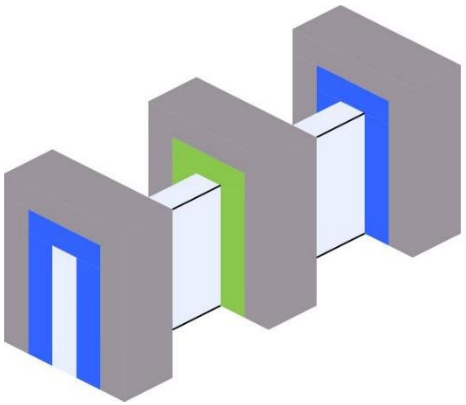


Maximum g_m, minimum C→ upper limit on f_τ.
about 350-400 GHz.

Tungsten via resistances reduce the gain

Inac et al, CSICS 2011

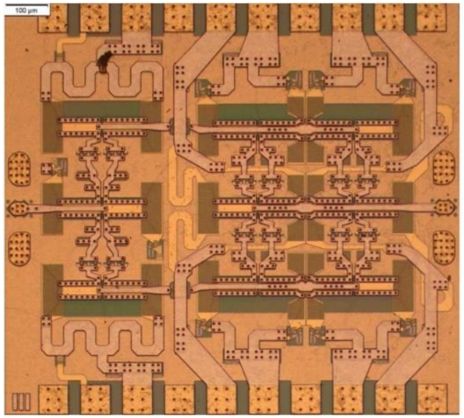
Present finFETs have yet <u>larger</u> end capacitances



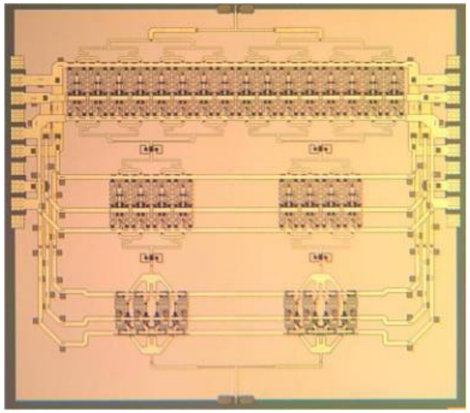
III-V high-power transmitters, low-noise receivers

Cell phones & WiFi:
GaAs PAs, LNAs

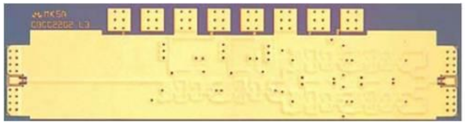
mm-wave links need
high transmit power,
low receiver noise



0.47 W @86GHz
H Park, UCSB, IMS 2014



0.18 W @220GHz
T Reed, UCSB, CSICS 2013



1.9mW @585GHz
M Seo, TSC, IMS 2013

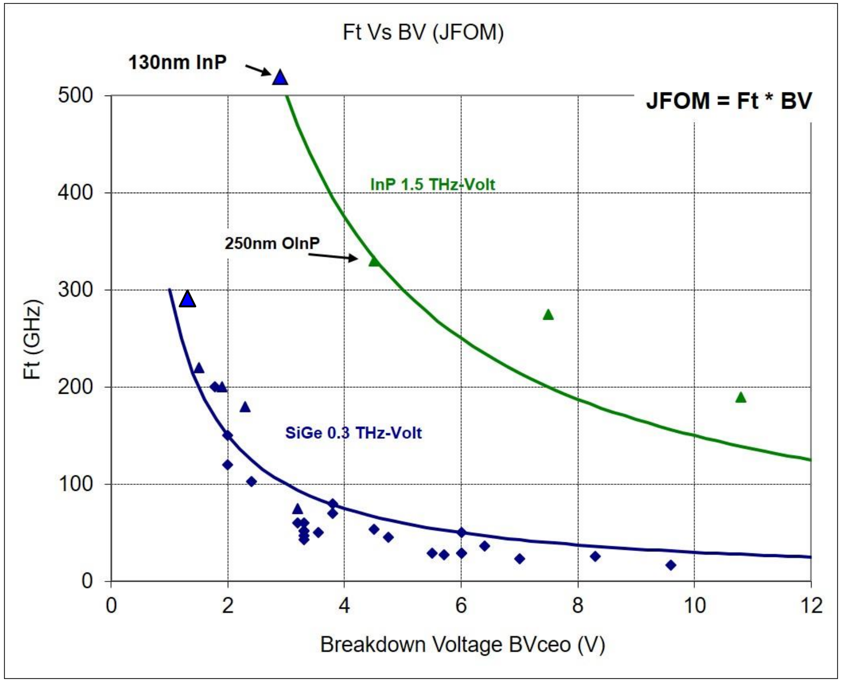
InP Bipolar Transistors

Why InP Bipolar Transistors ?

InP better electron transport than Si collectors
higher electron velocity 3.5 vs 1.0 × 10^7 cm/s
plus wider bandgap→ higher breakdown field

InGaAs base, base-emitter heterojunction:
very low base sheet resistances

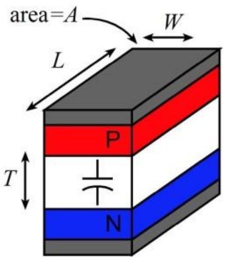
Implications:
~3:1 higher (f_τ, f_{max}) at a given scaling node
higher breakdown* at a given (f_τ, f_{max})
but...InP HBT not a production technology



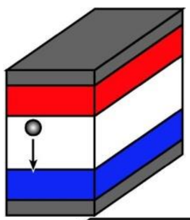
*Breakdown is too complicated to summarize with BVCEO.
BVCBO vs. BVCEO vs. safe operating area ?
Bottom line: look at V_{ce} used in published IC data for a given IC technology.

Transistor scaling laws: (V,I,R,C,τ) vs. geometry

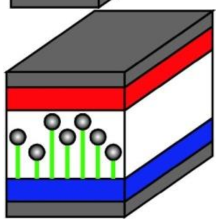
Depletion Layers



$$C = \varepsilon \cdot \frac{A}{T}$$

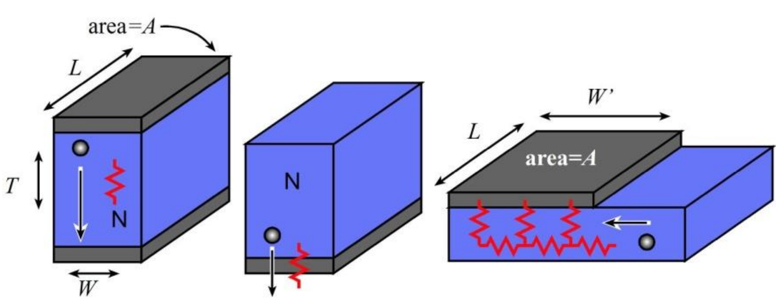


$$\tau = \frac{T}{2v}$$



$$\frac{I_{\max}}{A} = \frac{4\varepsilon v_{sat}(V_{appl} + \phi)}{T^2}$$

Bulk and Contact Resistances

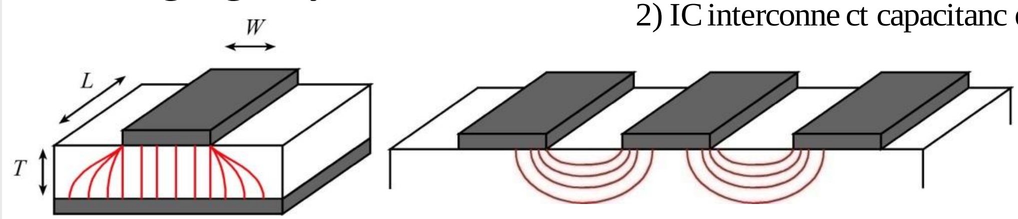


$R \cong \rho_{contact} / A$ contact te rms dominate

Fringing Capacitances

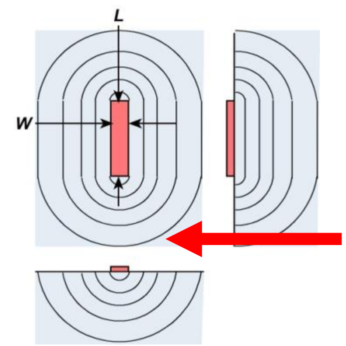
1) FET fringing capacitanc es

2) IC interconne ct capacitanc es

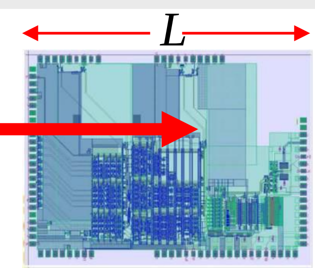


$C_{finging} / L \sim \varepsilon$ $C_{finging} / L \sim \varepsilon$

Thermal Resistance

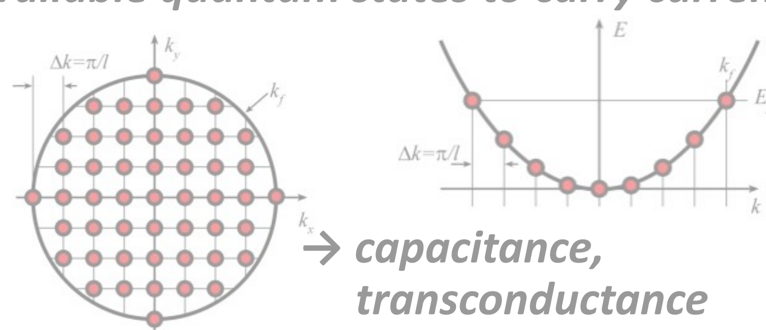


$$\Delta T_{IC} \propto \frac{P_{IC}}{K_{th} L}$$



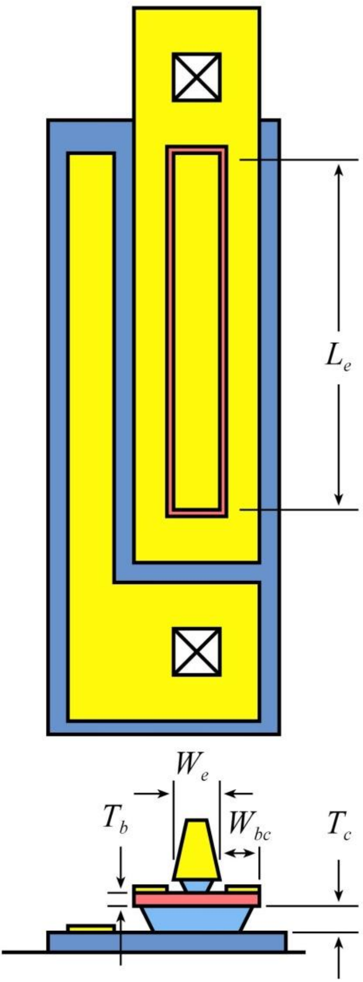
$$\Delta T_{\text{transistor}} \sim \frac{P}{\pi K_{th} L} \ln\left(\frac{L}{W}\right)$$

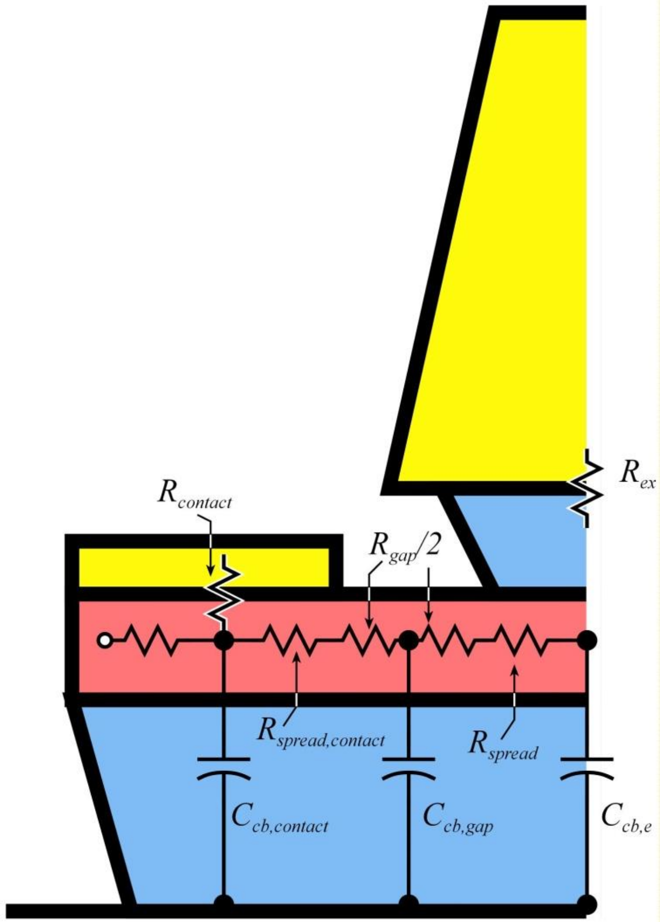
Available quantum states to carry current

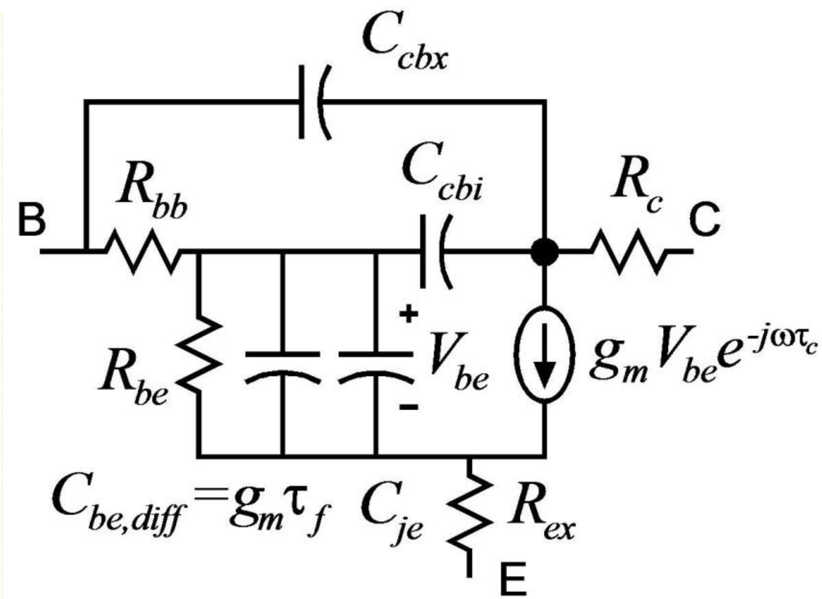


→ capacitance, transconductance contact resistance

Bipolar Transistor: Structure & Models







$$R_{be} = \beta / g_m$$

$$g_m = qI_E / nkT$$

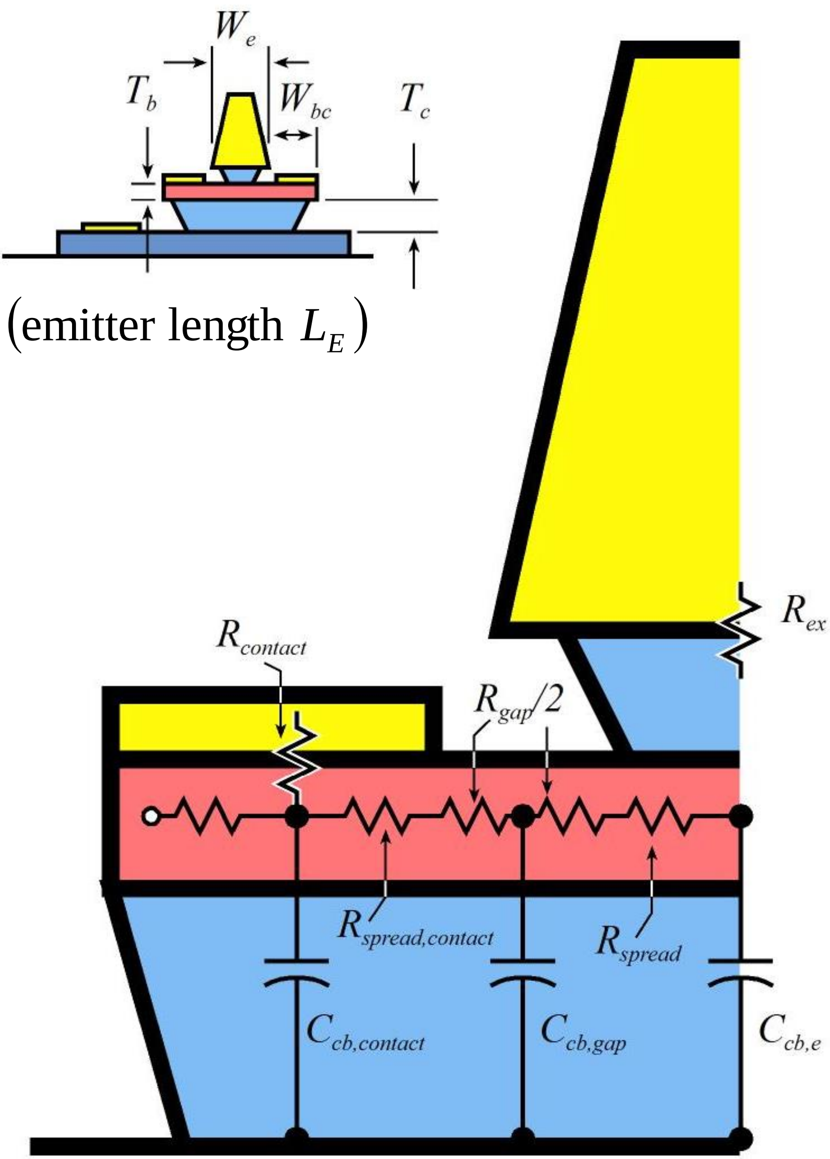
$$C_{be} = C_{je} + g_m(\tau_b + \tau_c)$$

$$\tau_b \approx T_b^2 / 2D_n + T_b / v_{thermal}$$

$$\tau_c \approx T_c / 2v_{"sat"}$$

$$\frac{1}{2\pi f_\tau} = \tau_{base} + \tau_{collector} + C_{je}\frac{nkT}{qI_E} + C_{bc}\left(\frac{nkT}{qI_E} + R_{ex} + R_{coll}\right)$$

Base-Collector Distributed RC Parasitics



$$R_{ex} = \rho_{contact,emitter} / A_{emitter}$$

$$R_{spread} = \rho_s W_e / 12 L_E$$

$$R_{gap} = \rho_s W_{gap} / 4 L_E$$

$$R_{spread,contact} = \rho_s W_{bc} / 6 L_E$$

$$R_{contact} = \rho_{contact,base} / A_{base\_contacts}$$

$$C_{cb,e} = \varepsilon A_{emitter} / T_c$$

$$C_{cb,gap} = \varepsilon A_{gap} / T_c$$

$$C_{cb,contact} = \varepsilon A_{base\_contacts} / T_c$$

$R_{bb}C_{cb}$ Time Constant, F_{max}, Simple Hybrid-π model

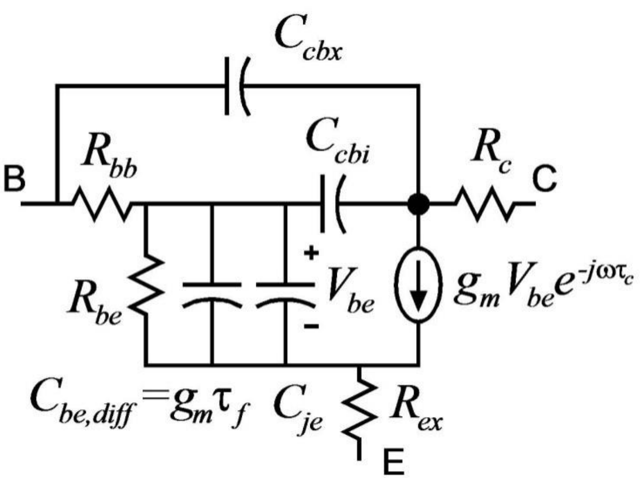
$$f_{\max} \cong \sqrt{f_\tau / 8\pi R_{bb} C_{cbi}} \text{ where}$$

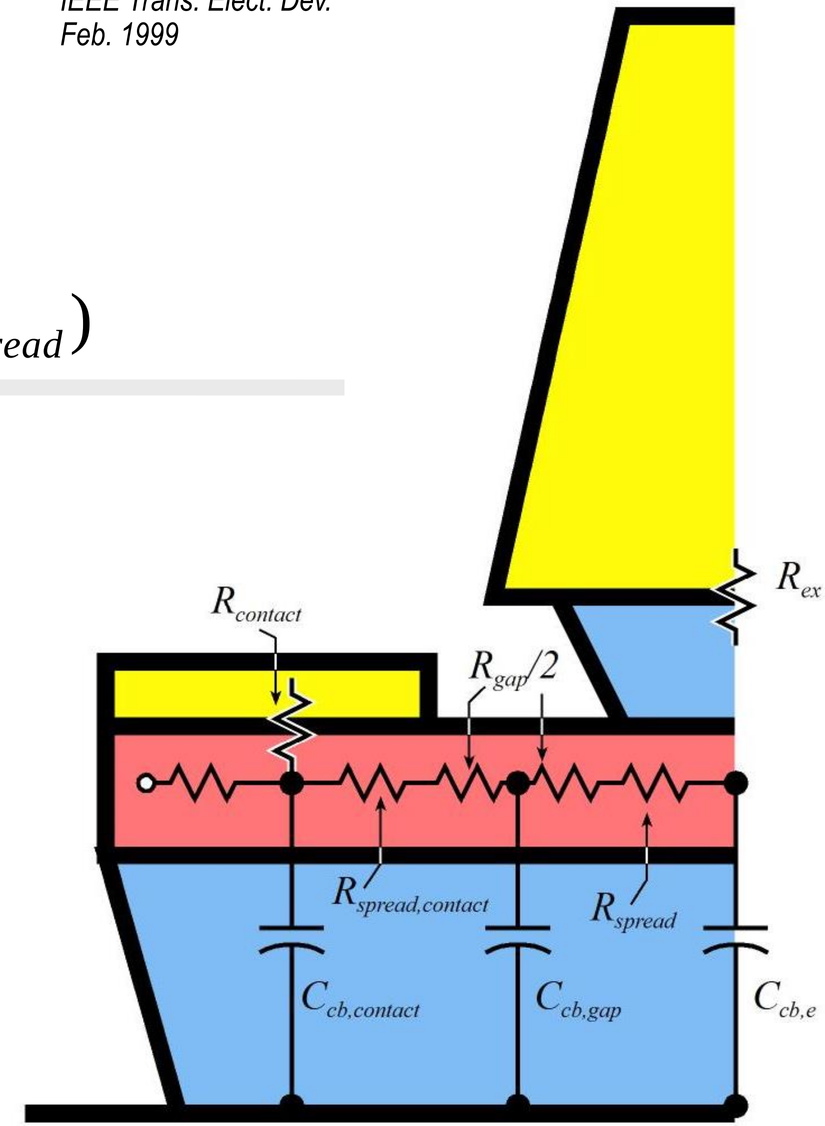
Vaidyanathan & Pulfrey
IEEE Trans. Elect. Dev.
Feb. 1999

$$\tau_{cb} = R_{bb}C_{cbi} = C_{cb,contact}R_{contact}$$

$$+ C_{cb,gap}(R_{contact} + R_{spread,contact} + R_{gap}/2)$$

$$+ C_{cb,e}(R_{contact} + R_{spread,contact} + R_{gap} + R_{spread})$$



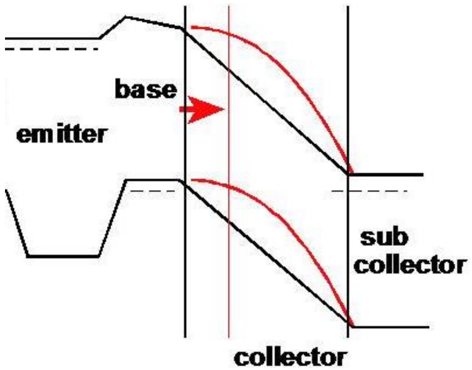


R_{bb} = true total base resistance

$C_{cbi} + C_{cbx}$ = true total C_{cb}

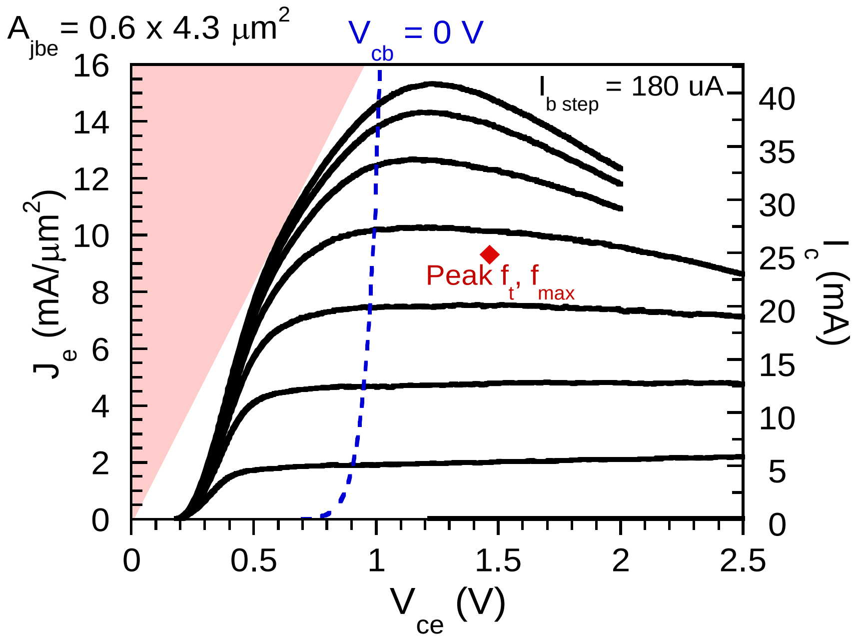
$C_{cbi} : C_{cbx}$ ratio set to fit $f_{\max}$ from above

BJT Space-Charge-Limited Current (Kirk effect)



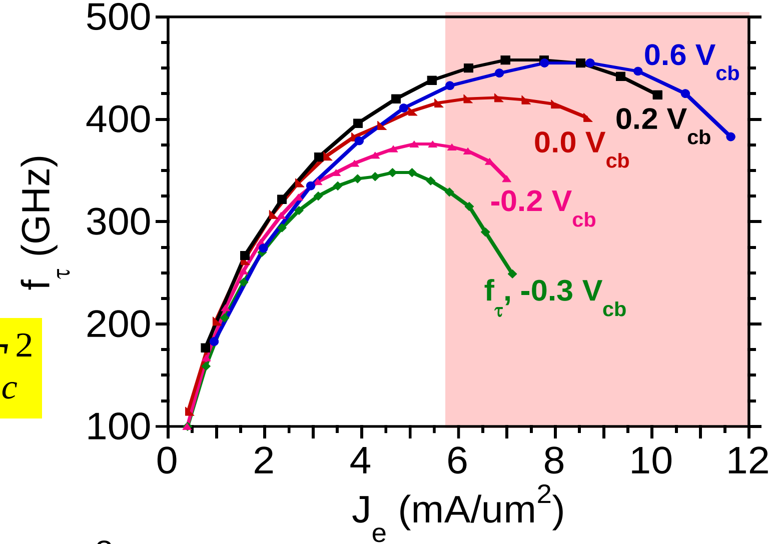
$$\partial^2\phi/\partial x^2 = \rho/\varepsilon = (qN_D - J/v)/\varepsilon$$

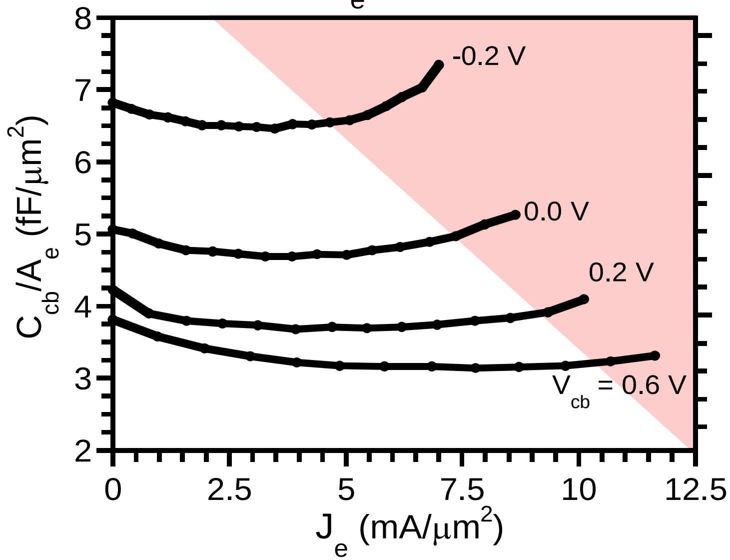
$$\Rightarrow I_{\max} = 2\varepsilon v_{eff} A_E (V_{cb} + V_{cb,\min} + 2\phi)/T_c^2$$



Decreased (f_τ, $f_{\max}$), increased C_{cb} at high J.

Kirk threshold increases with increased V_{ce}.

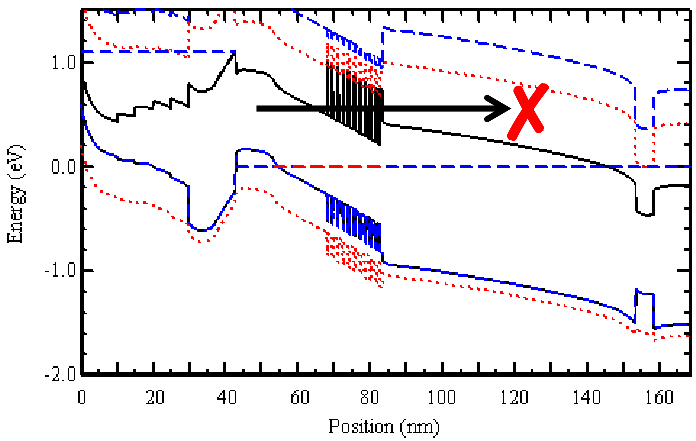




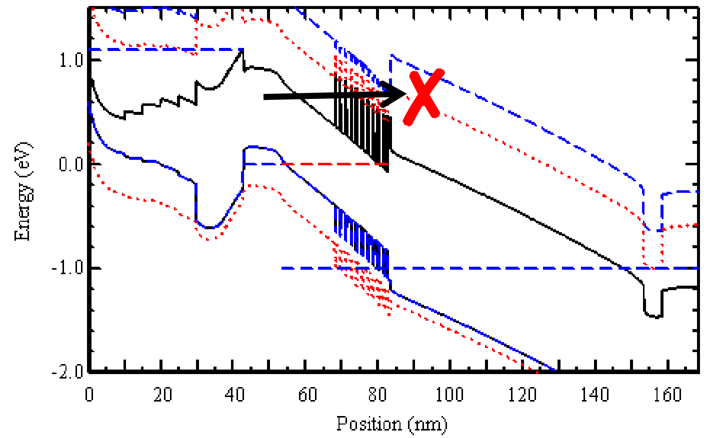
InP: Electron velocity modulation

More collector voltage→ less distance before scattering→ more transit time

less collector voltage

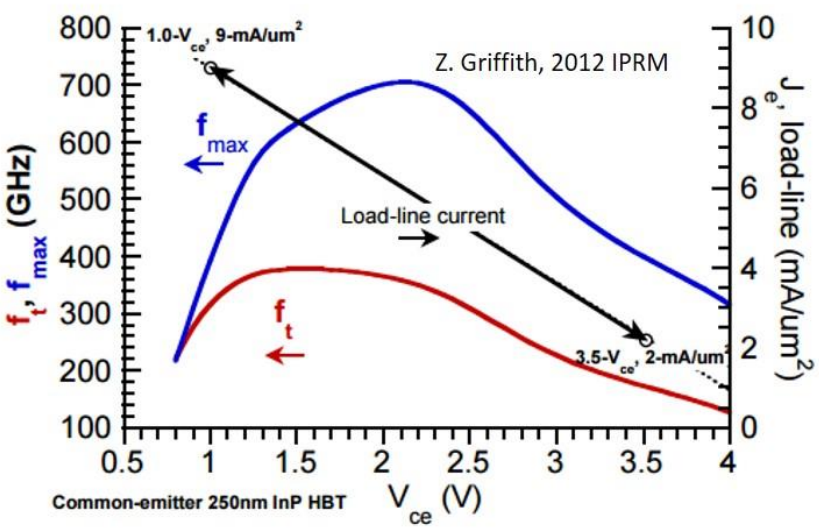


more collector voltage

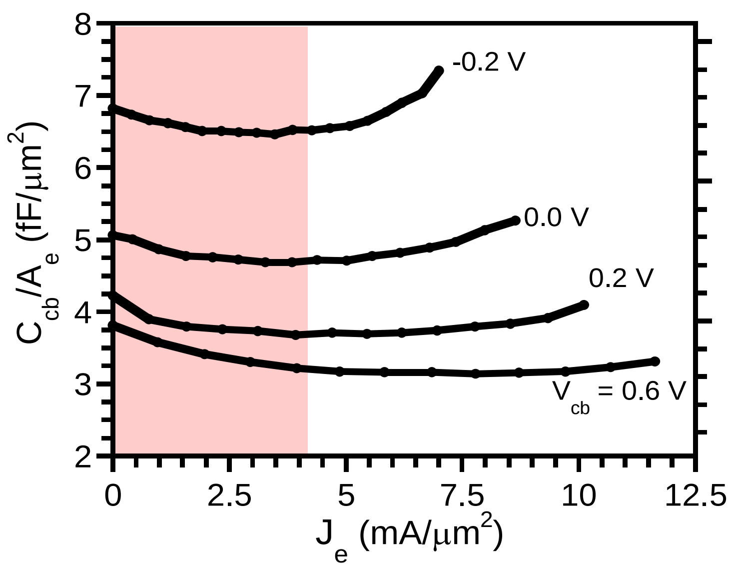


heavy X valley
heavy L valley
light Γ valley

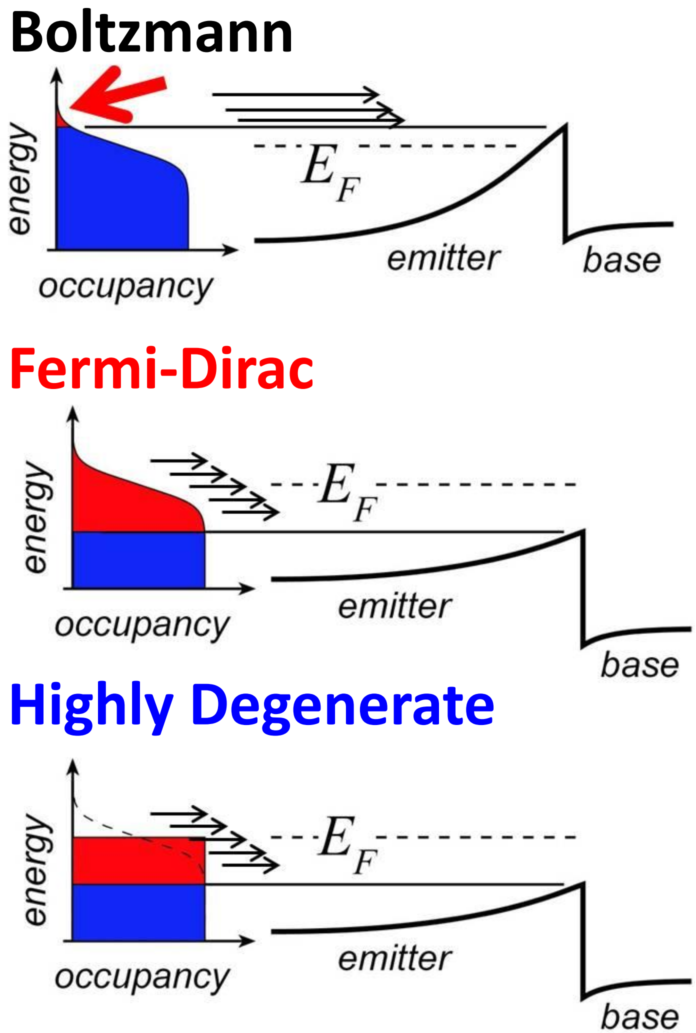
(f_τ, f_{max}) decrease with increased V_{ce}.

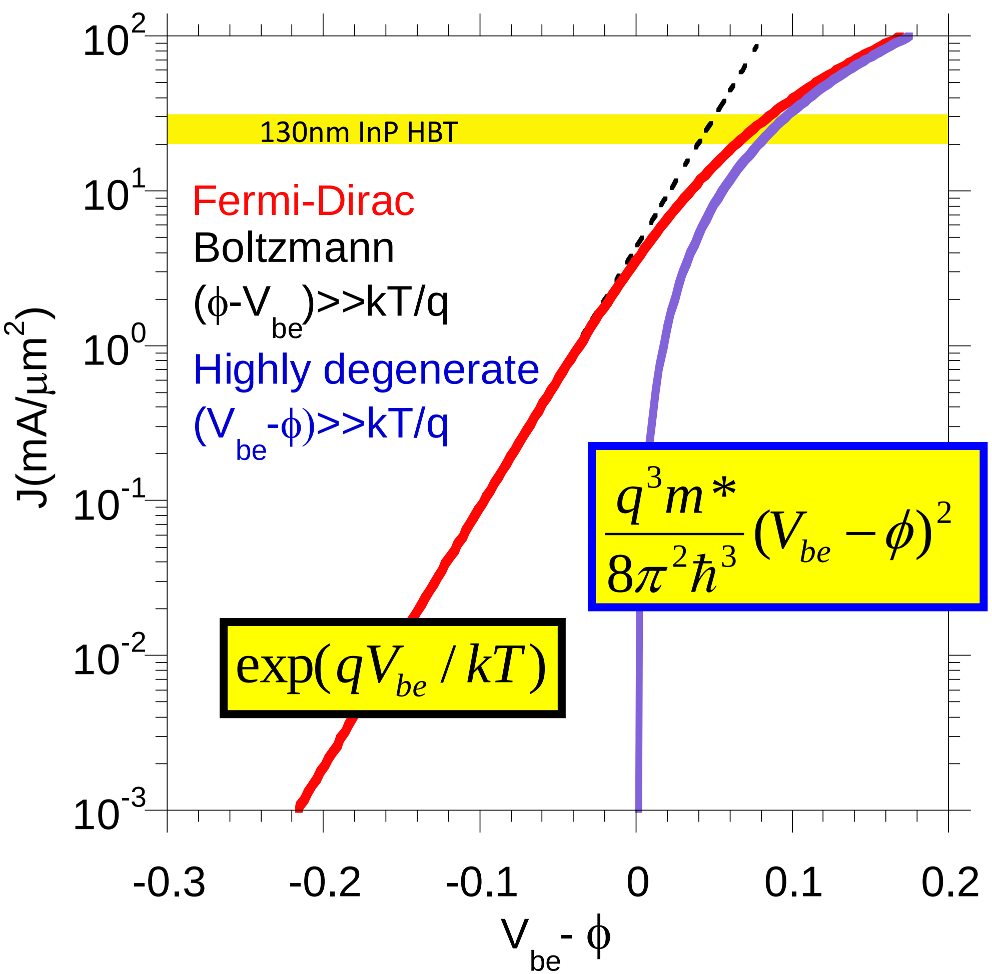


C_{cb} is modulated by I_c.



Reduced g_m at extreme current densities

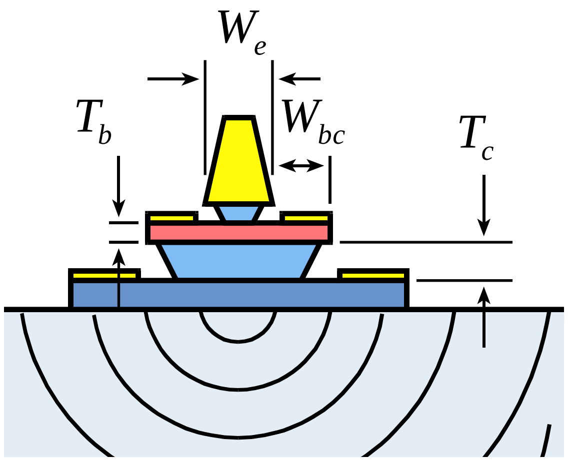




High currents→ transconductance less than qI/kT → bandwidth decreases

Problem in InP, not silicon: silicon has larger electron effective mass, more valleys

Bipolar Transistor Design



(emitter length L_E)

$$\tau_b \approx T_b^2 / 2D_n$$

$$\tau_c = T_c / 2v_{sat}$$

$$C_{cb} = \varepsilon A_c / T_c$$

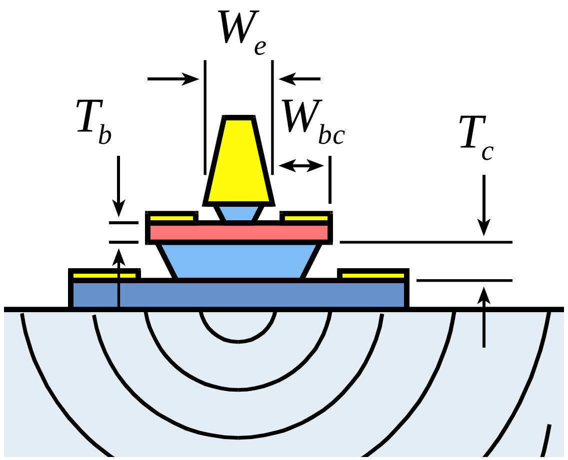
$$I_{c,\max} \propto v_{sat} A_e (V_{\text{ce,operating}} + V_{\text{ce,punch-through}}) / T_c^2$$

$$\Delta T \propto \frac{P}{L_E}\left[1 + \ln\left(\frac{L_e}{W_e}\right)\right]$$

$$R_{ex} = \rho_{\text{contact}} / A_e$$

$$R_{bb} = \rho_{\text{sheet}}\left(\frac{W_e}{12L_e} + \frac{W_{bc}}{6L_e}\right) + \frac{\rho_{\text{contact}}}{A_{\text{contacts}}}$$

Bipolar Transistor Design: Scaling



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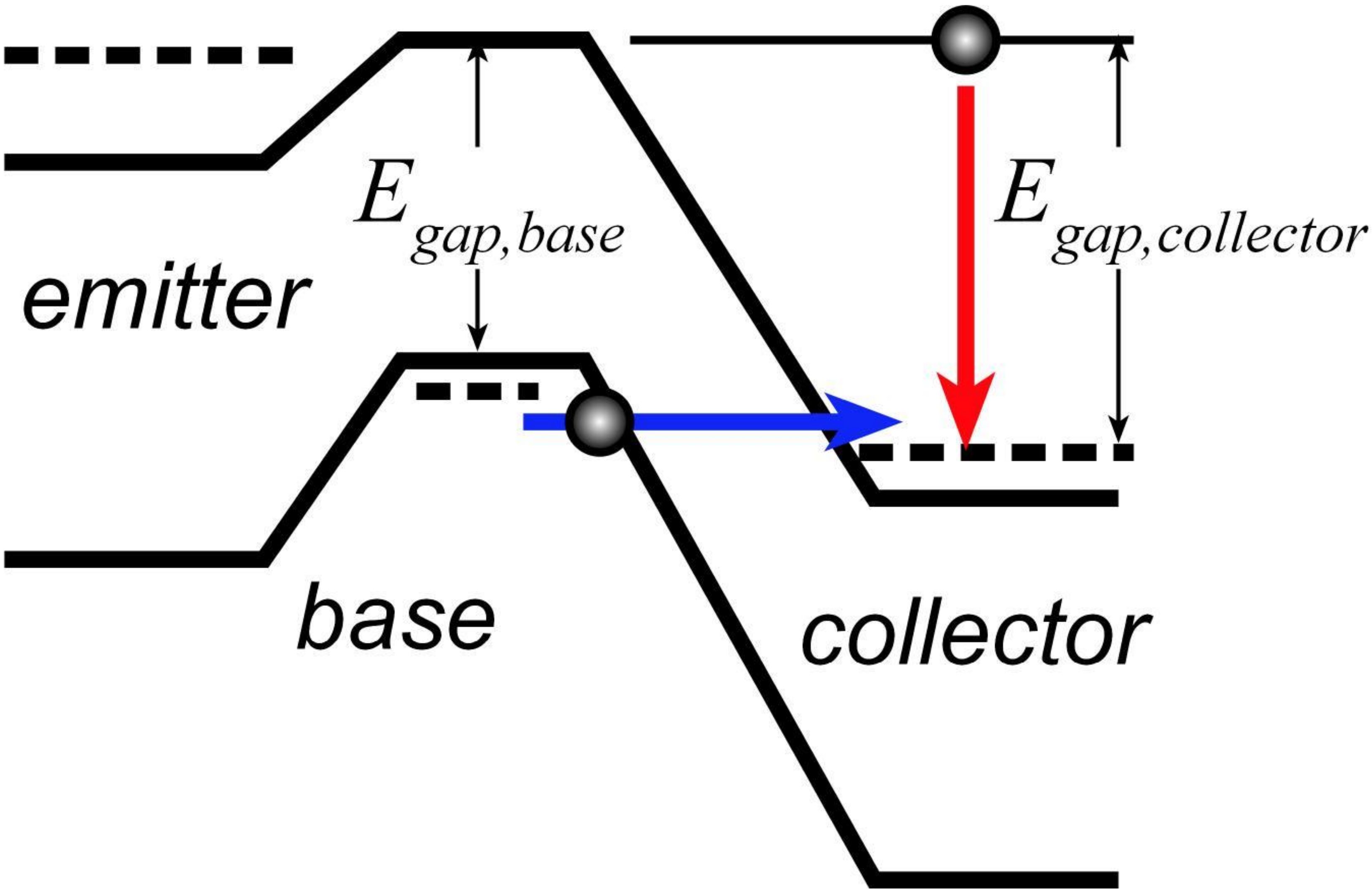
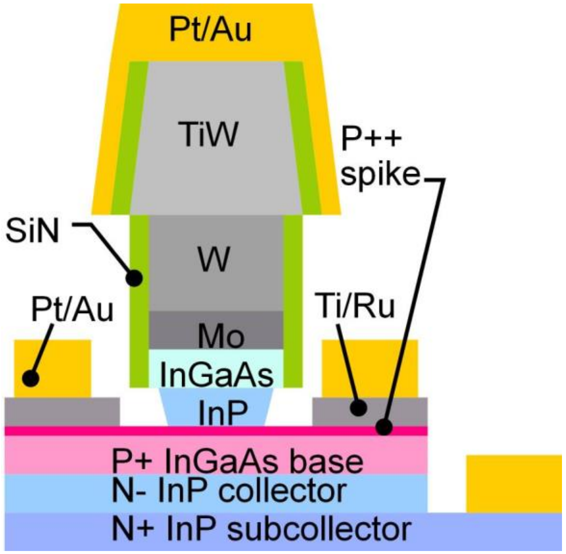
Energy-limited vs. field-limited breakdown



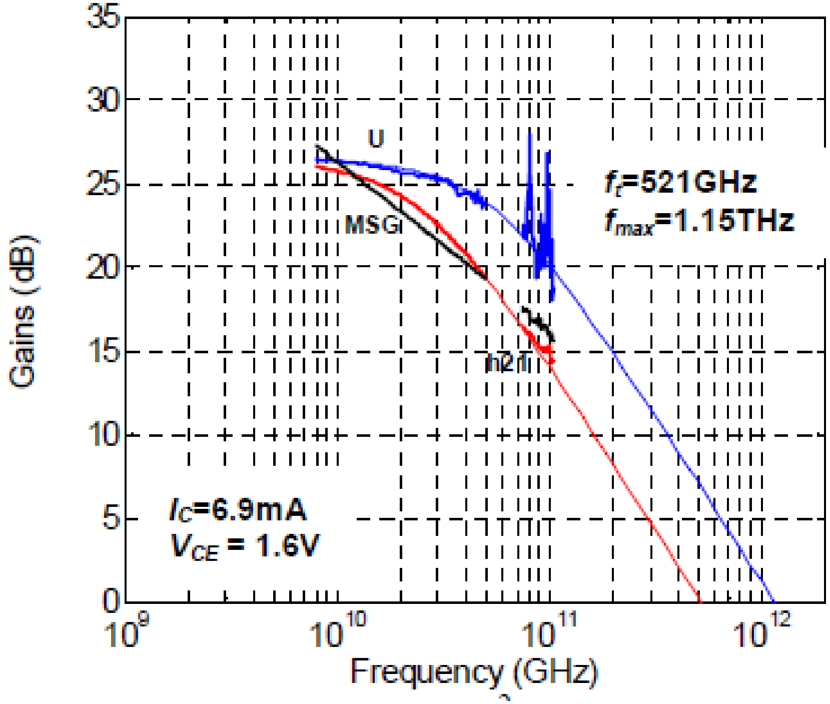
band-band tunneling: base bandgap
impact ionization: collector bandgap

Making faster bipolar transistors



to double the bandwidth:	change
emitter & collector junction widths	decrease 4:1
current density (mA/μm^2)	increase 4:1
current density (mA/μm)	constant
collector depletion thickness	decrease 2:1
base thickness	decrease 1.4:1
emitter & base contact resistivities	decrease 4:1

Teledyne: M. Urteaga *et al*: 2011 DRC



Narrow junctions.

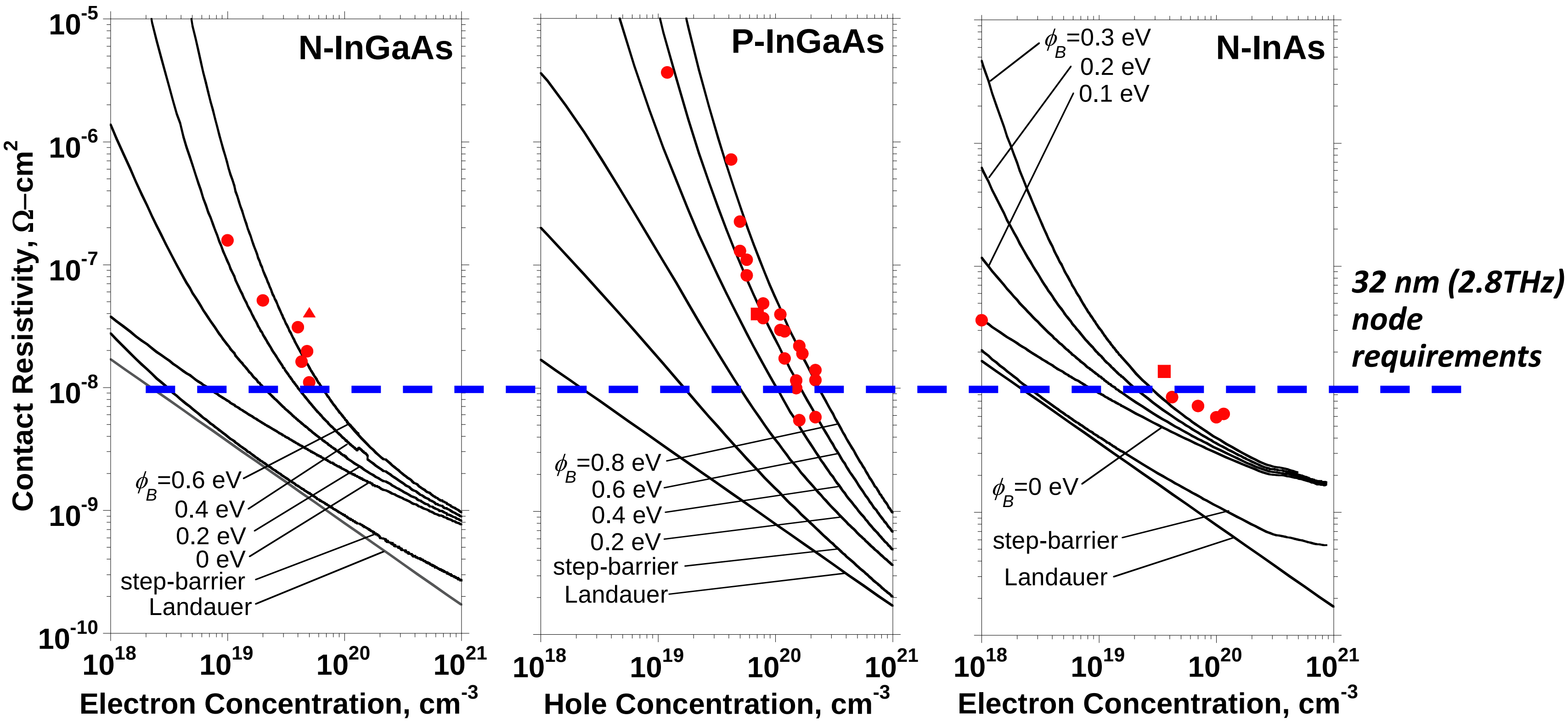
Thin layers

High current density

Ultra low resistivity contacts

Refractory Contacts to In(Ga)As

Baraskar *et al*, Journal of Applied Physics, 2013



Refractory: robust under high-current operation / Low penetration depth: ~ 1 nm / Performance sufficient for 32 nm /2.8 THz node.

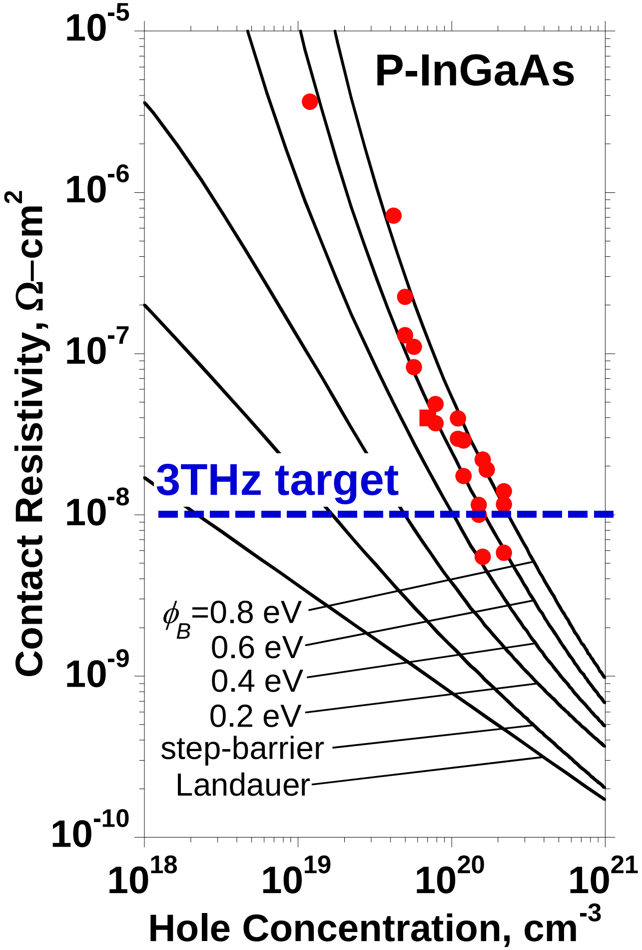
Why no ~2THz HBTs today ?

Problem: reproducing these base contacts in full HBT process flow

THz HBTs: The key challenges

Obtaining good base contacts

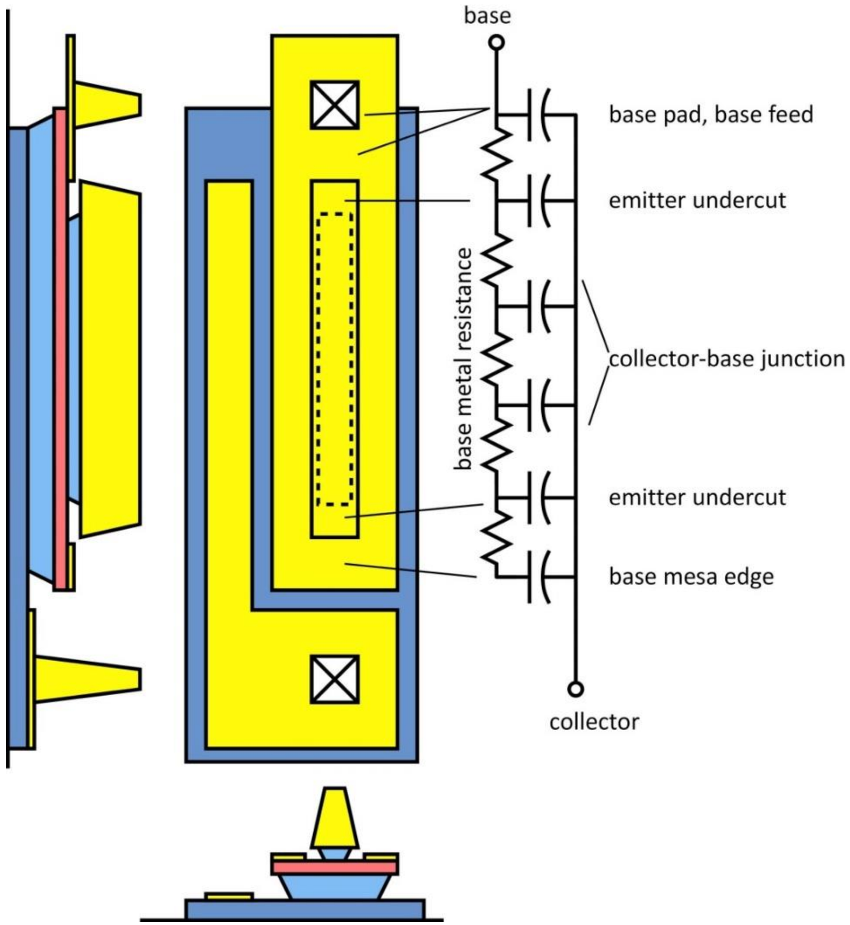
in HBT vs. in contact test structure
(emitter contacts are fine)



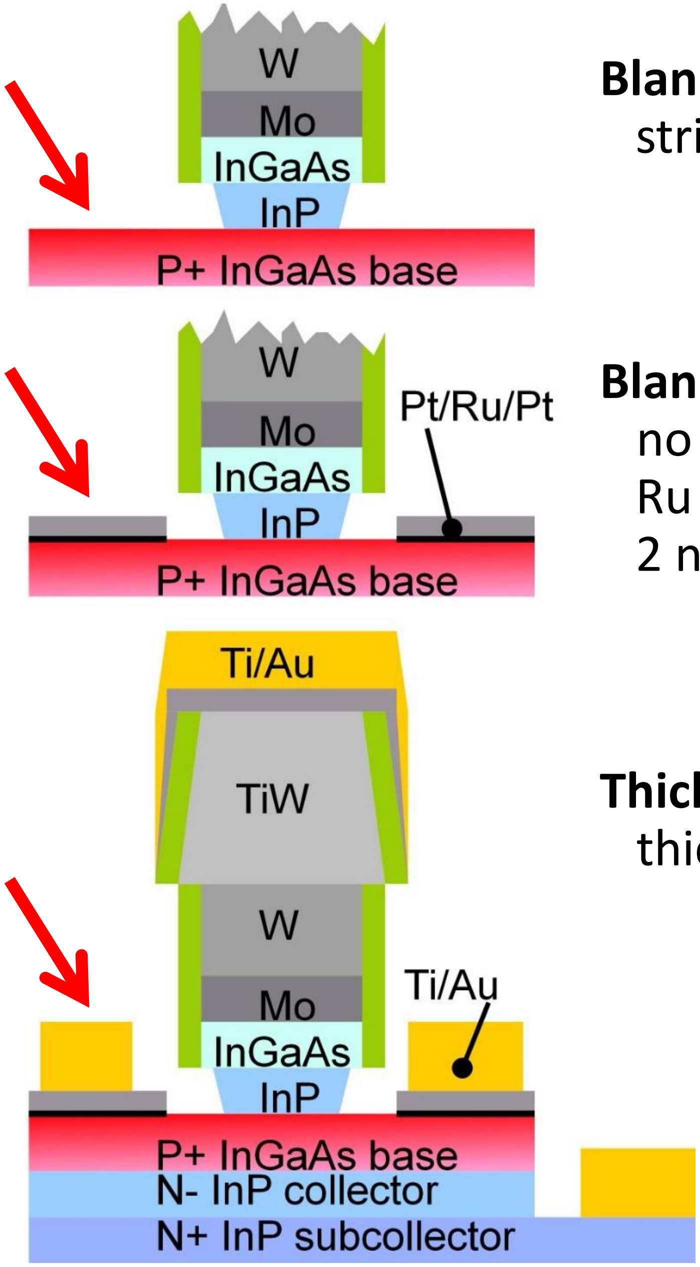
Baraskar *et al*, Journal of Applied Physics, 2013

RC parasitics along finger length

metal resistance, excess junction areas



THz HBTs: double base metal process



Blanket surface clean (UV O_3 / HCl)
strips organics, process residues, surface oxides

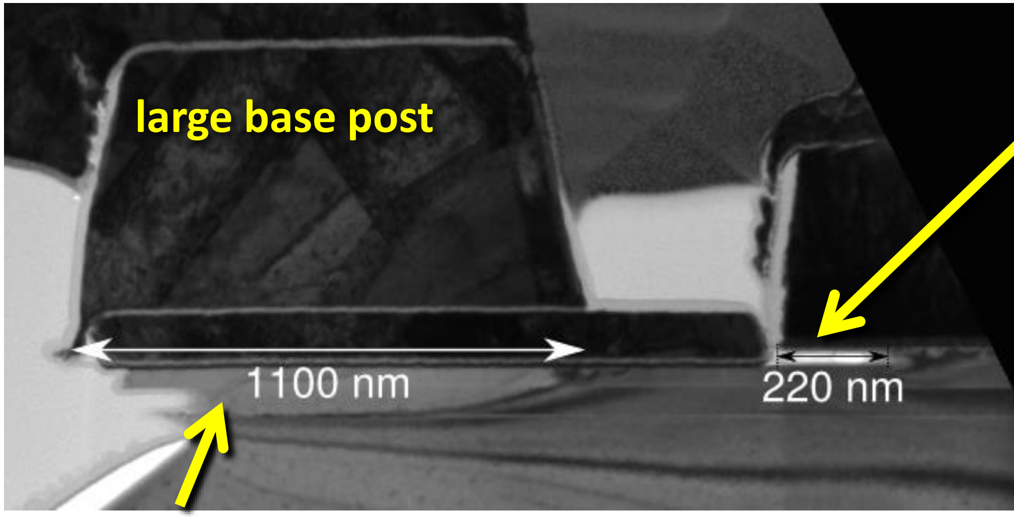
Blanket base metal
no photoresist; no organic residues
Ru refractory diffusion barrier
2 nm Pt : penetrates residual oxides

Thick Ti/Au base pad metal liftoff
thick metal→ low resistivity

Rode et al., IEEE TED, Aug. 2015

Reducing Emitter Length Effects

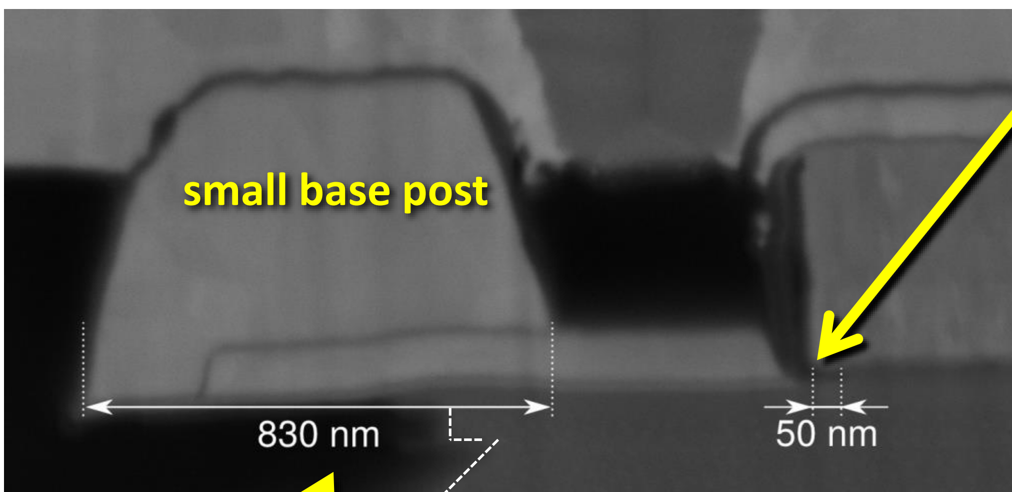
before



large emitter end undercut

small base post undercut

after

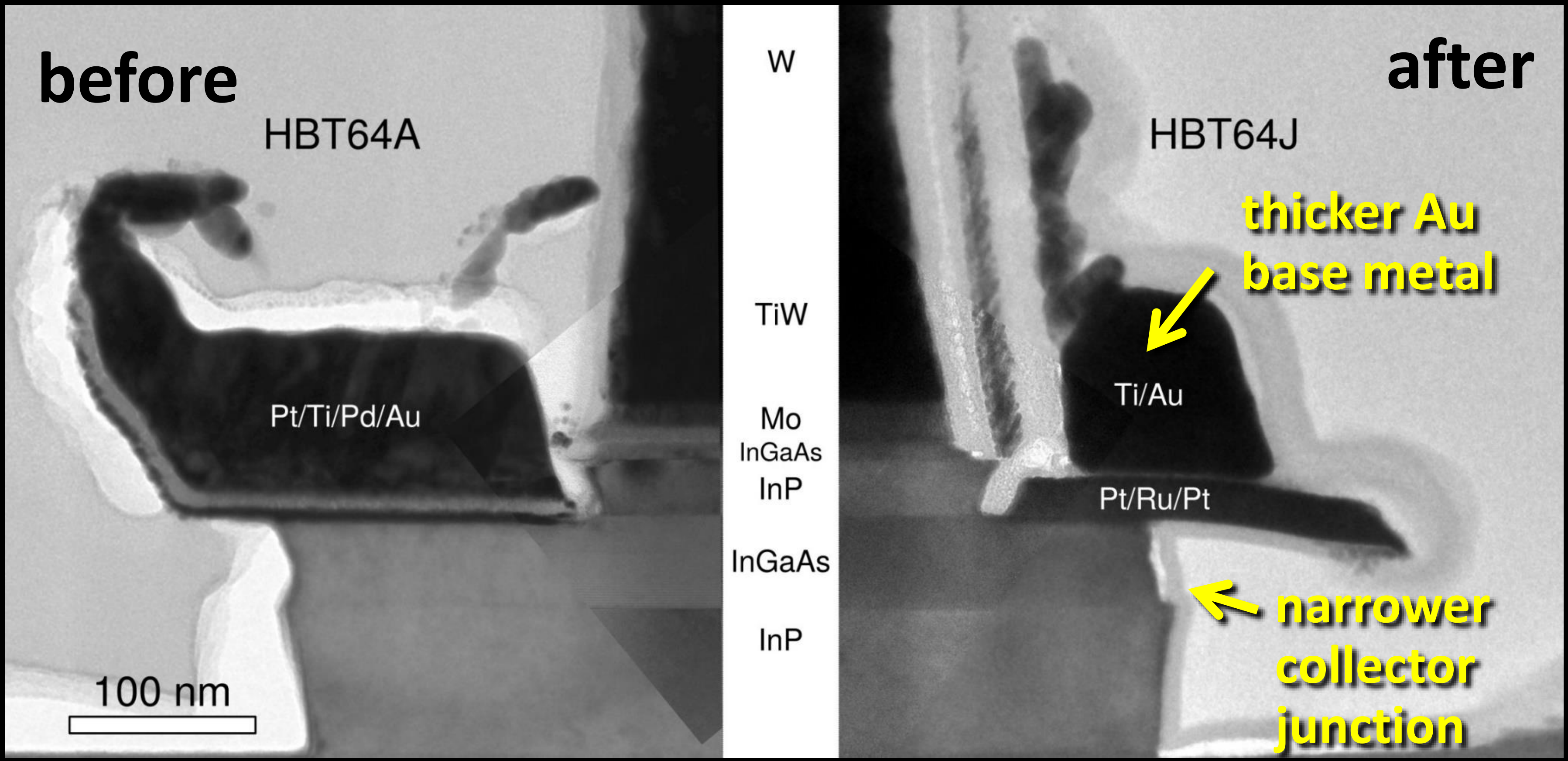


small emitter end undercut

large base post undercut

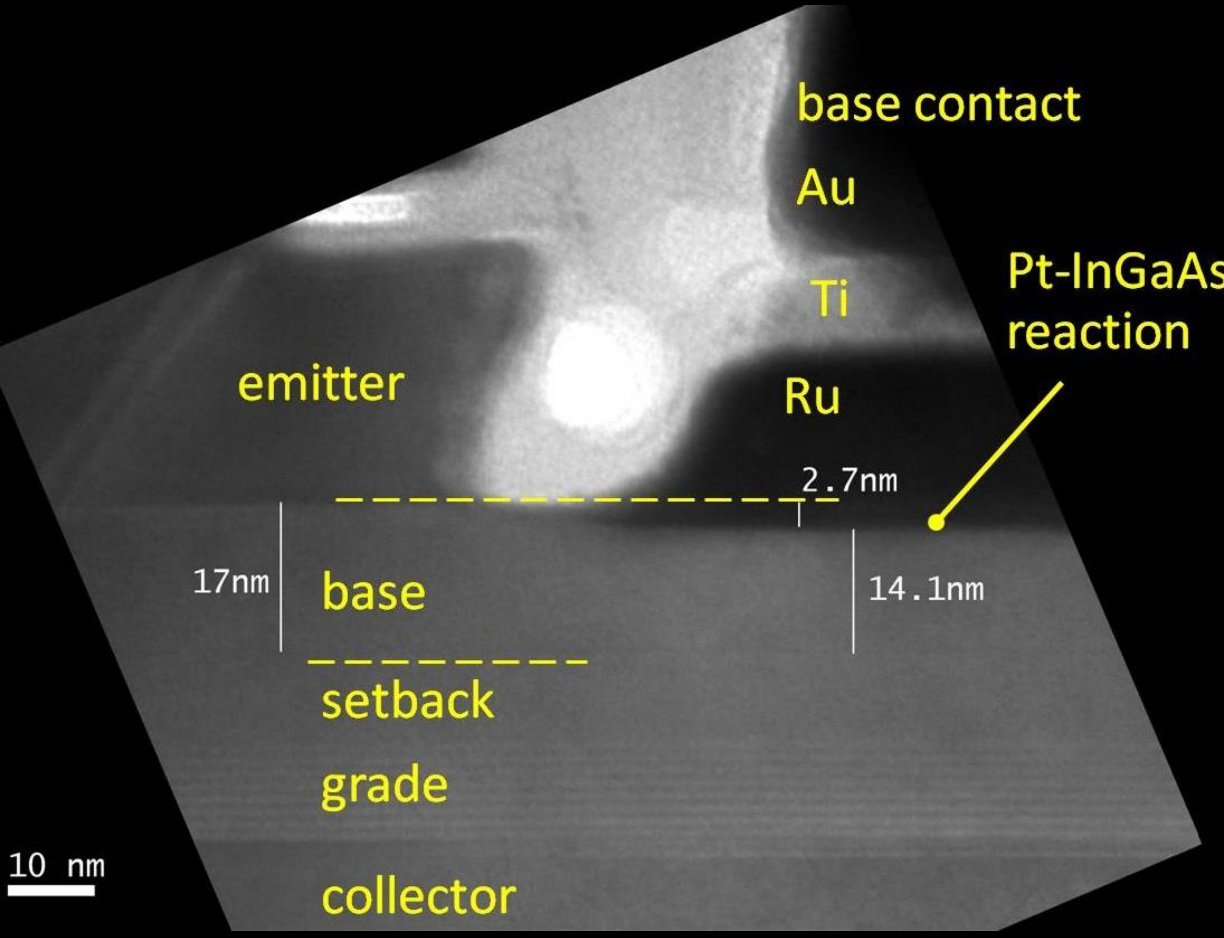
Rode et al., IEEE TED, Aug. 2015

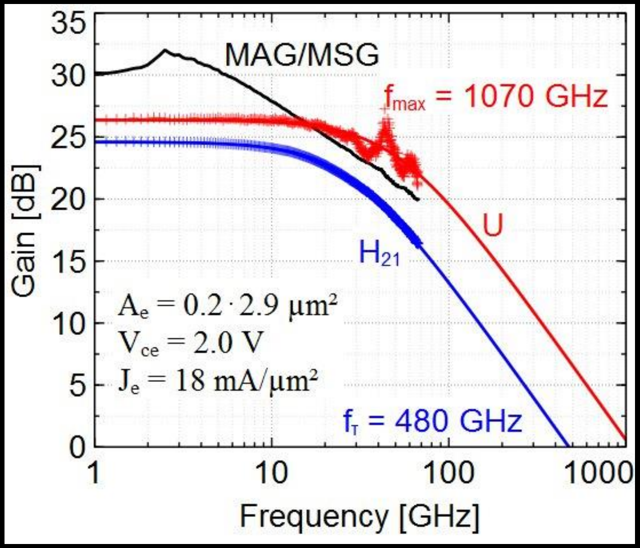
Reducing Emitter Length Effects

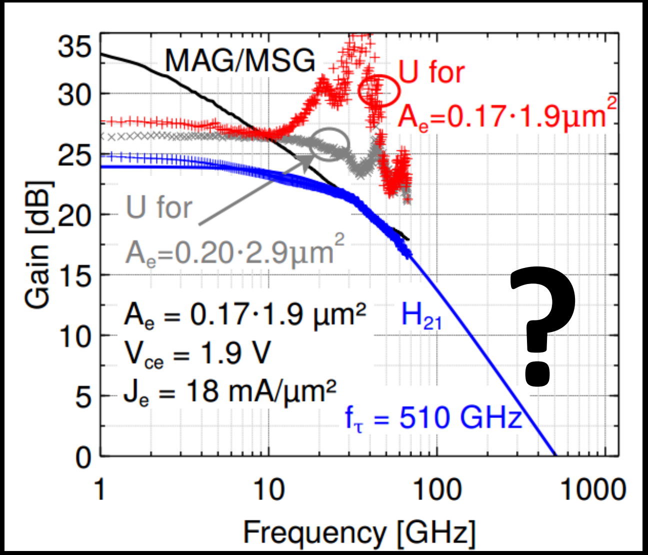


Rode et al., IEEE TED, Aug. 2015

InP HBTs: 1.07 THz @200nm, ?? @ 130nm







Rode et al., IEEE TED, Aug. 2015

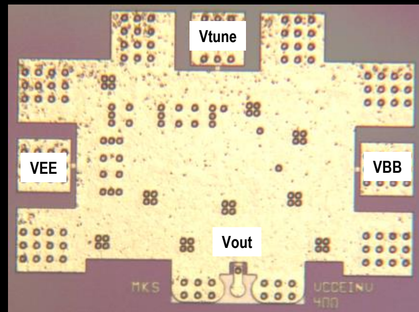
130nm /1.1 THz InP HBT: ICs to 670 GHz

TELEDYNE SCIENTIFIC COMPANY
A Teledyne Technologies Company

UCSB

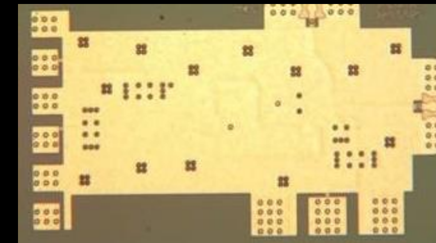
614 GHz fundamental VCO

M. Seo, TSC / UCSB



340 GHz dynamic frequency divider

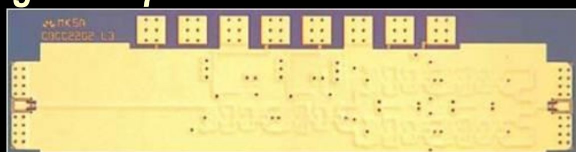
M. Seo, UCSB/TSC
IMS 2010



620 GHz, 20 dB gain amplifier

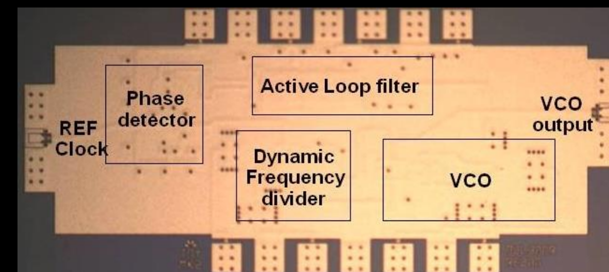
M Seo, TSC
IMS 2013

also: 670GHz amplifier
J. Hacker , TSC
IMS 2013 (not shown)



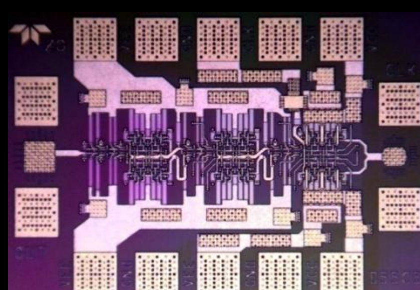
300 GHz fundamental PLL

M. Seo, TSC
IMS 2011



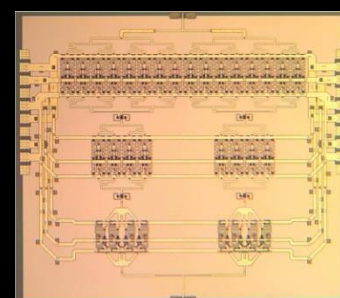
204 GHz static frequency divider (ECL master-slave latch)

Z. Griffith, TSC
CSIC 2010



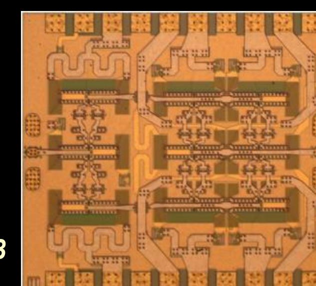
220 GHz 180 mW power amplifier

T. Reed, UCSB
CSICS 2013



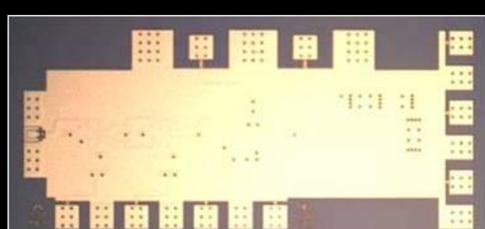
81 GHz 470 mW power amplifier

H-C Park UCSB
IMS 2014



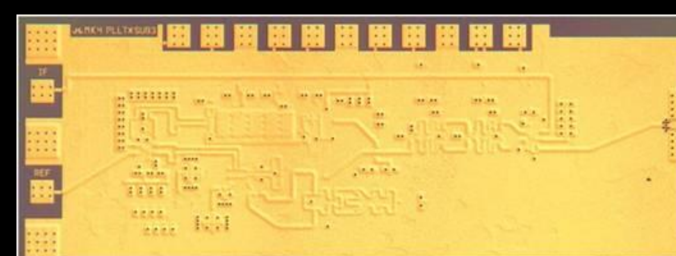
Integrated 300/350GHz Receivers:

LNA/Mixer/VCO
M. Seo TSC

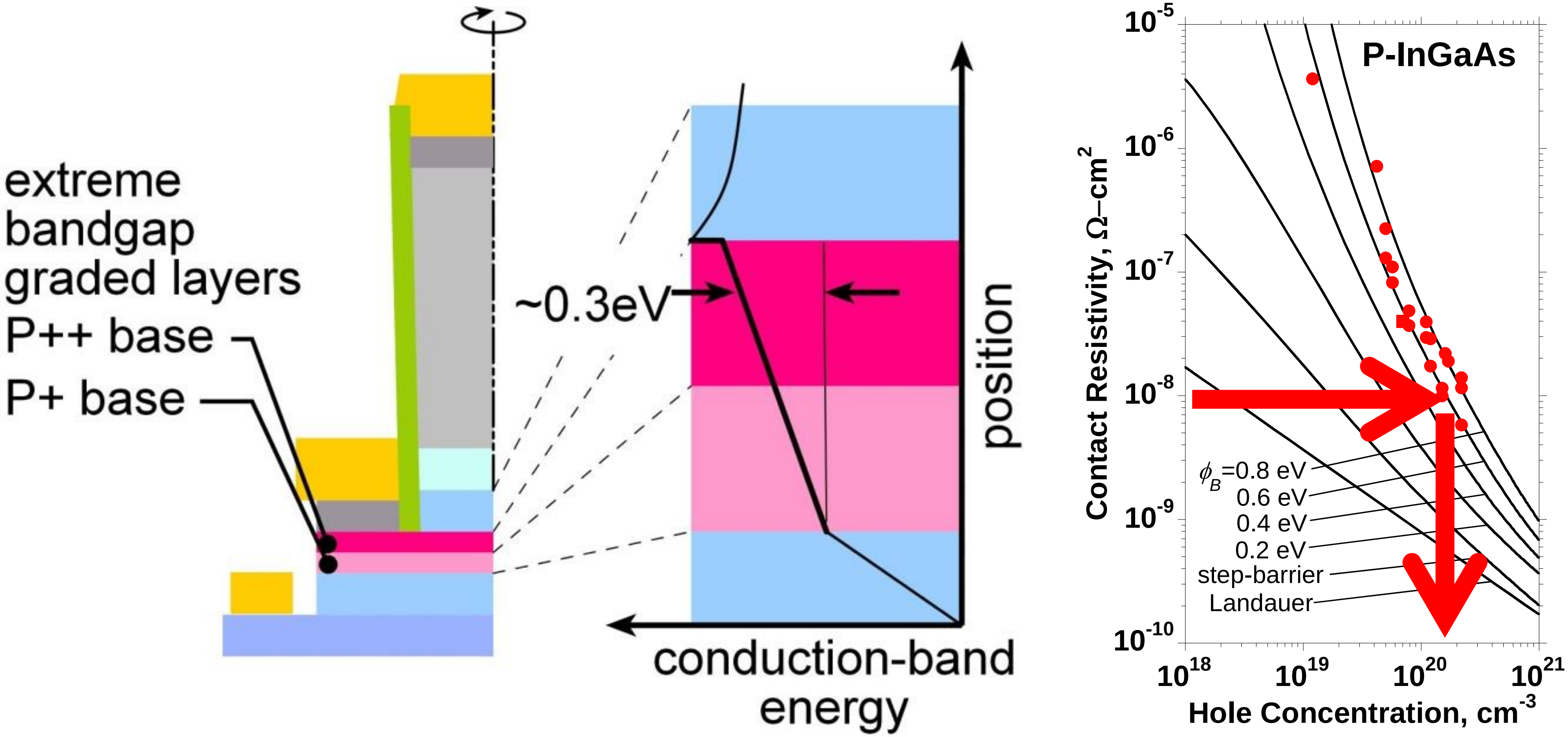


600 GHz Integrated Transmitter

PLL + Mixer
M. Seo TSC



Towards a 3 THz InP Bipolar Transistor



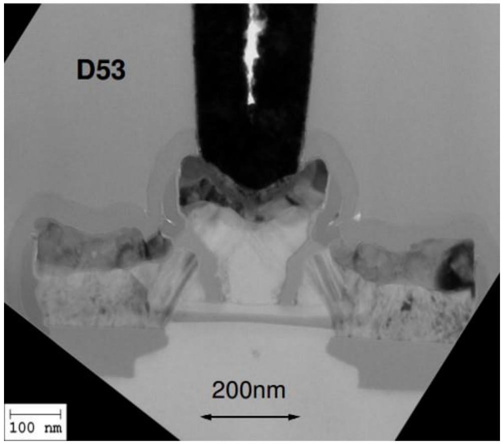
Extreme base doping→ low-resistivity contacts→ high f_{max}

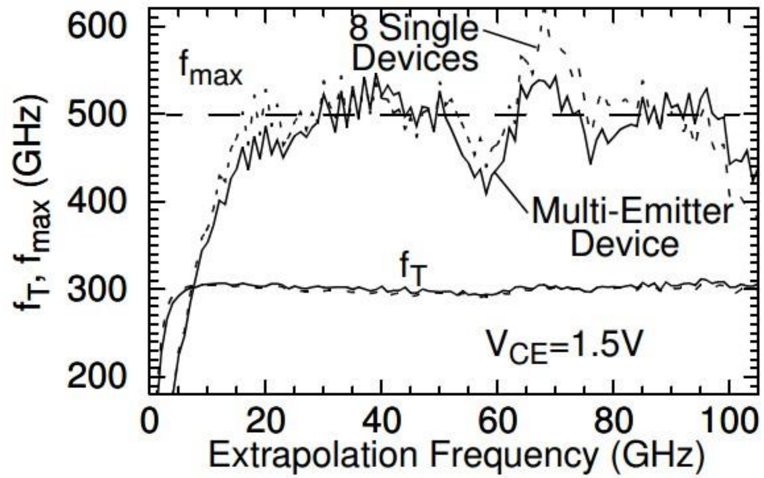
Extreme base doping→ fast Auger (NP^2) recombination→ low β.

Solution: very strong base compositional grading→ high β

1/2-THz SiGe HBTs

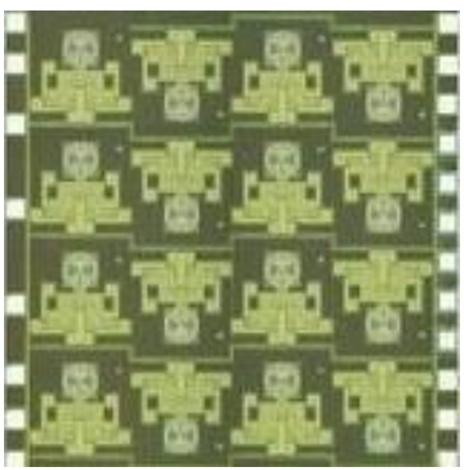
500 GHz f_{max} SiGe HBTs Heinemann et al. (IHP), 2010 IEDM





16-element multiplier array @ 500GHz (1 mW total output)

U. Pfeiffer et. al. (Wuppertal / IHP) , 2014 ISSCC



Towards a 2 THz SiGe Bipolar Transistor

Similar scaling
InP: 3:1 higher collector velocity
SiGe: good contacts, buried oxides

Key distinction: Breakdown
InP has:
thicker collector at same f_τ,
wider collector bandgap

Key requirements:
low resistivity Ohmic contacts
note the high current densities

	InP	SiGe	
emitter			
junction width	64	**18**	nm
access resistivity	2	**0.6**	Ω–μm^2
base			
contact width	64	18	nm
contact resistivity	2.5	**0.7**	Ω–μm^2
collector			
thickness	53	15	nm
current density	36	**125**	mA/μm^2
breakdown	2.75	1.3?	V
f_τ	1000	1000	GHz
f_{max}	2000	2000	GHz

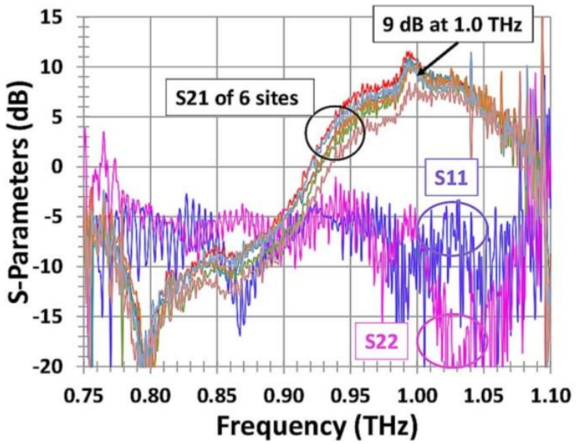
Assumes collector junction 3:1 wider than emitter.
Assumes SiGe contacts no wider than junctions

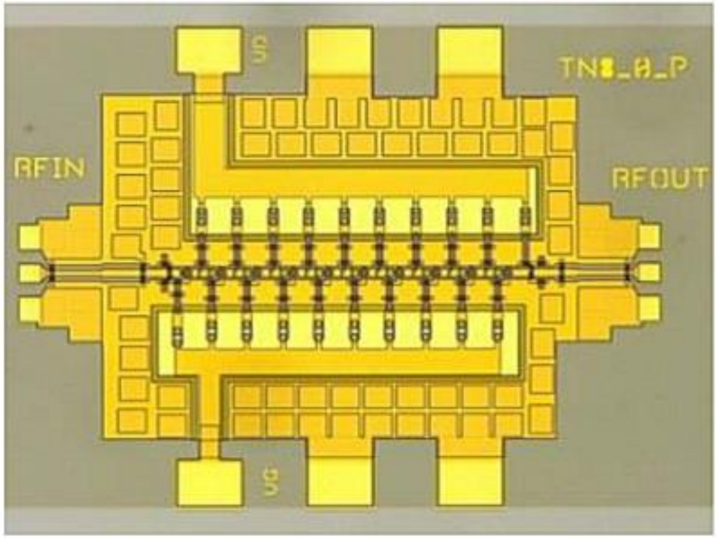
InP Field-Effect Transistors

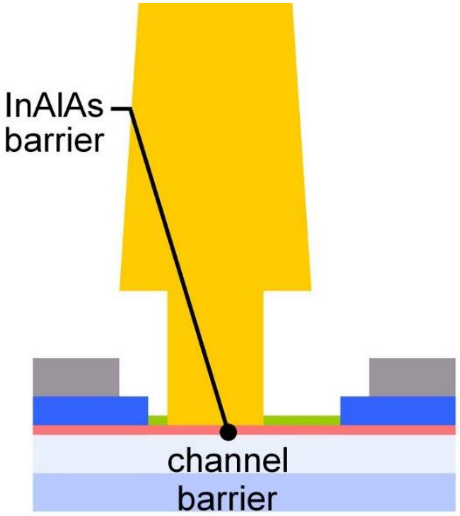
State of the art in InP HEMTs

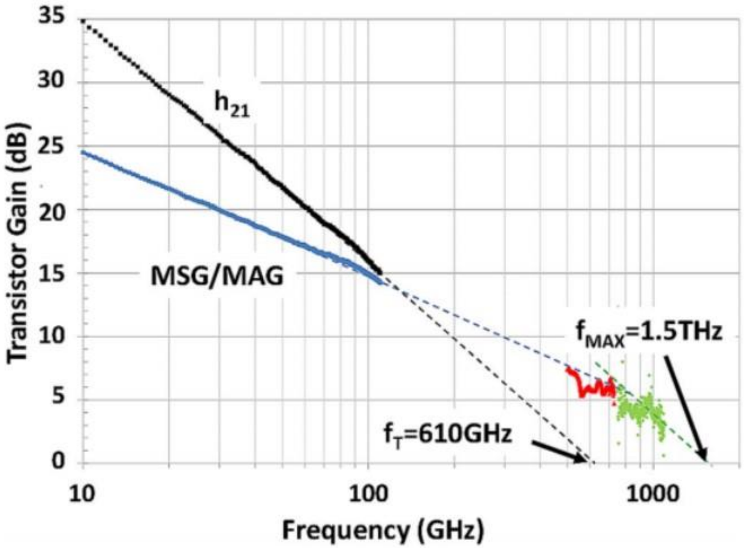
First Demonstration of Amplification at 1 THz Using 25-nm InP High Electron Mobility Transistor Process

Xiaobing Mei, et al, IEEE EDL, April 2015 **(Northrop-Grumman)**

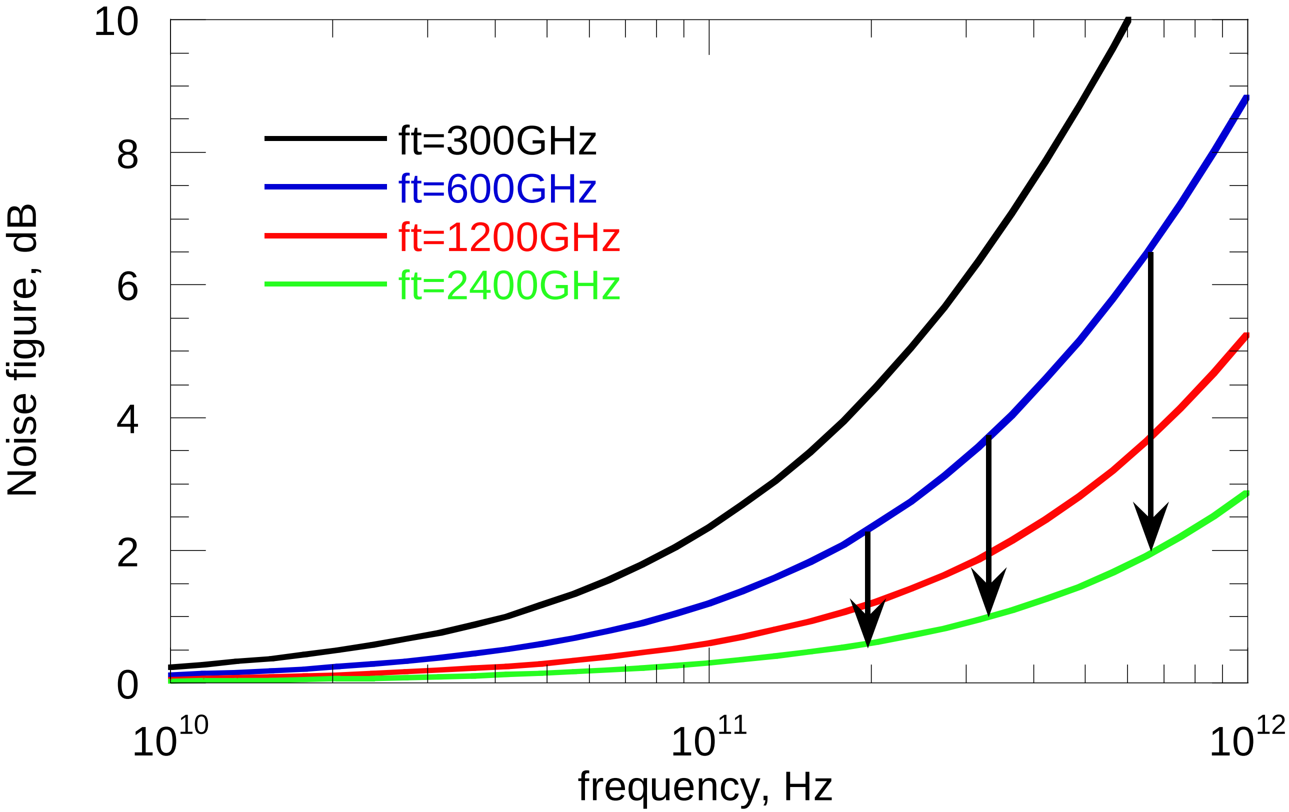








HEMTs: Key Device for Low Noise Figure



$$F_{\min} \approx 1 + 2\sqrt{g_m(R_s + R_g + R_i)\Gamma} \cdot \left(\frac{f}{f_\tau}\right) + 2g_m(R_s + R_g + R_i)\Gamma \cdot \left(\frac{f}{f_\tau}\right)^2$$

$$\Gamma \approx 1$$

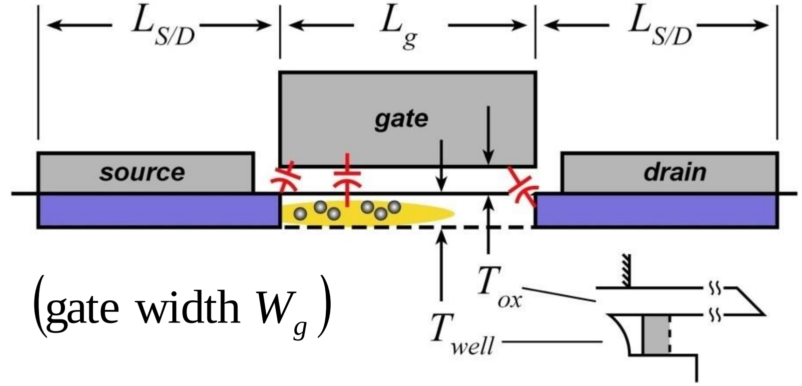
Hand-derived modified Fukui Expression, fits CAD simulation extremely well.

2:1 to 4:1 increase in f_τ → greatly improved noise @ 200-670 GHz.

Better range in sub-mm-wave systems; or use smaller power amps.

or enable yet higher-frequency systems

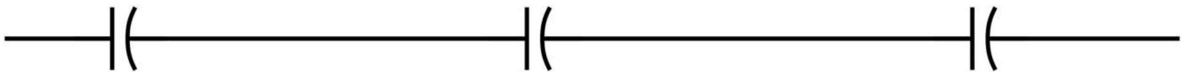
FET Design



$$C_{gd} \cong C_{gs,f} \cong \varepsilon W_g$$

$$g_m = C_{g-ch} \cdot (v / L_g)$$

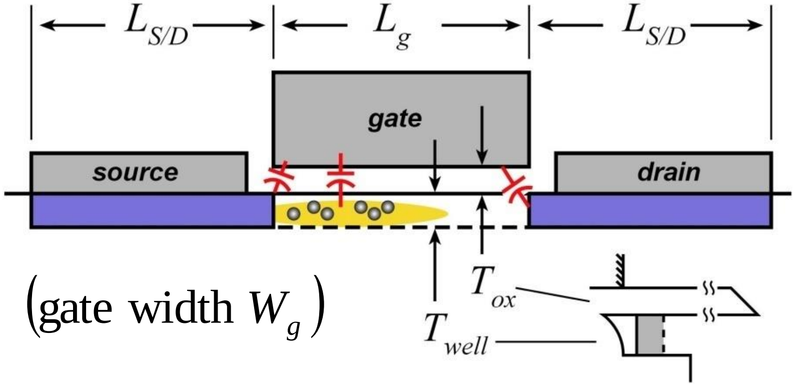
$$C_{g-ch} = \frac{L_g W_g}{T_{ox}/\varepsilon_{ox} + T_{\mathrm{well}}/2\varepsilon_{\mathrm{well}} + (q^2/\text{well state density})}$$



$$v \propto \begin{pmatrix} \text{voltage division ratio between} \\ \text{the above three capacitors} \end{pmatrix}^{-1/2} \cdot \frac{1}{\sqrt{\text{transport mass}}}$$

$$R_{DS} \approx L_g / (W_g v \varepsilon) \qquad R_S = R_D = \frac{\rho_{\mathrm{contact}}}{L_{\mathrm{S/D}} W_g}$$

FET Design: Scaling



$$C_{gd} \cong C_{gs,f} \cong \varepsilon W_g$$

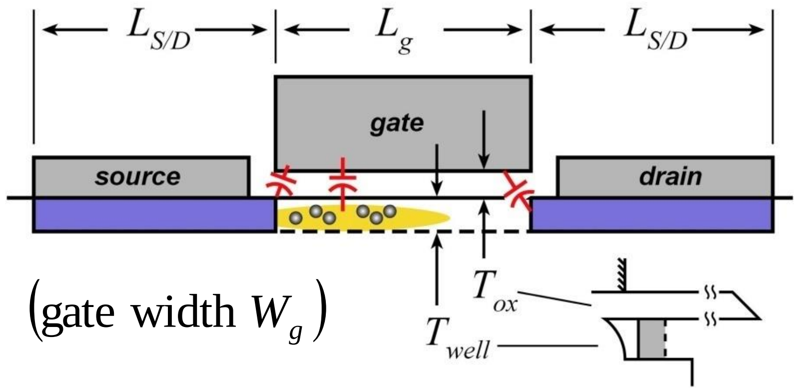
$$g_m = C_{g-ch} \cdot (v / L_g)$$

$$C_{g-ch} = \frac{L_g W_g}{T_{ox}/\varepsilon_{ox} + T_{\text{well}}/2\varepsilon_{\text{well}} + (q^2/\text{well state density})}$$

$$v \propto \begin{pmatrix} \text{voltage division ratio between} \\ \text{the above three capacitors} \end{pmatrix}^{-1/2} \cdot \frac{1}{\sqrt{\text{transport mass}}}$$

$$R_{DS} \approx L_g/(W_g v \varepsilon) \qquad R_S = R_D = \frac{\rho_{\text{contact}}}{L_{\text{S/D}} W_g}$$

FET Design: Scaling



2:1 ↓ $$C_{gd} \cong C_{gs,f} \cong \varepsilon W_g$$ 2:1 ↓

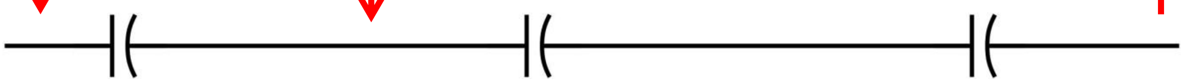
constant 2:1 ↓

$$g_m = C_{g-ch} \cdot (v / L_g)$$ 2:1 ↓

2:1 ↓ 2:1 ↓ 2:1 ↓

$$C_{g-ch} = \frac{L_g W_g}{T_{ox}/\varepsilon_{ox} + T_{\text{well}}/2\varepsilon_{\text{well}} + (q^2/\text{well state density})}$$

2:1 ↓ 2:1 ↓ 2:1 ↑



$$v \propto \left(\begin{array}{c}\text{voltage division ratio between} \\ \text{the above three capacitors}\end{array}\right)^{-1/2} \cdot \frac{1}{\sqrt{\text{transport mass}}}$$

constant constant constant

constant

$$R_{DS} \approx L_g / (W_g v \varepsilon)$$

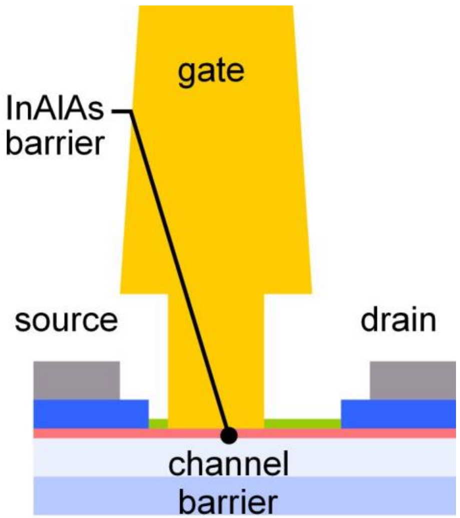
2:1 ↓ 2:1 ↓

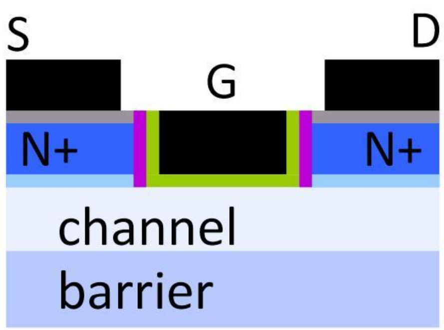
4:1 ↓

$$R_S = R_D = \frac{\rho_{\text{contact}}}{L_{\text{S/D}} W_g}$$

constant 2:1 ↓ 2:1 ↓

FET Scaling Laws (these now broken)



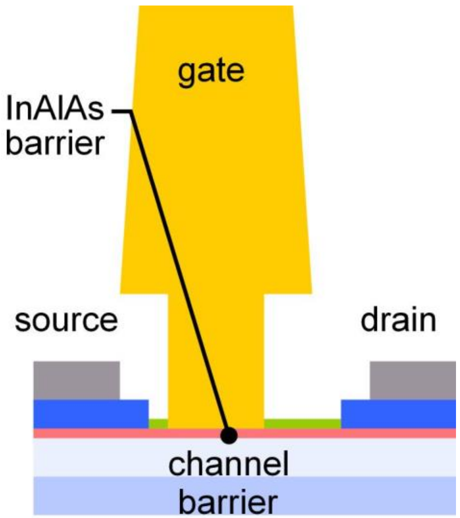


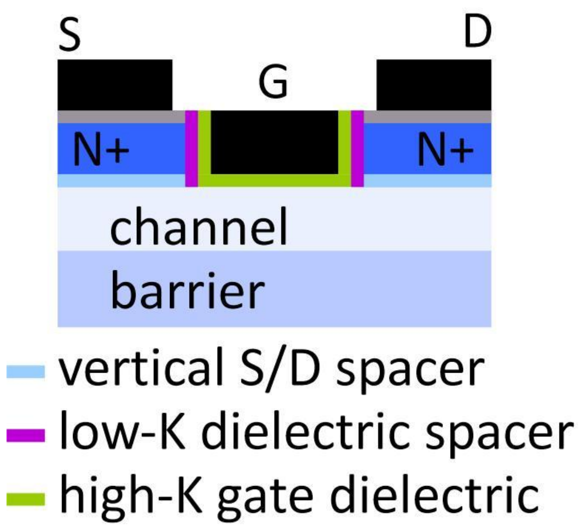
vertical S/D spacer
low-K dielectric spacer
high-K gate dielectric

FET parameter	change
gate length	decrease 2:1
current density (mA/mm)	increase 2:1
transport mass	constant
2DEG electron density	increase 2:1
gate-channel capacitance density	increase 2:1
dielectric equivalent thickness	decrease 2:1
channel thickness	decrease 2:1
channel state density	increase 2:1
contact resistivities	decrease 4:1

fringing capacitance does not scale → linewidths scale as (1 / bandwidth)

FET Scaling Laws (these now broken)





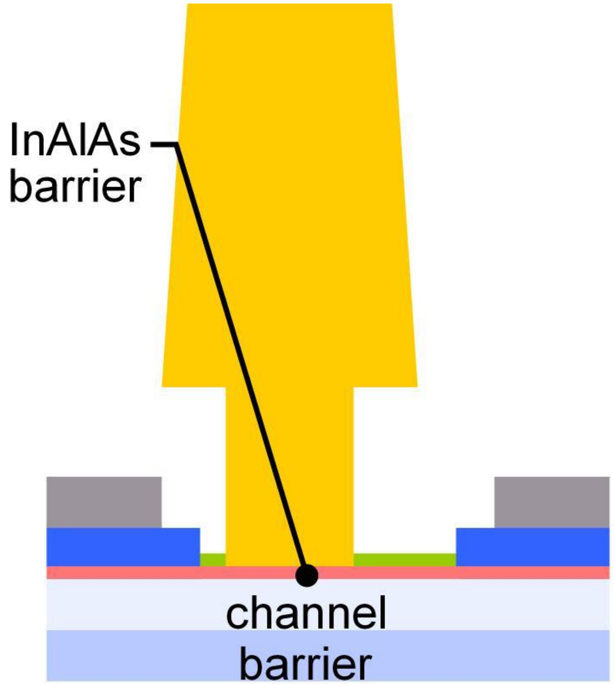
FET parameter	change
gate length	decrease 2:1
current density (mA/mm)	increase 2:1
transport mass	constant
2DEG electron density	increase 2:1
gate-channel capacitance density	increase 2:1
dielectric equivalent thickness	decrease 2:1
channel thickness	decrease 2:1
channel state density	increase 2:1
contact resistivities	decrease 4:1

Gate dielectric can't be much further scaled.
Not in CMOS VLSI, not in mm-wave HEMTs

g_m/W_g (mS/μm) hard to increase
→ C_{end}/g_m prevents f_τ scaling.

Shorter gate lengths degrade electrostatics
→ reduced g_m/G_{ds} → reduced f_{max}/f_τ

Why THz HEMTs no longer scale



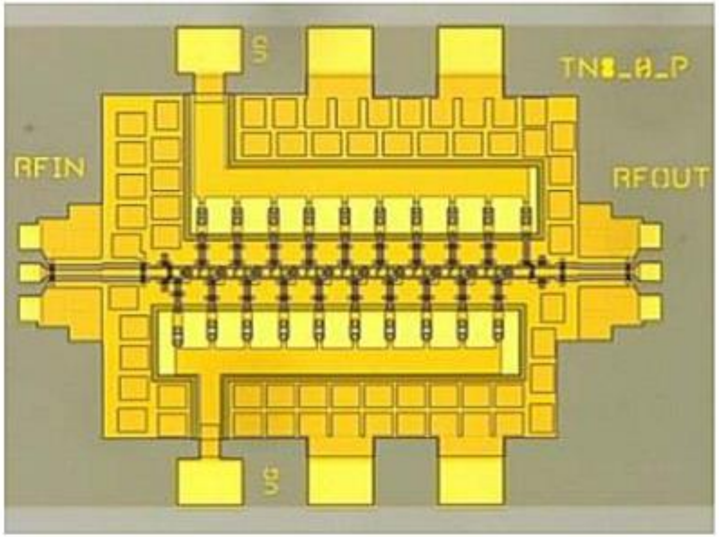
HEMTs: gate barrier also lies under S/D contacts → high S/D access resistance

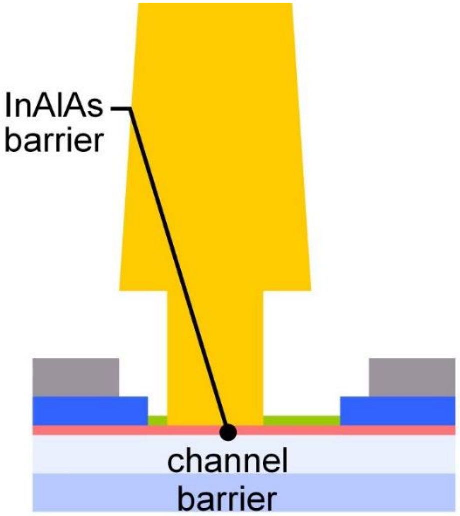
As gate length is scaled, gate barrier must be thinned for high g_m, low G_{ds}
HEMTs: High gate leakage when gate barrier is thinned→ cannot thin barrier

Towards at 2.5 THz HEMT

First Demonstration of Amplification at 1 THz Using 25-nm InP High Electron Mobility Transistor Process

Xiaobing Mei, et al, IEEE EDL, April 2015 **(Northrop-Grumman)**

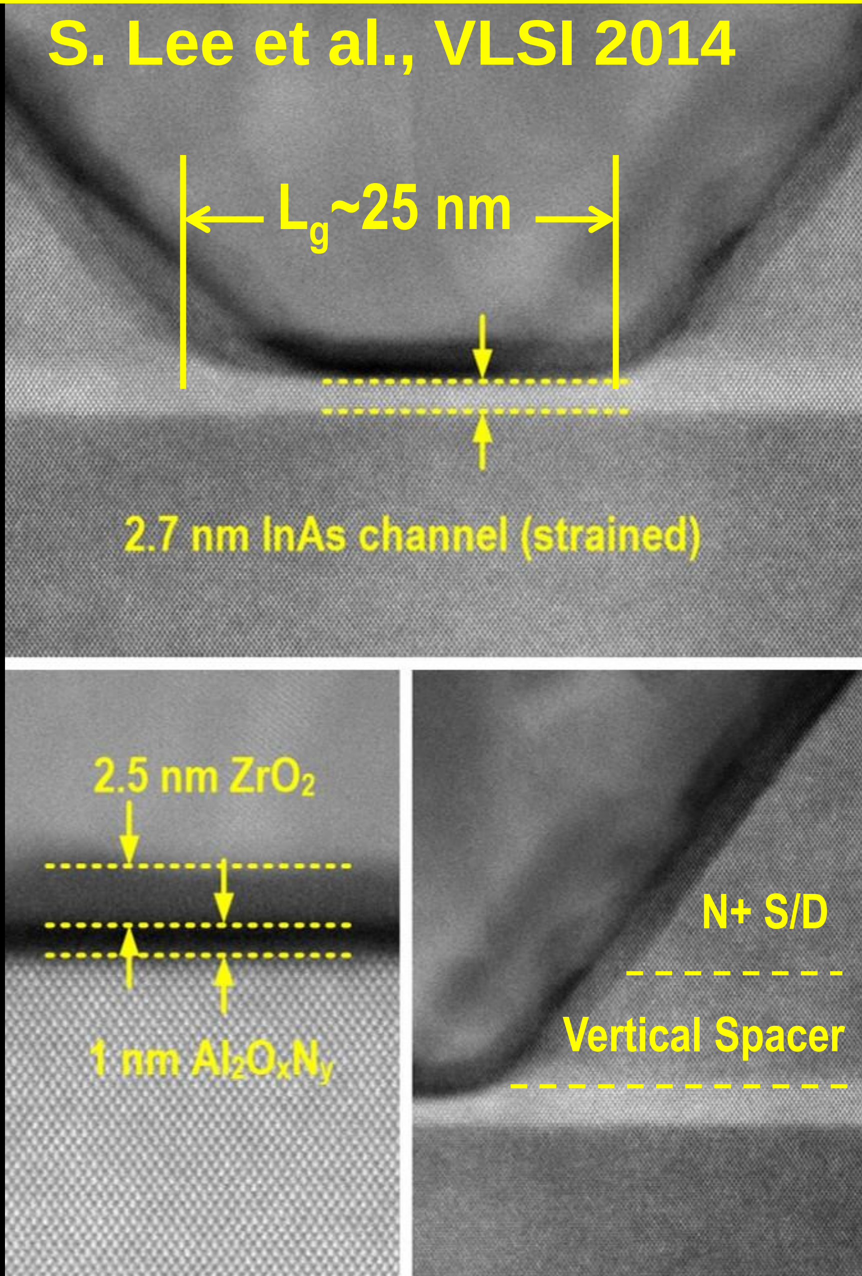


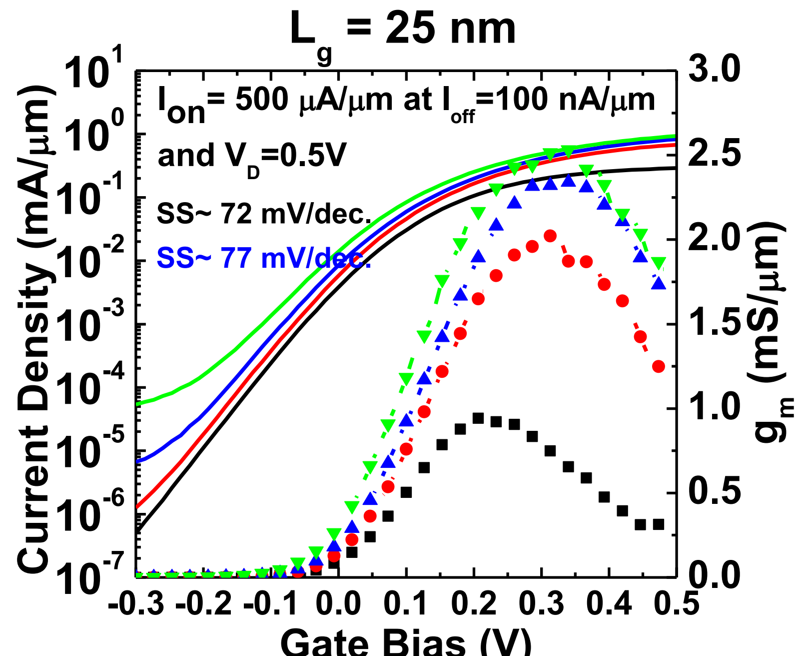


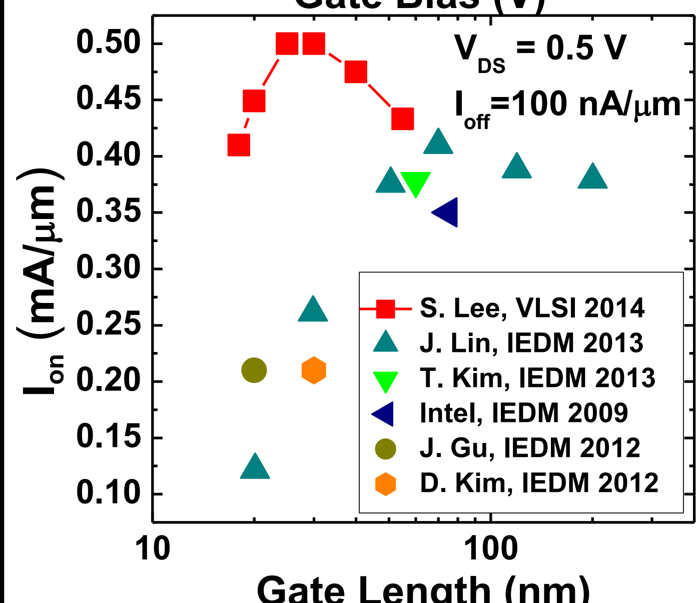
FET scaling laws; 2:1 higher bandwidth	change
gate length	decrease 2:1
current density (mA/mm), g_m (mS/mm)	increase 2:1
transport mass	constant
gate-channel capacitance density	increase 2:1
contact resistivities	decrease 4:1

Need thinner dielectrics, better contacts

Record III-V MOS



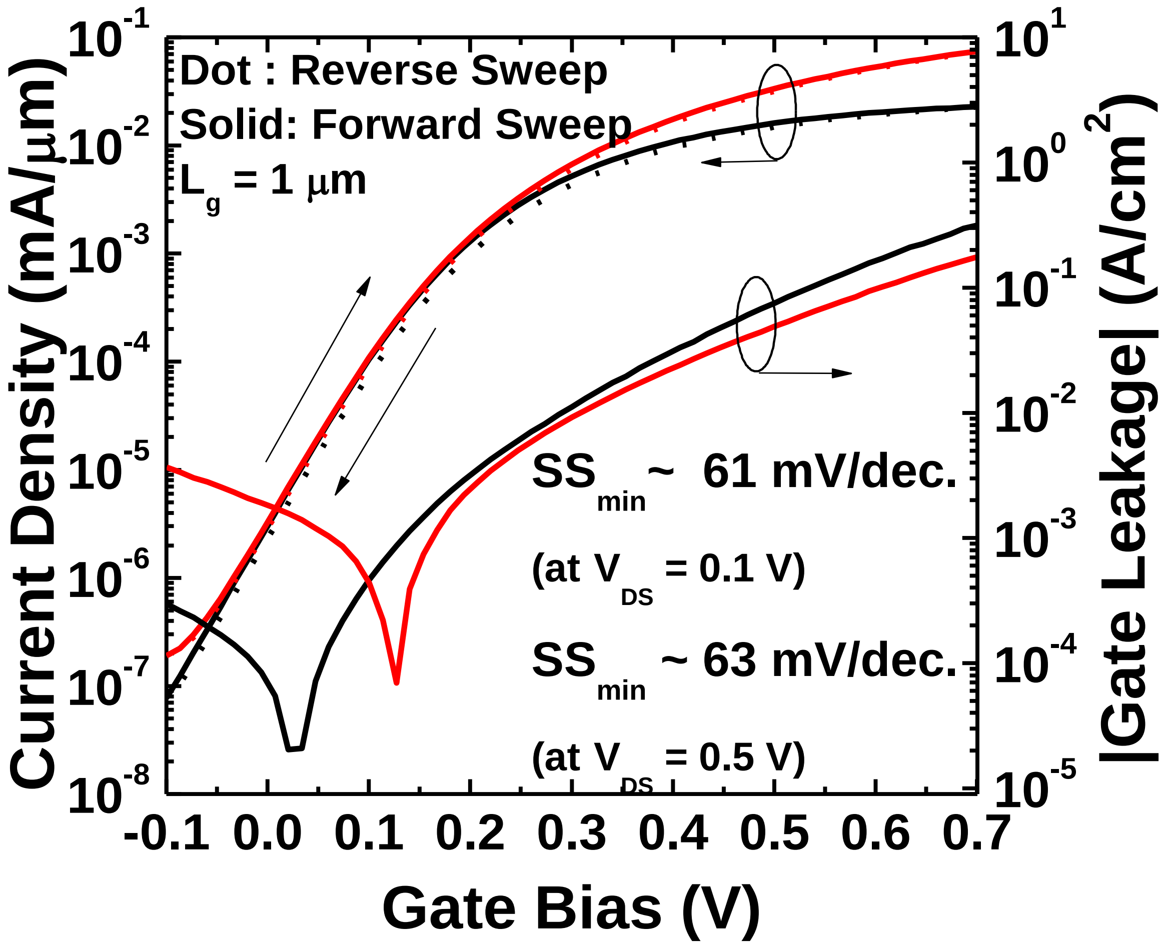




record for III-V

= best UTB SOI silicon

Excellent III-V gate dielectrics



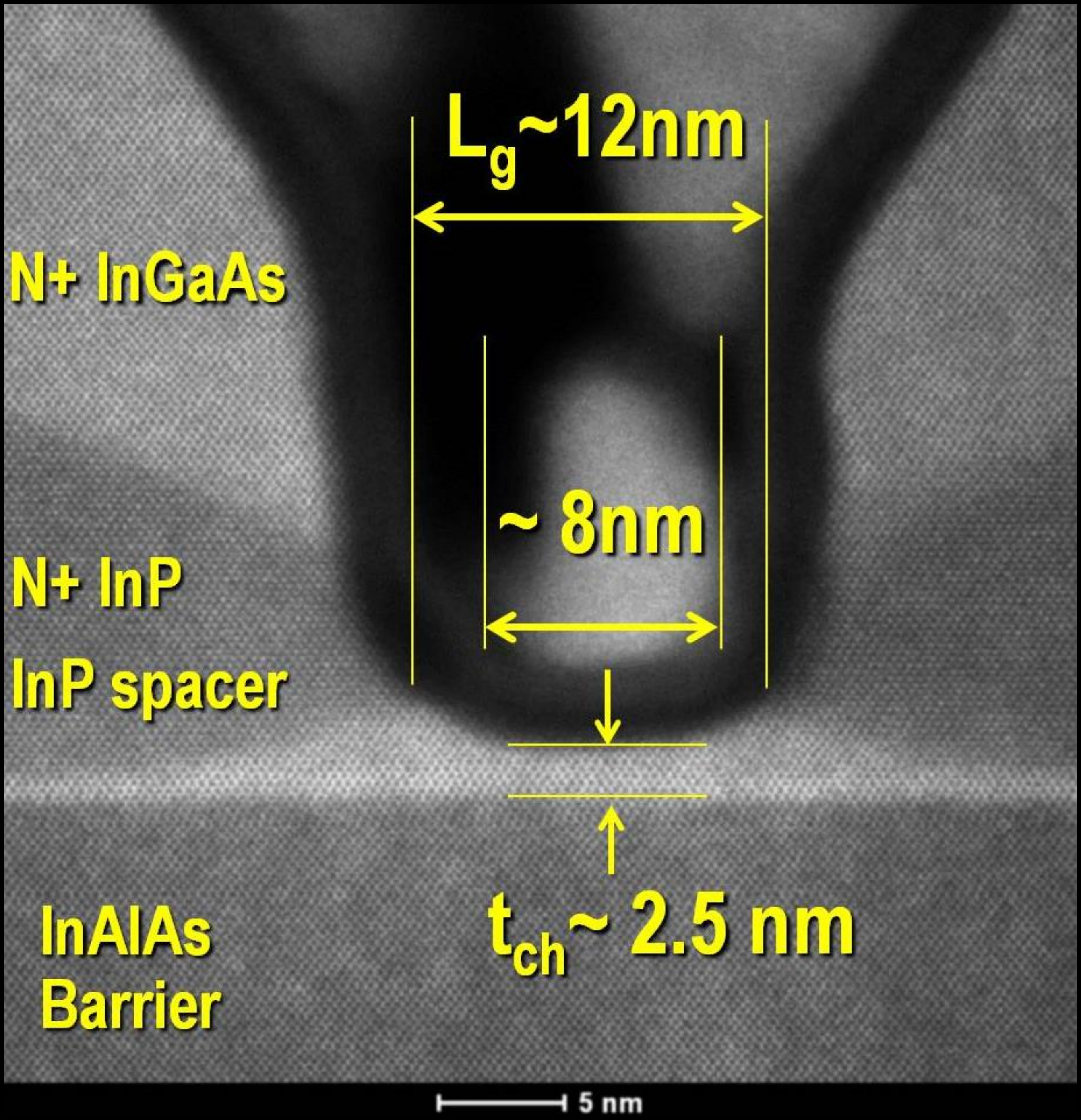
2.5nm ZrO_2
1nm Al_2O_3
2.5nm InAs

V. Chobpattanna, S. Stemmer
FET data: S Lee, 2014 VLSI Symp.

61 mV/dec Subthreshold swing at V_{DS}=0.1 V

Negligible hysteresis

III-V MOS @ L_g = ???

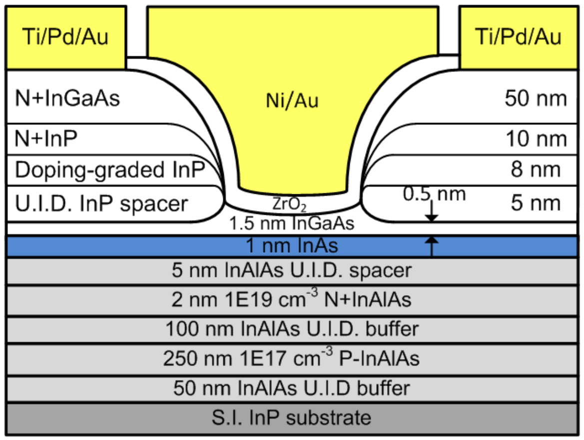


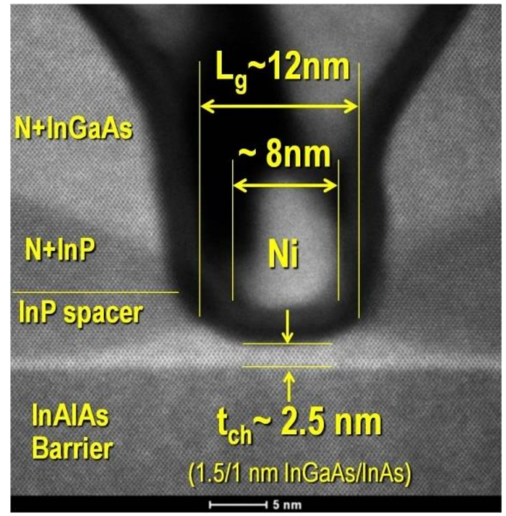
Huang *et al.*, 2015 DRC

Image courtesy of S. Kraemer (UCSB)

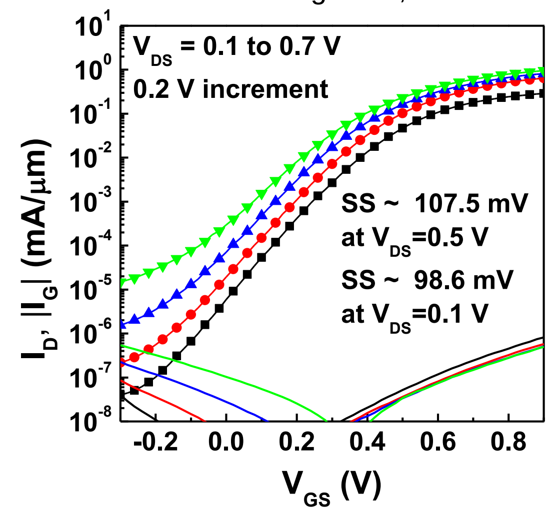
Towards at 2.5 THz HEMT

VLSI III-V MOS

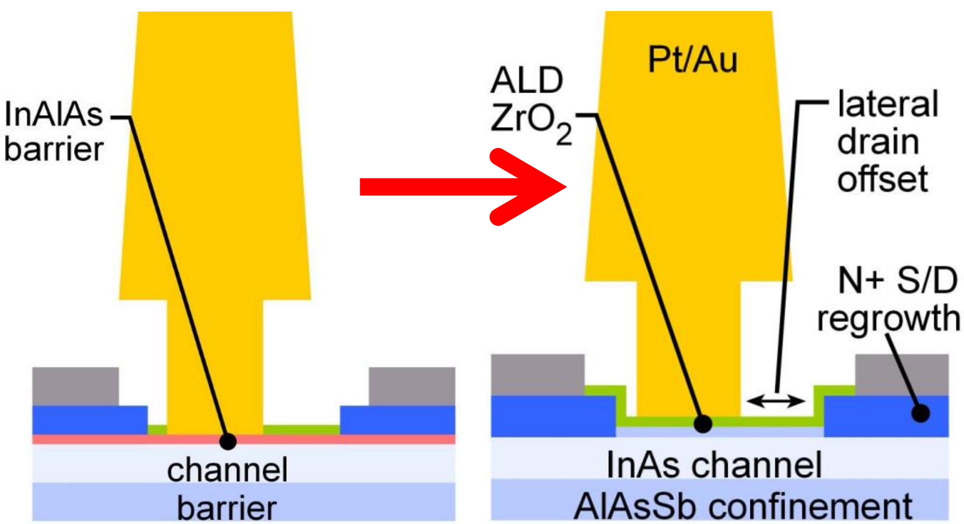




C. Y. Huang et al., DRC 2015



THz III-V MOS

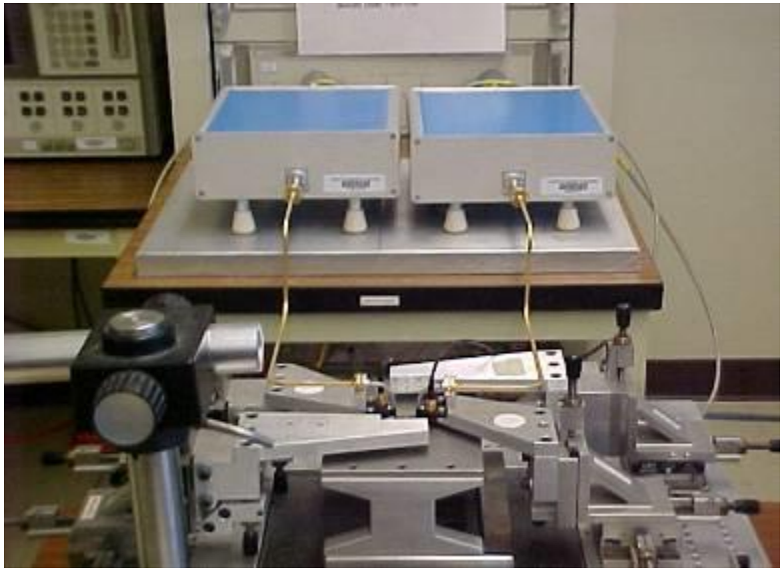


gate length	36	18	9	nm
EOT	0.8	0.4	0.2	nm
well thickness	5.6	2.8	1.4	nm
effective mass	0.05	0.08	0.08	times m_0
# bands	1	1	1	--
S/D resistivity	150	74	37	Ω-μm
extrinisic g_m	2.5	4.2	6.4	mS/μm
on-current	0.55	0.8	1.1	mA/μm
f_τ	0.70	1.2	2.0	THz
f_{max}	0.81	1.4	2.7	THz

mm-wave measurements

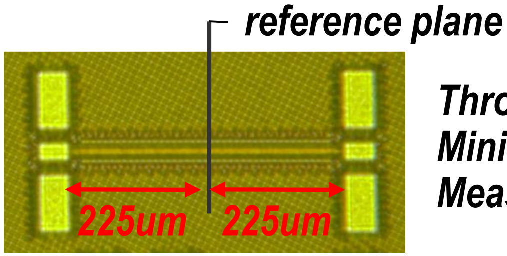
On-Wafer Network Analysis: 750+ GHz

- Agilent, Rhode/Schwarz network analyzer,
- *Oleson Microwave Lab or Virginia Diodes* frequency extenders
- micro-coax wafer probes with waveguide connections
  - GGB Industries,
  - Cascade Microtech
  - University of Virgina.
- Internal bias Tee's in probes
- Mostly on-wafer calibration standards.



On-Wafer Through-Reflect-Line (TRL) Calibration

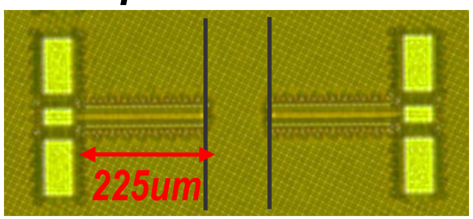
Through



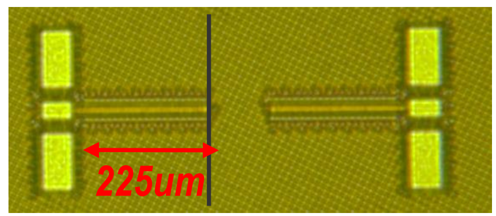
Through line should be long for large probe separation.
Minimizes probe-probe coupling.
Measurements normalized to the line characteristic impedance.

Reflect

open

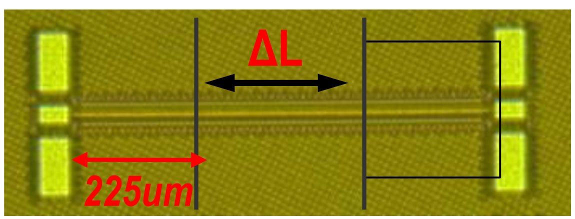


short



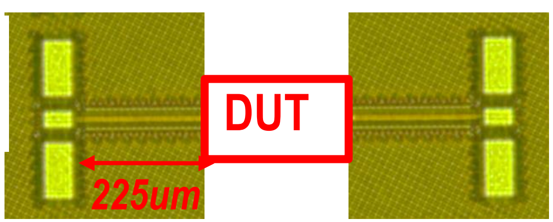
Either open or short needed.
Standards need not be accurate.
"Open" must have Γ closer to that of open than that of short.
Ports 1 & 2 must be symmetric.

Line



ΔL= 90 deg @center frequency.
$\lambda/8<\Delta L<3\lambda/8$

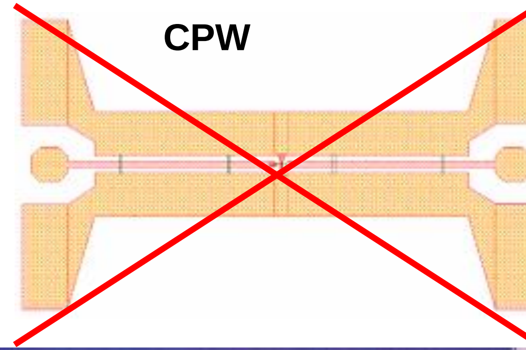
Device Under Test



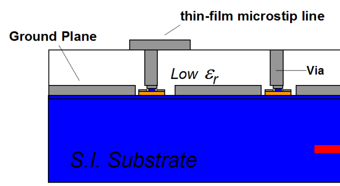
Please see also:
http://www.ece.ucsb.edu/Faculty/rodwell/publications_and_presentations/publications/204vg.ppt

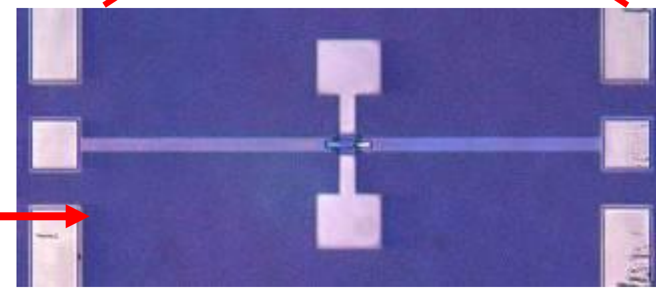
On-Wafer Line Reflect Linie Calibration

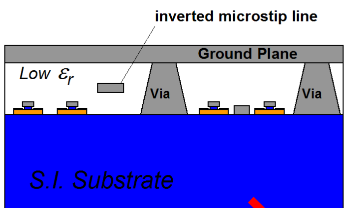
Extended Reference planes
transistors placed at center of long on-wafer line
LRL standards placed on wafer
large probe separation → probe coupling reduced
still should use the best-shielded probes available

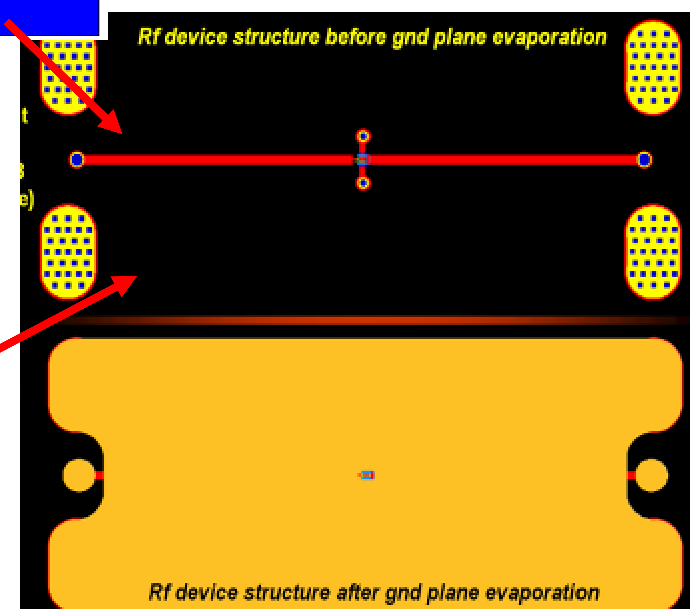


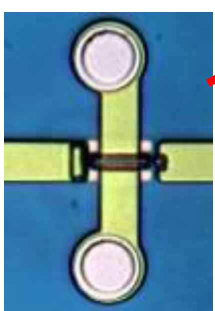
Problem: substrate mode coupling
method will FAIL if lines couple to substrate modes
→ method works very poorly with CPW lines
need on wafer thin-film microstrip lines

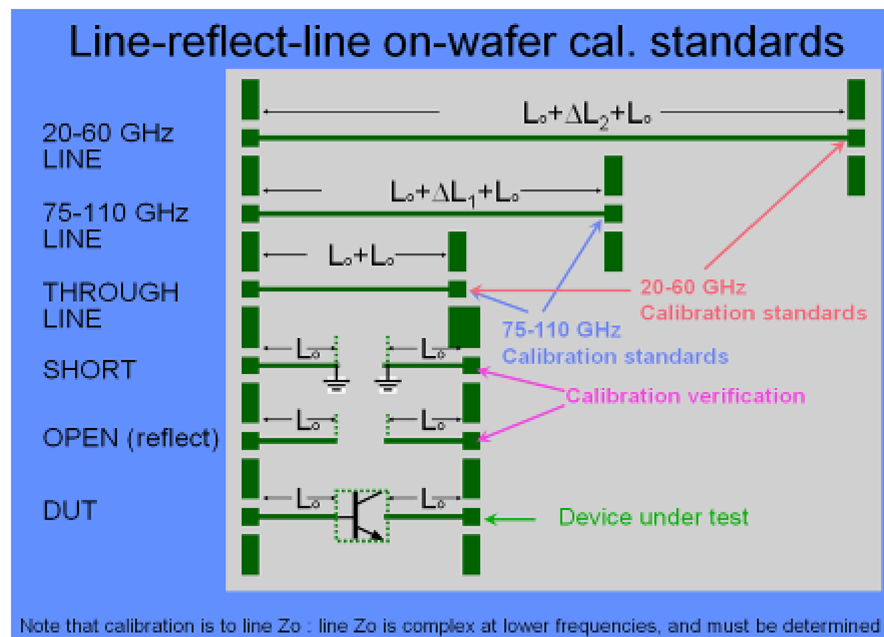












Difficulties with >100 GHz On-Wafer Calibration

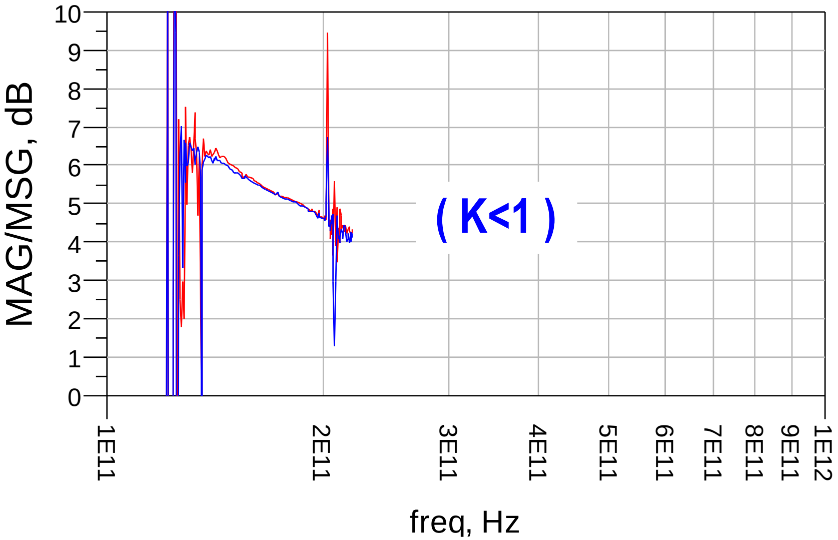
Data on two layouts of 65 nm MOSFET

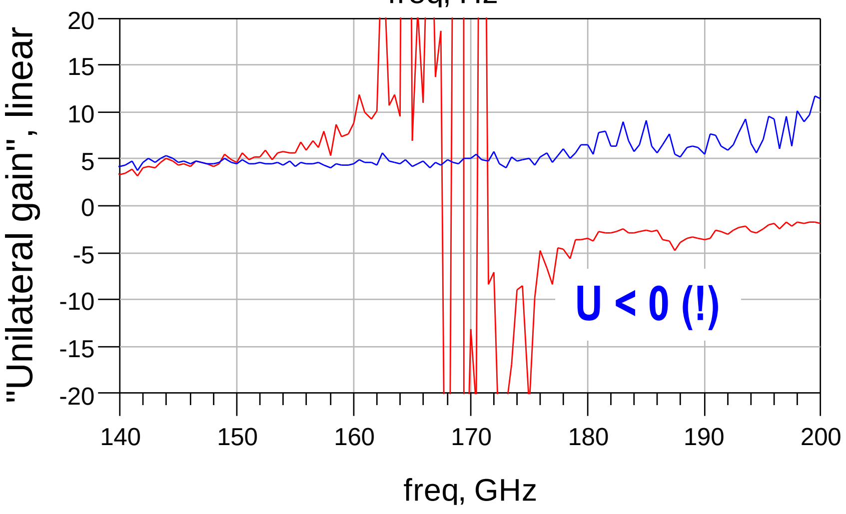
Measured Y-parameters correlate reasonably with expected device model.

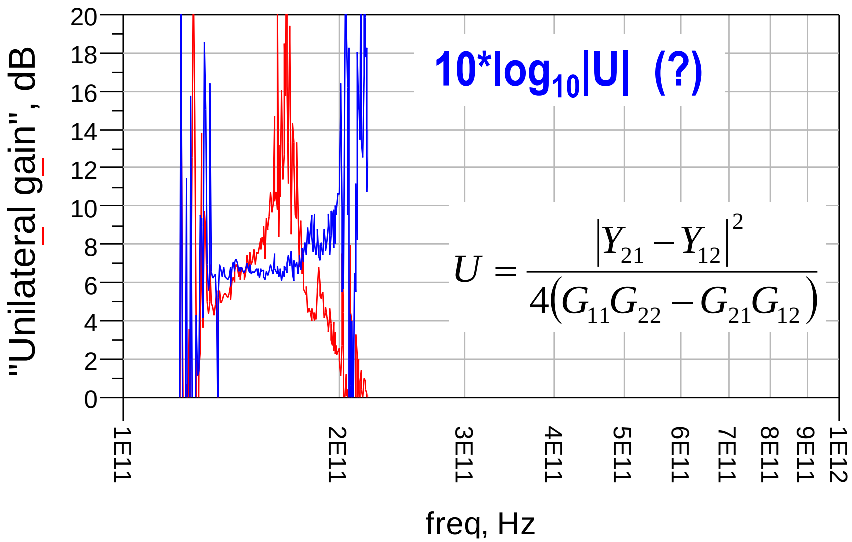
Small errors in measured 2-port parameters result in large changes in Unilateral gain and Rollet's stability factor; neither measurement is credible.

Y_{12} appears to be the key problem.

IC S_{ij} measurements are fine.
Transistor f_{max} measurements are hard.





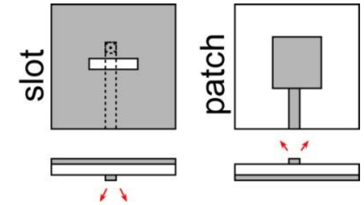


$$U = \frac{|Y_{21} - Y_{12}|^2}{4(G_{11}G_{22} - G_{21}G_{12})}$$

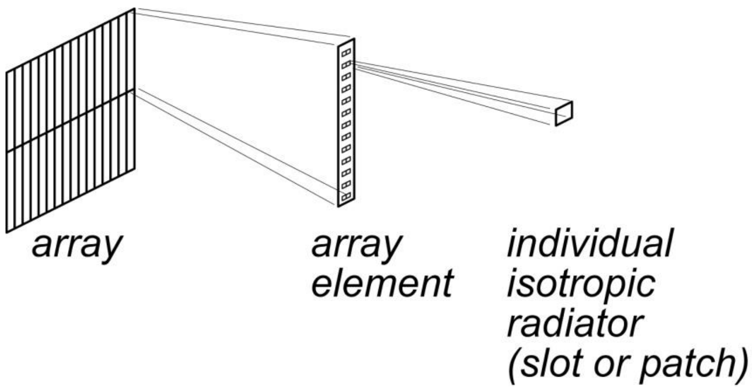
Packaging and antennas

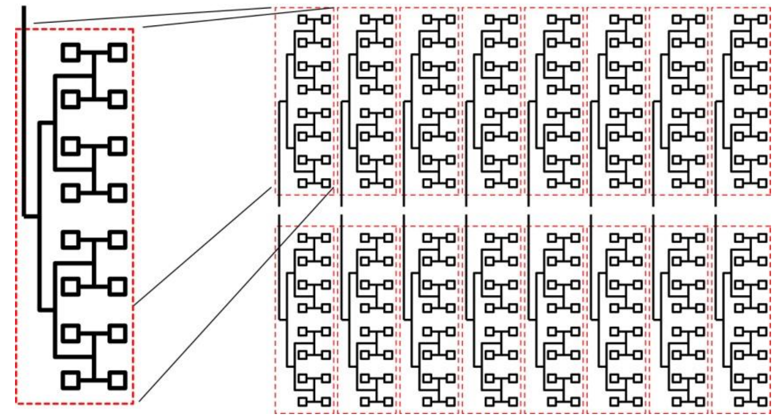
The Antenna Feed Loss Problem

array elements are many λ long
overall array can be very big
→ ***high feed line losses***



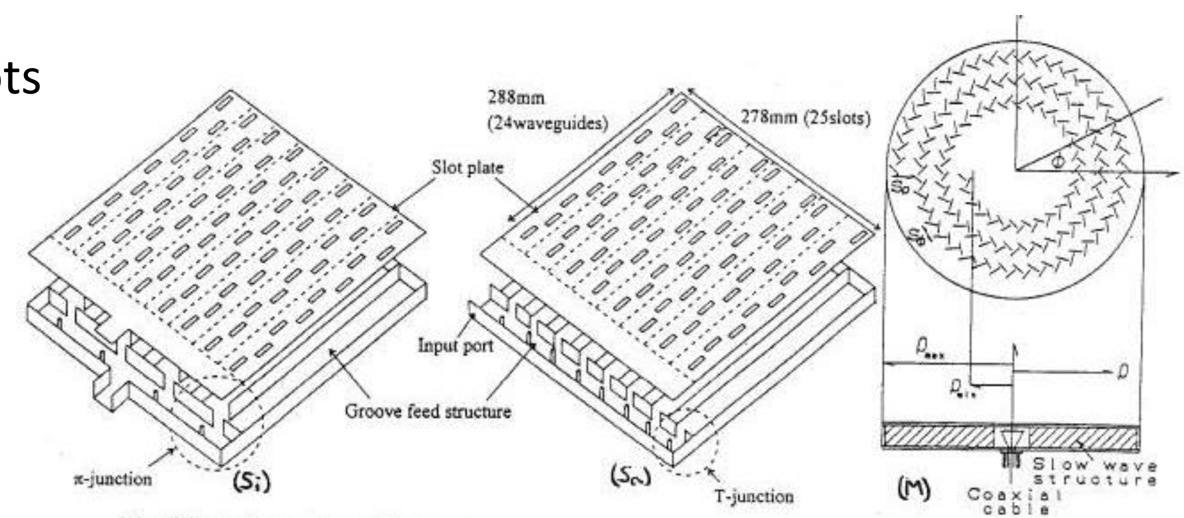
Use distribution amplifiers ?





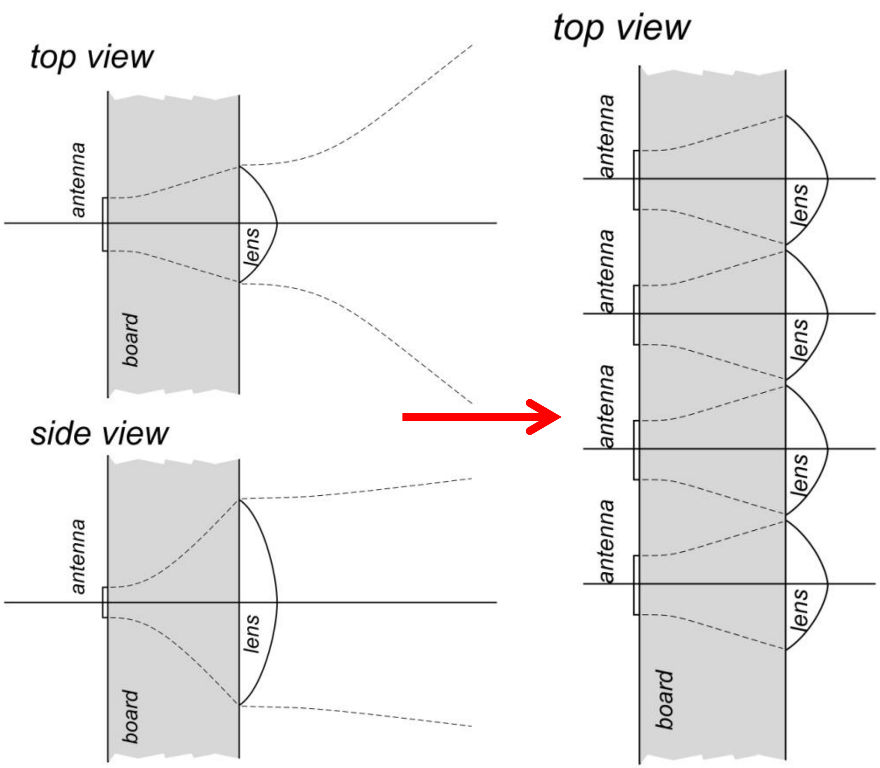
One solution:
waveguide-fed arrays of slots

Use to feed array tile:
overall array needs steering

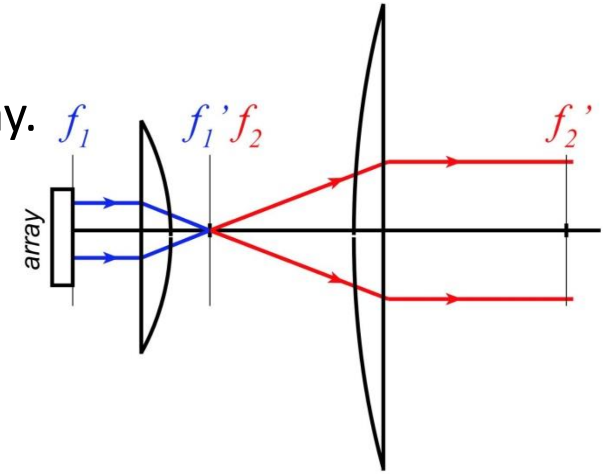


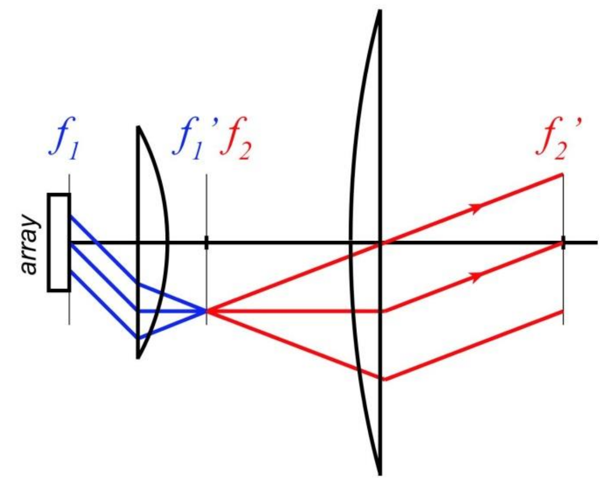
Using lenses to reduce feed loss

Lenses on
individual
array elements.



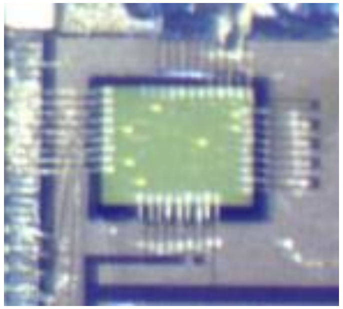
...or on the
overall array.





Here the challenge is
maintaining constant beamwidth
over wide steering angles.

mm-wave interfaces: packaging



Wire-bonds:

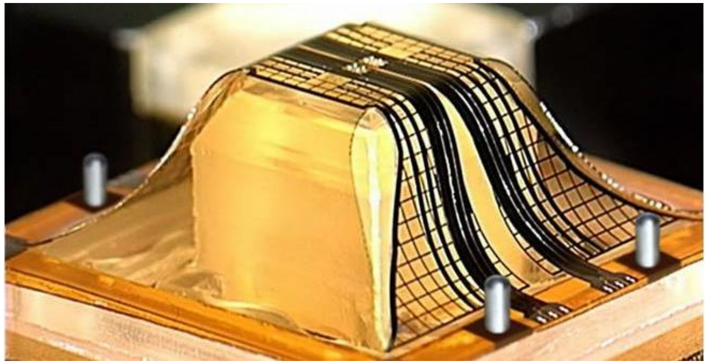
With care, >60GHz can be coupled over wire-bonds.
Coupling of multiple lines remains problematic .

Flip-chip bonds

Standard C4 bonds very capacitive; tuning OK @ 60GHz. Possibly higher.
Option: more highly scaled bonds. Must contact vendors.
Heat removal problematic in flip-chip ICs

Flexible polyimide interconnect substrate

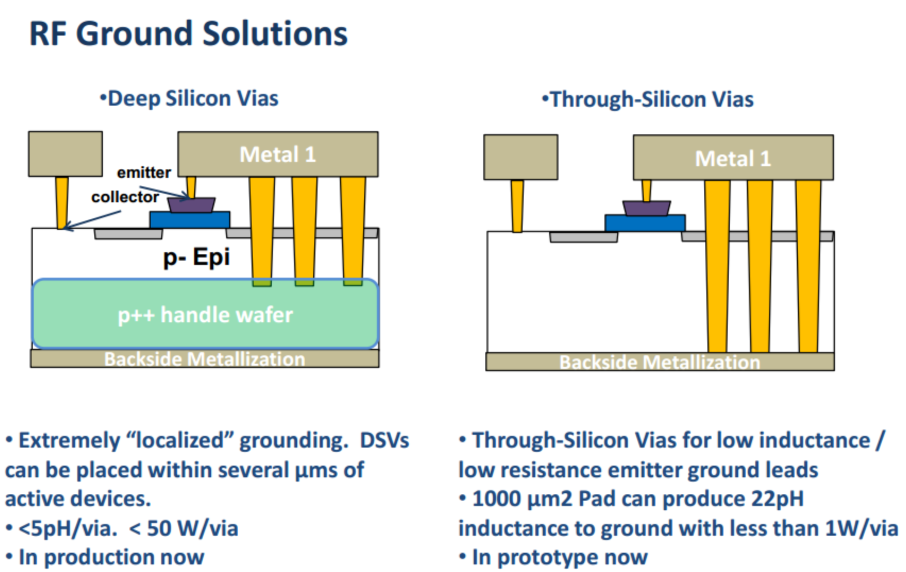
Used in Cascade micotech multi-signal probes, in some 60GHz products.
Ground integrity, low inductance mm-wave connections.
Must identify vendor.

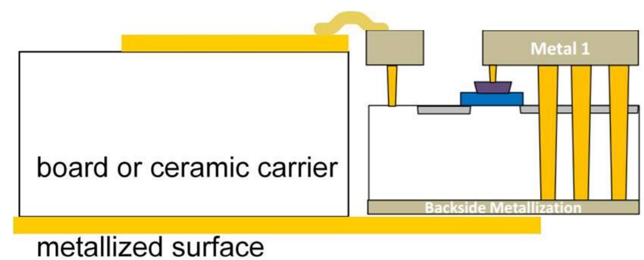


https://www.cmicro.com/products/probe-cards/the-technology/thin-film-technology/cascade-microtech-s-thin-film-technology

mm-wave interfaces: packaging

<u>Through-silicon vias for RF grounding (TowerJazz, also IBM/GF)</u>
very low ground inductance
low losses, low crosstalk in mm-wave IC-package connections





mm-wave
IC Design

Reactively-Tuned IC Design: Concepts

What's the most gain we can get ? Do we care ?

Maximum available gain : unconditionally stable transistor. No feedback. Match.

$$G_{ma} = \left\| \frac{S_{21}}{S_{12}} \right\| \cdot \left(K - \sqrt{K^2 - 1} \right) \qquad \text{where } K = \frac{1 - \|S_{11}\|^2 - \|S_{22}\|^2 + \|S_{11}S_{22} - S_{12}S_{21}\|^2}{2 \cdot \|S_{12}S_{21}\|} \text{ (Rollet stability factor).}$$

Maximum stable gain : potentially unstable transistor. No feedback. Stabilize. Match.

$$G_{ms} = \left\| \frac{S_{21}}{S_{12}} \right\|$$

Unilateral gain : lossless feedback until $S_{12} = 0$, then match

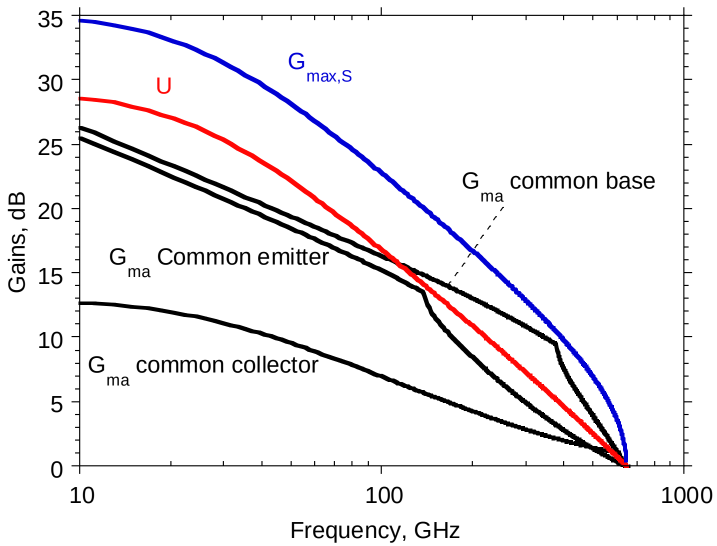
$$U = \frac{|Y_{21} - Y_{12}|^2}{4(G_{11}G_{22} - G_{21}G_{12})}$$

Singhakowinta's gain :

appropriate lossless reactive feedback, match

$$G_{\max,S} = (2U - 1) + 2U^{1/2}(U - 1)^{1/2}$$

Highest feasible gain given unconditional stability



A. Singhakowinta & A. R. Boothroyd, International Journal of Electronics, Volume 21, Issue 6, 1966, pages 549-560, DOI:10.1080/00207216608937931
O. Momeni and E. Afshari, 2011 IEEE Custom Integrated Circuits Conference (CICC), San Jose, CA, 2011, pp. 1-4, doi: 10.1109/CICC.2011.6055322

What's the most gain we can get ? Do we care ?

Low-noise amplifiers
designed for low noise figure, fairly high IP3

Power amplifiers
designed for high Psat, PAE, sufficiently low IM3

IF amplifiers
designed for low noise figure, high IP3.

Practical amplifiers are rarely designed for highest gain.

Real-world relevance of G_{ma}, G_{ms}, $G_{max,S}$ is not clear.

Practical designs would benefit from ***new theory***
Quantities similar to G_{ma}, G_{ms}, $G_{max,S}$ above
But under constraints of high-power or low-noise tuning.
I know of no such published work.

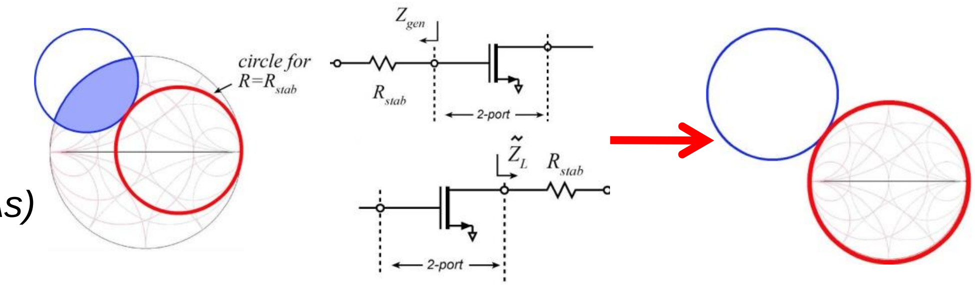
RF-IC Design: Simple & Well-Known Procedures

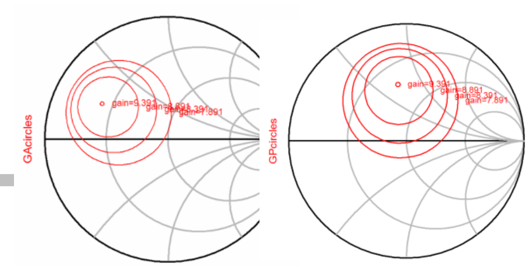
1: (over)stabilize at the design frequency
guided by stability circles

2: Tune input for F_{min} (LNAs) or output for P_{sat} (PAs)

3: Tune remaining port for maximum gain

4: Add out-of-band stabilization.

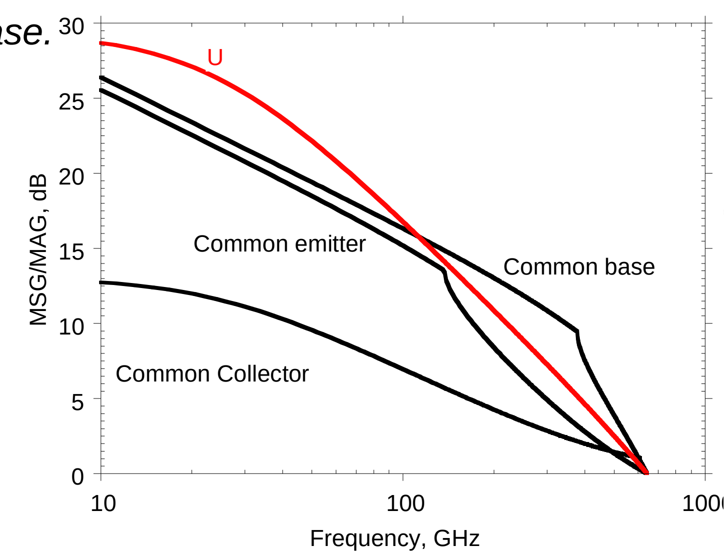


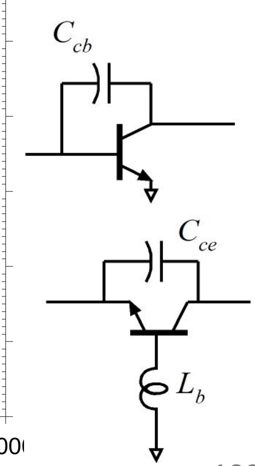


There are many ways to tune port impedances: microstrip lines, MIM capacitors, transformers
Choice guided by tuning losses. No particular preferences.

For BJT's, MAG/MSG usually highest for common-base.

Common-base gain is however reduced by:
base (layout) inductance
emitter-collector layout capacitance.



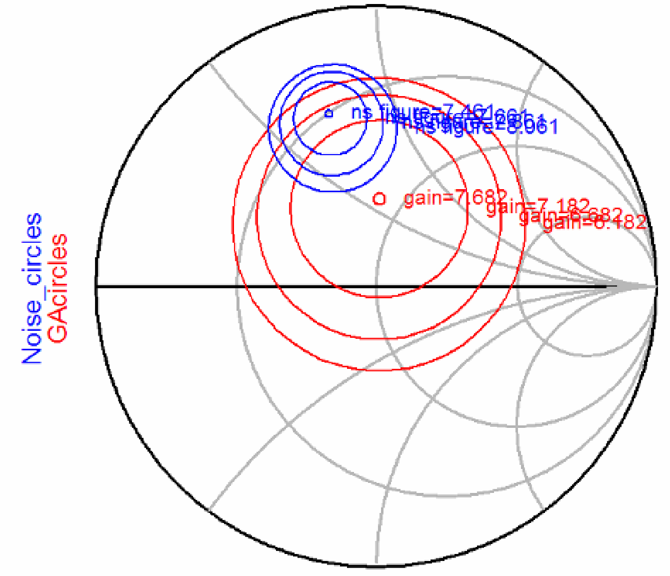


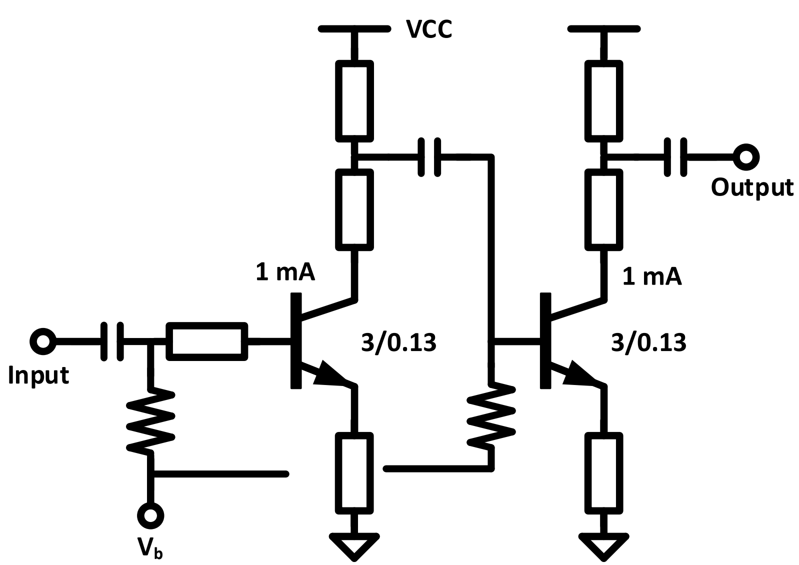
Low-Noise Amplifier Design

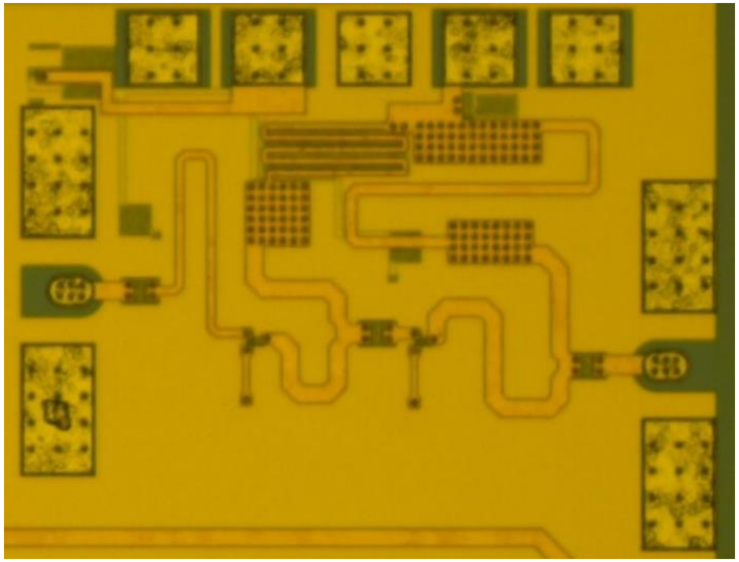
Inductive emitter/source degeneration
simultaneous S11 and noise match
reduces gain, improves IP3

Additional in-band stabilization (output port) as needed
Input tuning for F_{min}
Output match
Out-of-band stabilization

Noise and Available Gain Circles



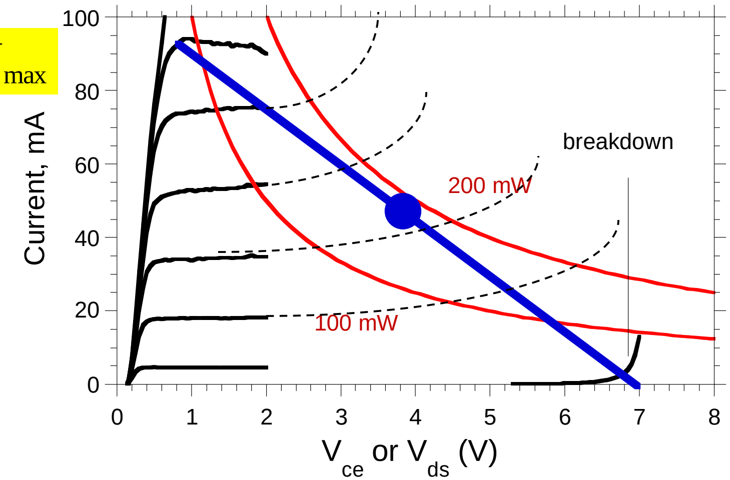


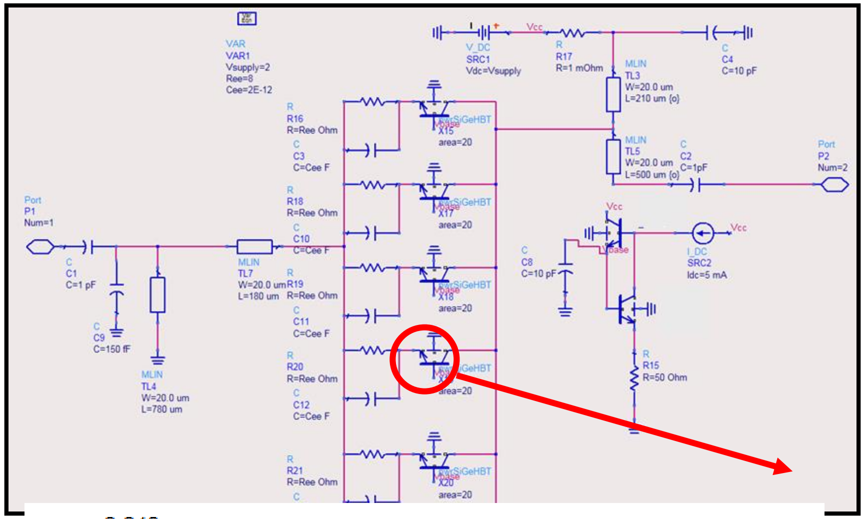


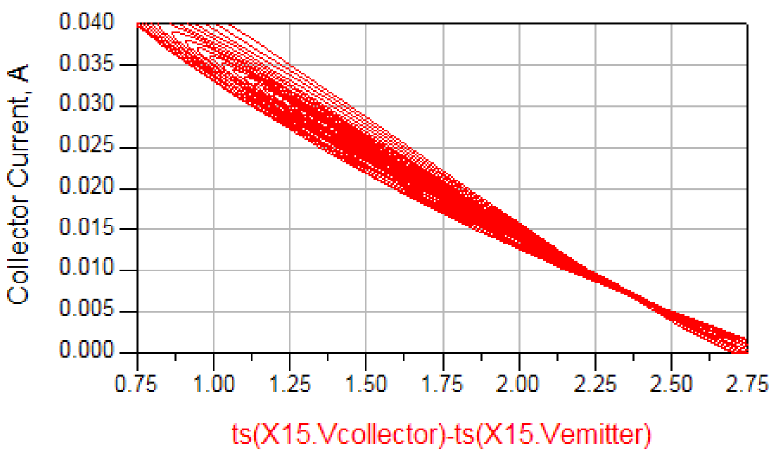
Power Amplifier Design (Cripps method)

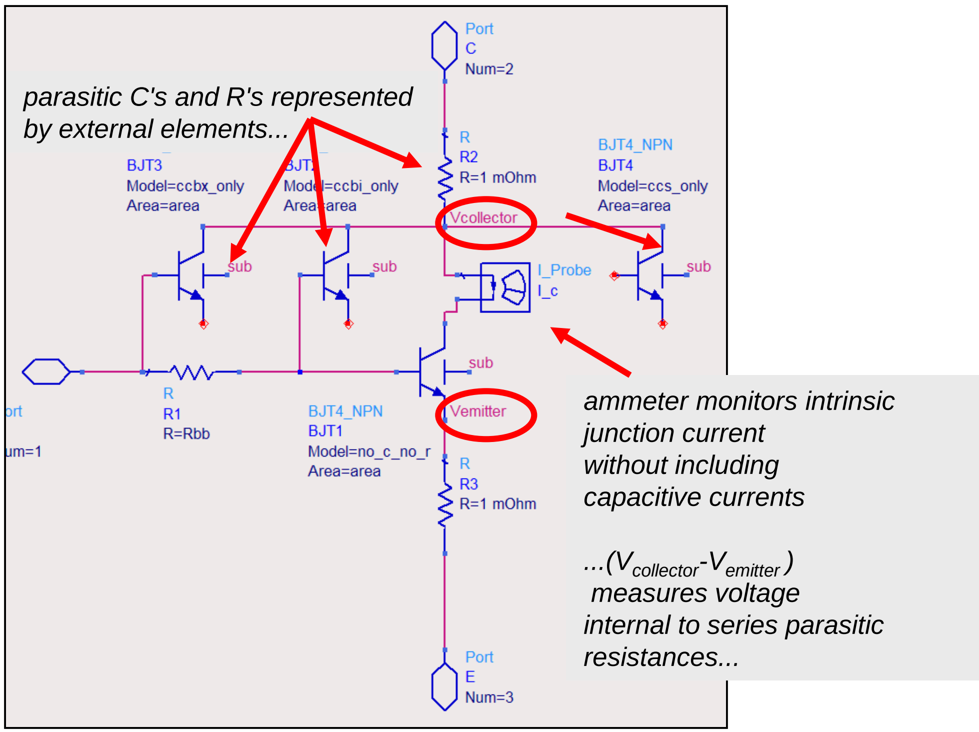
For maximum saturated output power,
& maximum efficiency
device intrinsic output must see
optimum loadline set by:
breakdown, maximum current, maximum power density.

$$P_{max} = (1/8)(V_{max} - V_{min}) I_{max}$$

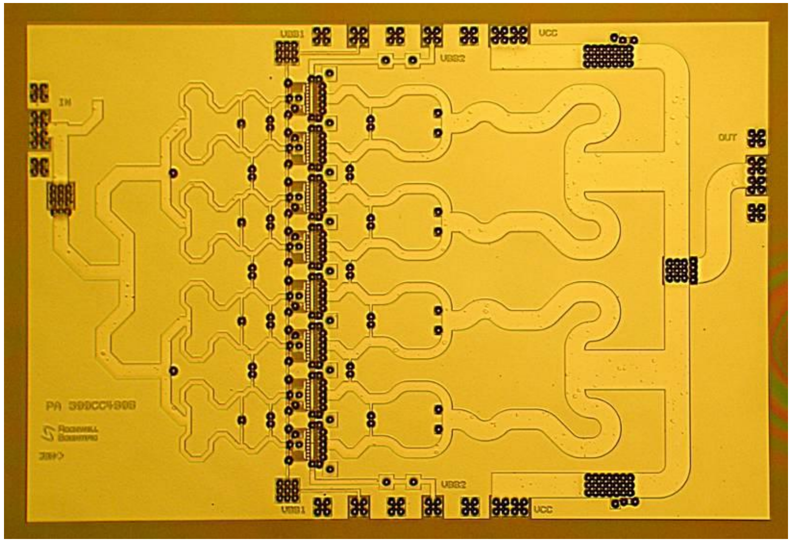




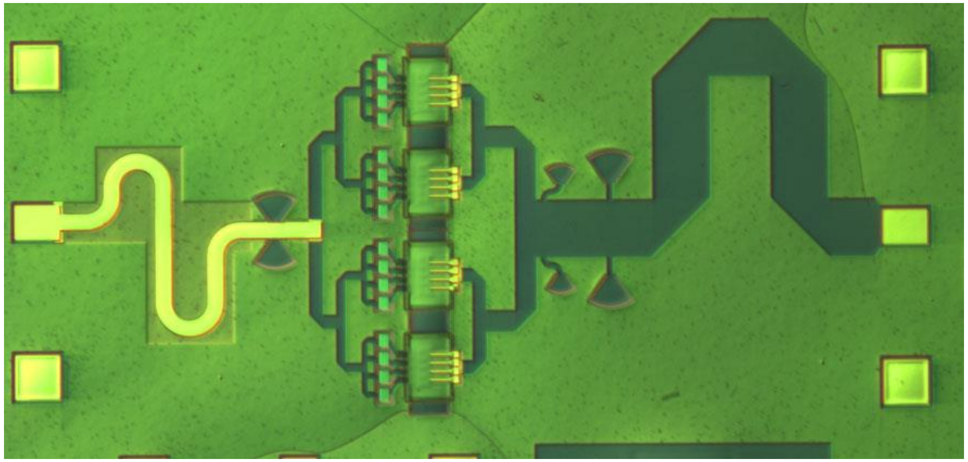




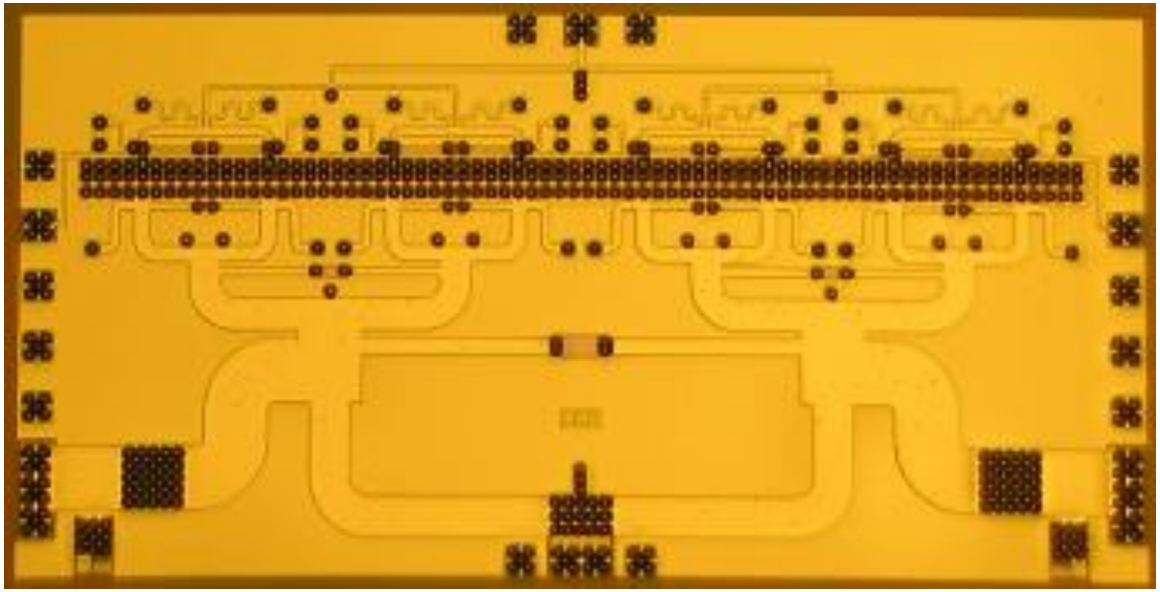
PAs with corporate combining



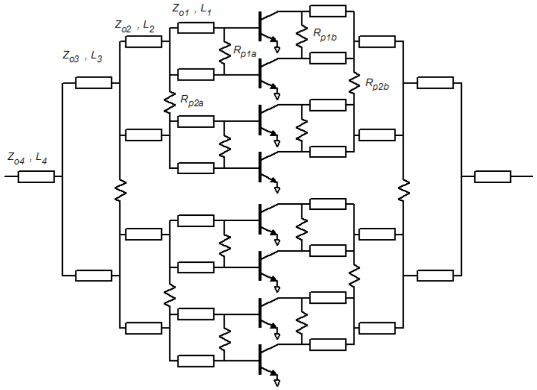
34 GH InP HBT power amplifier - J. Hacker Teledyne



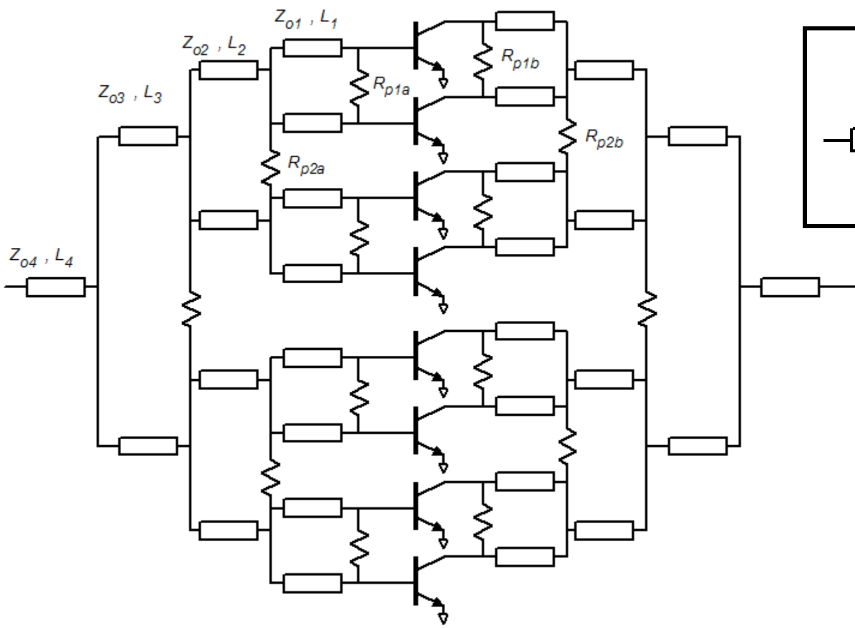
W-band InP HBT power amplifier - UCSB

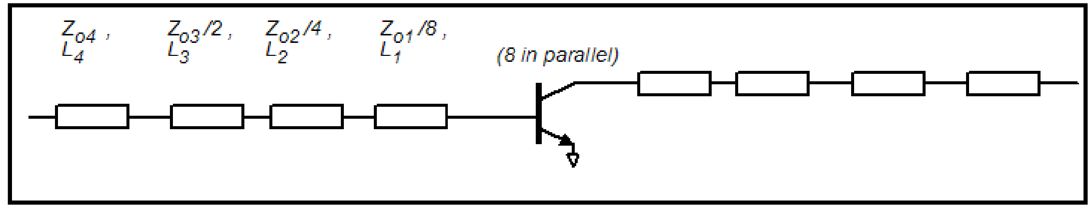


34 GH InP HBT power amplifier - J. Hacker Teledyne



Power amplifier design: combiners





Even-mode equivalent circuit

The equivalent circuit : a multi - section transmission - line transformer.

Shunt elements (inductors, capacitors) can also be added.

Line parameters are adjusted to reach $Z_{l,opt}$ and to match input.

CAD approach :

all similar lines defined by shared variables, simultaneously adjusted

mm-wave
IC Interconnects

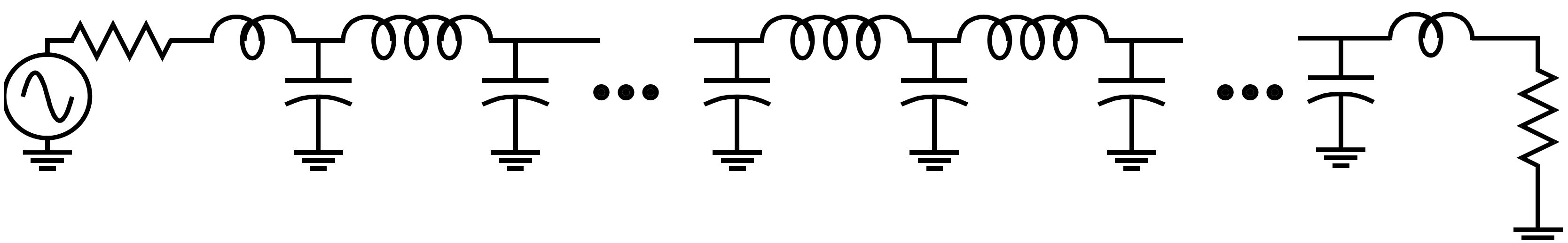
Transmission Lines

A pair of wires with *regular spacing, dielectric loading* along the length.

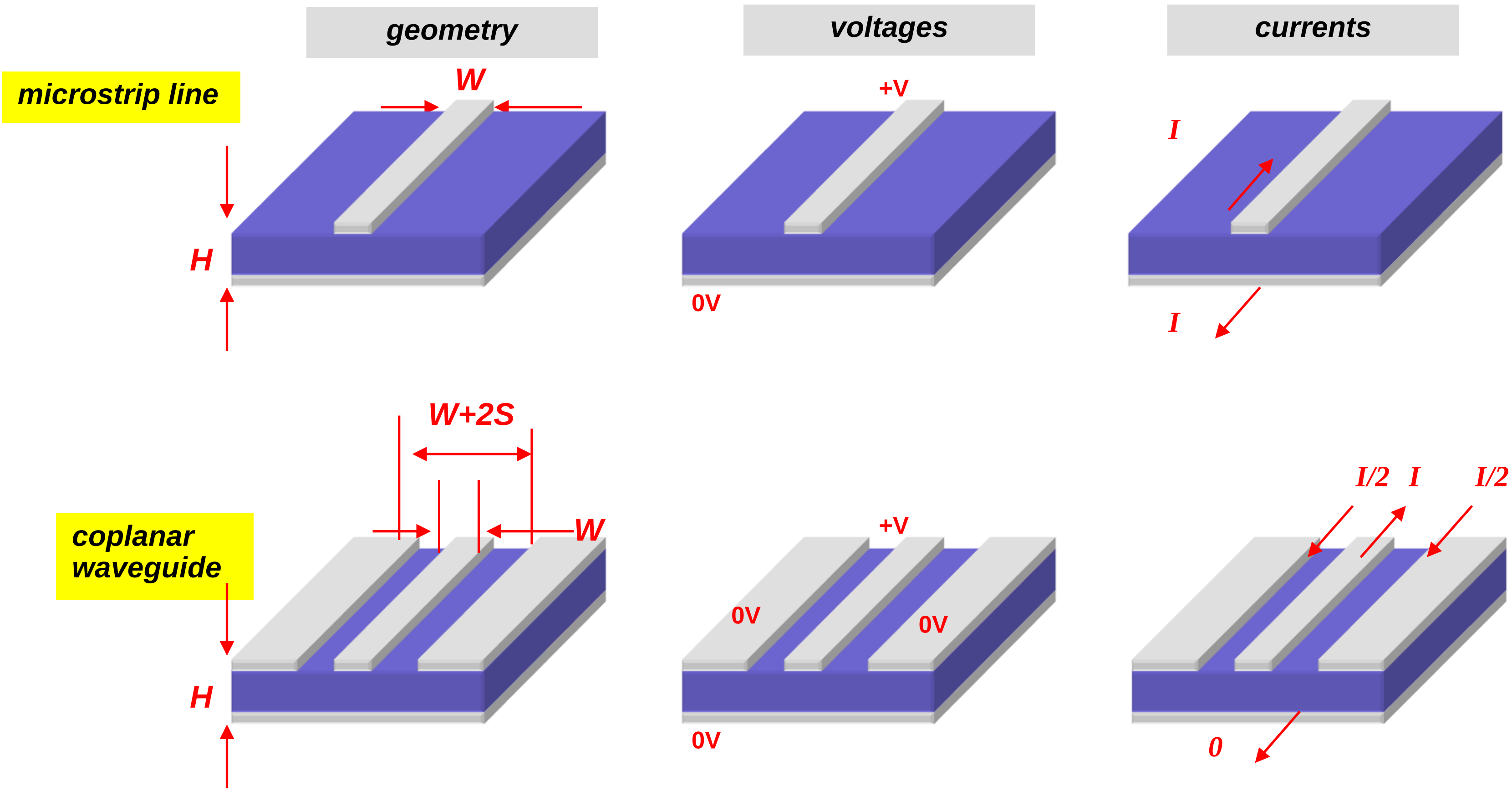
These have inductance per unit length and capacitance per unit length.

Forward and reverse waves propagate.

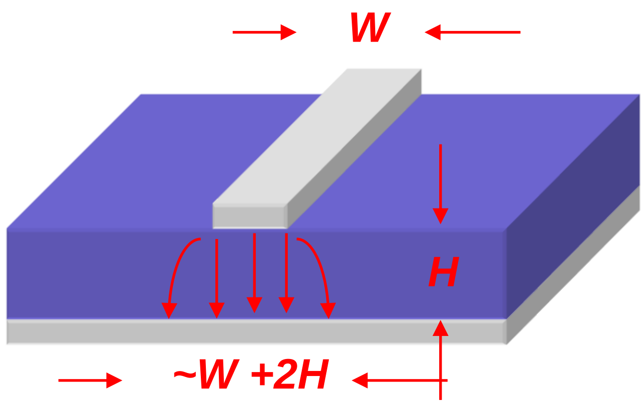
Reflections will occur if lines are not terminated in Z_o



Transmission Lines for On-Wafer Wiring



Skin loss



Skin depth $\delta = \sqrt{2/\omega\mu\sigma}$:

Gold : $\delta \cong 200$ nm @ 100GHz,

640 nm @ 10 GHz

Series resistance per unit length :

$$R_{series}/L \approx \frac{1}{\delta\sigma}\frac{1}{W} + \frac{1}{\delta\sigma}\frac{1}{W+2H}$$

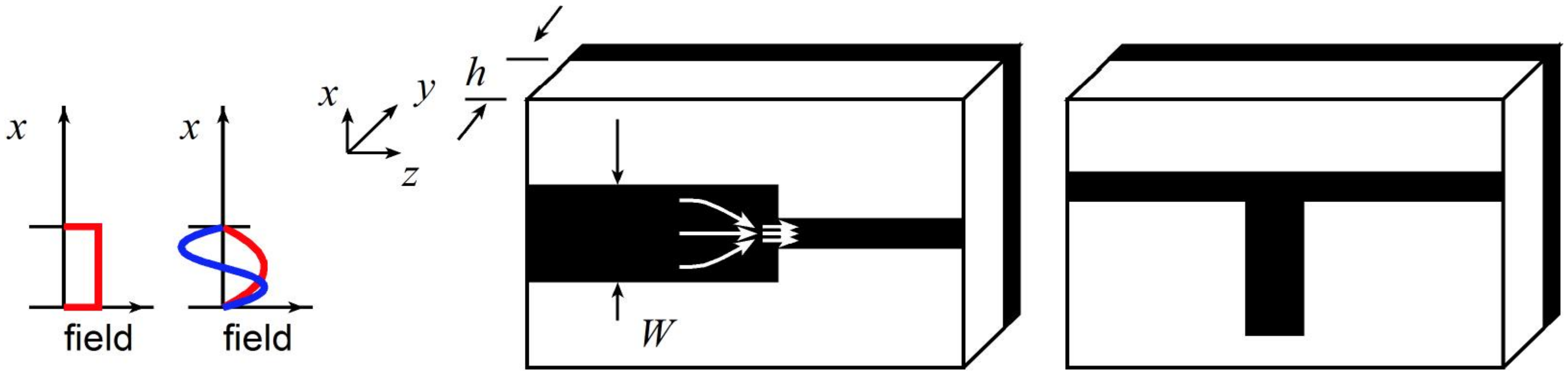
Attenuation per unit distance

$$\alpha \cong \frac{R_{series}/L}{2Z_0} \propto \sqrt{f}$$

Exponential signal decay

$$V(z) = V_o \exp(-\alpha z)\exp(-j2\pi z/\lambda_g)$$

Lateral Modes (1)



In dielectric : waves of form $\vec{E}_0 e^{j\omega t} e^{\pm jk_x x} e^{\pm jk_y y} e^{\pm jk_z z}$

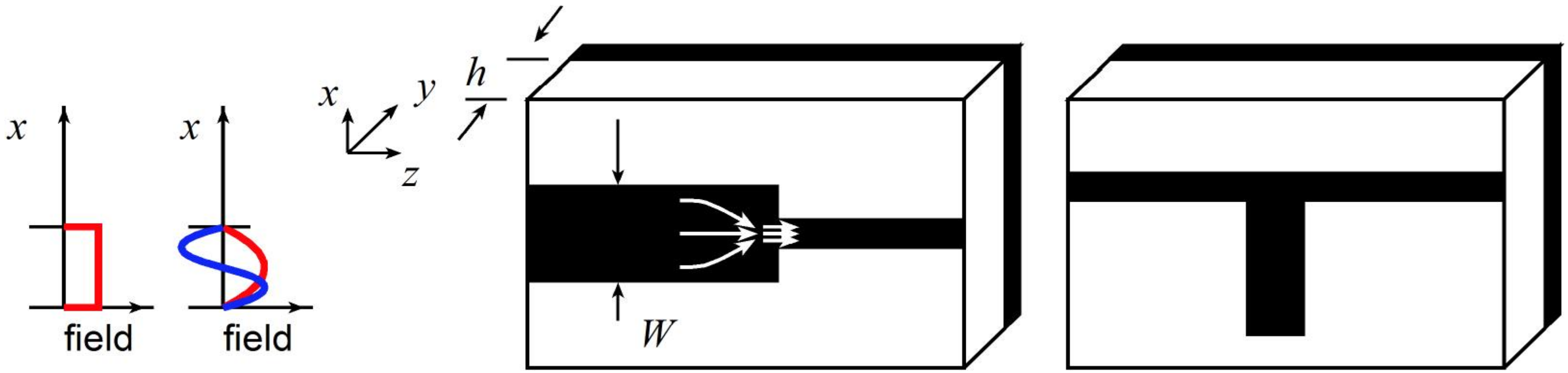
$$k_x^2 + k_y^2 + k_z^2 = k^2 = \varepsilon_r \omega^2 / c^2 = (2\pi/\lambda_d)^2$$

Waves can propagate *laterally* on transmission-line :

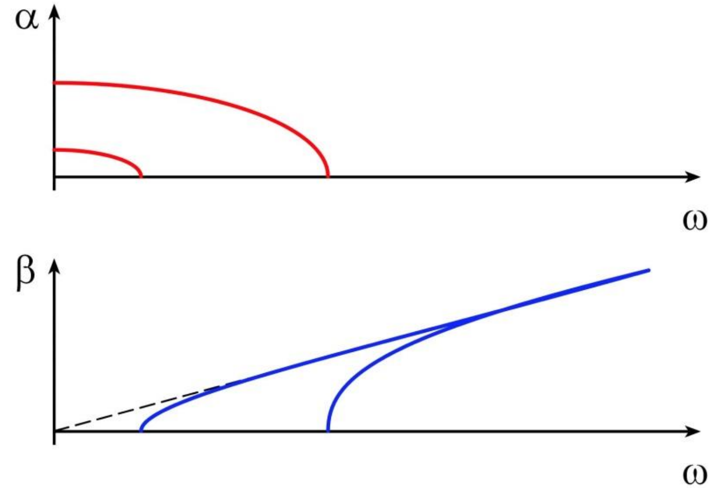
$k_y = 0$ and $k_x = n\pi / W$ for $n = 0, 1, 2, ...$

$$\rightarrow k_z^2 = \varepsilon_r \omega^2 / c^2 - (n\pi / W)^2$$

Lateral Modes (2)



$$k_z^2 = \varepsilon_r \omega^2 / c^2 - (n\pi / W)^2$$



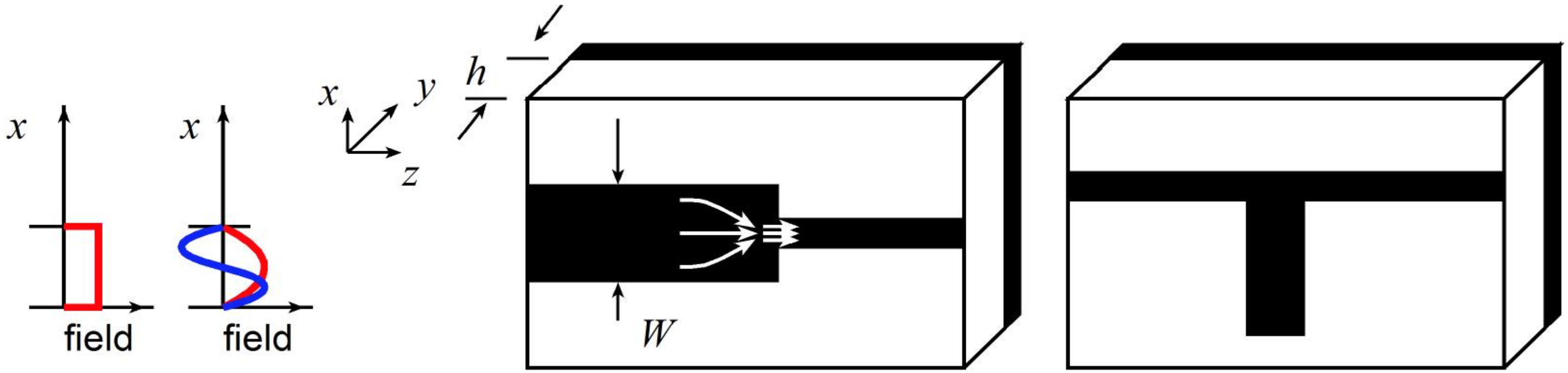
1) Multi-mode propagation if $W > \lambda_d / 2$.

$$\beta_z = \sqrt{\varepsilon_r \omega^2 / c^2 - (n\pi / W)^2}$$

2) Evanescent propagation $e^{-\alpha_z z}$ if $W < \lambda_d / 2$:

$$\alpha_z = \sqrt{(n\pi / W)^2 - \varepsilon_r \omega^2 / c^2}$$

Lateral Modes (3)→ Junction Parasitics



Evanescent propagation $e^{-\alpha_z z}$ if $W \cong \lambda_d/2$:

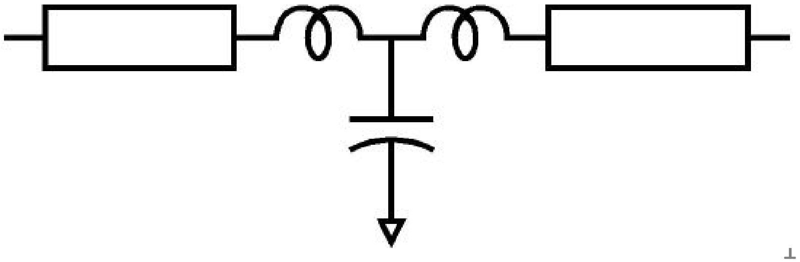
Reactive power in evanescent modes → junction parasitics

ADS library junction models, or electromagnetic simulation.

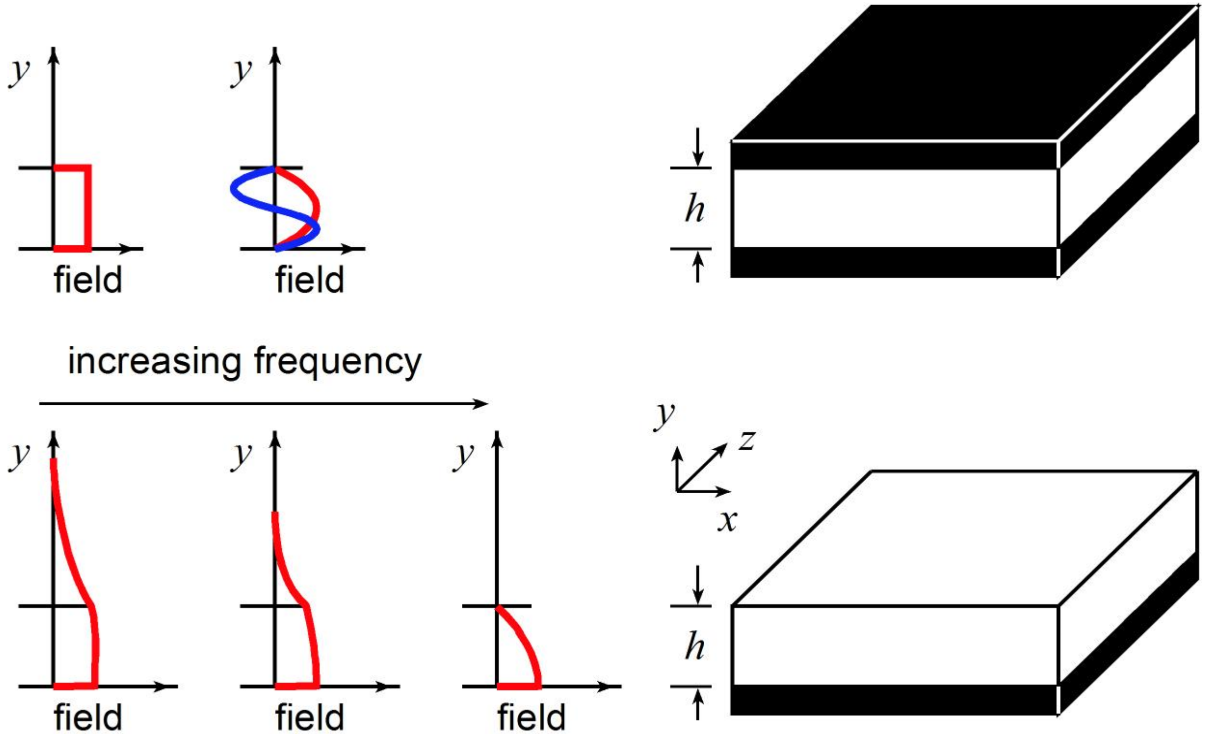
Lessons :

lines must be much narrower than a half-wavelength.

must model junction parasitics



Substrate Modes



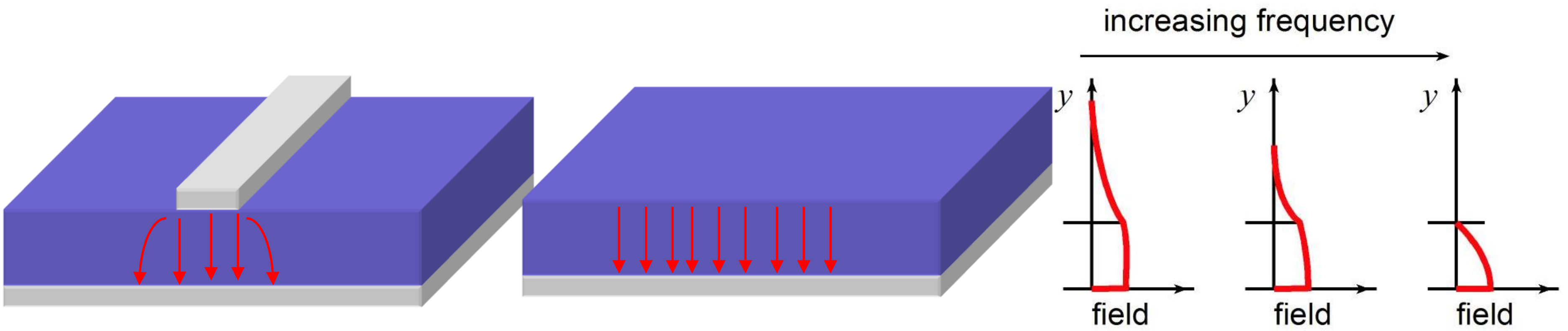
Substrate with top, bottom metal surfaces

$\rightarrow$ modes with $h = \lambda_d/2, \lambda_d, 3\lambda_d/2 \ldots$

Substrate with no top metal $\rightarrow$ tranverse E - mode;

strongly confined as $\lambda_d/4 \rightarrow T$; weakly confined at low frequencie s.

Substrate Mode Coupling: Microstrip

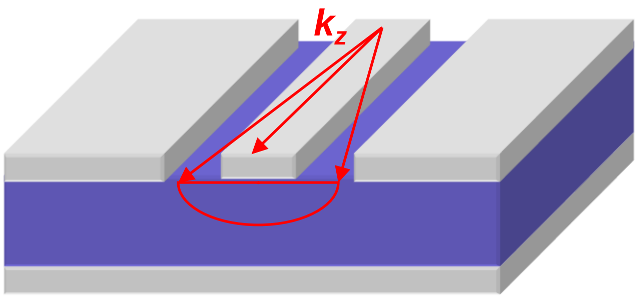


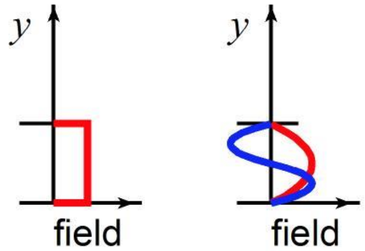
These dielectric slab modes can propage in x and in z.

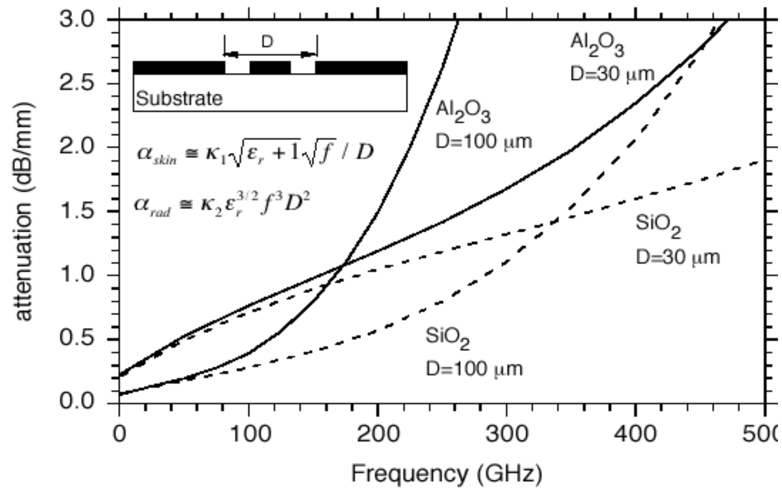
Nonzero mode coupling ("radiation") loss at all frequencies.

Very strong mode coupling when $h \geq \lambda_d / 4$

Substrate Mode Coupling: CPW







Modes couple strongly when $k_{y,\text{CPW}} = k_{y,\text{substrate mode}}$

Given thick substrate, $H >> \lambda_d$:

mode coupling loss, dB/mm $\propto \left(\text{line transverse dimensions}\right)^2 \cdot \text{frequency}^2$

"radiation loss"

Transmission lines: the problem

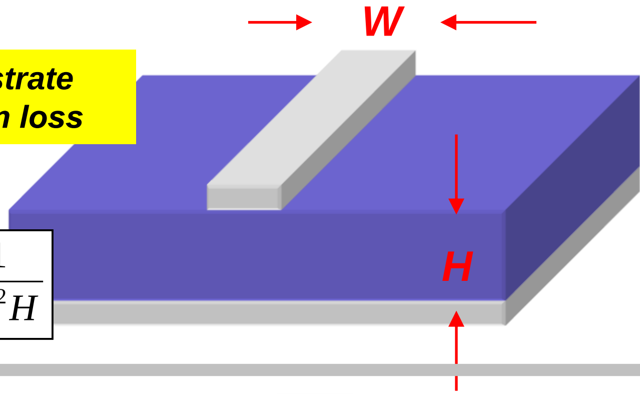
If we use narrow lines and thin substrates
then skin-effect losses will be large.

If we use wide lines and thick substrates
then lateral modes and substrate radiation will be major problems.

III-V MIMIC Interconnects -- Classic Substrate Microstrip

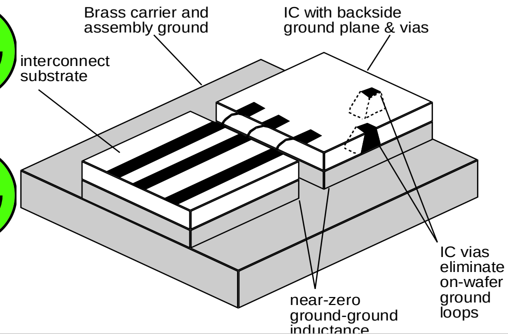
Thick Substrate → low skin loss

$$\alpha_{skin} \propto \frac{1}{\varepsilon_r^{1/2} H}$$

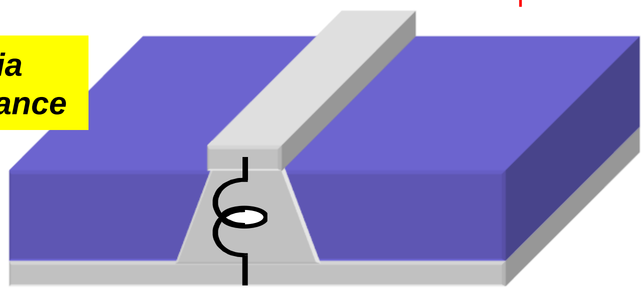


Zero ground inductance in package

No ground plane breaks in IC

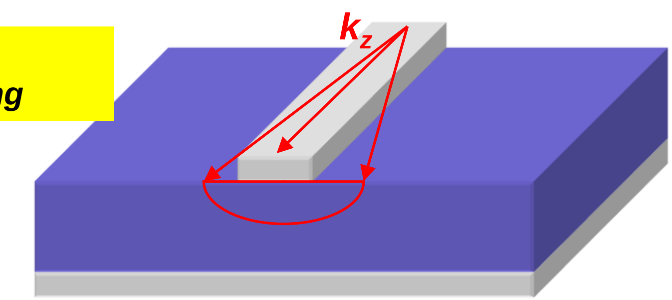


High via inductance



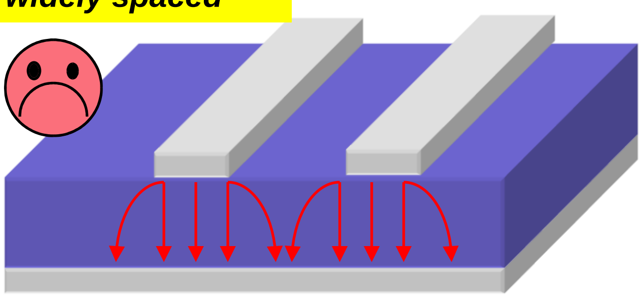
12 pH for 100 μm substrate -- 7.5 Ω @ 100 GHz

TM substrate mode coupling



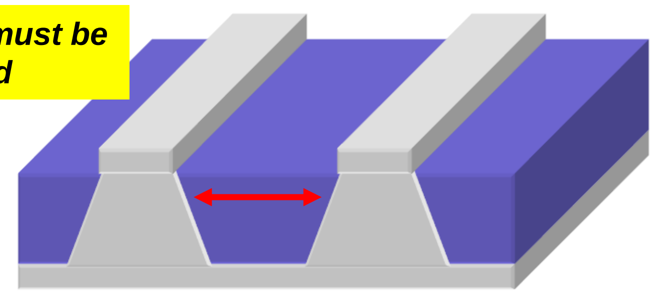
Strong coupling when substrate approaches ~λ_d / 4 thickness

lines must be widely spaced



Line spacings must be ~3(substrate thickness)*

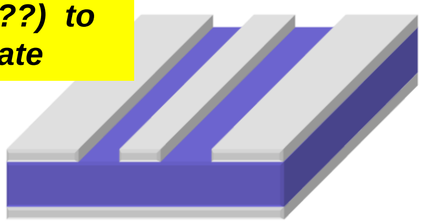
ground vias must be widely spaced



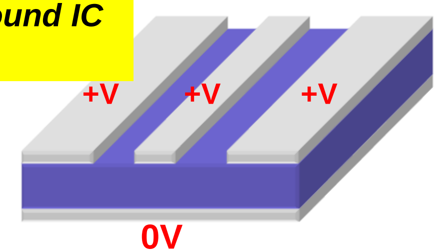
all factors require very thin substrates for >100 GHz ICs
→ lapping to ~50 μm substrate thickness typical for 100+ GHz

Coplanar Waveguide

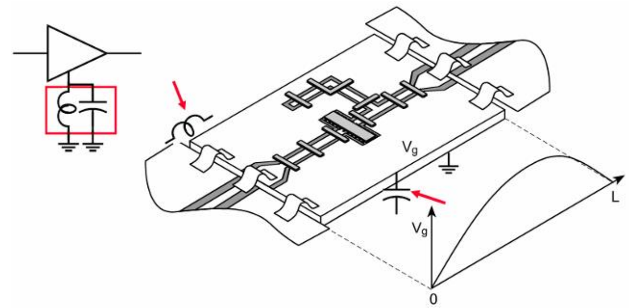
No ground vias
No need (???) to thin substrate



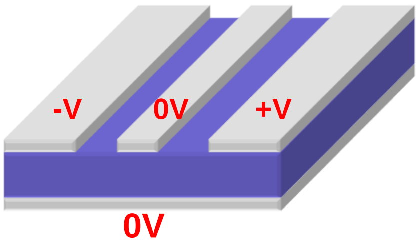
Hard to ground IC to package



Parasitic microstrip mode

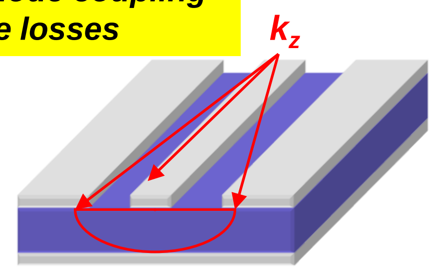


ground plane breaks → loss of ground integrity



Parasitic slot mode

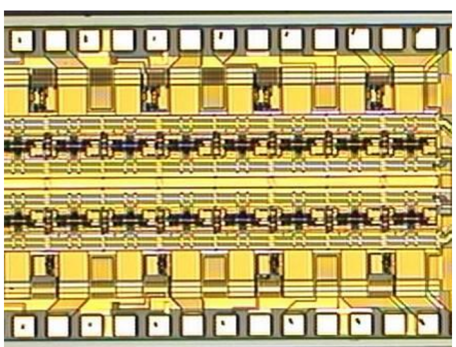
substrate mode coupling or substrate losses



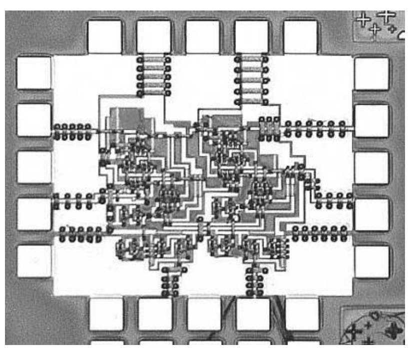
III-V: semi-insulating substrate→ substrate mode coupling

Silicon conducting substrate → substrate conductivity losses

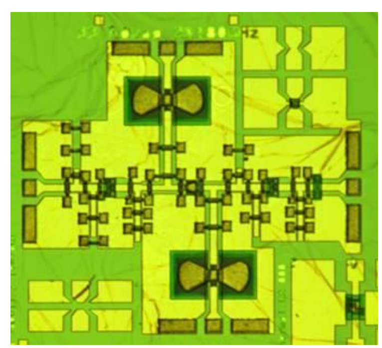
Repairing ground plane with ground straps is effective only in simple ICs
In more complex CPW ICs, ground plane rapidly vanishes
→ common-lead inductance → strong circuit-circuit coupling



40 Gb/s differential TWA modulator driver
note CPW lines, fragmented ground plane



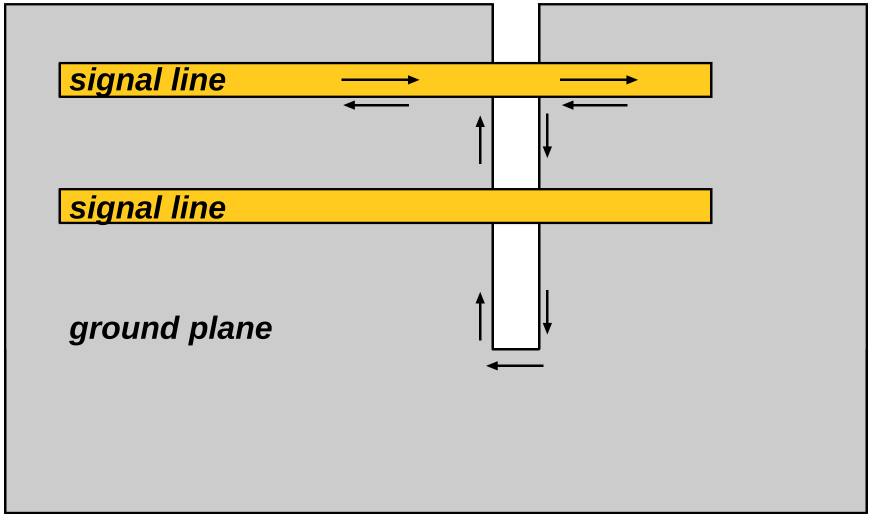
35 GHz master-slave latch in CPW
note fragmented ground plane

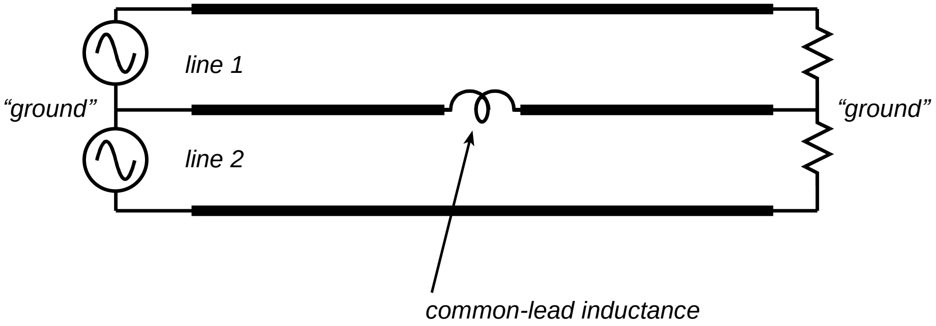


175 GHz tuned amplifier in CPW
note fragmented ground plane

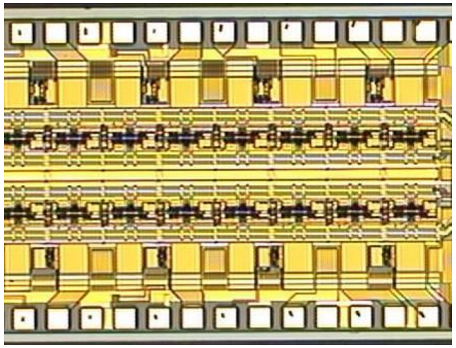
poor ground integrity
↓
loss of impedance control
↓
ground bounce
↓
coupling, EMI, oscillation

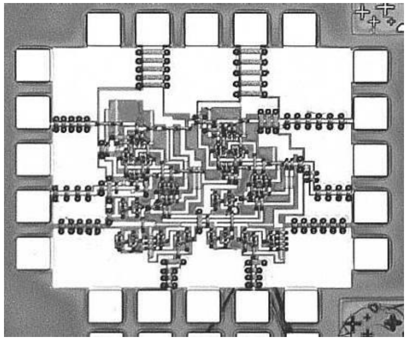
If It Has Breaks, It Is Not A Ground Plane !

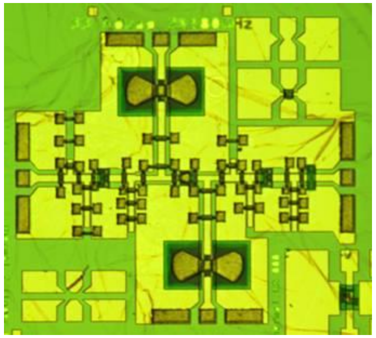




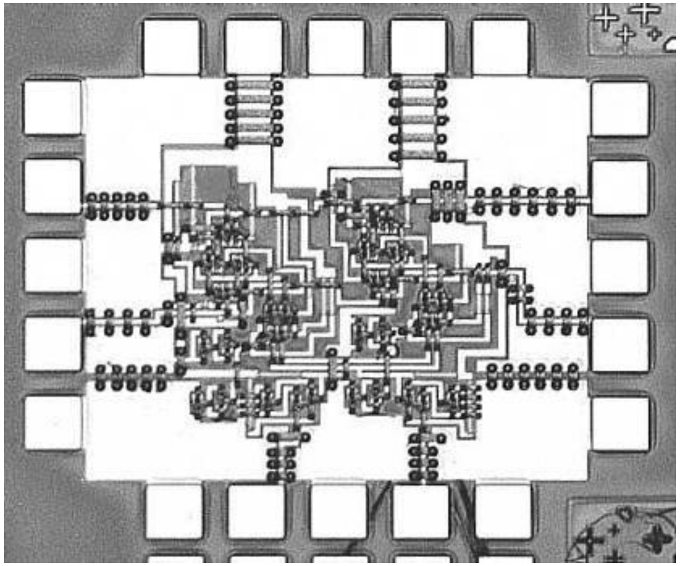
coupling / EMI due to poor ground system integrity is common in high-frequency systems
whether on PC boards
...or on ICs.



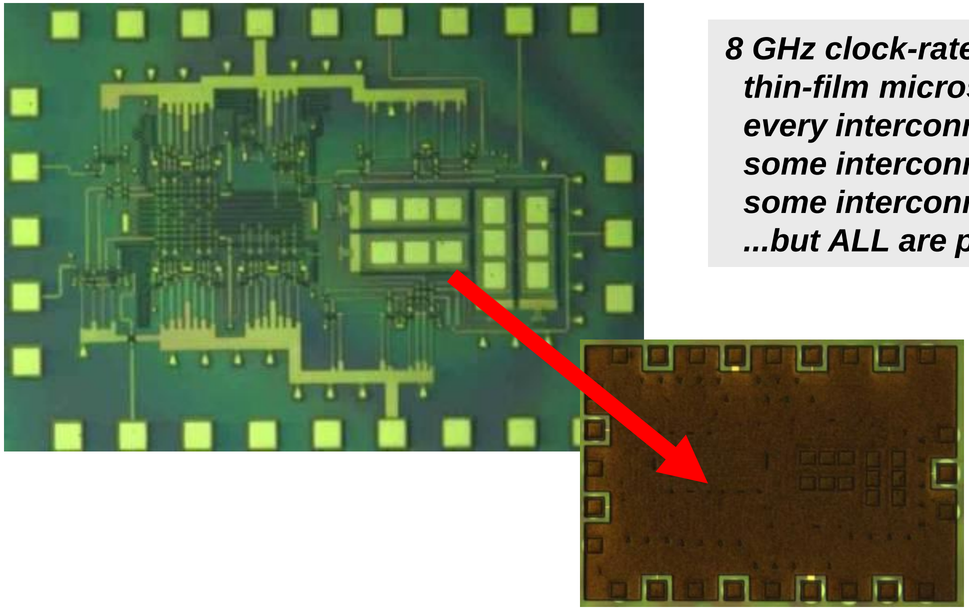




No clean ground return ? → interconnects hard to model



35 GHz static divider
interconnects have no clear local ground return
interconnect inductance is non-local
interconnect inductance has no compact model



8 GHz clock-rate delta-sigma ADC
thin-film microstrip wiring
every interconnect can be modeled as microstrip
some interconnects are terminated in their Zo
some interconnects are not terminated
...but ALL are precisely modeled

InP 8 GHz clock rate delta-sigma ADC

III-V MIMIC Interconnects -- Thin-Film Microstrip

narrow line spacing → IC density

no substrate radiation, no substrate losses

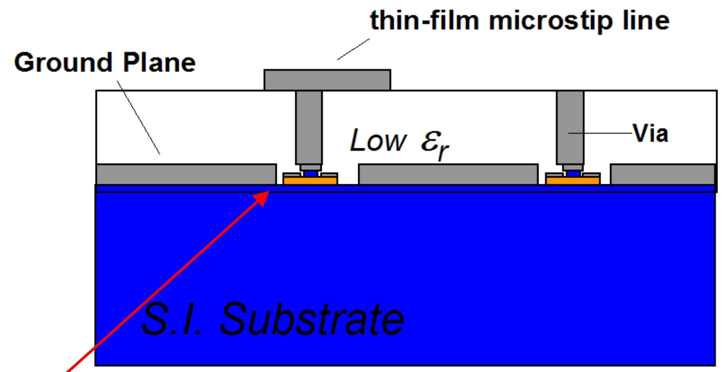
fewer breaks in ground plane than CPW

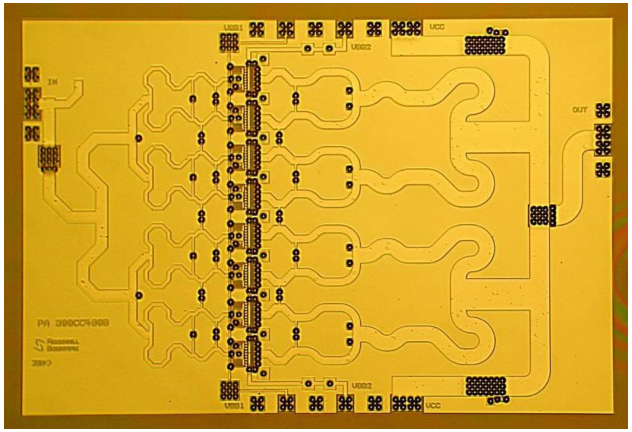
... but ground breaks at device placements

still have problem with package grounding

...need to flip-chip bond

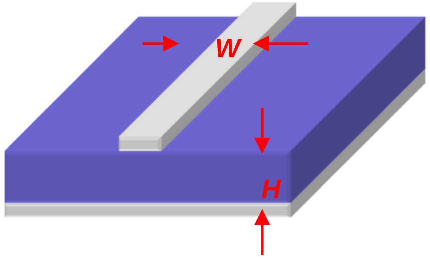
thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines





InP 34 GHz PA
(Jon Hacker , Teledyne)

$$Z_o \sim \frac{\eta_o}{\varepsilon_r^{1/2}}\left(\frac{H}{W+H}\right)$$



III-V MIMIC Interconnects -- Inverted Thin-Film Microstrip

narrow line spacing → IC density

Some substrate radiation / substrate losses

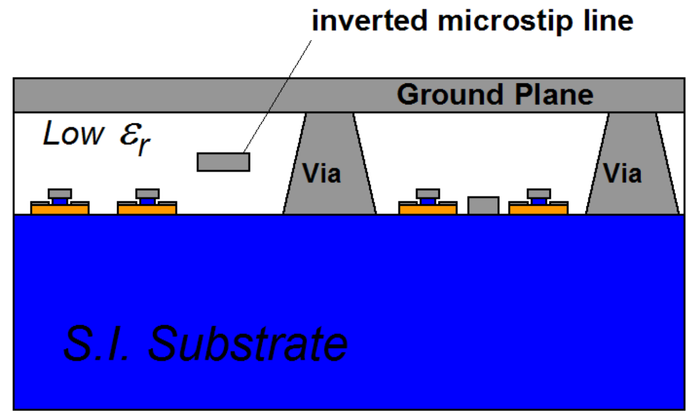
No breaks in ground plane

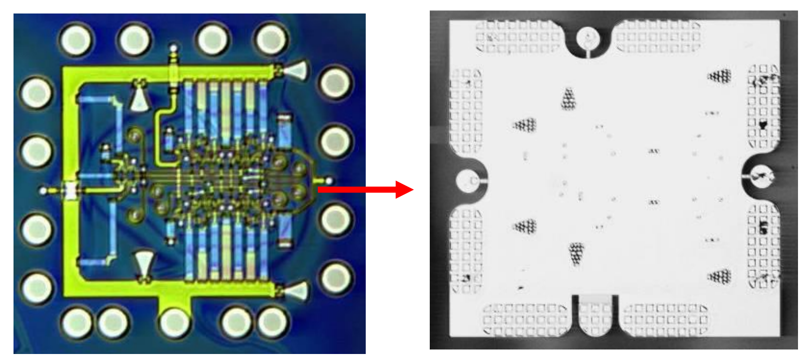
... no ground breaks at device placements

still have problem with package grounding

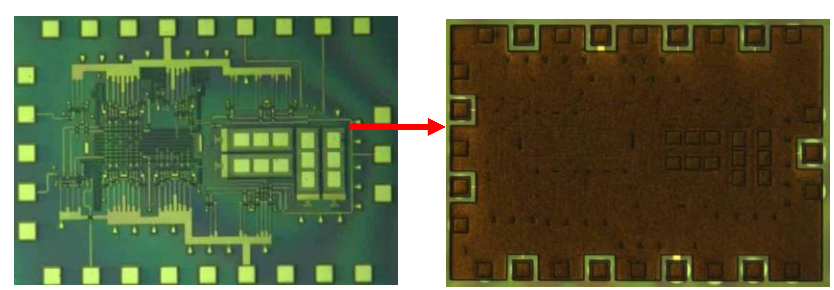
...need to flip-chip bond

thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines





InP 150 GHz master-slave latch



InP 8 GHz clock rate delta-sigma ADC

VLSI mm-wave interconnects with ground integrity

narrow line spacing → IC density 🙂

no substrate radiation, no substrate losses 🙂

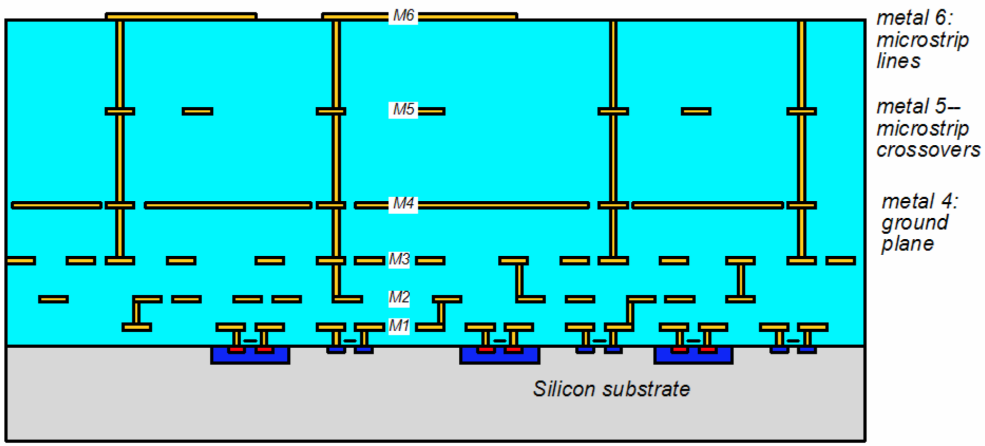
negligible breaks in ground plane 🙂

negligible ground breaks @ device placements 🙂

still have problem with package grounding 🙁

...need to flip-chip bond

thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines 🙁



Also:
Ground plane at *intermediate level* permits critical signal paths to cross supply lines, or other interconnects without coupling.
(critical signal line is placed above ground, other lines and supplies are placed below ground)

Modeling Interconnects, Passives in Tuned IC's

Interconnects are tuning elements

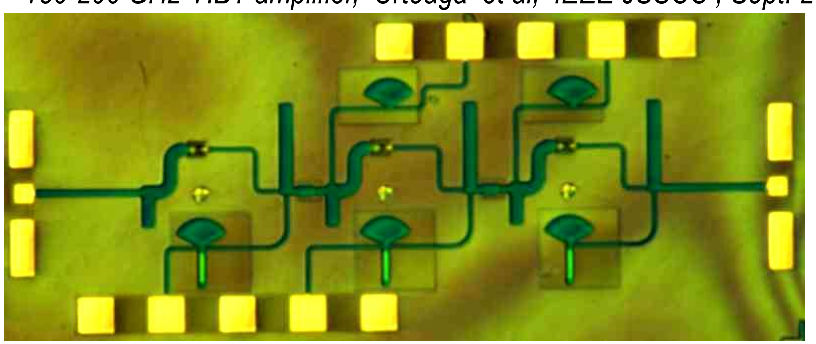
Narrow bandwidths→ precision is critical

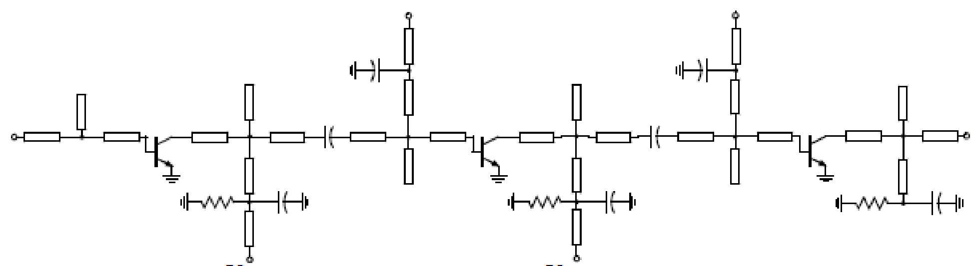
Initial IC simulation uses CAD-systems' library of passive element models.

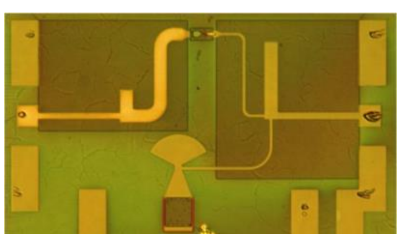
Second design cycle: 2.5-Dimensional electromagnetic simulation of:
lines, junctions, stubs, capacitors, resistors, pads.

Third design cycle: 2.5-D simulation of entire IC wiring (if possible);
otherwise, of large blocks (gain stages)

150-200 GHz HBT amplifier, Urteaga et al, IEEE JSSCC , Sept. 2003

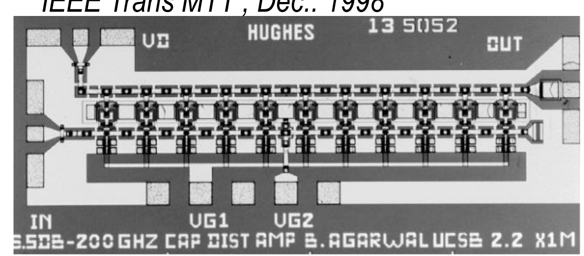




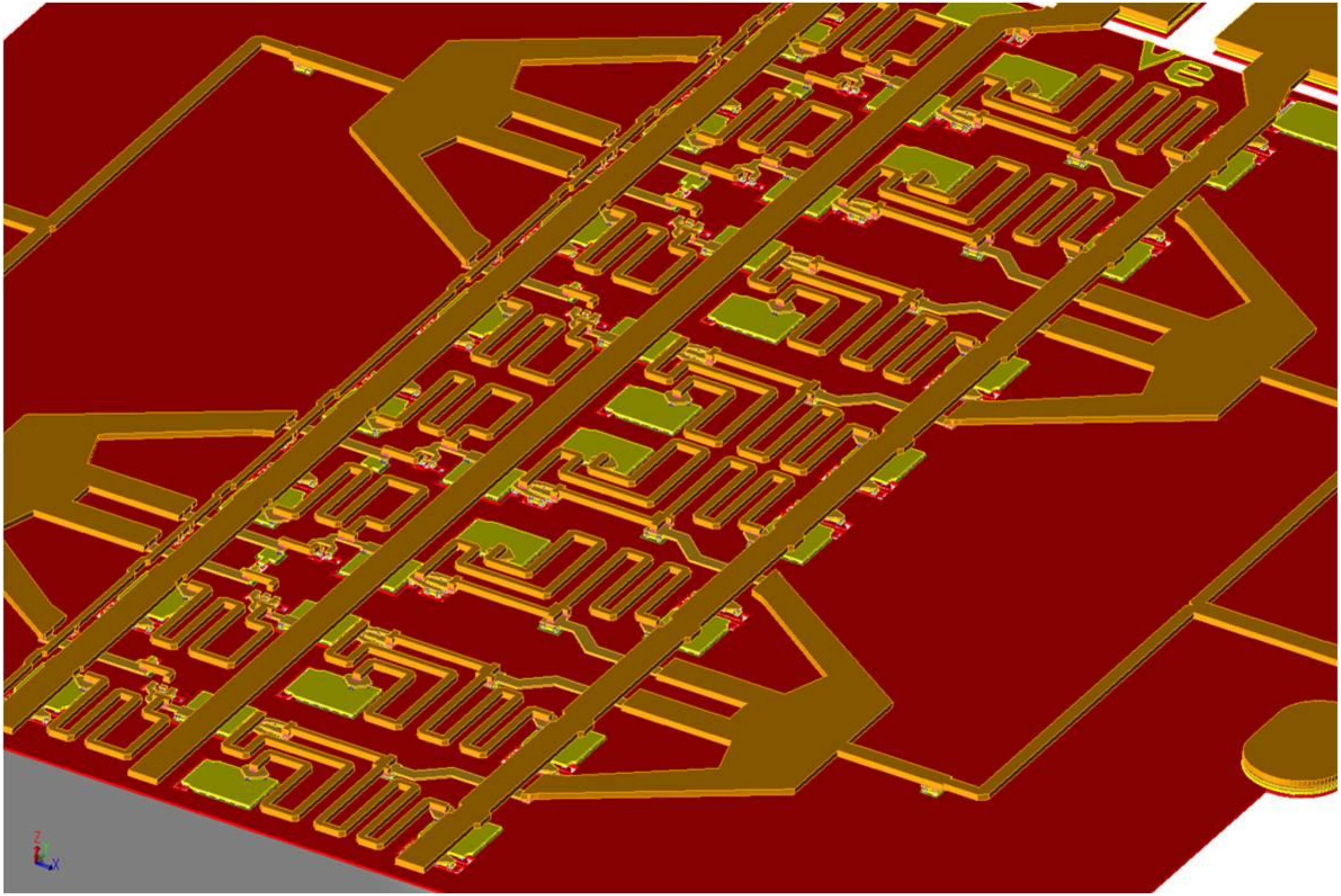


185GHz HBT amplifier, Urteaga et al,
IEEE IMS, May. 2001

1-180GHz HBT amplifier, Agarwal et al,
IEEE Trans MTT , Dec.. 1998

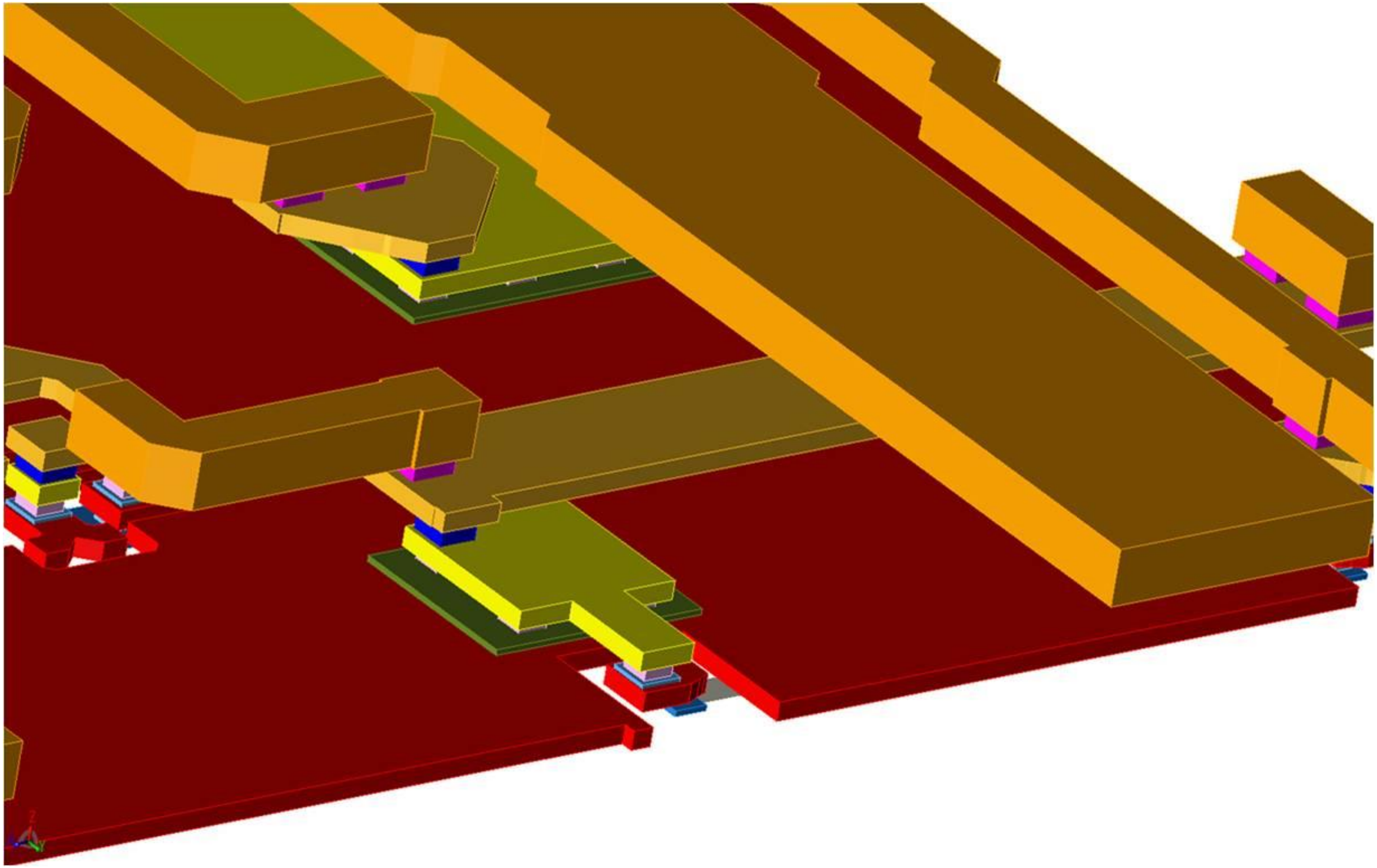


ICs in Thin-Film (Not Inverted) Microstrip



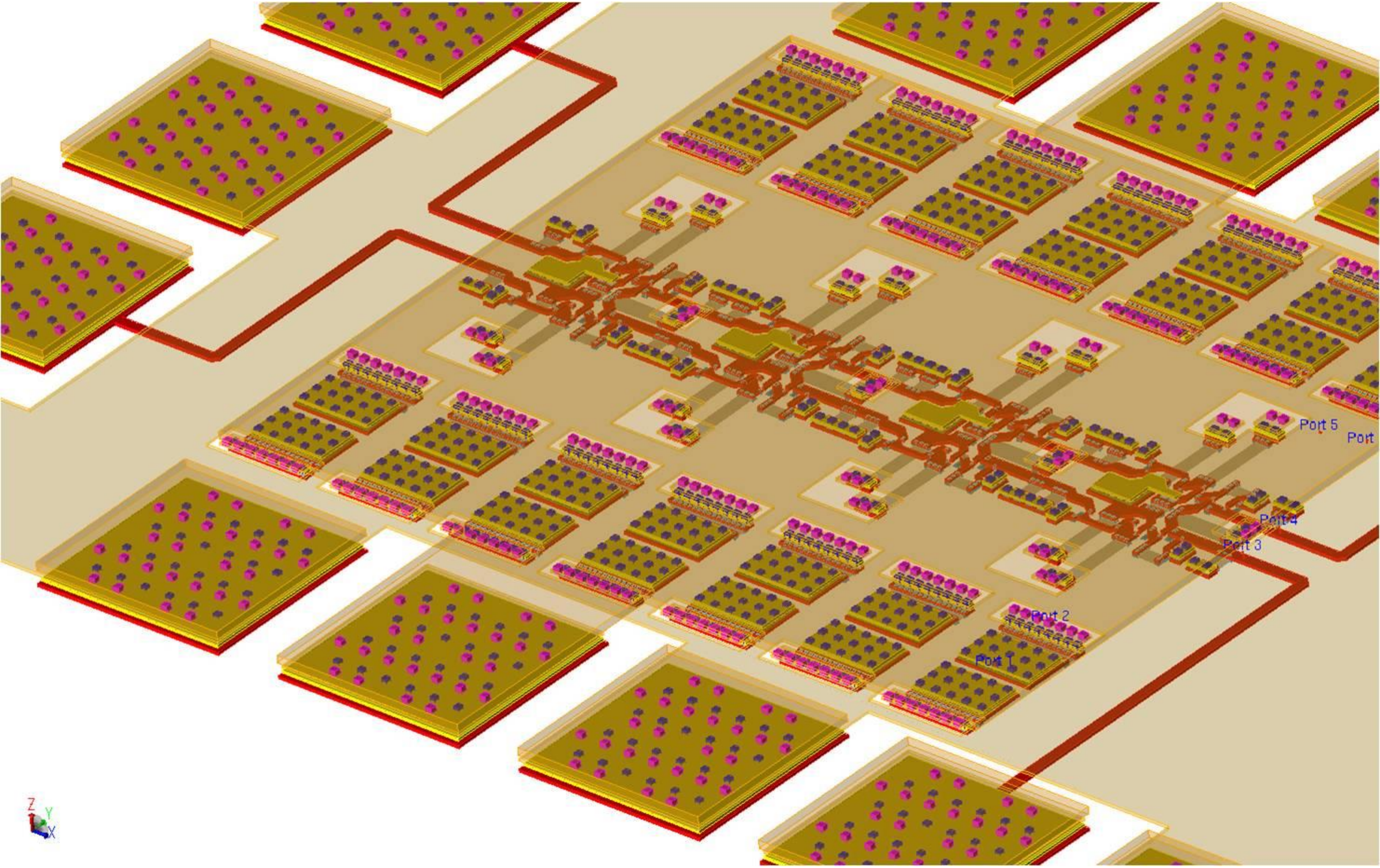
Note breaks in ground plane at transistors, resistors, capacitors

ICs in Thin-Film (Not Inverted) Microstrip



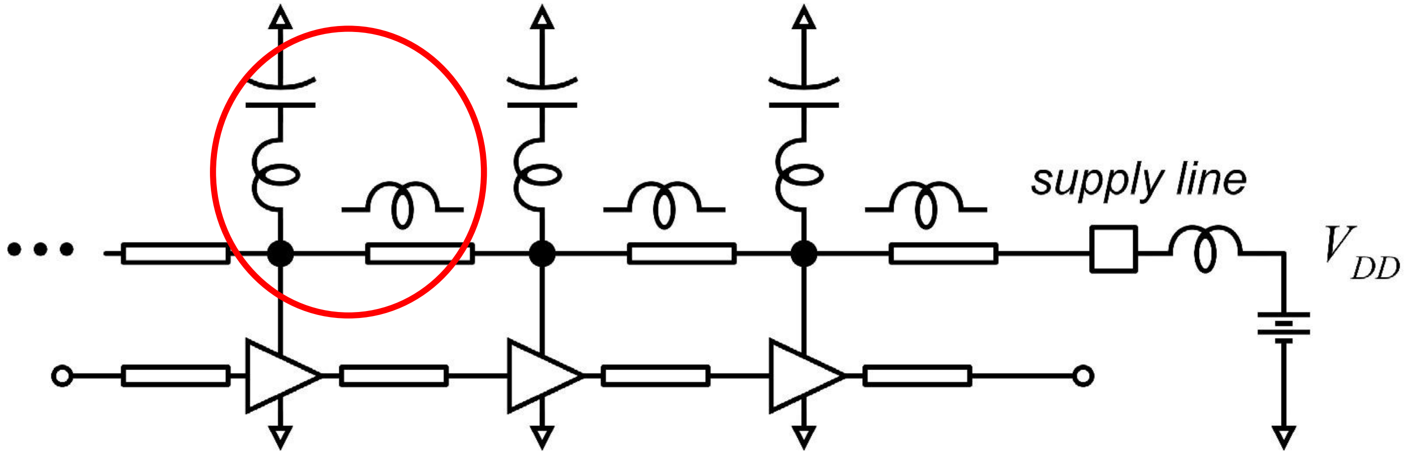
Note breaks in ground plane at transistors, resistors, capacitors

ICs in Thin-Film Inverted Microstrip



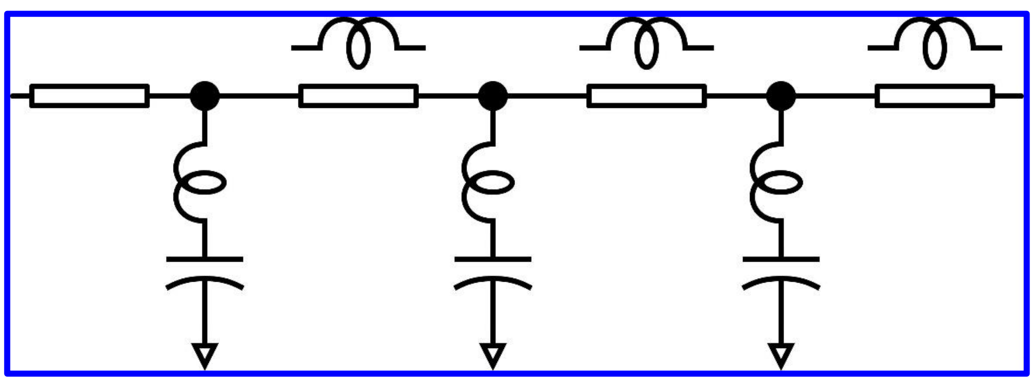
100 GHz differential TASTIS Amp. 512nm InP HBT

Power supply problems



local resonances between bypass cap and supply interconnects

global LC standing-wave resonances on supply bus

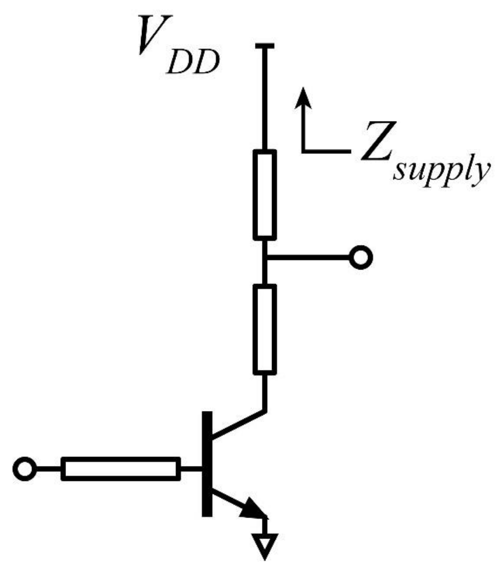


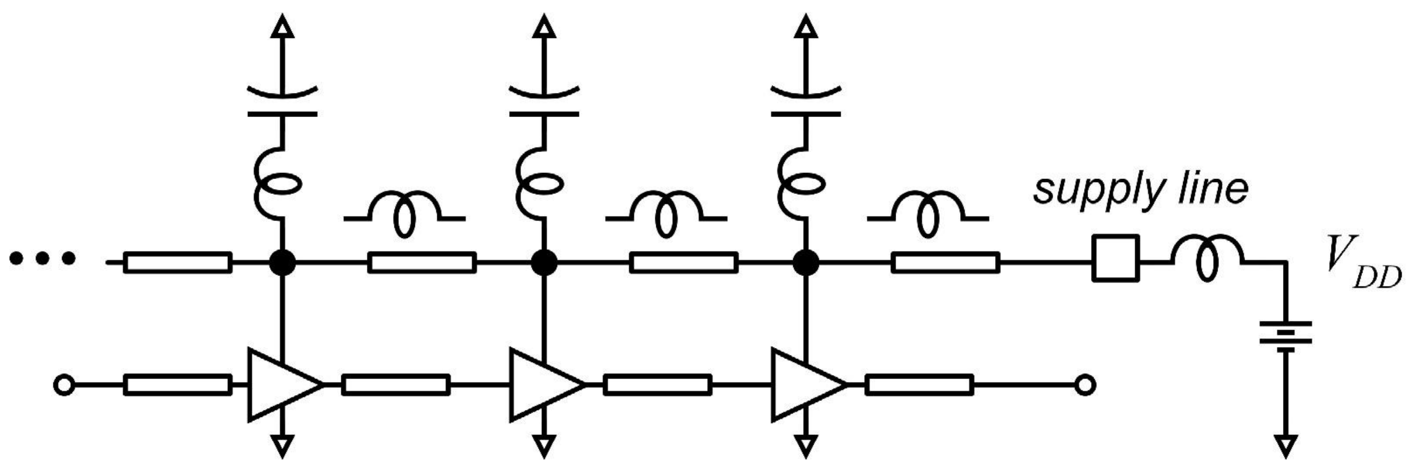
Detuning of individual stages

Coupling, feedback via supply→ oscillation, loss of path isolation

Power supply problems

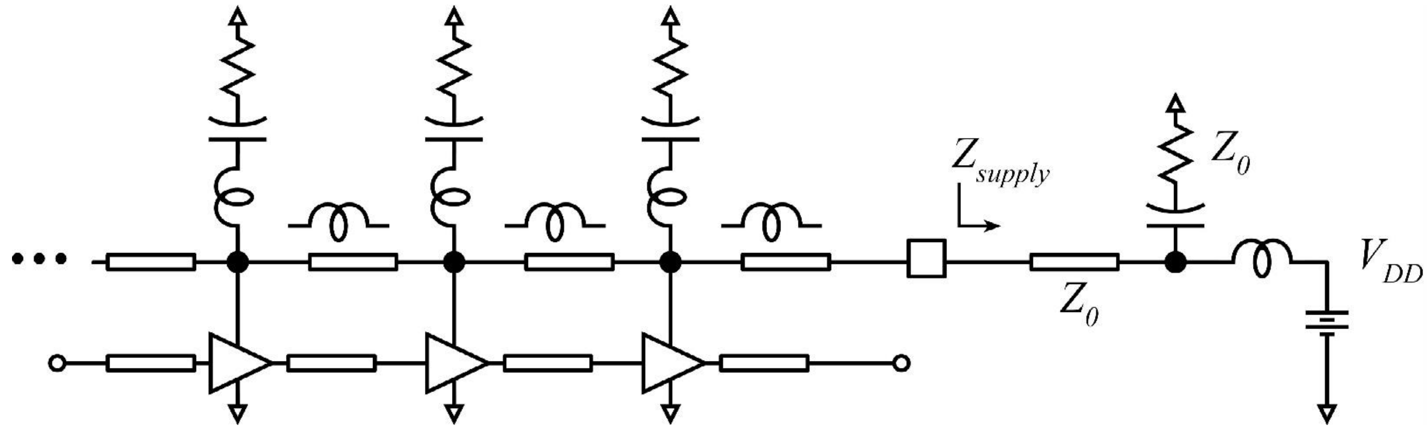
The supply impedance will detune individual stages.





Power supply problems

Model the supply in all simulations.
"If it is on the {IC, PCB, probe station}, put it in the simulation."

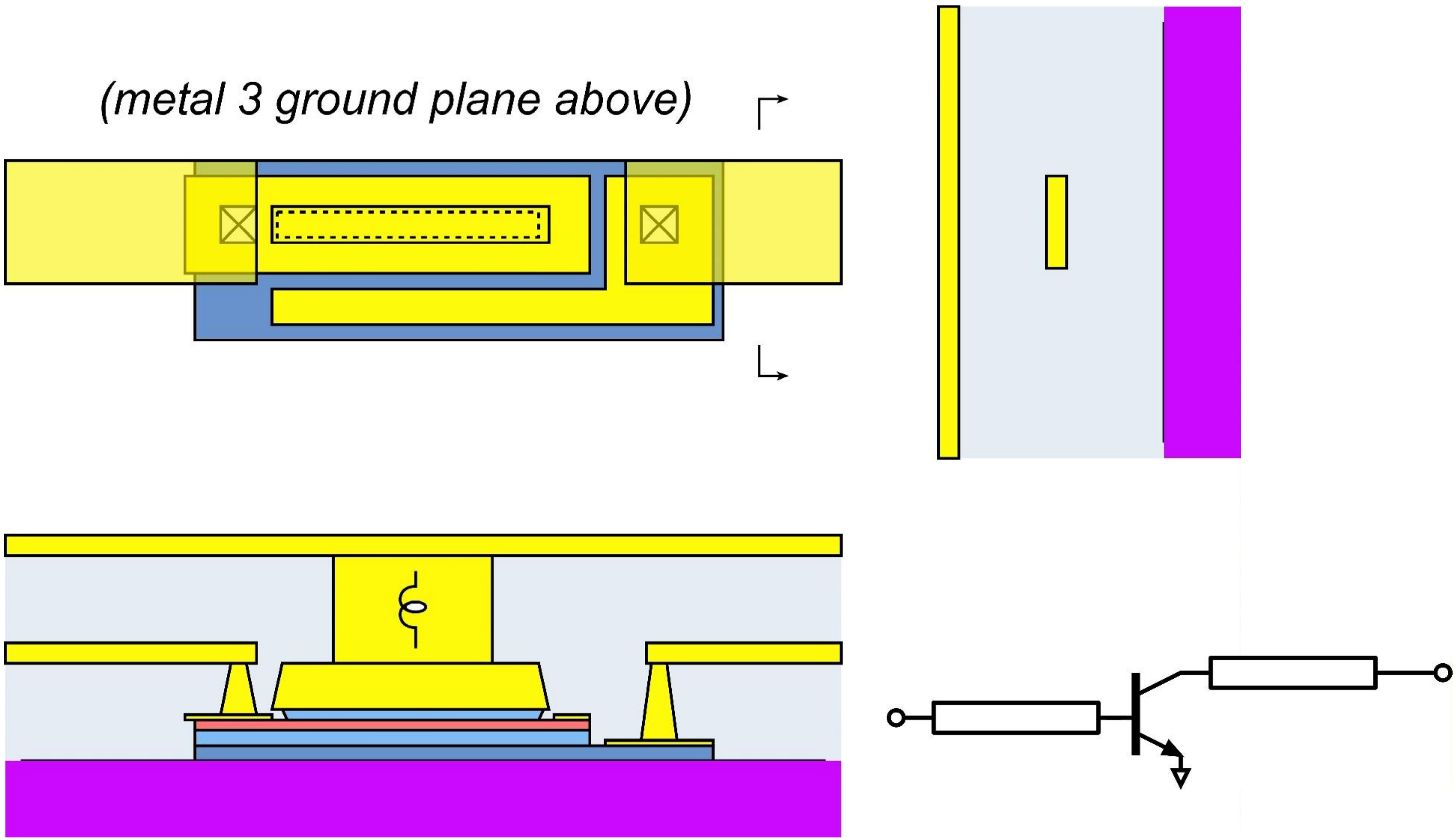


Here, the supply is terminated by 50 Ohms through a bias T.
This avoids resonances.

More generally, we must simulate system
for wide range of external supply impedance.

Transmission-lines in 500+ GHz ICs

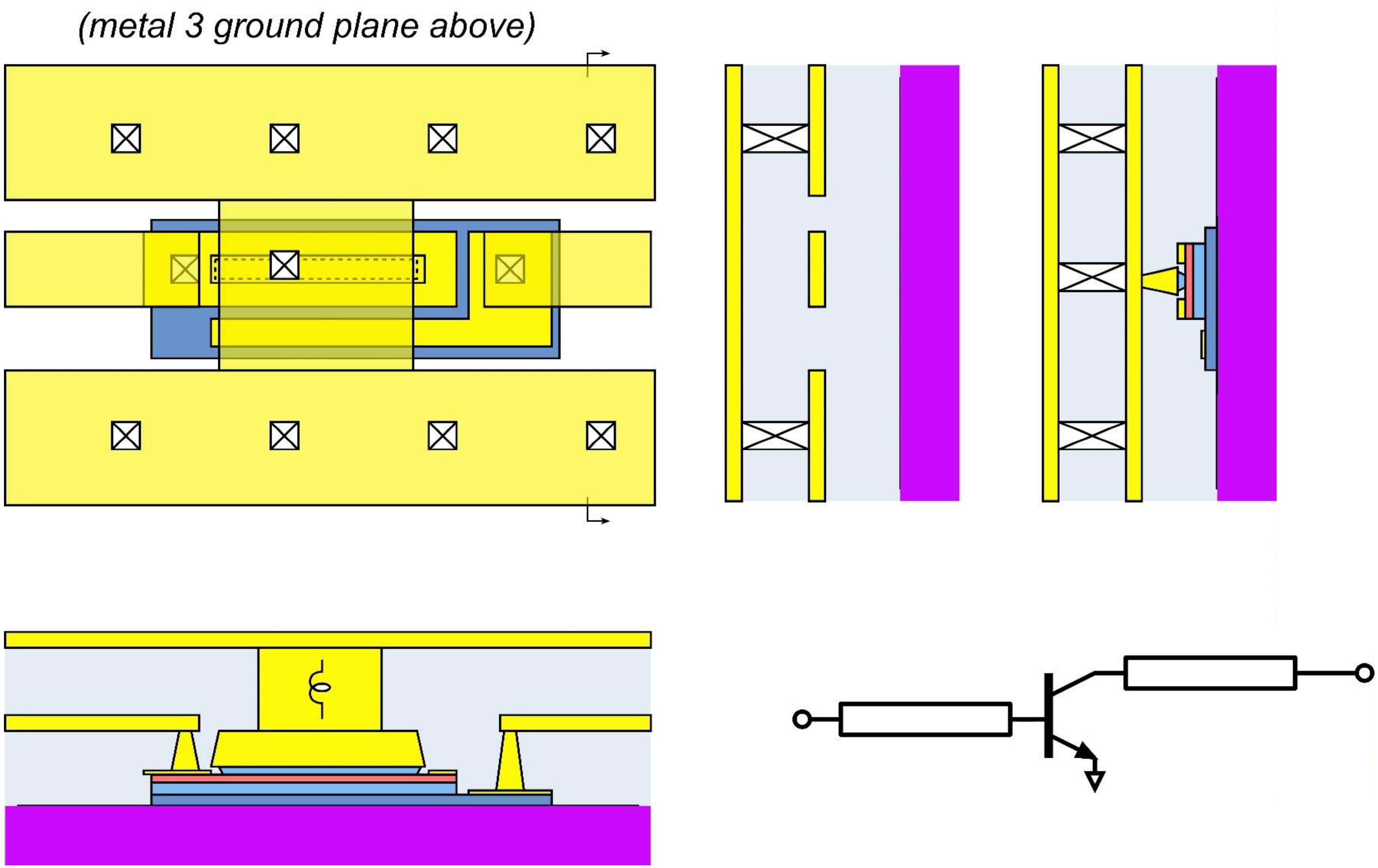
Inverted microstrip: the problem is ground via inductance



Transmission-lines in 500+ GHz ICs

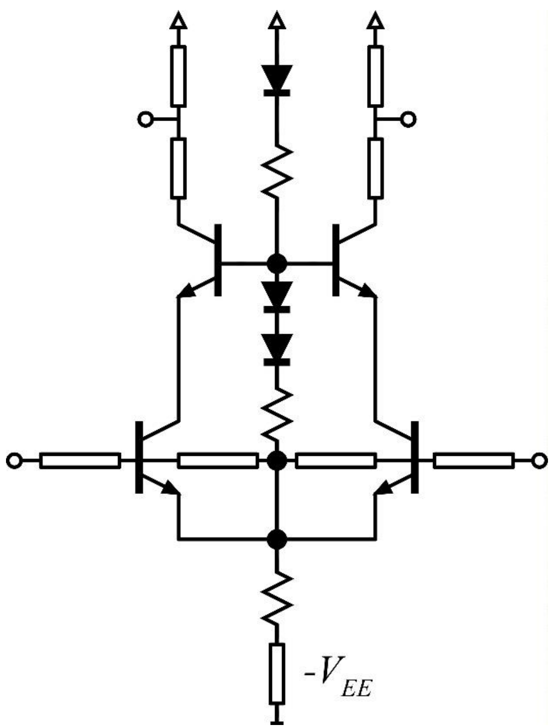
Grounded CPW: lower ground inductance,
metal 3 ground plane suppresses ground bounce

J. Hacker , Teledyne IMS 2013

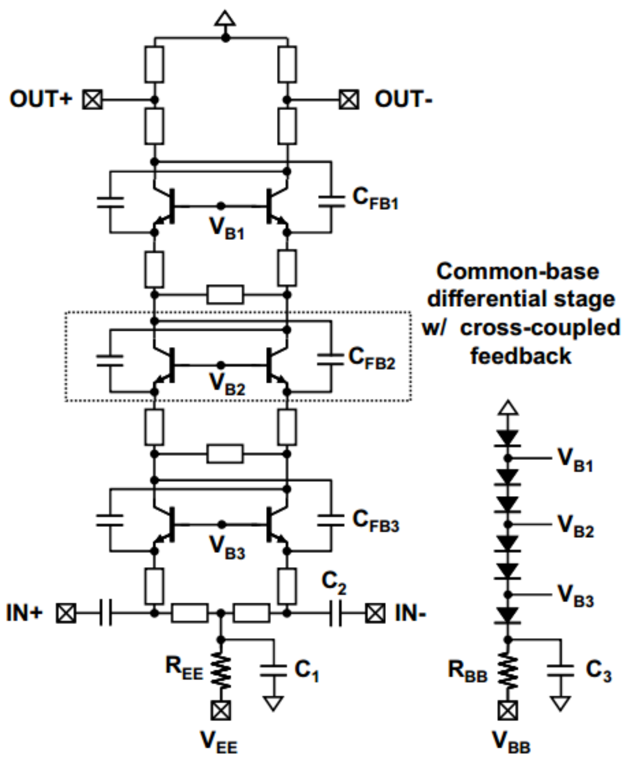


Differential mm-wave stages

Common-emitter
M. Seo, Teledyne

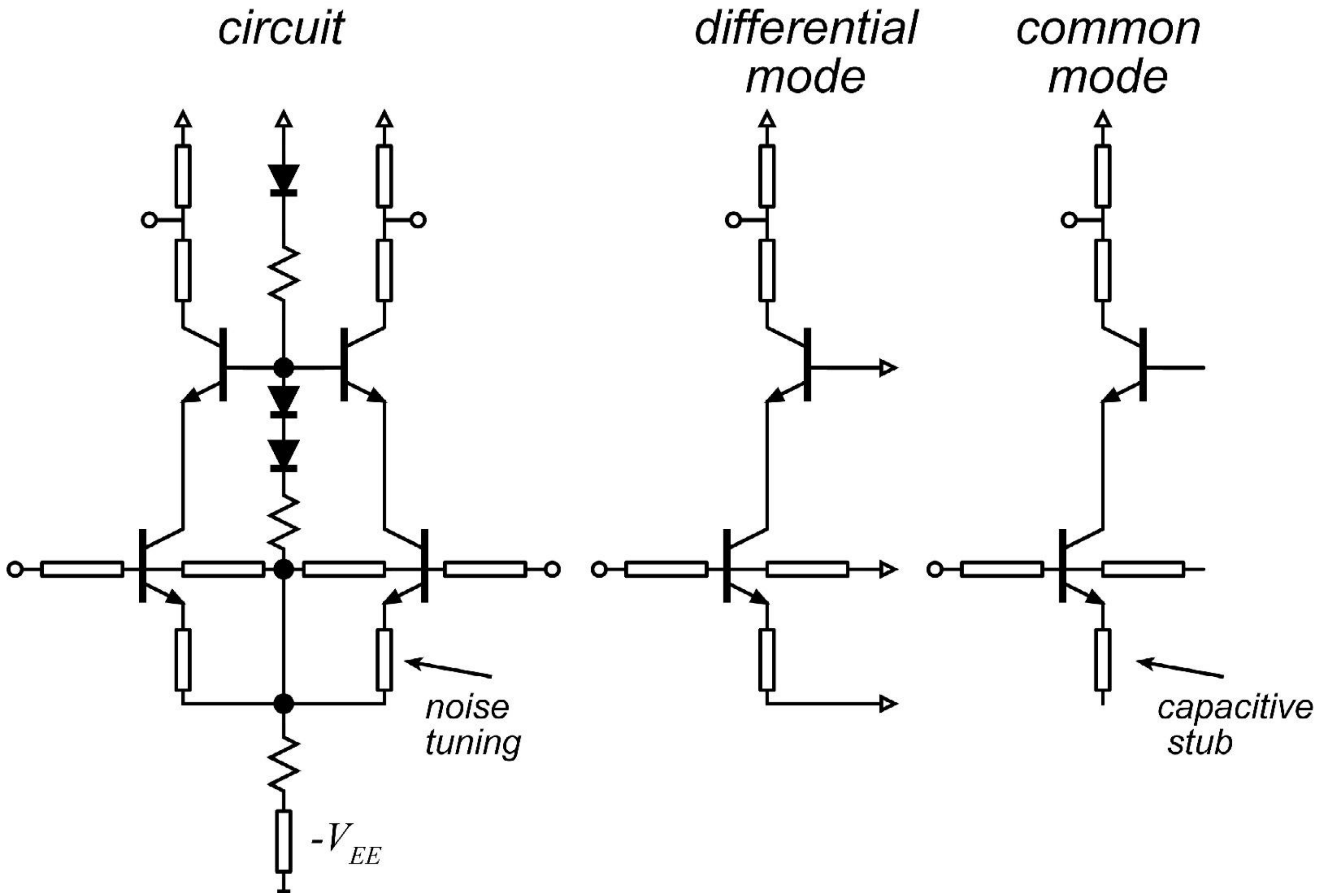


Common-base
M. Seo, 2013 IMS



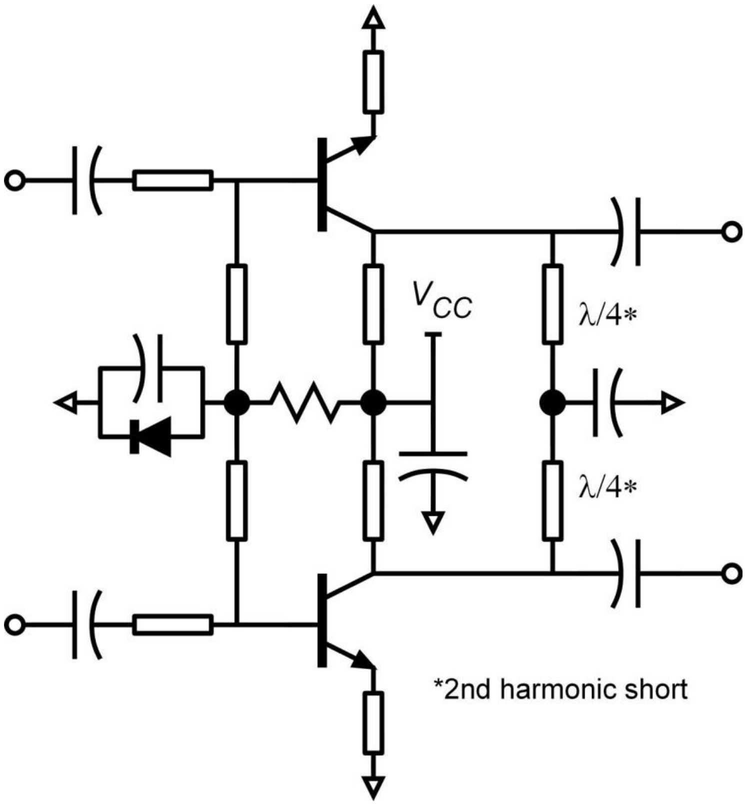
Virtual ground→ avoids ground via inductance ✓
Avoids power-supply coupling ✓
Potential problems with common mode ✗

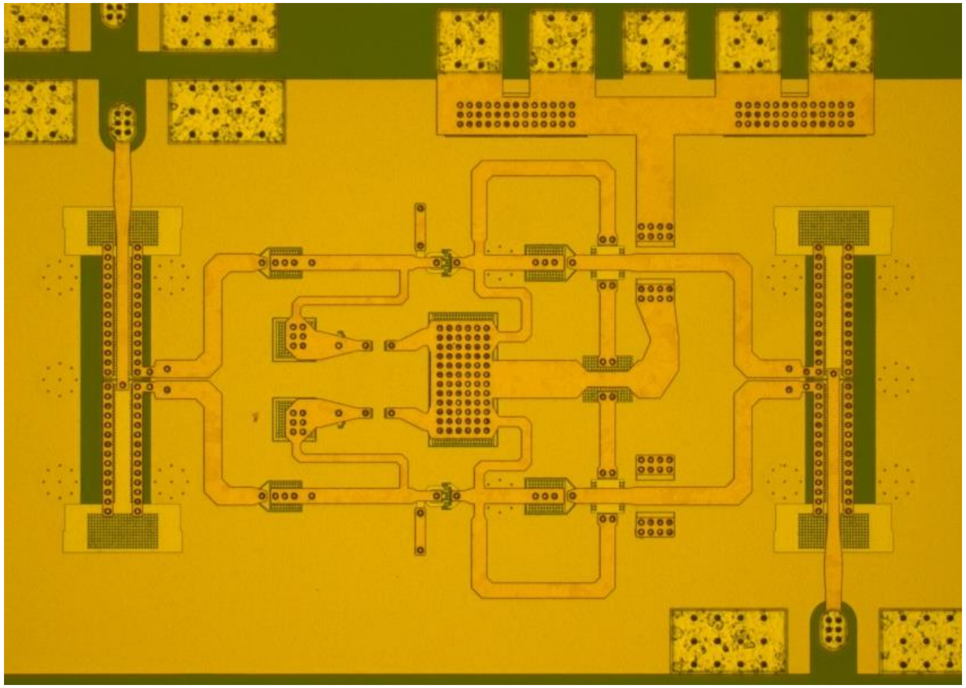
mm-wave common-mode instability



In all amplifiers, stability must be ensured from DC-f_{max}.
Differential ***& common-mode*** stability must be ensured from DC-f_{max}
Simple LNA inductive tuning is, for example, problematic

Pseudo-Differential Stages



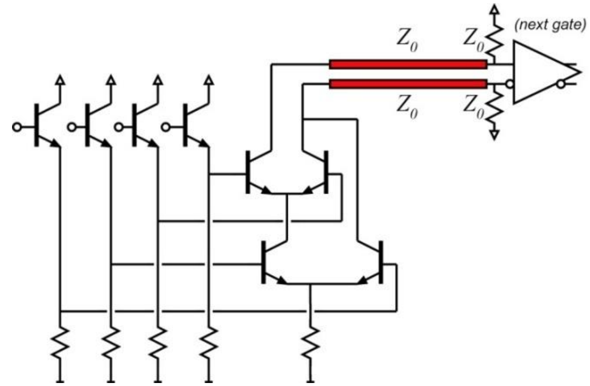


No common-mode instability problem.
Power-supply is virtual ground.
No supply detuning of output network
Improved power-supply isolation (oscillation, unwanted signal coupling)

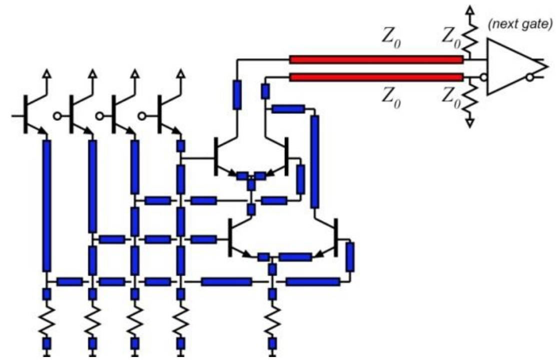
20+ GHz digital & mixed-signal design

Modeling Interconnects: Digital & Mixed-Signal IC's

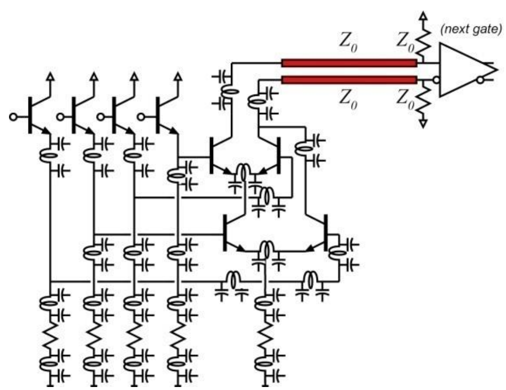
longer interconnects:
lines terminated in Zo → no reflections.



Shorter interconnects:
lines NOT terminated in Zo .
But they are *still* transmission-lines.
Ignore their effect at your peril !



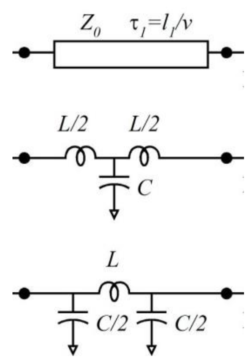
If length << wavelength,
or line delay<<risetime,
short interconnects behave
as lumped L and C.



$L = Z_0 \tau$,

$C = \tau / Z_0$,

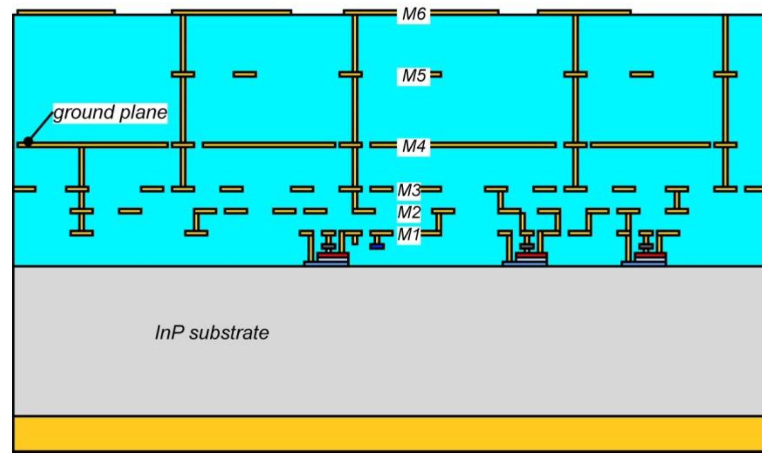
$\tau = l / v$



Modeling: 2.5D, library Tline, or L-C

Design Flow: Digital & Mixed-Signal IC's

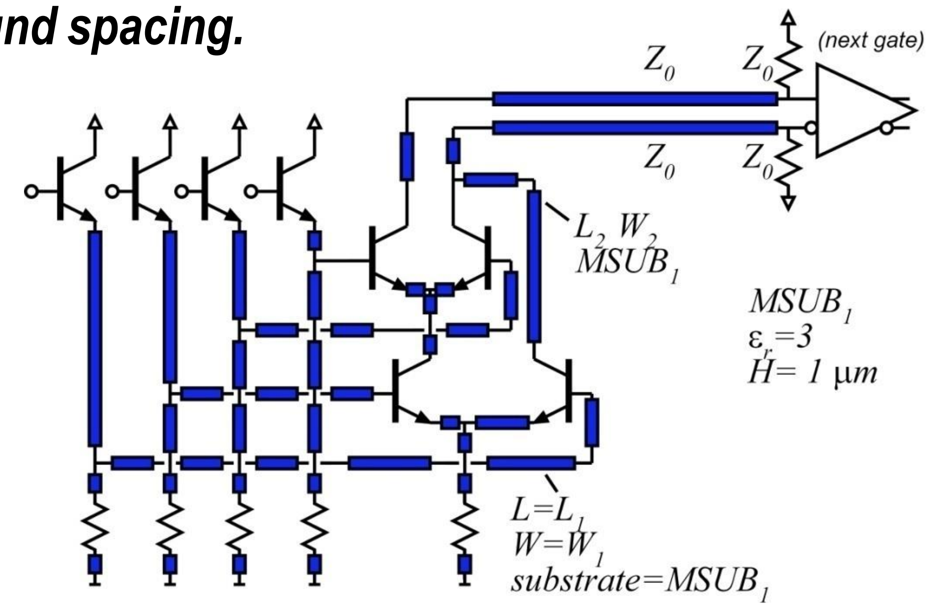
All interconnects: thin-film microstrip environment.
<u>Continuous</u> ground on one plane.



2.5-D simulations run on representative lines.
various widths, various planes
same reference (ground) plane.

Simulation data manually fit to CAD line model
effective substrate ε_r, effective line-ground spacing.

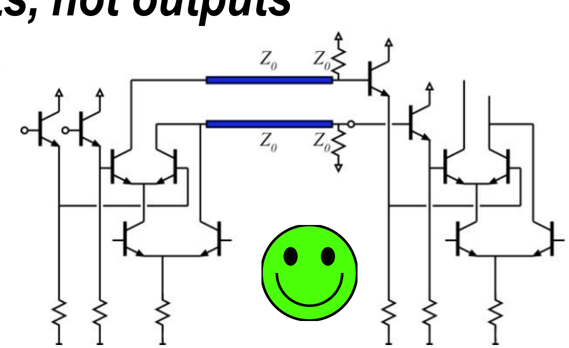
Width, length, substrate of each line
entered on CAD schematic.
rapid data entry, rapid simulation.

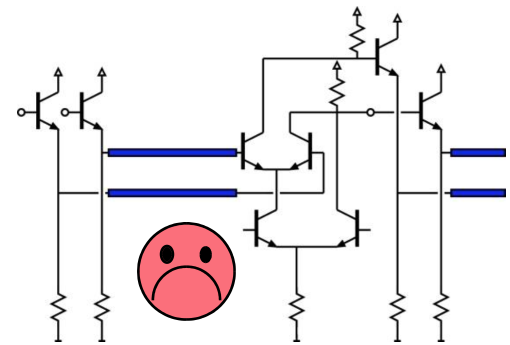


Resistors and capacitors:
2.5-D simulation→ RLC fit
RLC model used in simulation.

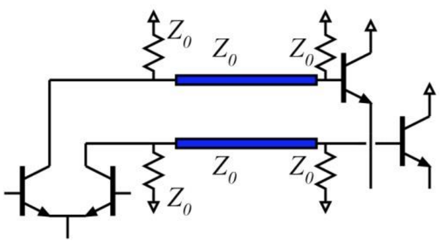
High Speed ECL Design

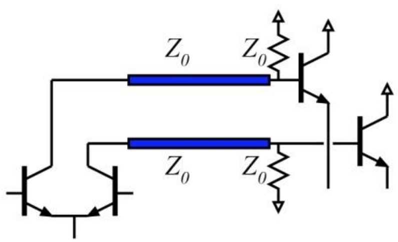
Followers associated with inputs, not outputs
Emitters never drive long wires.
(instability with capacitive load)

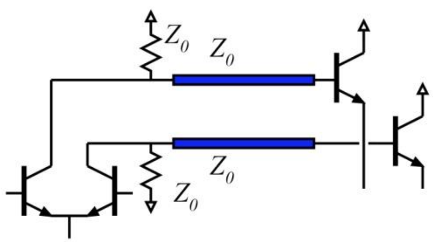


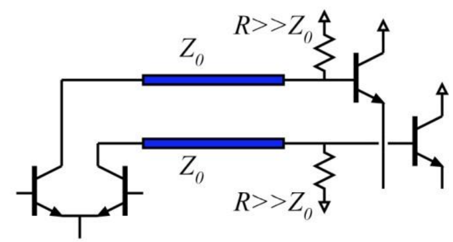


Double termination for least ringing, send or receive termination for moderate-length lines, high-Z loading saves power but kills speed.

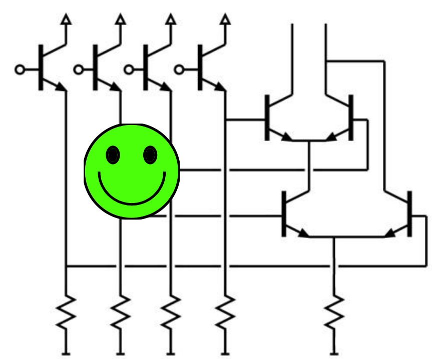


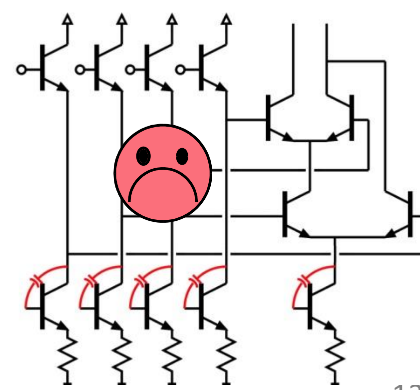






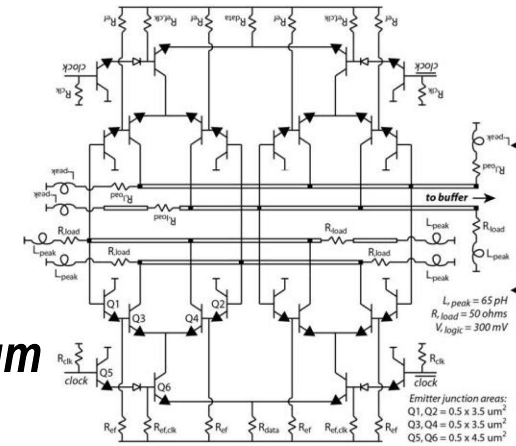
Current mirror biasing is more compact.
Mirror capacitance→ ringing, instability.
Resistors provide follower damping.

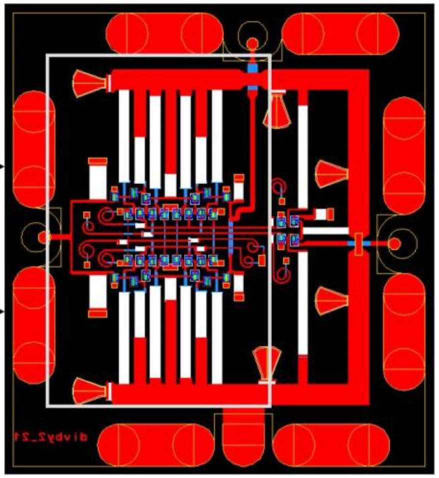




High Speed ECL Design

Layout: short signal paths at gate centers, bias sources surround core. Inverted thin film microstrip wiring.

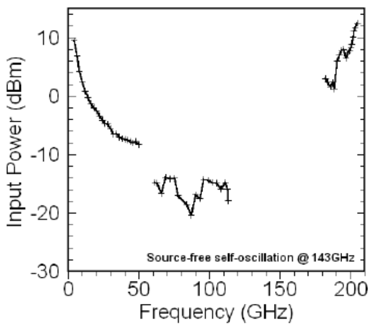


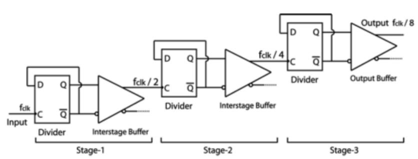


Key: transistors in on-state operate at Kirk limited-current.
→ minimizes C_{cb}/I_c delay.

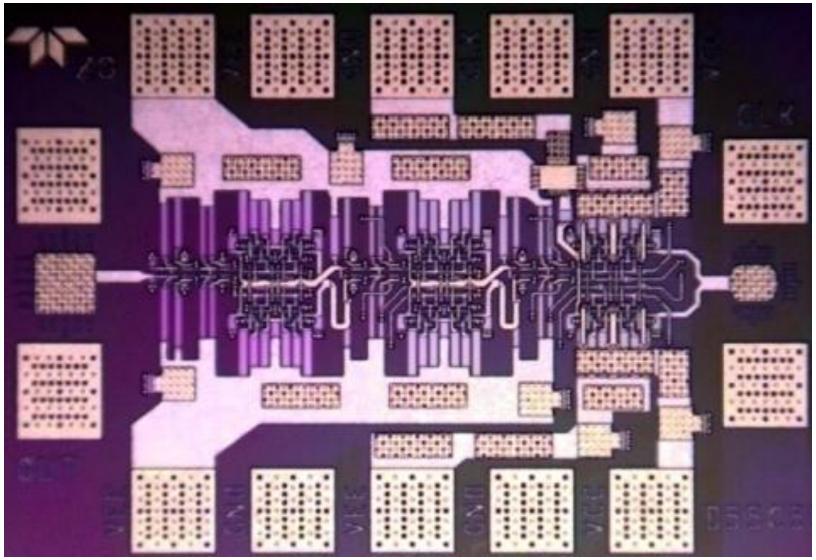
Key: transistors designed for minimum ECL gate delay*, not peak (f_τ, f_{max}).
**hand expression, charge-control analysis*

Example: 8:1 205 GHz static divider in 256 nm InP HBT.

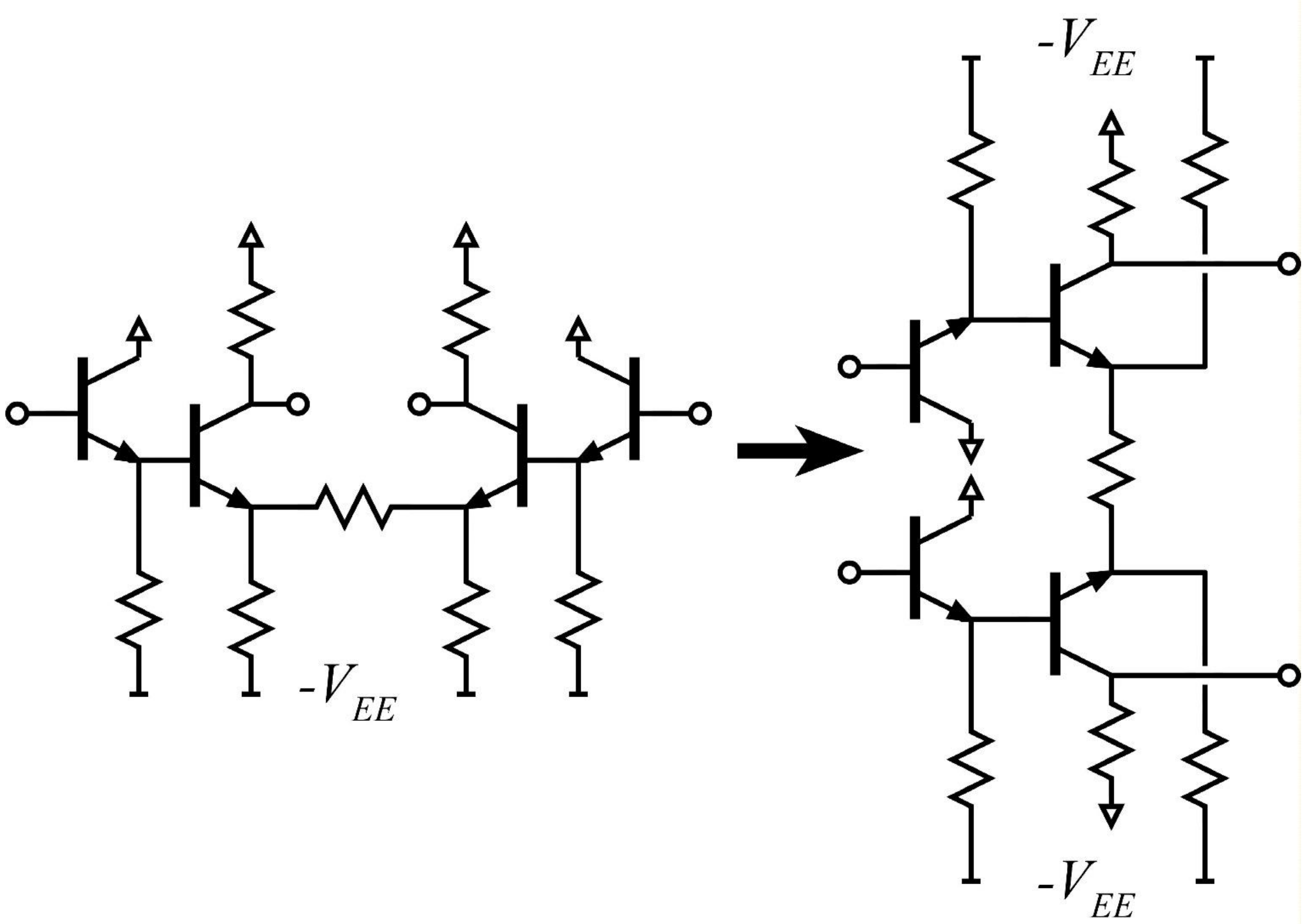




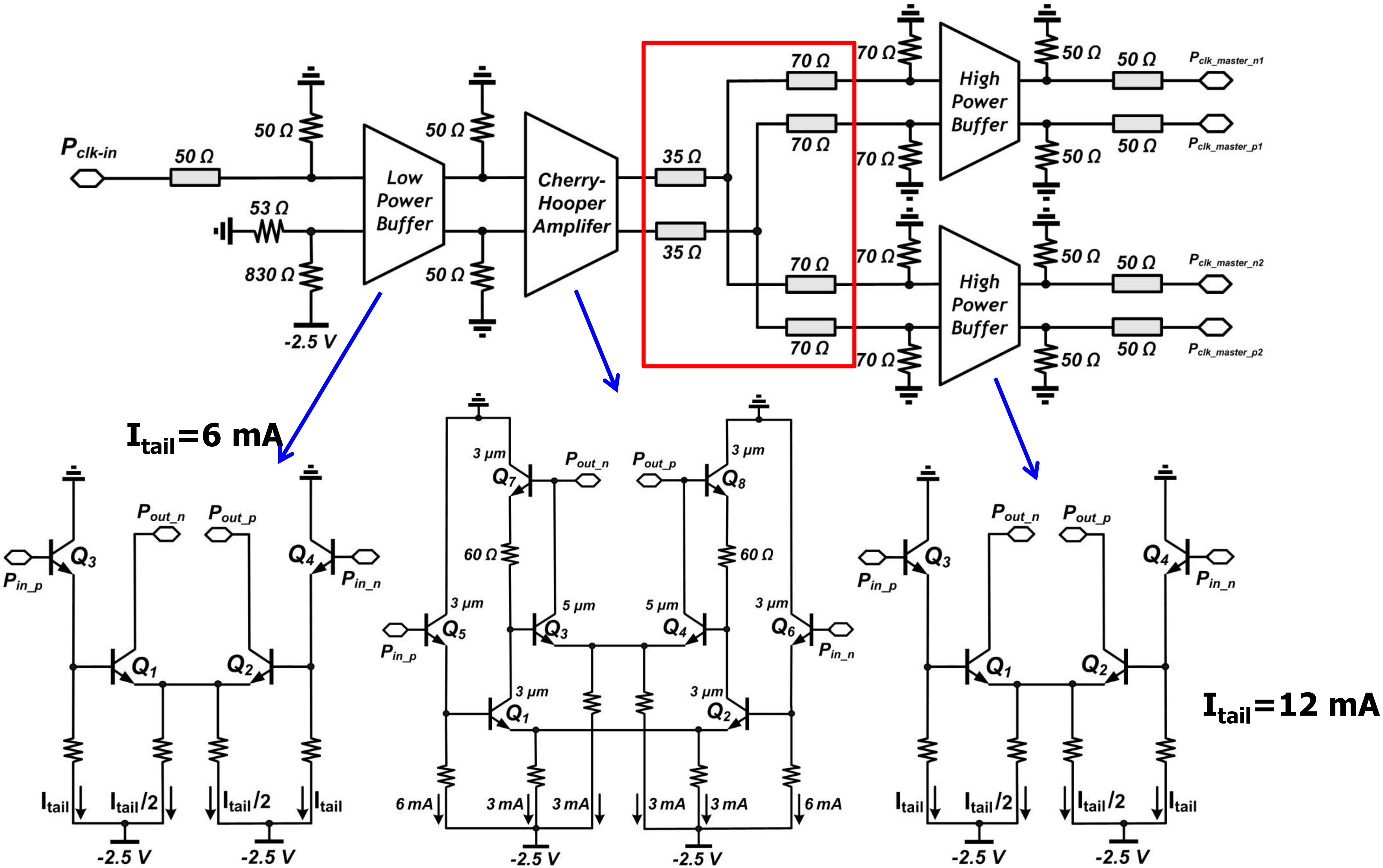
205 GHz divider, Griffith et al, IEEE CSIC, Oct. 2010



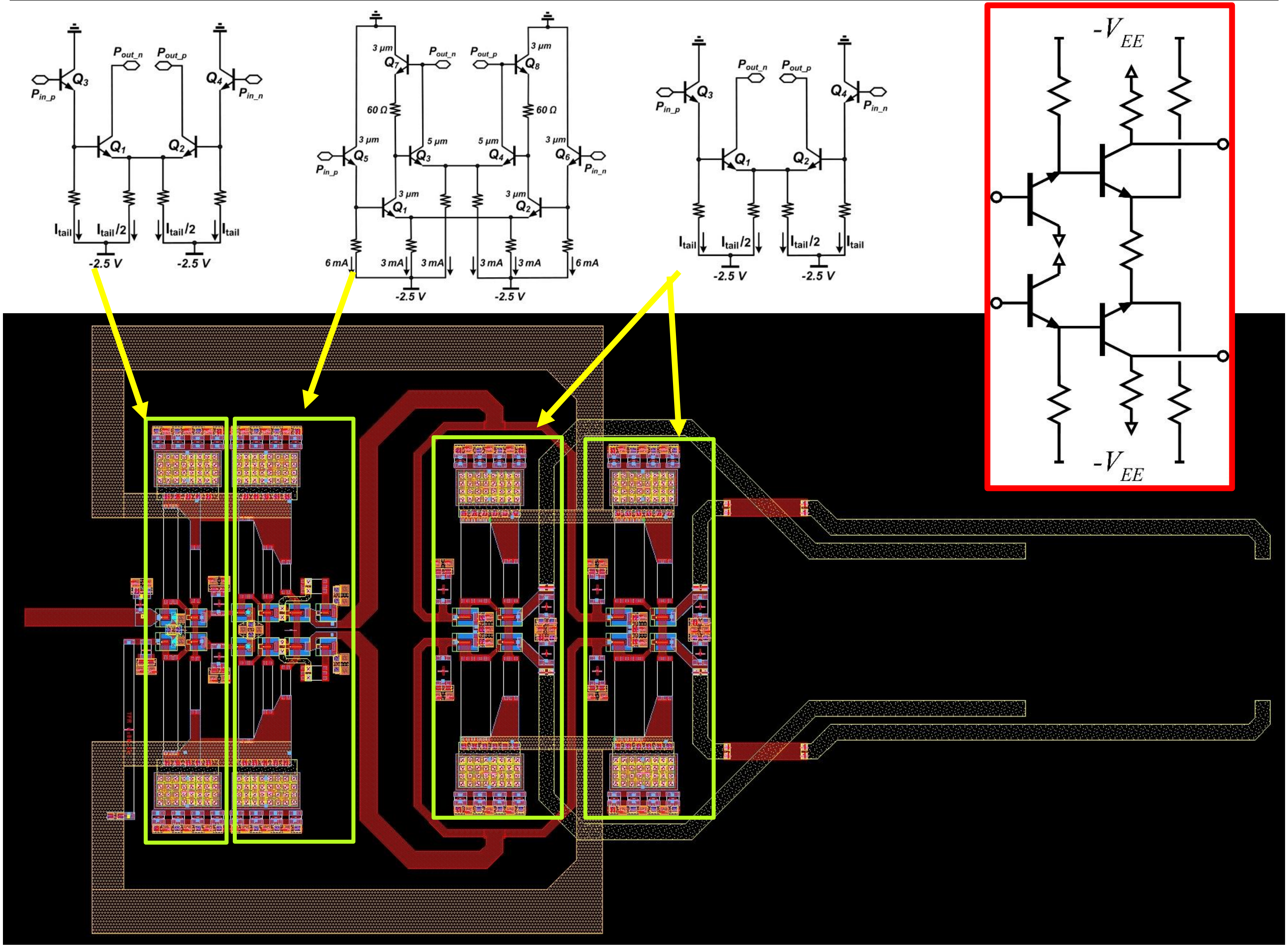
Differential stages: schematic vs. floorplan



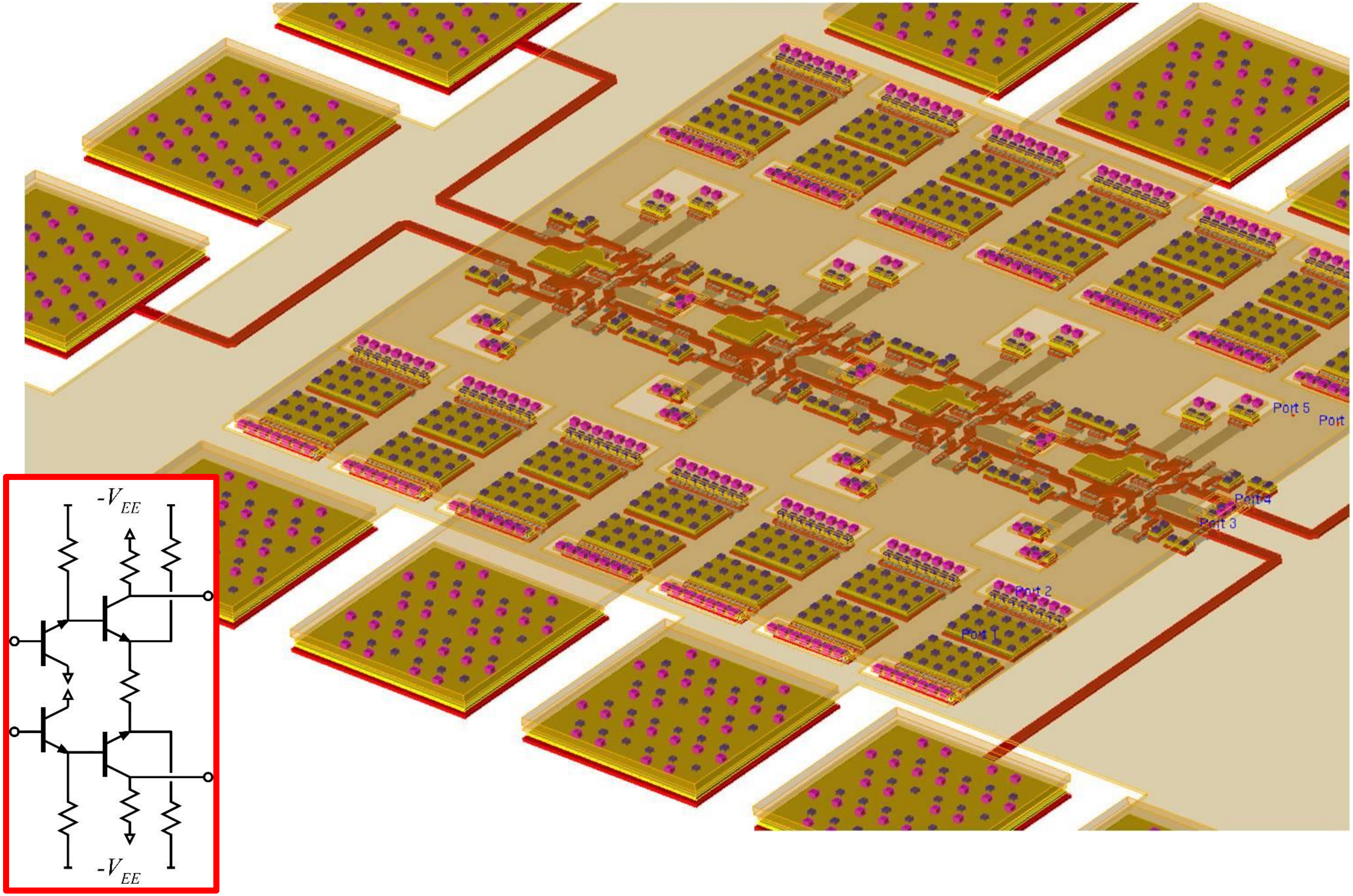
Example: 40 GS/s S/H clock buffer



Example: 40 GS/s S/H clock buffer



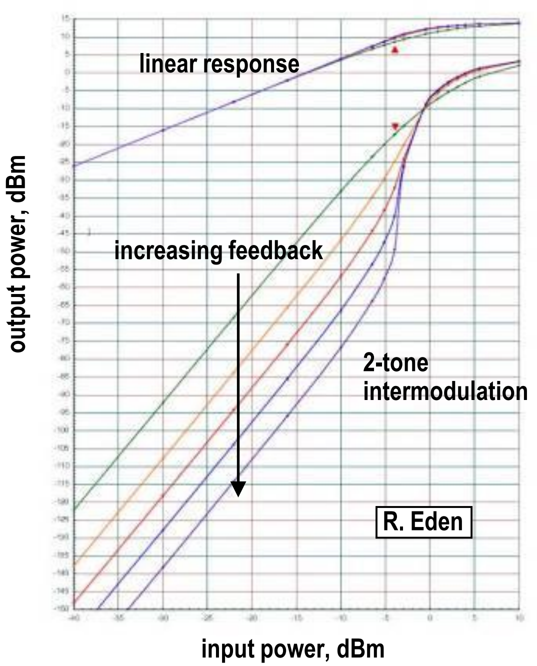
Example: 40 GS/s S/H clock buffer

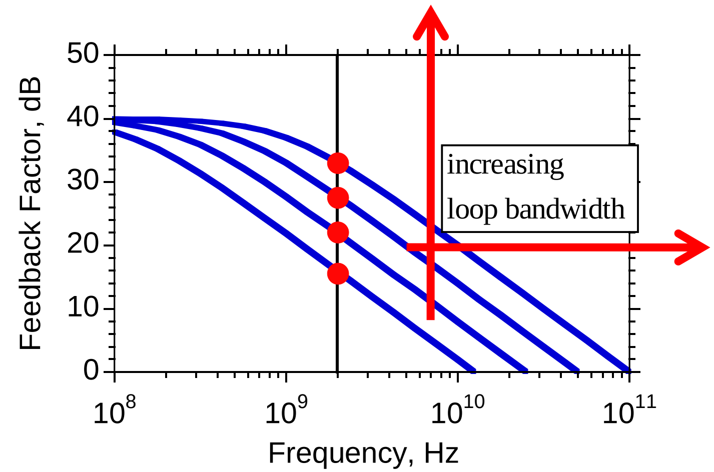


20GHz Op-Amps for Linear 2 GHz Amplification

Griffith et al, IEEE IMS, June. 2011

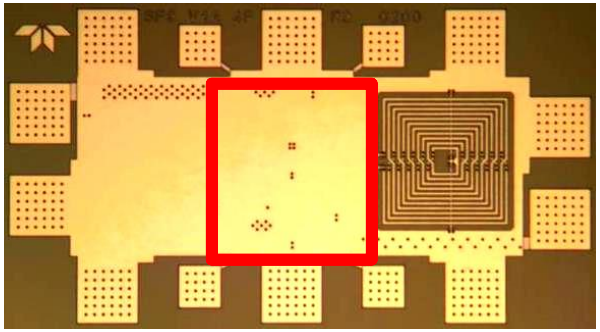
Reduce distortion with strong negative feedback

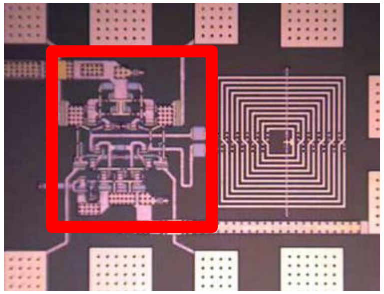




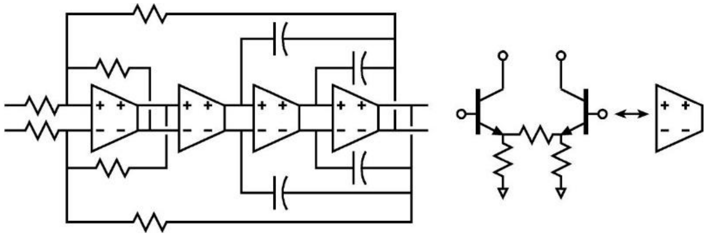
Even for 2 GHz operation, loop bandwidths must 20-40 GHz.

need very fast transistors





physically small feedback loop; bias components surround active core.



86 GHz
Power Amplifier

mm-Wave Power Amplifier: **Challenges**

needed: High power / High efficiency / Small die area (low cost)

***Extensive* power combining**

***Compact* power-combining**

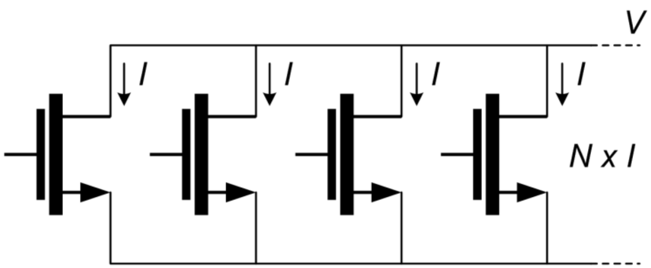
$$\mathrm{PAE} = \eta_{\substack{\mathrm{drain/}\\ \mathrm{collector}}} \left(1 - \frac{1}{\mathrm{Gain}}\right) \cdot \eta_{\substack{\mathrm{power-}\\ \mathrm{combiner}}}$$

Class E/D/F are poor @ mm-wave
insufficient f_{max} ,
high losses in harmonic terminations

***Efficient* power-combining**

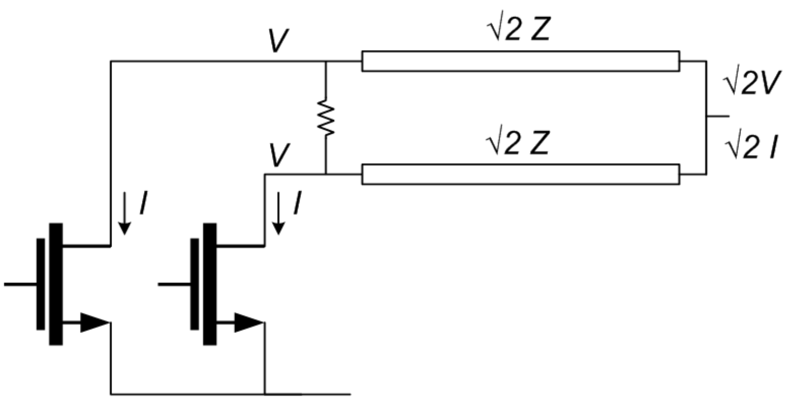
Goal: efficient, compact mm-wave power-combiners

Parallel Power-Combining



Output power: P_{OUT} = **N** x V x I
Parallel connection increases P_{OUT} ✓

Load Impedance: Z_{OPT} = V / (**N** x I)
Parallel connection decreases Z_{opt} ✗

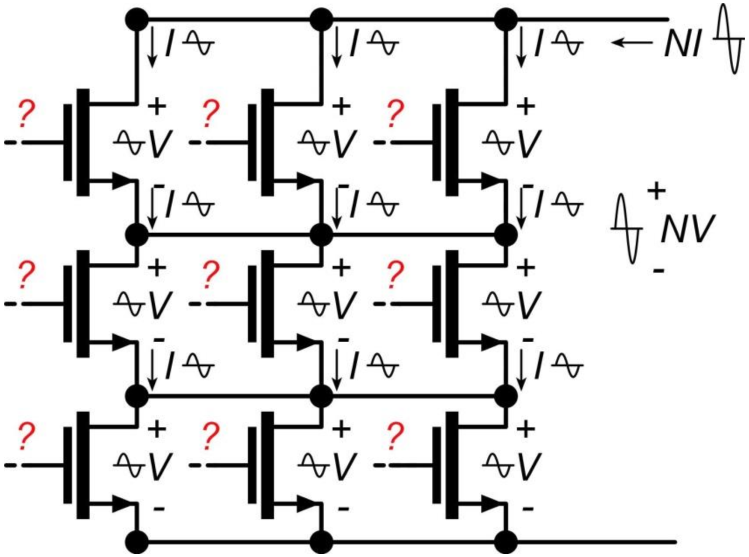


High P_{OUT} → Low Z_{opt}

Needs impedance transformation:
lumped lines, Wilkinson, ...

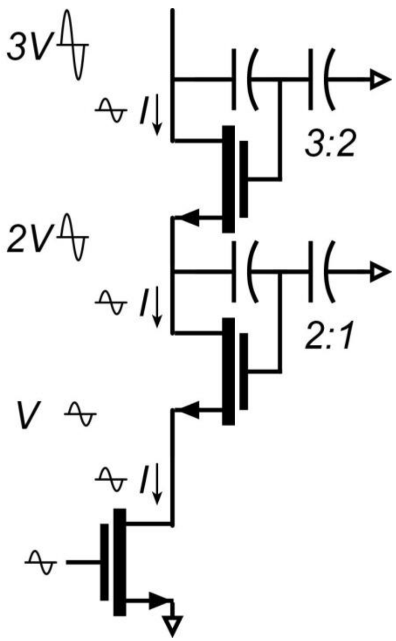
High insertion loss ✗
Small bandwidth
Large die area

Series Power-Combining & Stacks



Parallel connections: I_{out}=N x I
Series connections: V_{out}=N x V

Output power: P_{out}=**N^2** x V x I
Load impedance: Z_{opt}=V/I ✓
Small or zero power-combining losses ✓
Small die area ✓
How do we drive the gates ?



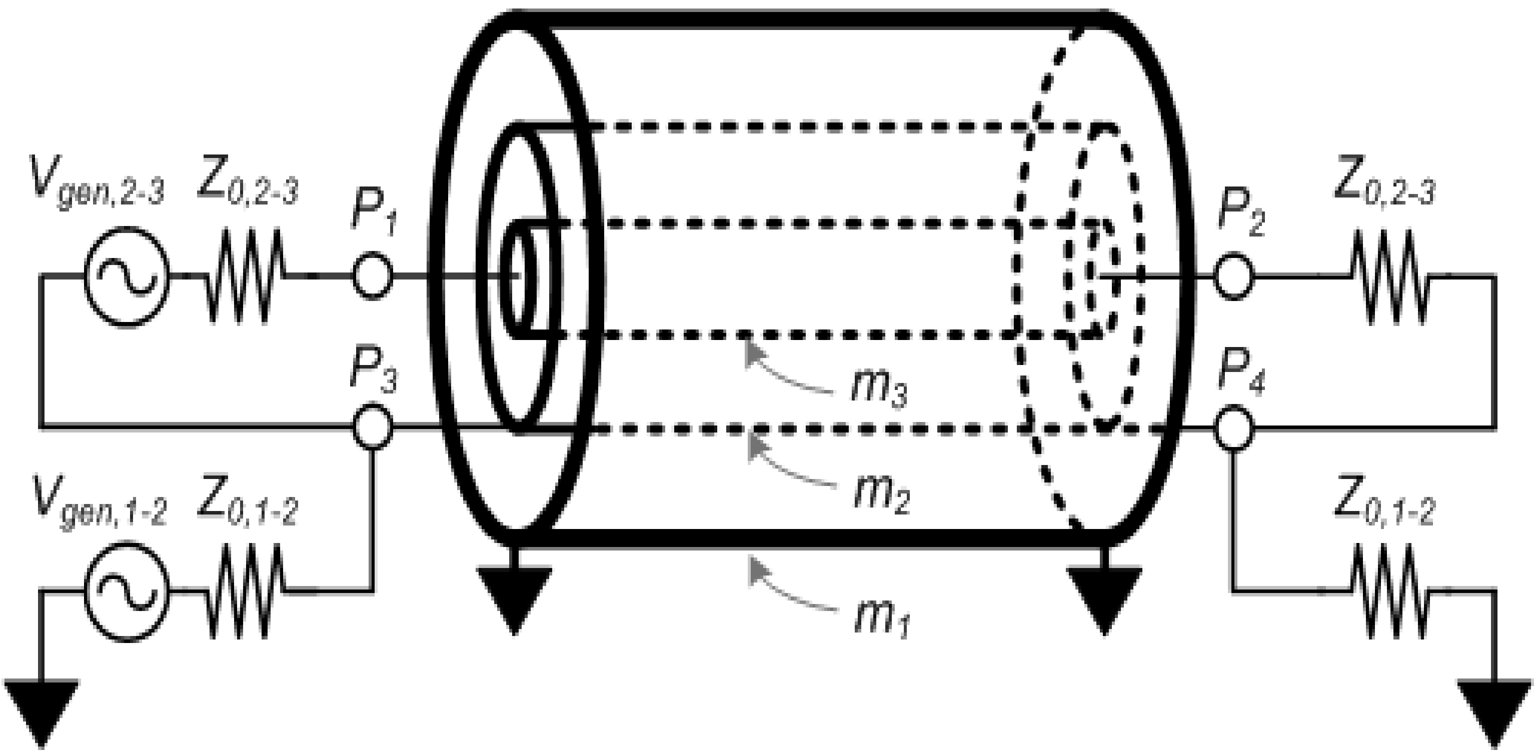
Local voltage feedback:
drives gates, sets voltage distribution

Design challenge:
need uniform RF voltage distribution
need ~unity RF current gain per element

...needed for simultaneous compression of all FETs.

Shifrin *et al.*, 1992 IEEE-IMS; Rodwell *et al.*, U.S. Patent 5,945,879, 1999; Pornpromlikit *et al.*, 2011 CSICS

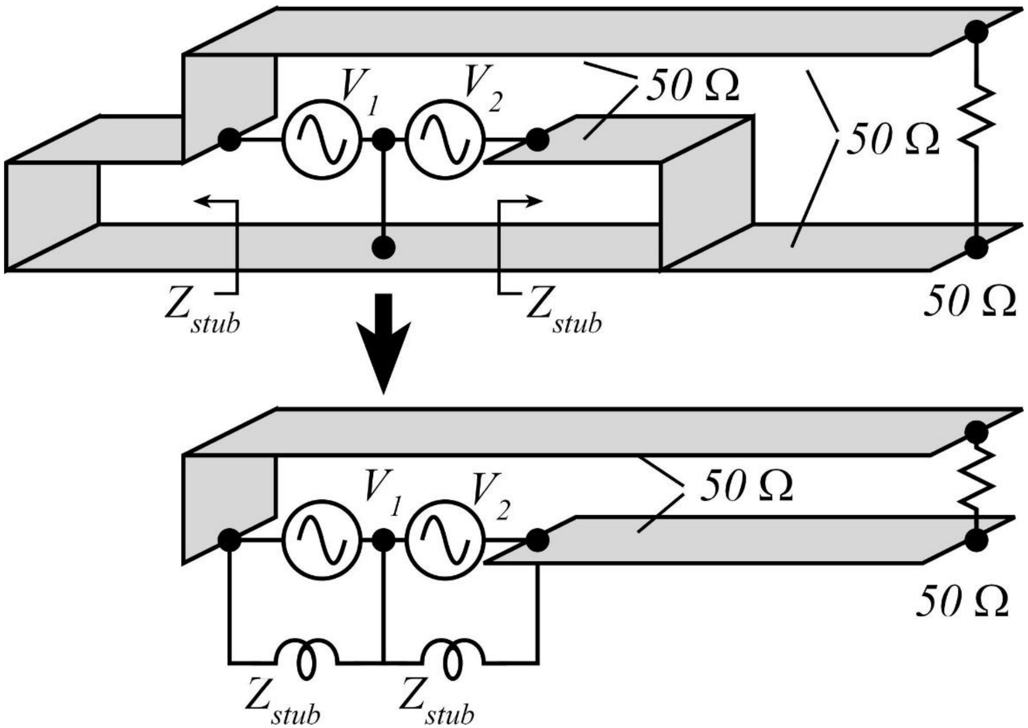
Ideal Tri-axial Line



Two separate transmission lines (m_3-m_2, m_2-m_1)

→ E, H fields between m_3 and m_1 perfectly shielded

Sub-λ/4 Baluns for **Series** Combining



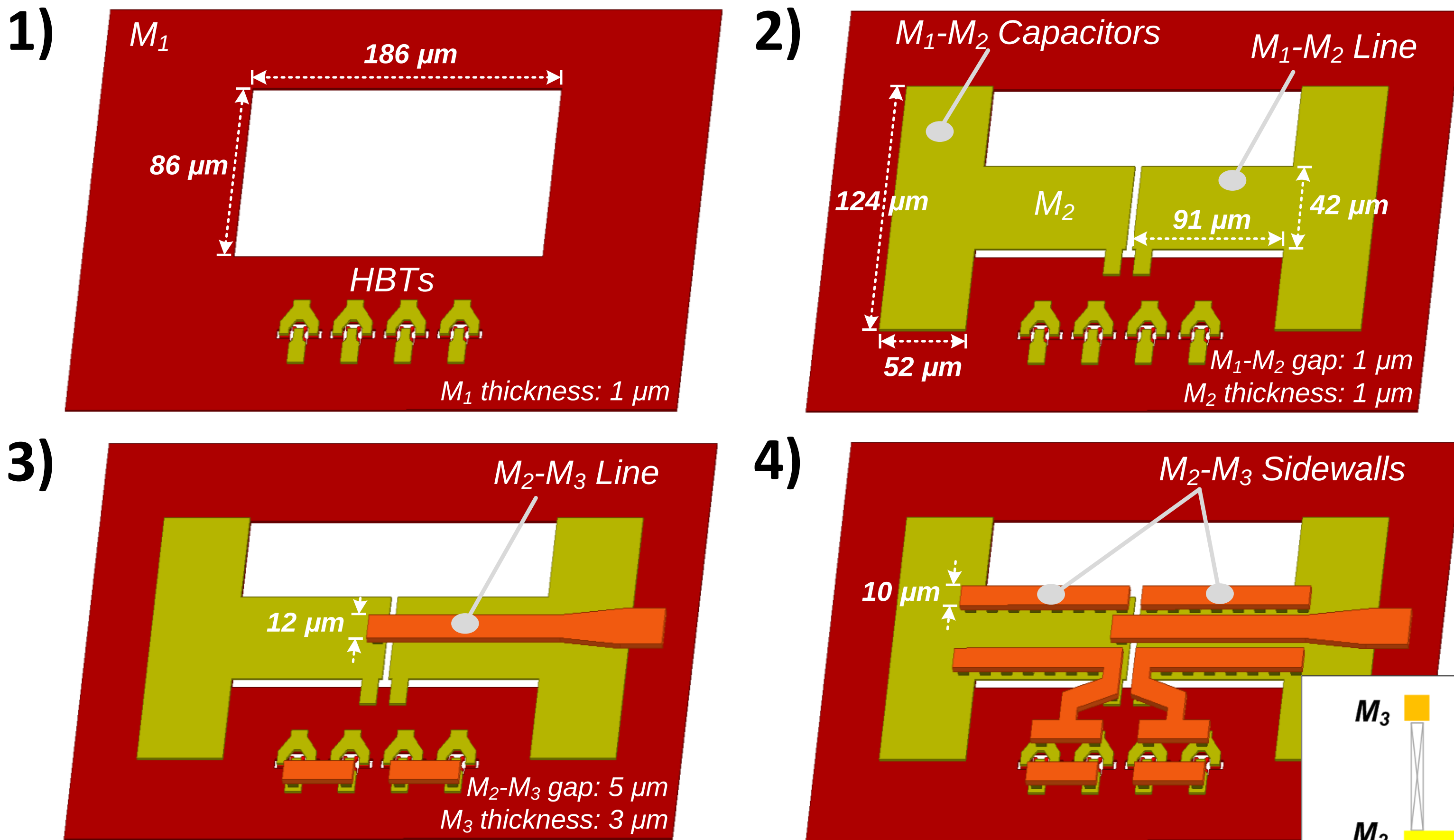
Balun combiner:
2:1 series connection ✓
each source sees 25 Ω
→ 4:1 increased P_{out} ✓

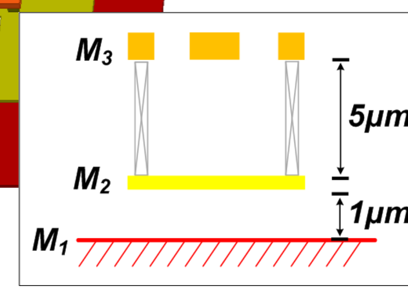
Standard λ/4 balun :
long lines
→ high losses ✗
→ large die ✗

Sub-λ/4 balun :
stub→ inductive
tunes transistor C_{out} ! ✓
short lines→ low losses ✓
short lines → small die ✓

Park *et al.*, 2013 CSICS, 2014 IEEE-IMS

Baluns in **Real ICs**





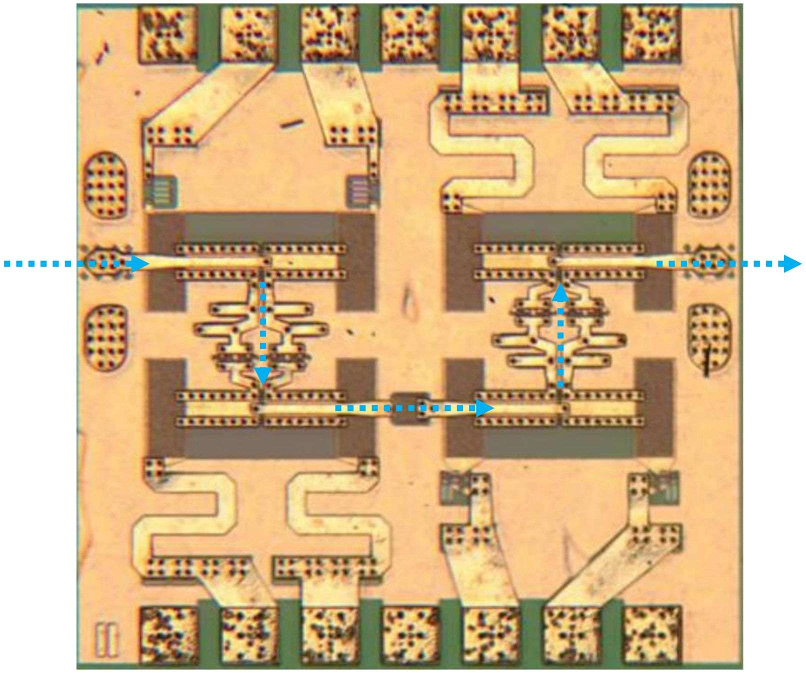
1) M_1 as a GND

2) Slot-type transmission lines (M_1-M_2), AC short (2 pF MIM)

3) Microstrip line (M_2-M_3), E-field shielding **NOT** negligible

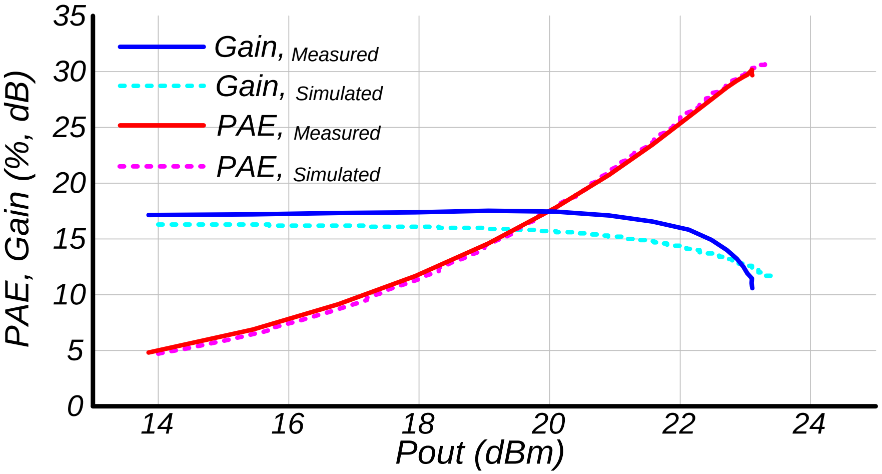
4) **Sidewalls** between M_3-M_1 (Faraday cages), **λ/16 length**

Two-Stage PA IC Test Results (86GHz)



IC size: 825 x 820 um²

Large signal measurements



Gain: 17.5 dB
P_{SAT}: >200 mW @ 3.0 V
PAE: >30 %

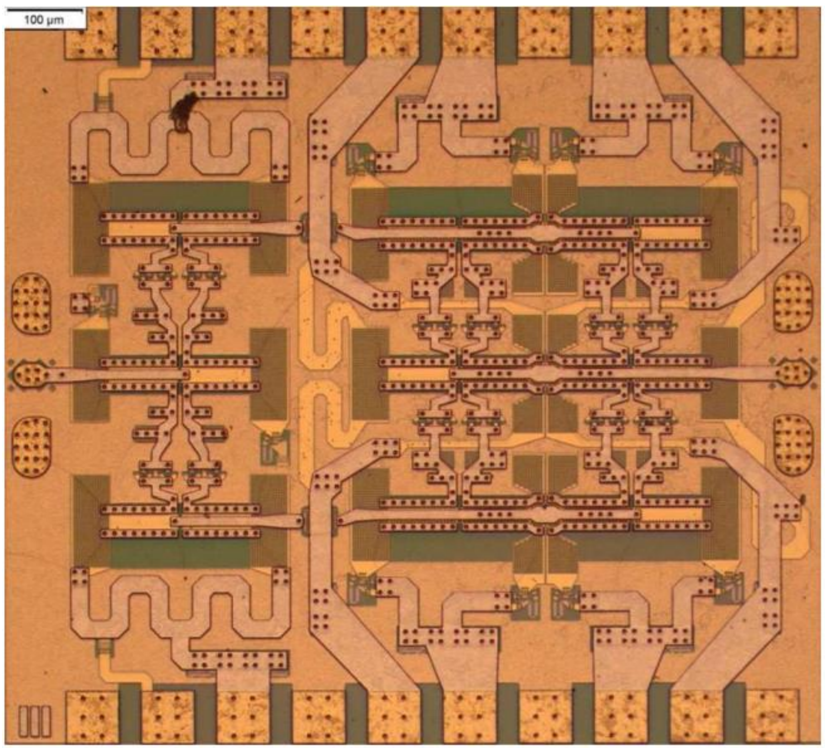
Power density (power/die area)
= 307 mW/mm² (including RF pads)
= 927 mW/mm² (core area)

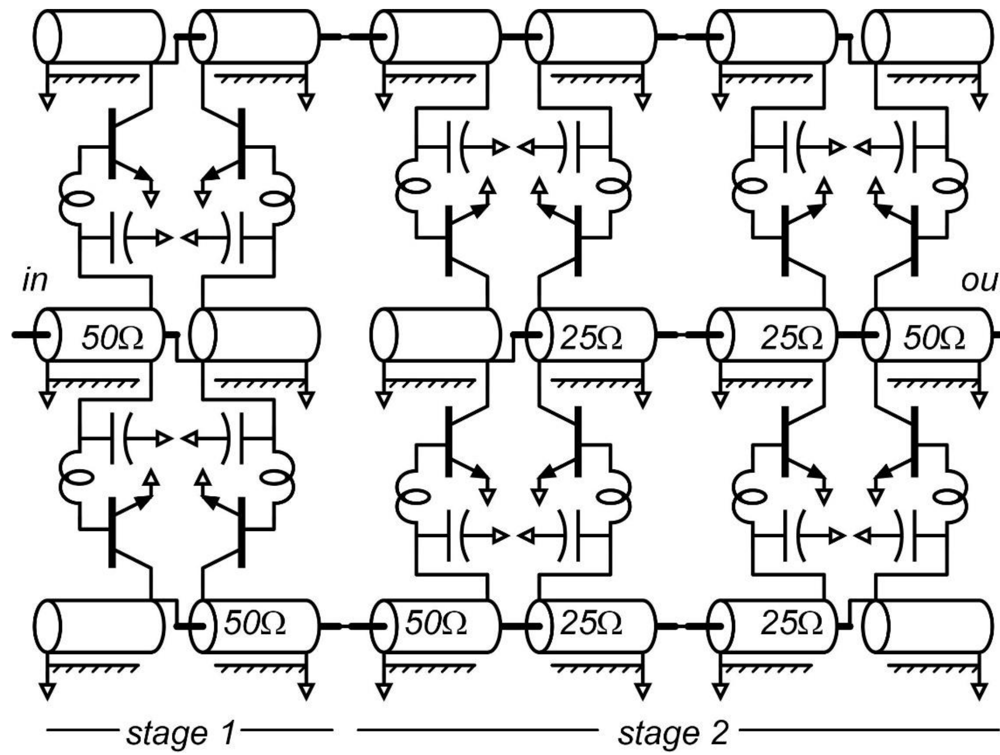
[H. Park et al, CSICS 2013]
30% PAE W-Band InP Power Amplifiers Using Sub-Quarter-Wavelength Baluns for Series-Connected Power-Combining

4:1 series-connected 81GHz power amplifier

Park *et al.*, 2014 IEEE-IMS

17 dB Gain
470 mW P_{sat}
23% PAE
Teledyne 250 nm InP HBT
2 stages, 1.0 mm^2(incl pads)

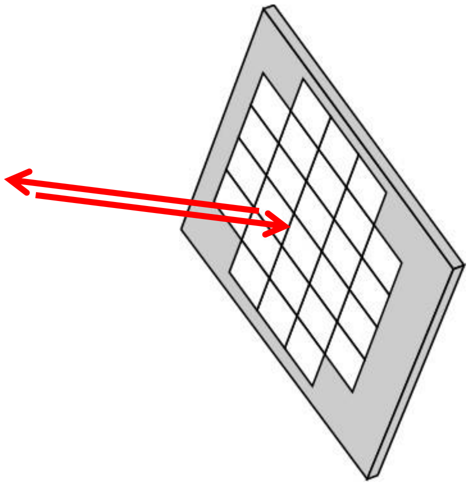


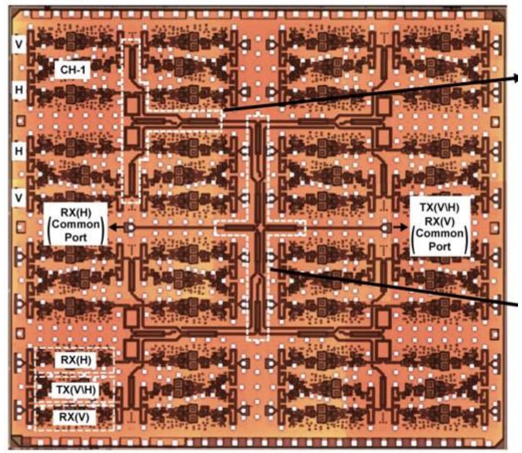


IC example:
220 GHz
power amplifier

Millimeter-wave imaging

10,000-pixel, 94GHz imaging array→ 10,000 elements





Golcuk: Trans MTT, Aug 2014

Demonstrated:

SiGe (UCSD/Rebeiz)

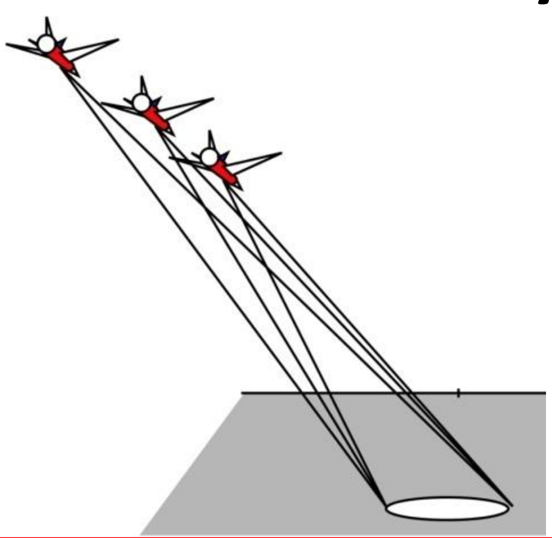
~1.3kW: 10,000 elements

Lower-power designs:

InP, CMOS, SiGe

(UCSB, UCSD, Virginia Poly.)

235 GHz video-rate synthetic aperture radar



1 transmitter, 1 receiver

100,000 pixels

20 Hz refresh rate

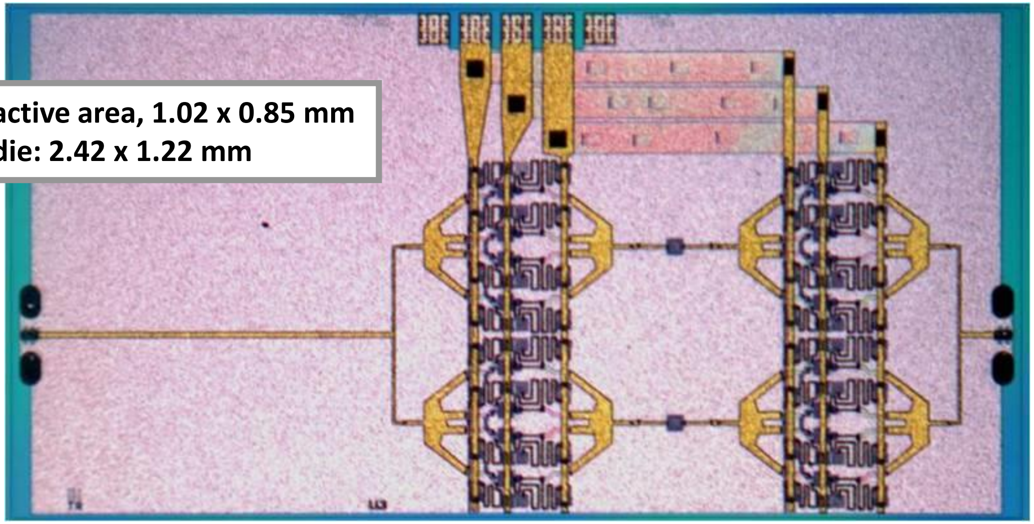
5 cm resolution @ 1km

50 Watt transmitter

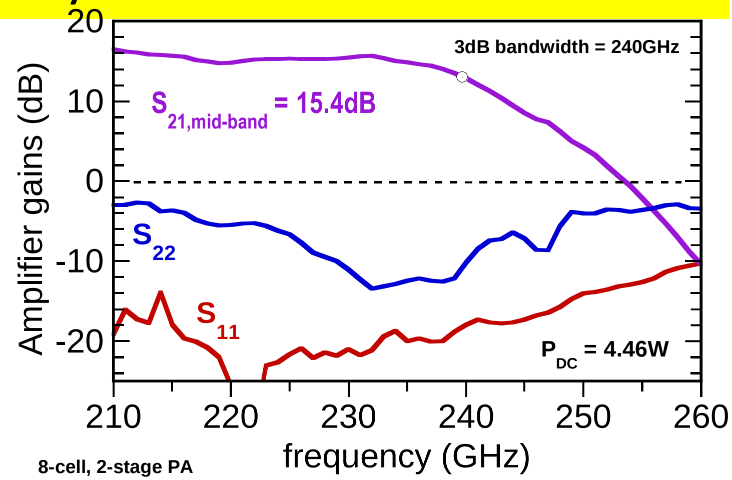
(tube, solid-state driver)

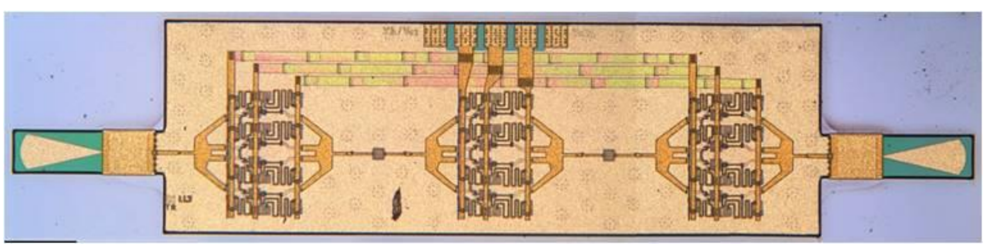
90 mW, 220 GHz Power Amplifier

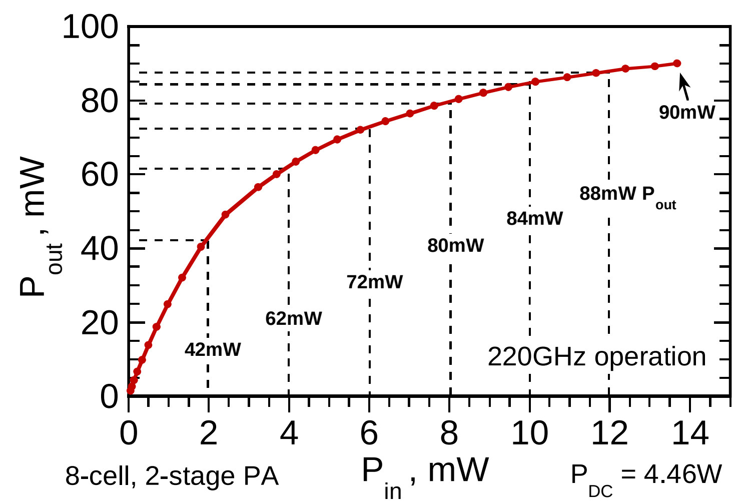
active area, 1.02 x 0.85 mm
die: 2.42 x 1.22 mm



Reed (UCSB) and Griffith (Teledyne): CSIC 2012
Teledyne 250 nm InP HBT







214 GHz InP HBT Power Amplifier

UCSB/Teledyne

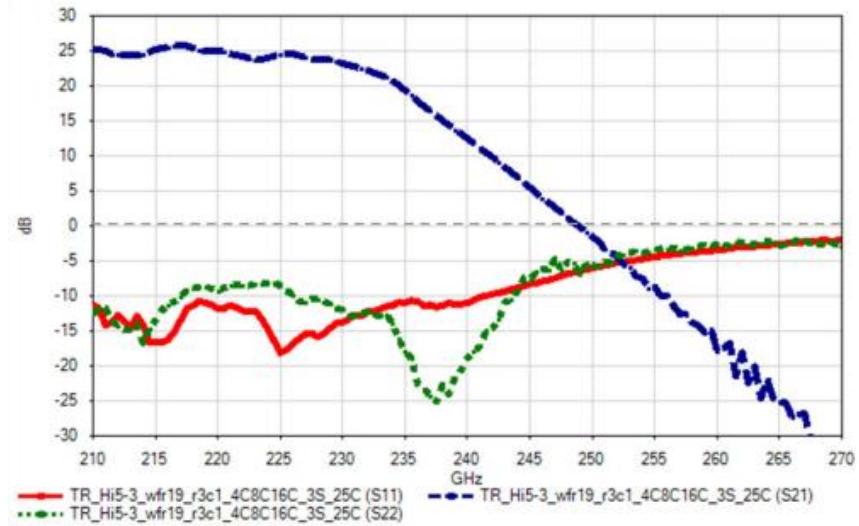
Gain: 25dB S21 Gain at 220GHz

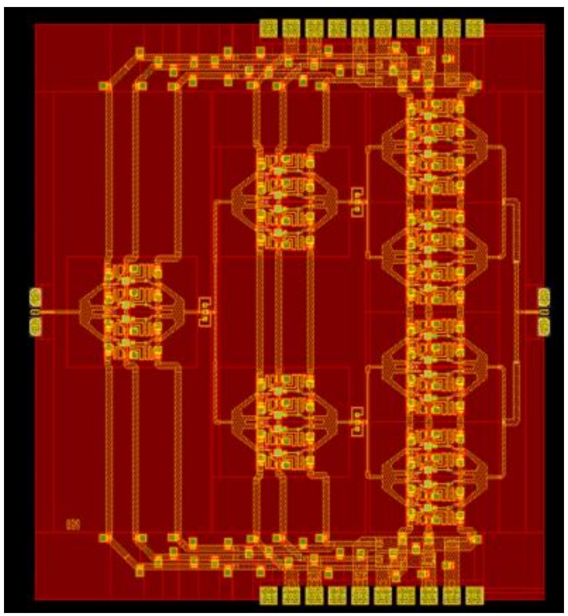
Saturated output power: 164mW at 214GHz

Output Power Density:0.43 W/mm

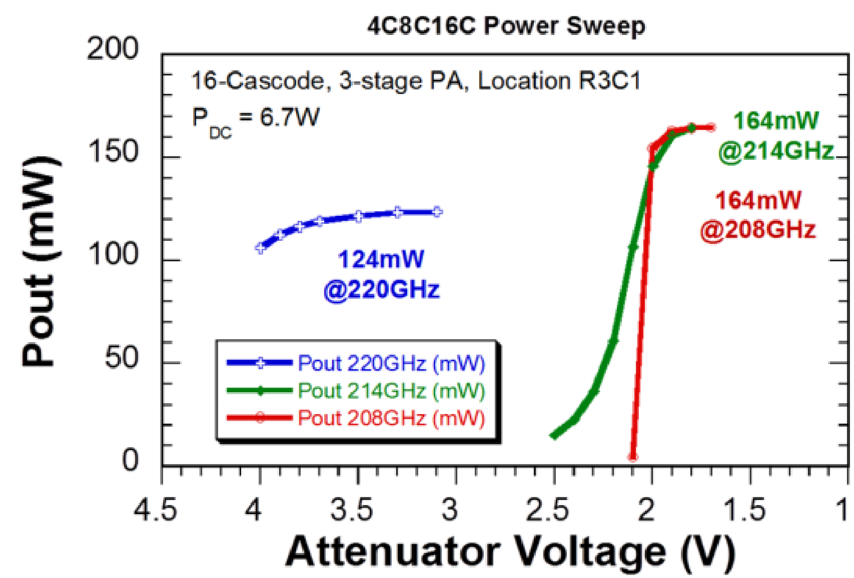
PAE: 2.4%

Technology: 250 nm InP HBT



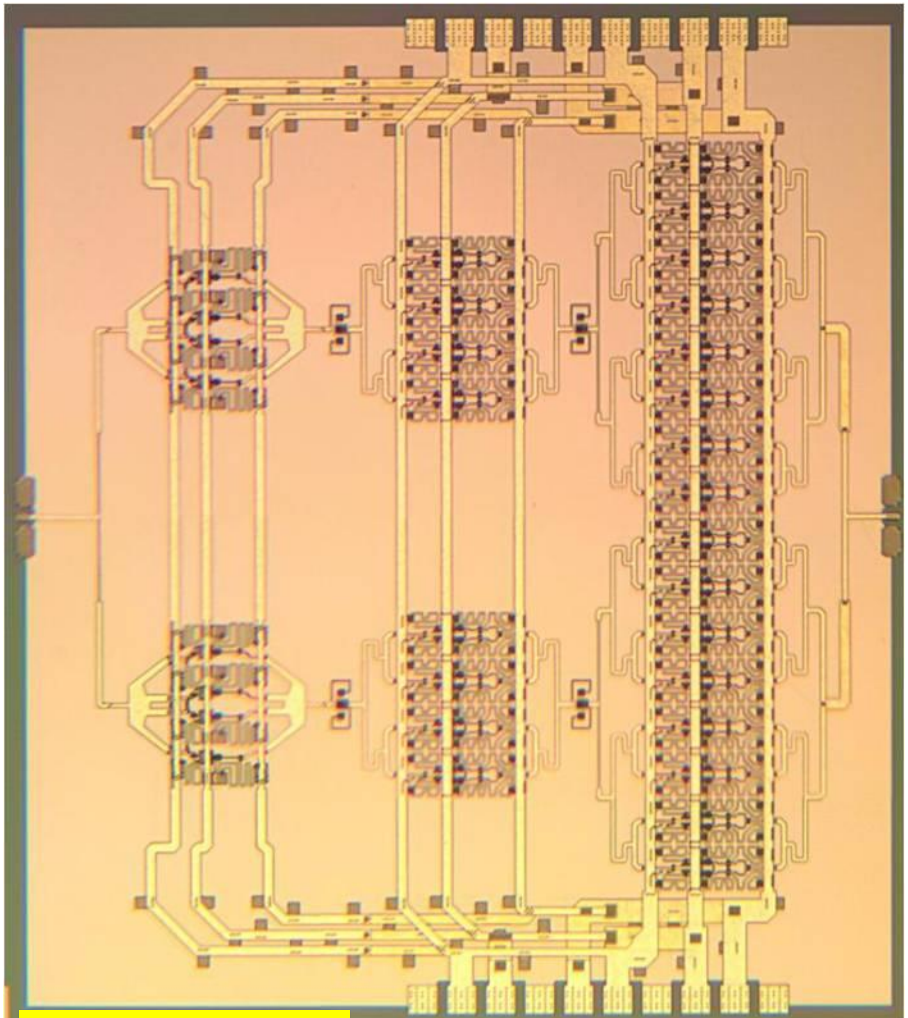


(no die photo) 2.5mm x 2.1 mm



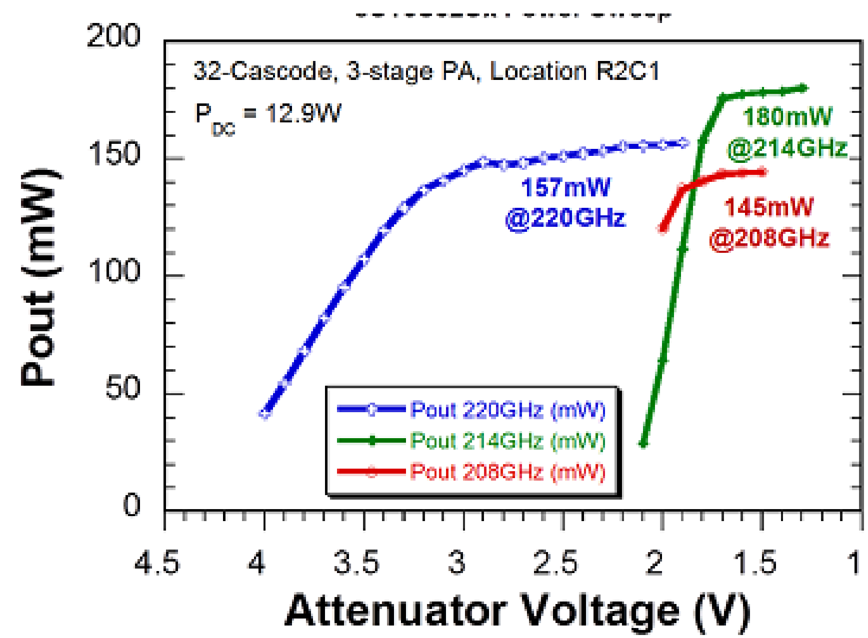
Reed et al, 2014 CSICS http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6659187&tag=1

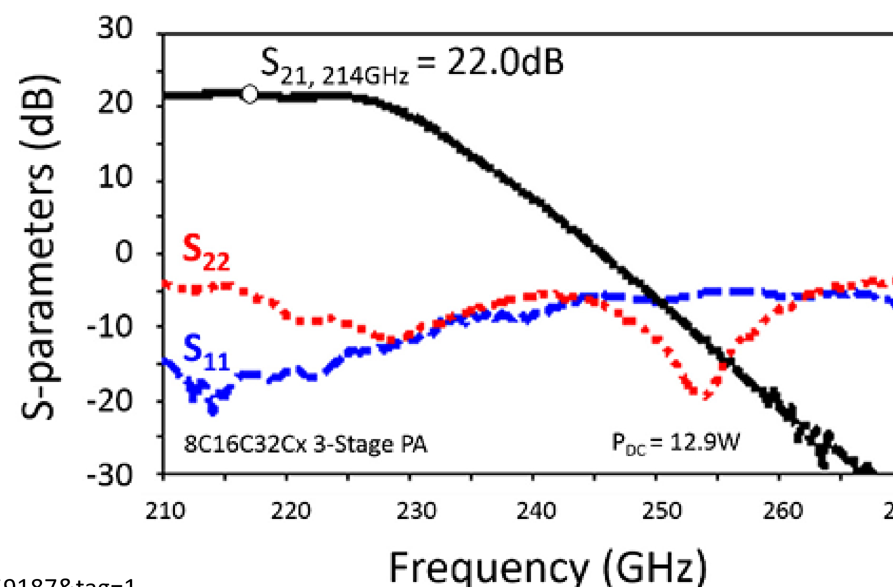
214 GHz 180mW Power Amplifier (330 mW design)



2.3 mm x 2.5 mm

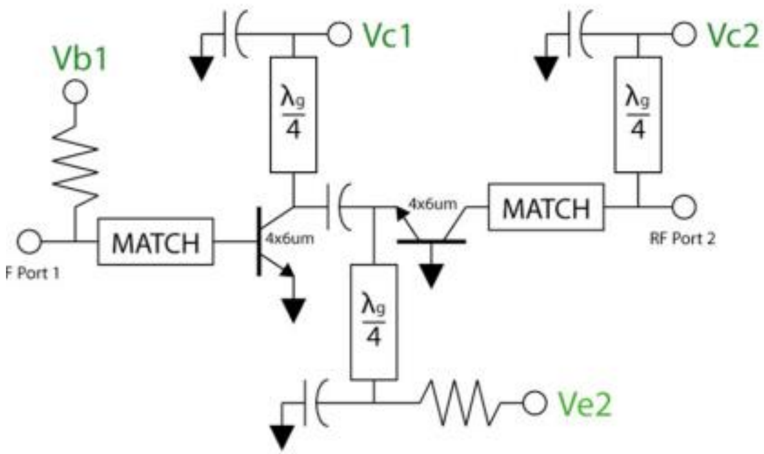
Reed, Griffith CSICS2013
Teledyne 250 nm InP HBT

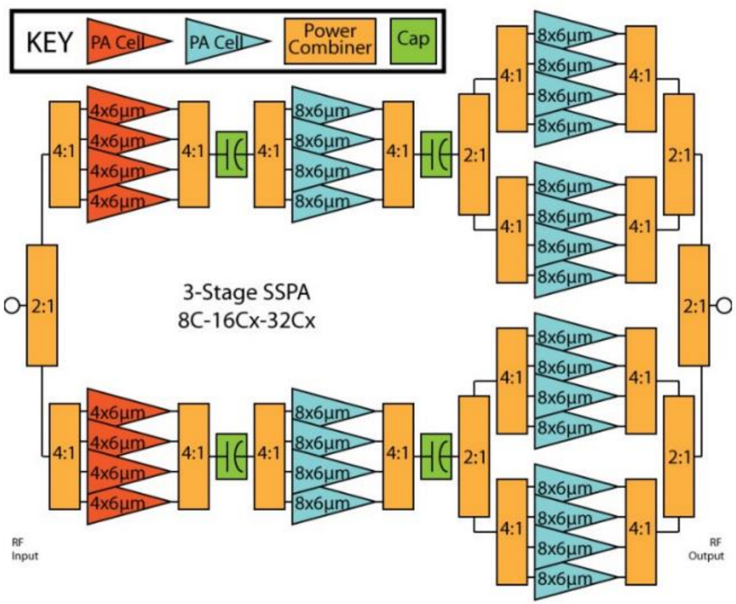


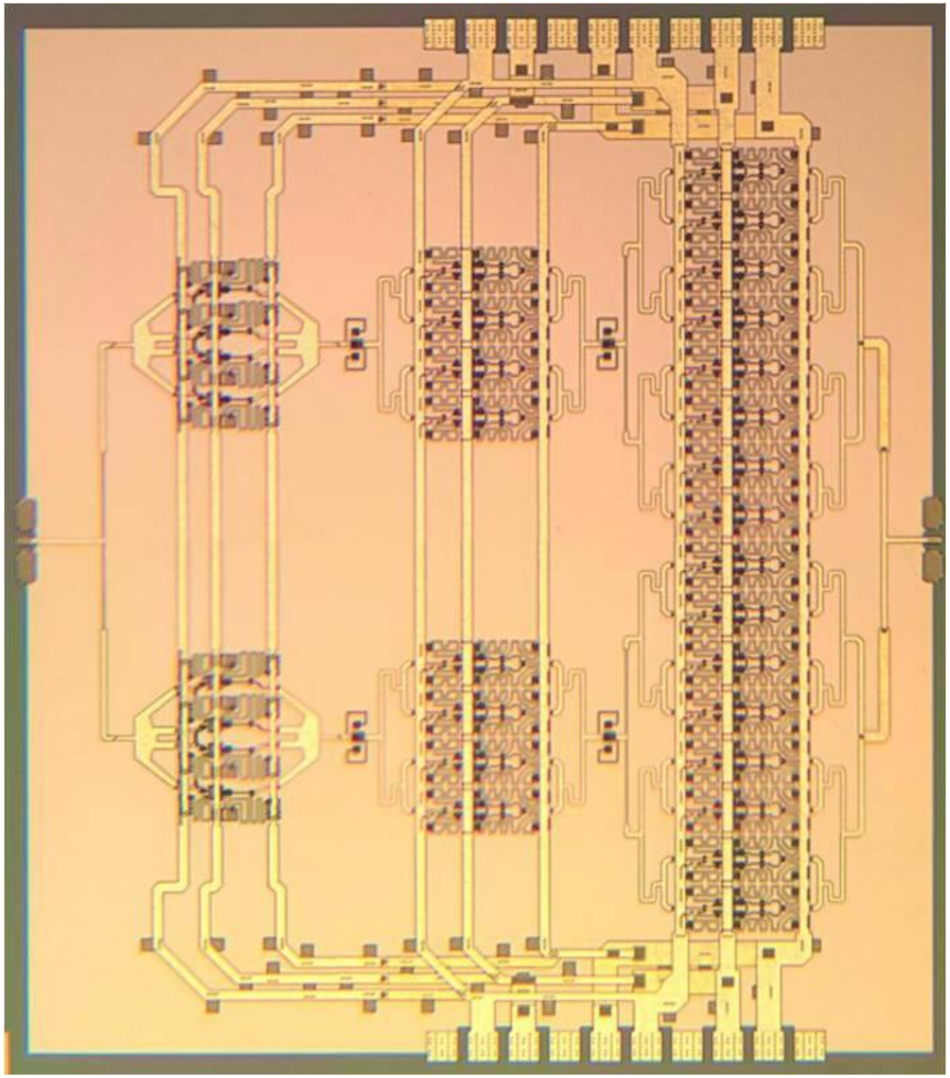


Reed et al, 2014 CSICS http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6659187&tag=1

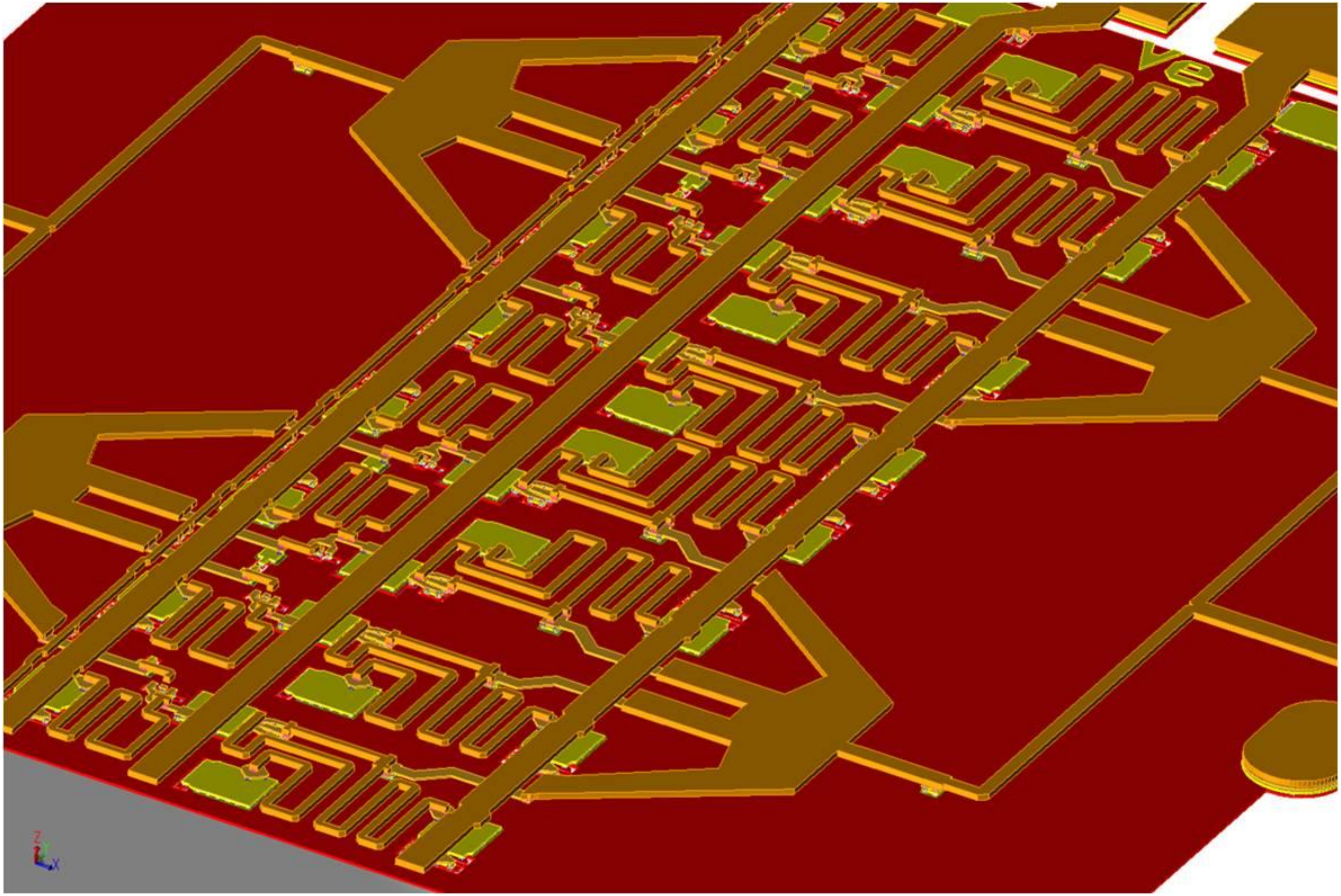
220 GHz power amplifiers; 256nm InP HBT







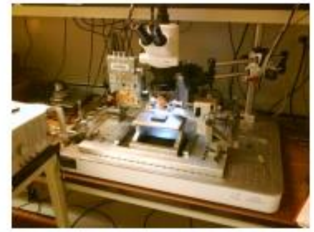
ICs in Thin-Film (Not Inverted) Microstrip

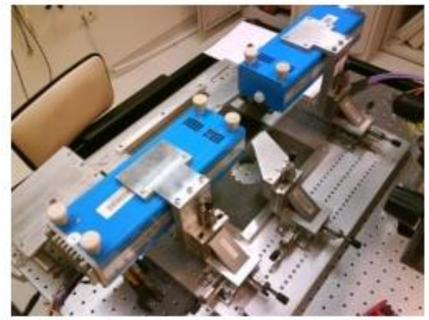


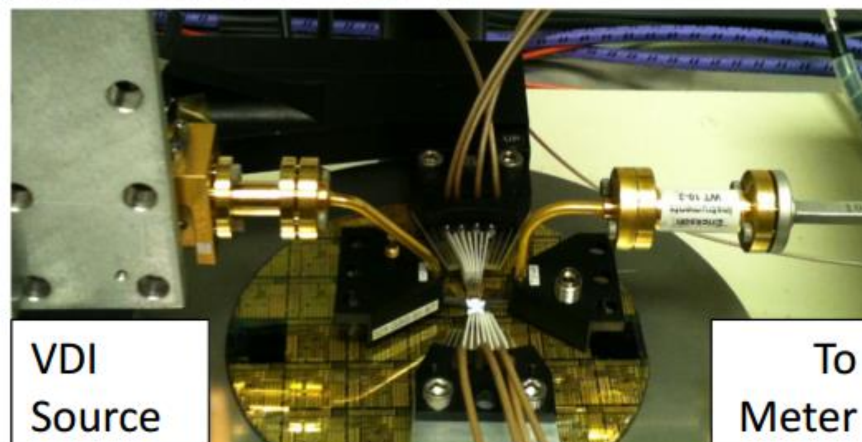
Note breaks in ground plane at transistors, resistors, capacitors

220 GHz measurement

- Small Signal Measurement
  - VNA with 140-220 and 206-340 GHz frequency extender heads
  - LRRM Probe-tip Calibration
- Power Sweep Measurement
  - 220 GHz frequency multiplier chains and sub-mm wave power meter
  - Insertion Loss Calibration
  - Forced Air cooling

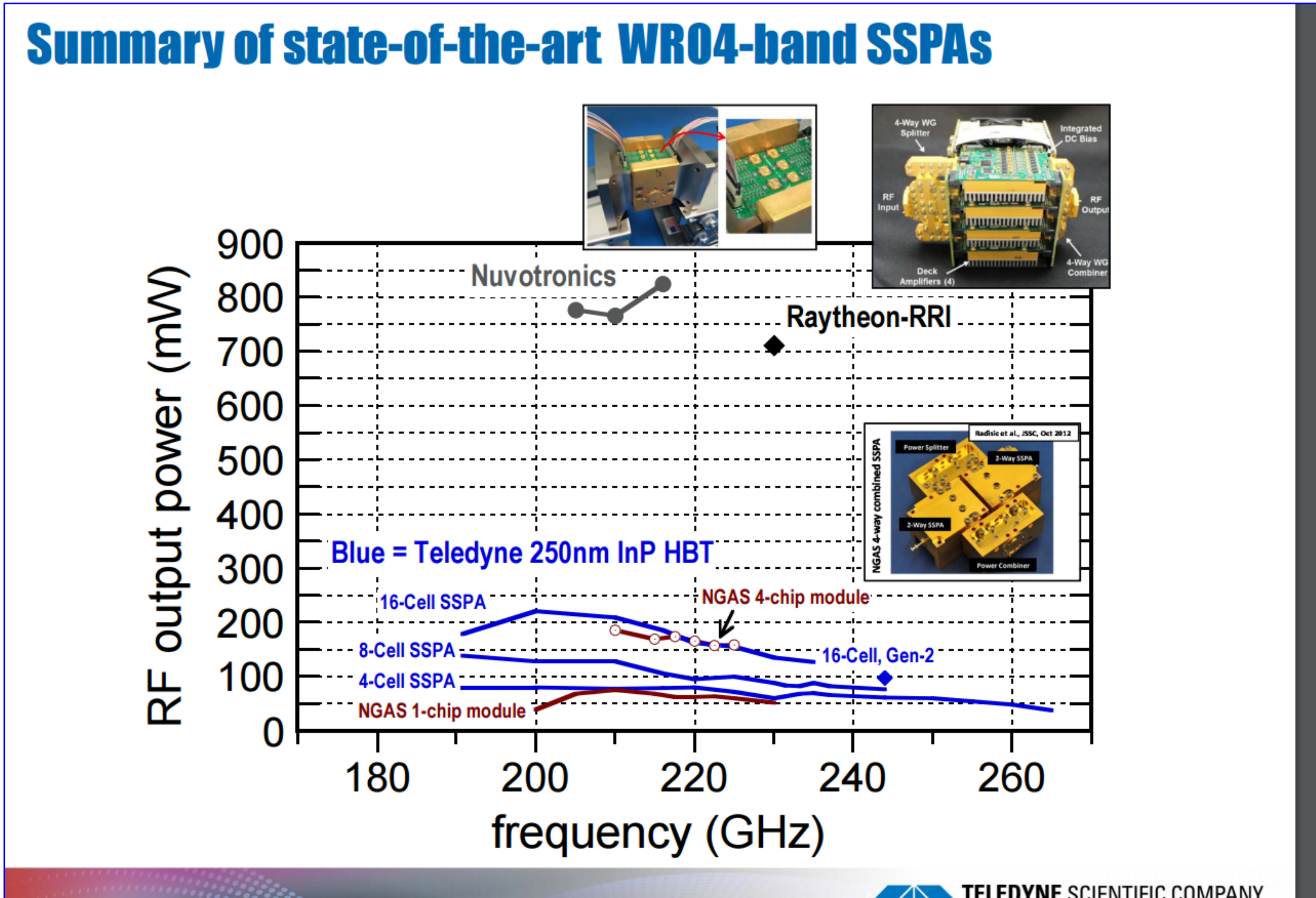






Power combined modules

Slide from Z. Griffith IMS 2016 Presentation

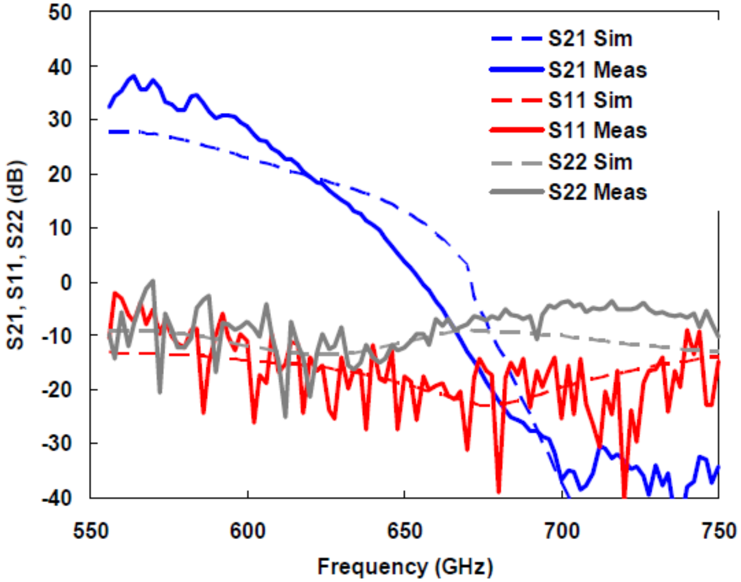


mm-Wave power

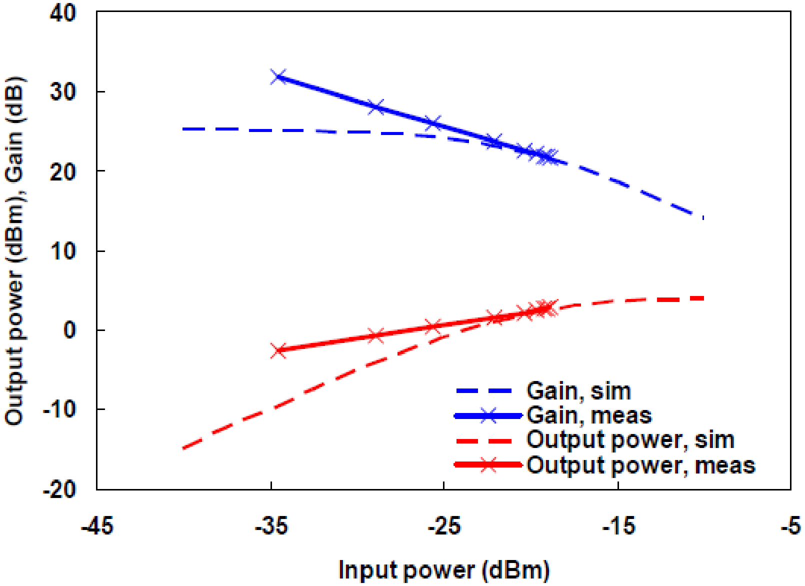
Teledyne: 1.9 mW, 585 GHz Power Amplifier

M. Seo *et al.*, Teledyne Scientific: IMS2013

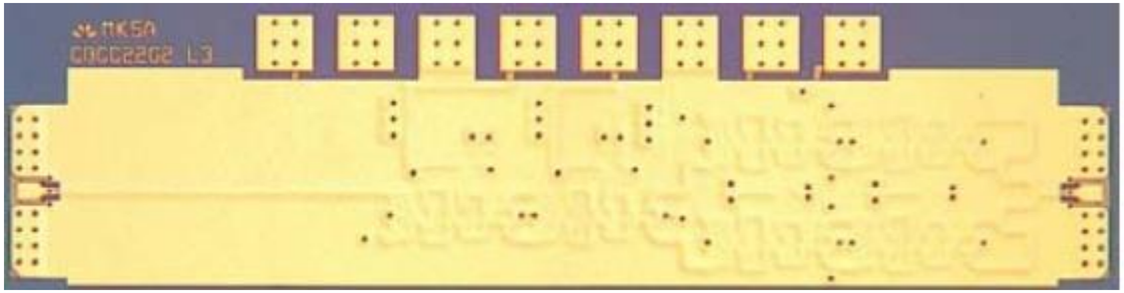
S-parameters



Output Power



- 12-Stage Common-base
- 2.8 dBm P_{sat}
- >20 dB gain up to 620 GHz



What limits output power in sub-mm-wave amplifiers ?

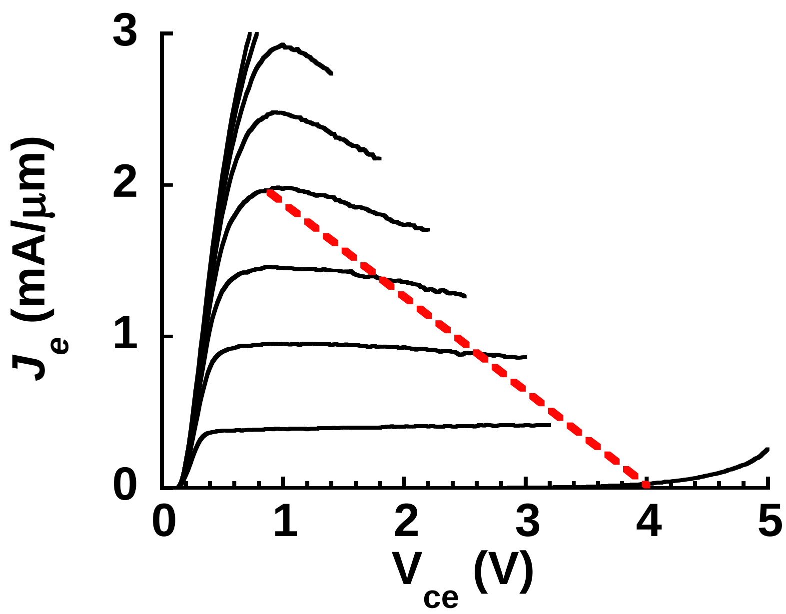
Sub-mm-wave PAs: need more current !

3 μm max emitter length (> 1 THz f_{max})
2 mA/μm max current density
I_{max}= 6 mA

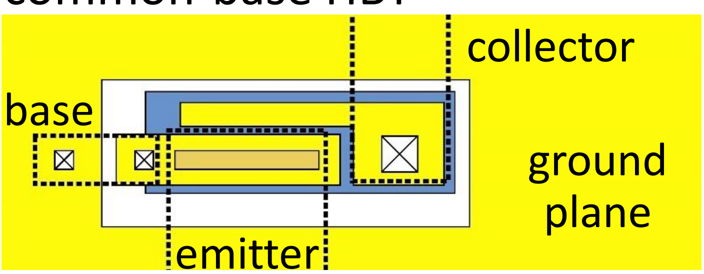
Maximum 3 Volt p-p output

Load: 3V/6mA= 500 Ω

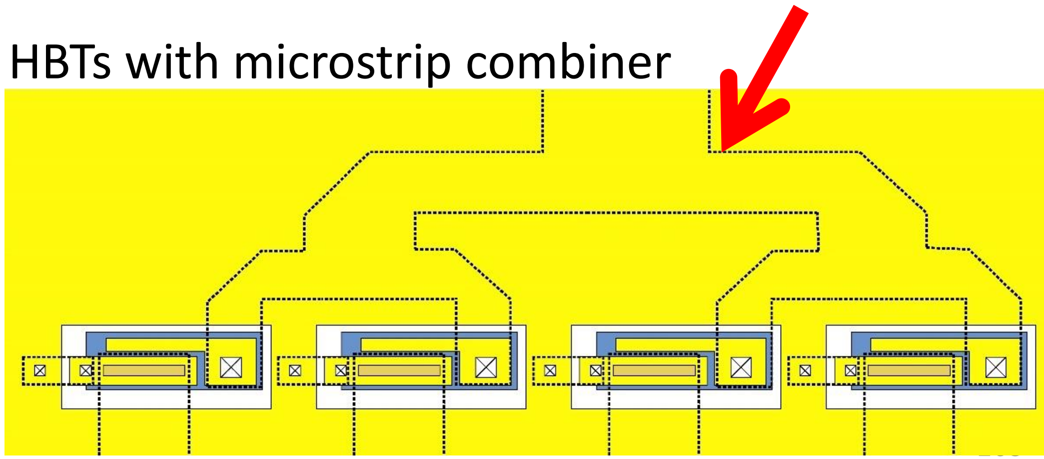
Combiner cannot provide 500 Ω loading



common-base HBT



HBTs with microstrip combiner



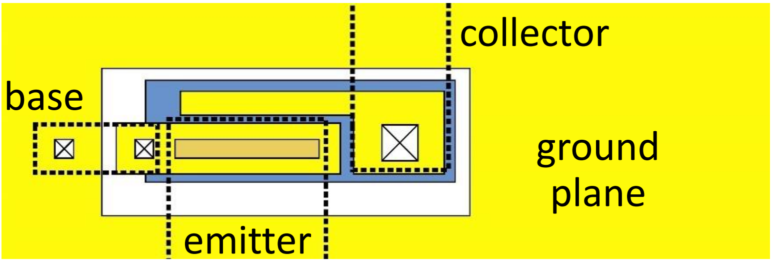
Multi-finger HBTs: more current, lower f_{max}

More current
→ lower cell load resistance

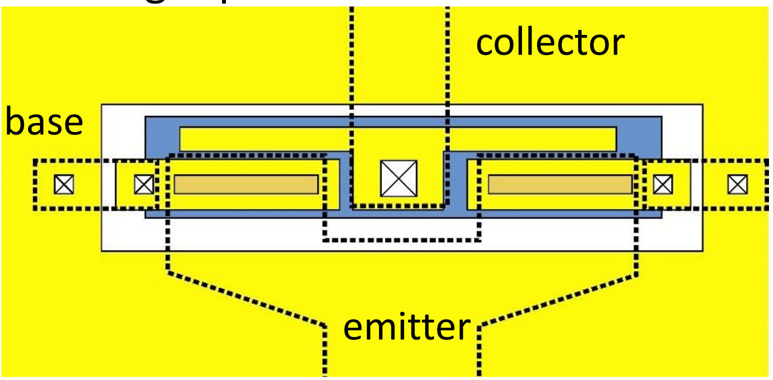
Reduced f_{max}, reduced RF gain:
common-lead inductance→ Z_{12}
feedback capacitance→ Y_{12}
phase imbalance between fingers.

Worse at higher frequencies:
less tolerant of cell parasitics
less current per cell
higher required load resistance
Can optimum load be reached ?

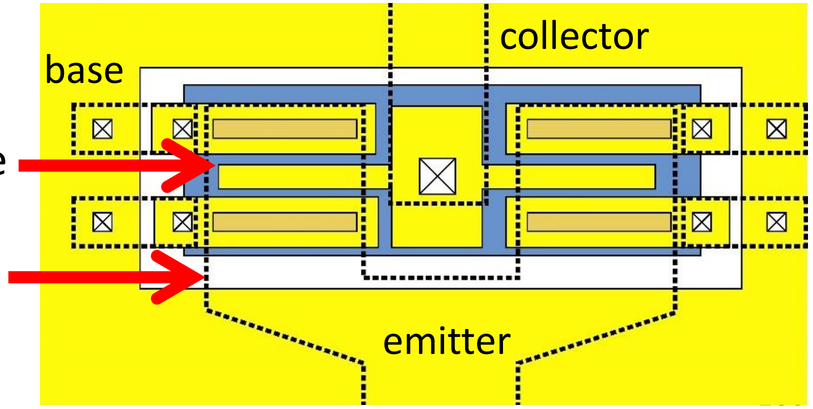
one-finger common-base HBT



two-finger power cell

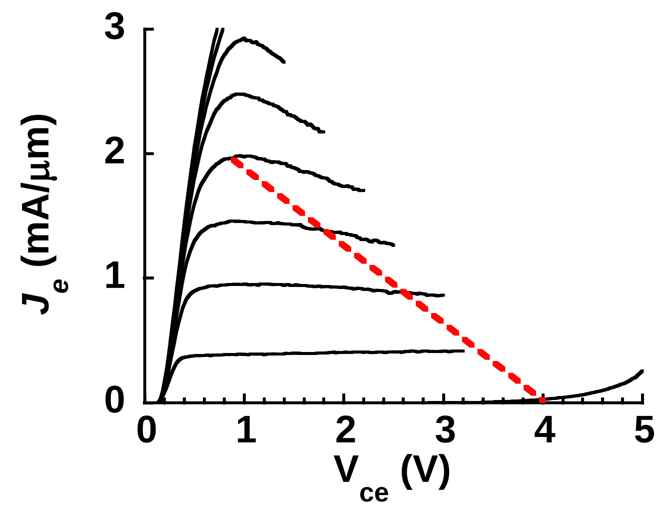


four-finger power cell: ***parasitics***



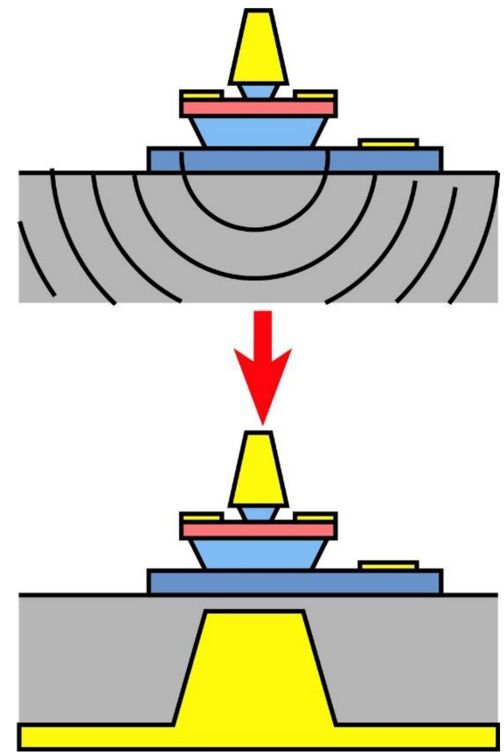
Sub-mm-wave transistors: need more current

InP HBTs:
thinner collector→ more current
hotter→ improve heat-sinking
or: longer emitters→ thicker base metal



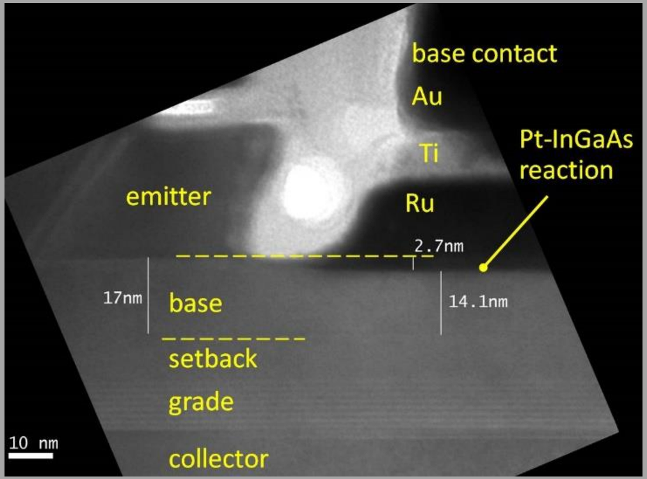
GaN HEMTs:
much higher voltage
100+ GHz: large multi-finger FETs not feasible
Need high current to exploit high voltage.

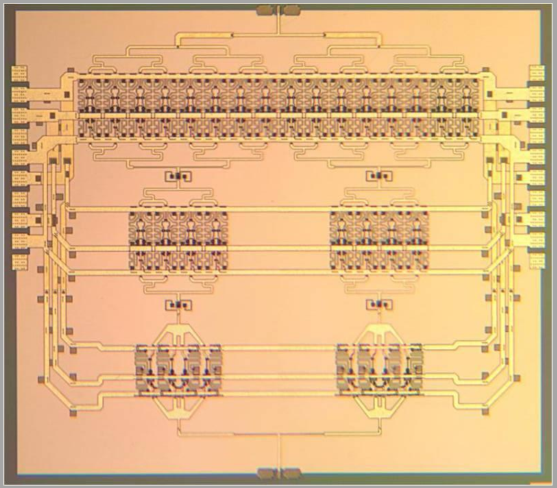
Example:
2mA/µm, 100 µm max gate width, 50 Volts
200mA maximum current
50 Volts/200mA= 250 Ω load→ unrealizable.

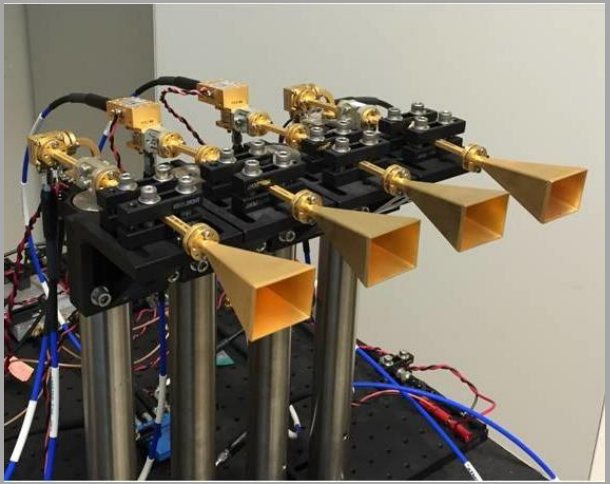


Need more mA/µm or longer fingers

50-500GHz Wireless





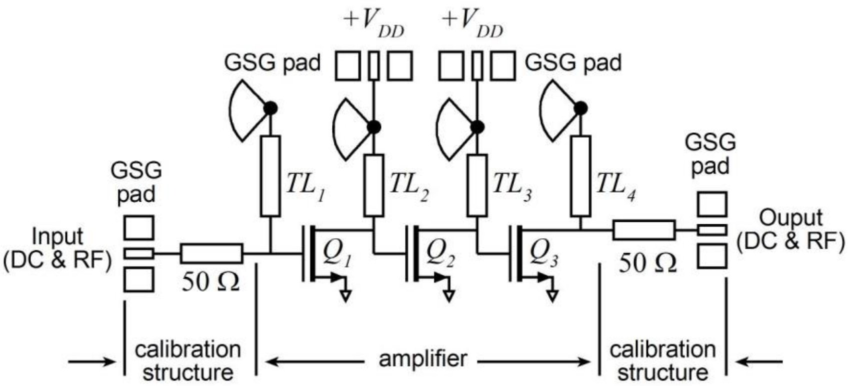


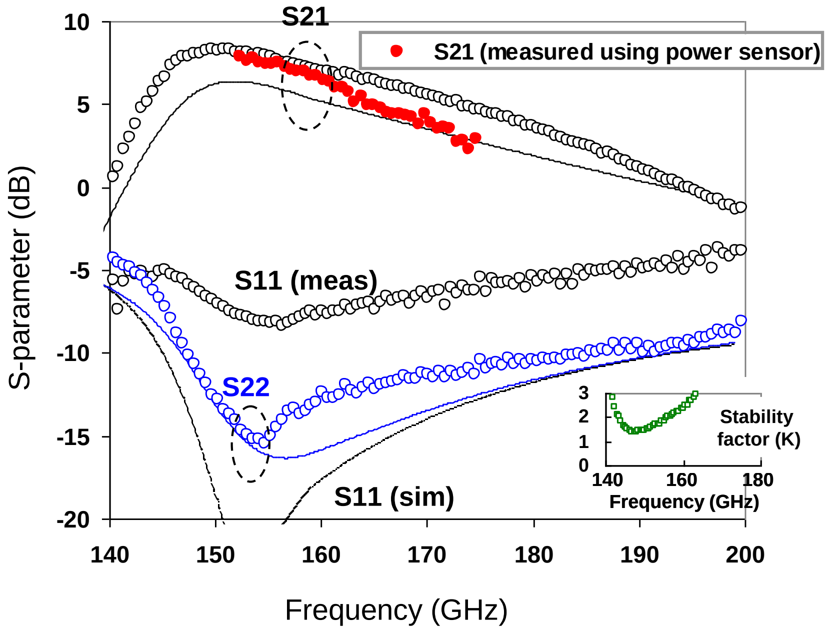
IC example: 150 GHz CMOS amplifier

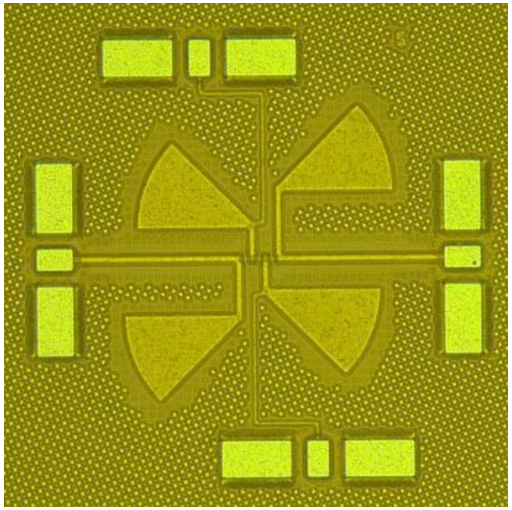
3-stage 150-GHz Amplifier; IBM 65 nm CMOS

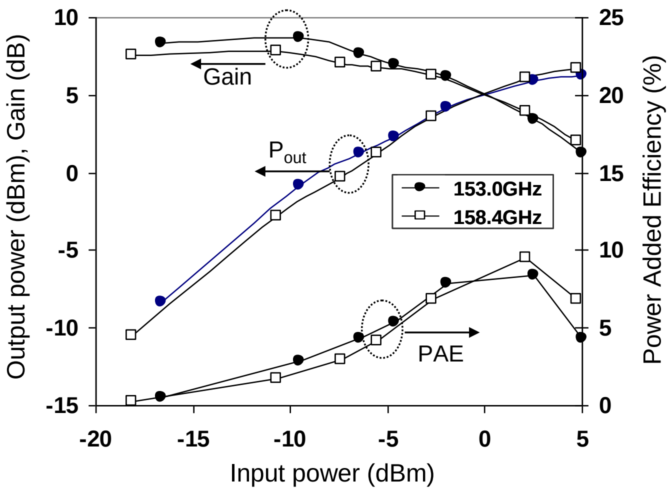
Acknowledgement: IBM

M. Seo, B. Jagannathan, J. Pekarik, M. Rodwell, IEEE JSSCC, Dec. 2009

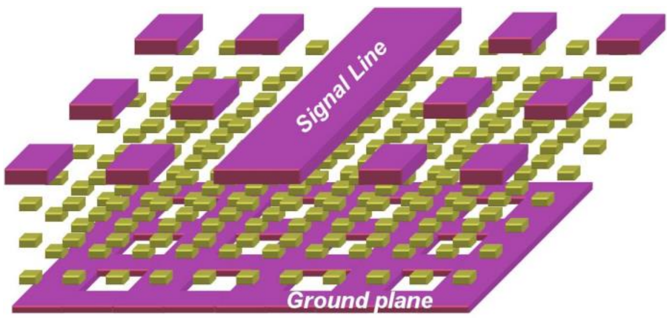




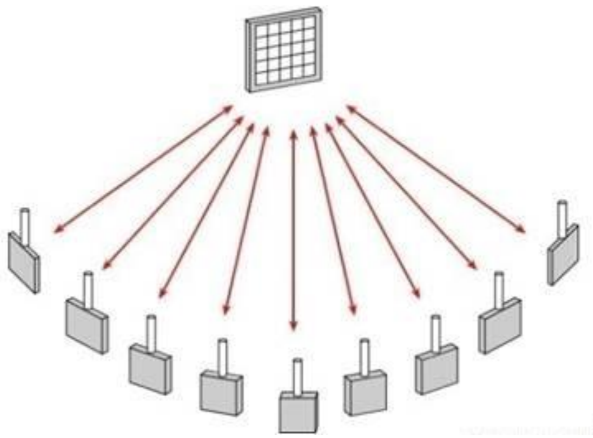


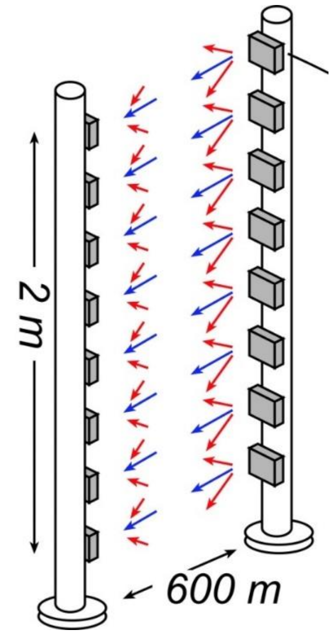


Dummy-prefilled microstrip lines



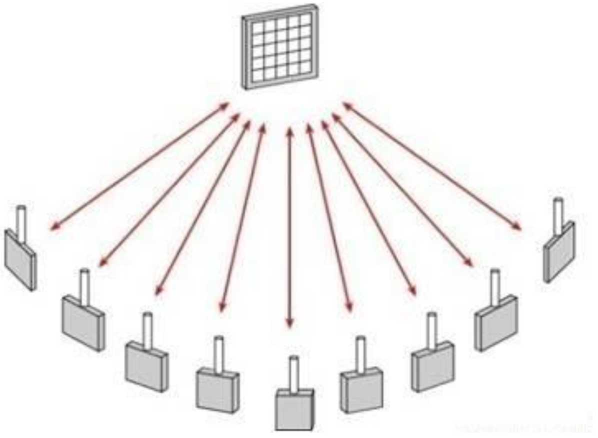
IC example: 140 GHz spatial multiplexing



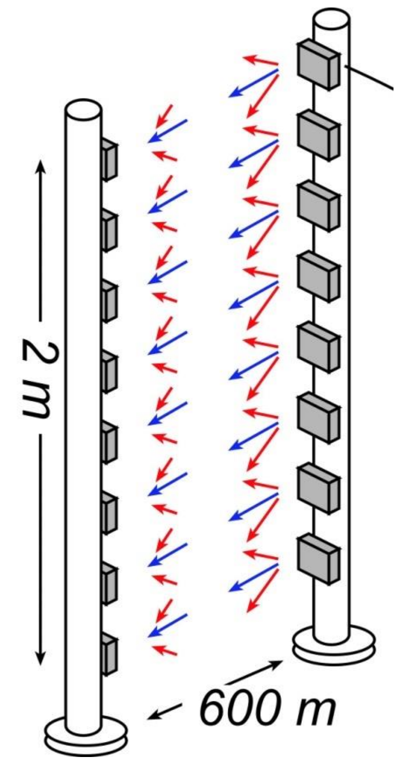


Massive Spatial Multiplexing

Two applications:



Spatially multiplexed networks
multiple independent beams
carrying independent data
→ spectral re-use for massive capacity



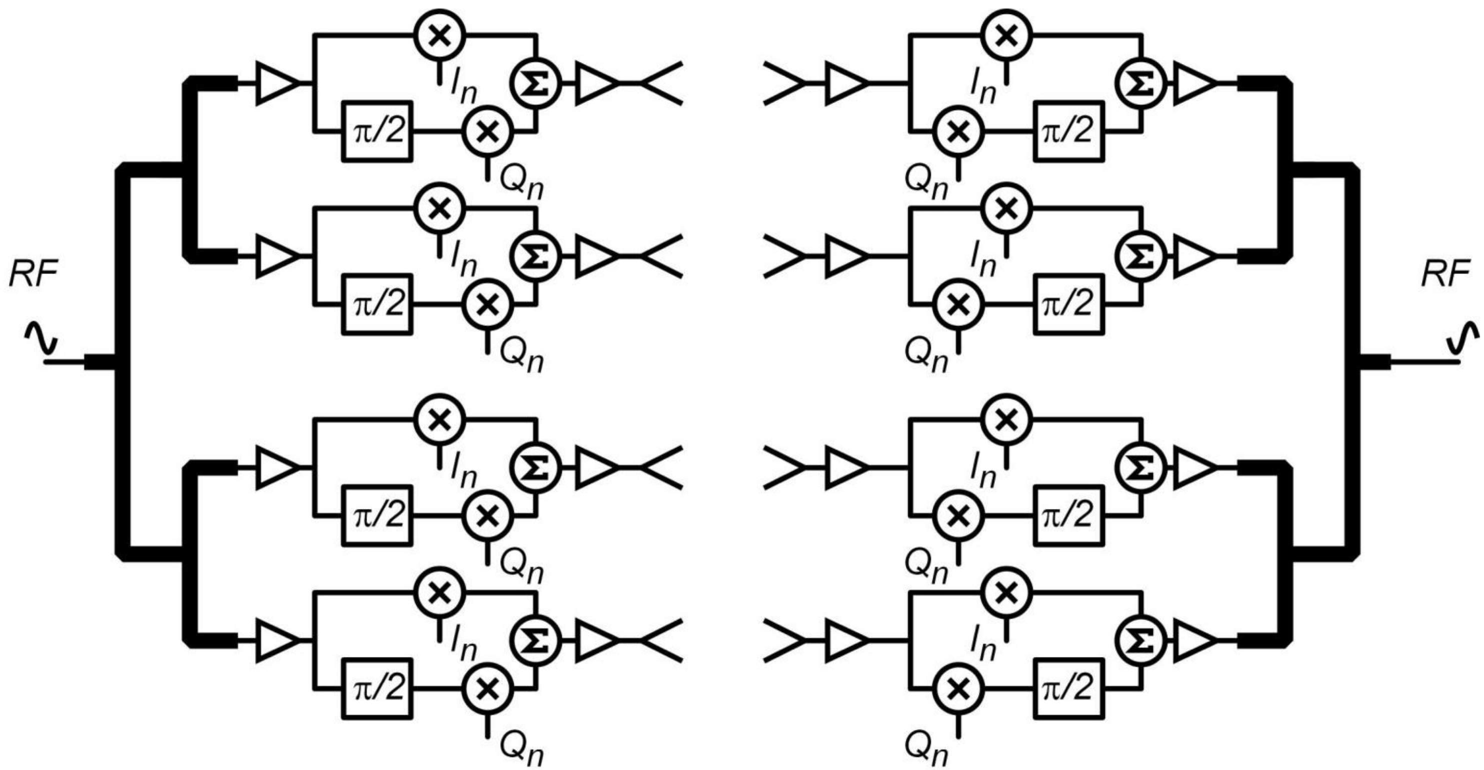
mm-wave line-of-sight MIMO
spatial multiplexing
for increased capacity

These use similar signal processing hardware

Arrays for single-beam links

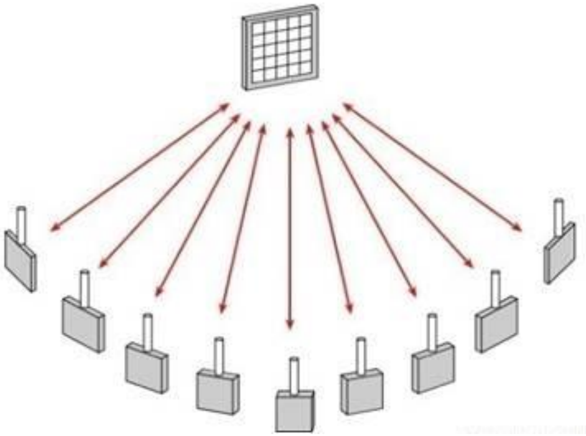
Single-beam arrays:
steerable, high gain, for mm-wave links.

Simple hardware:
one RF port for IC, one phase-shifter for each element

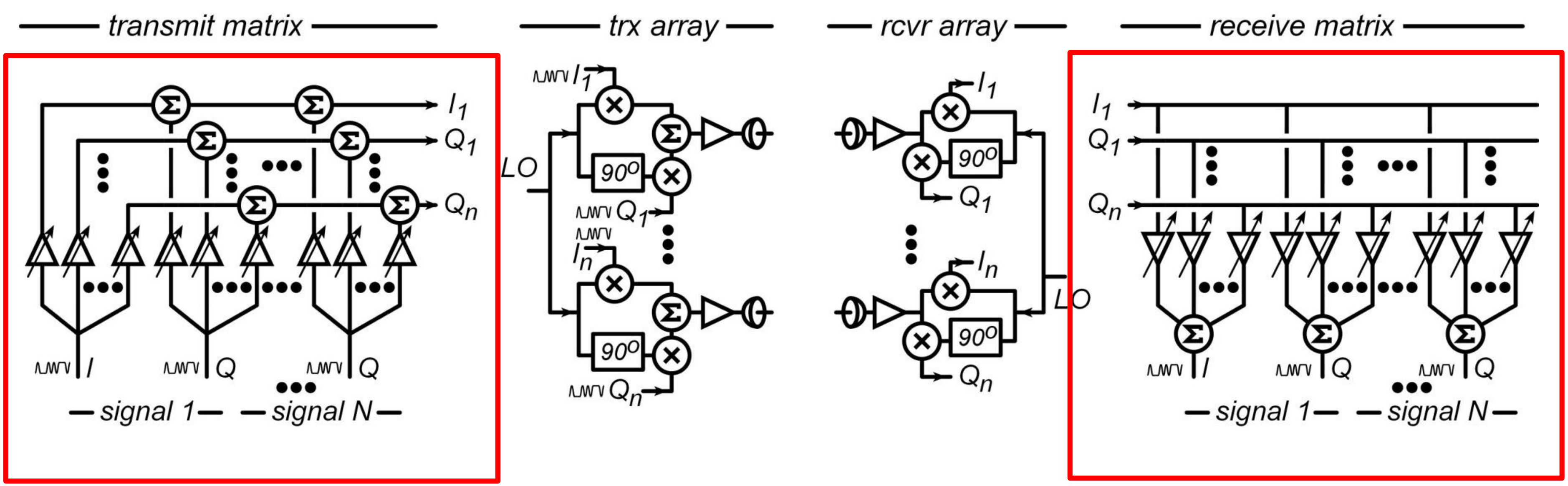


Multi-beam links: hardware design

multiple independent beams
- each carrying different data
- each independently aimed
- # beams = # array elements



Hardware: multi-beam phased array ICs



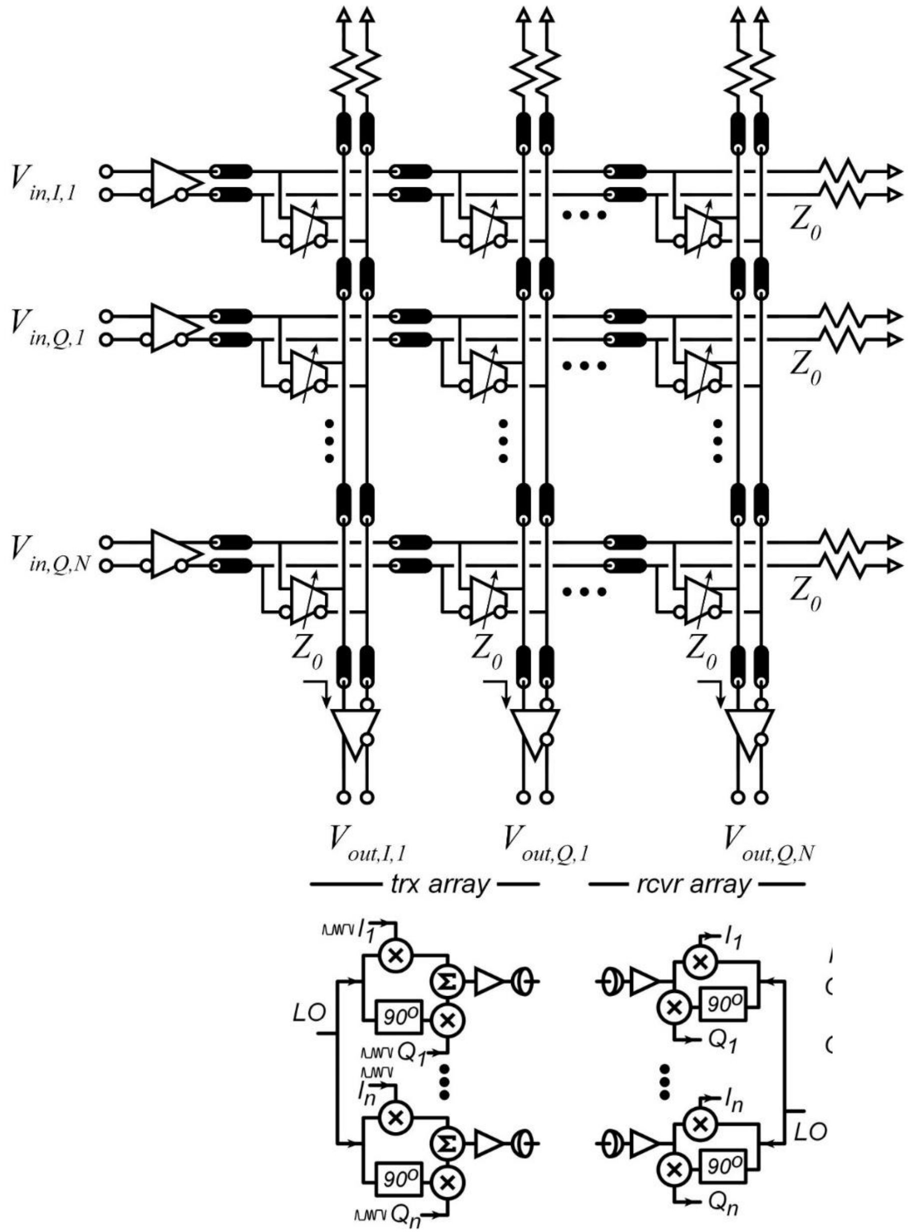
Multi-Beam Links: Analog Beamformer Matrix

I/Q matrix at baseband

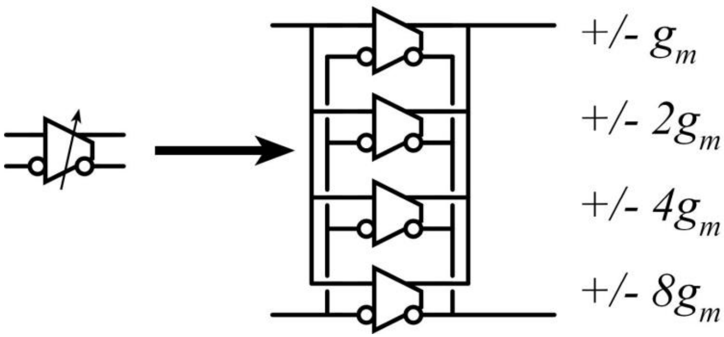
varying coefficients
→ track/aim beams

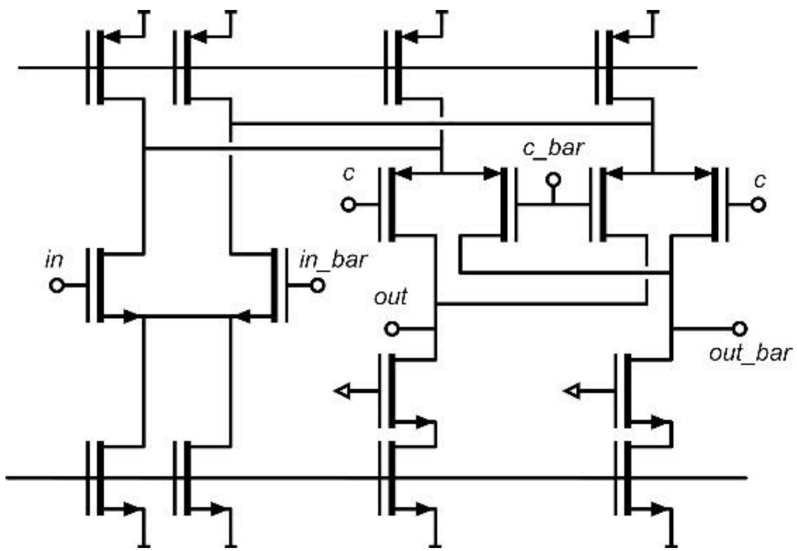
Designs: March tapeout
GF (ex IBM) 45nm SOI
16 beams: 32 x 32 matrix
1024 matrix elements
area: 2.25 mm^2
power: 2.25W
bandwidth: ~5 GHz ?
aggregate ~160 Gb/s.

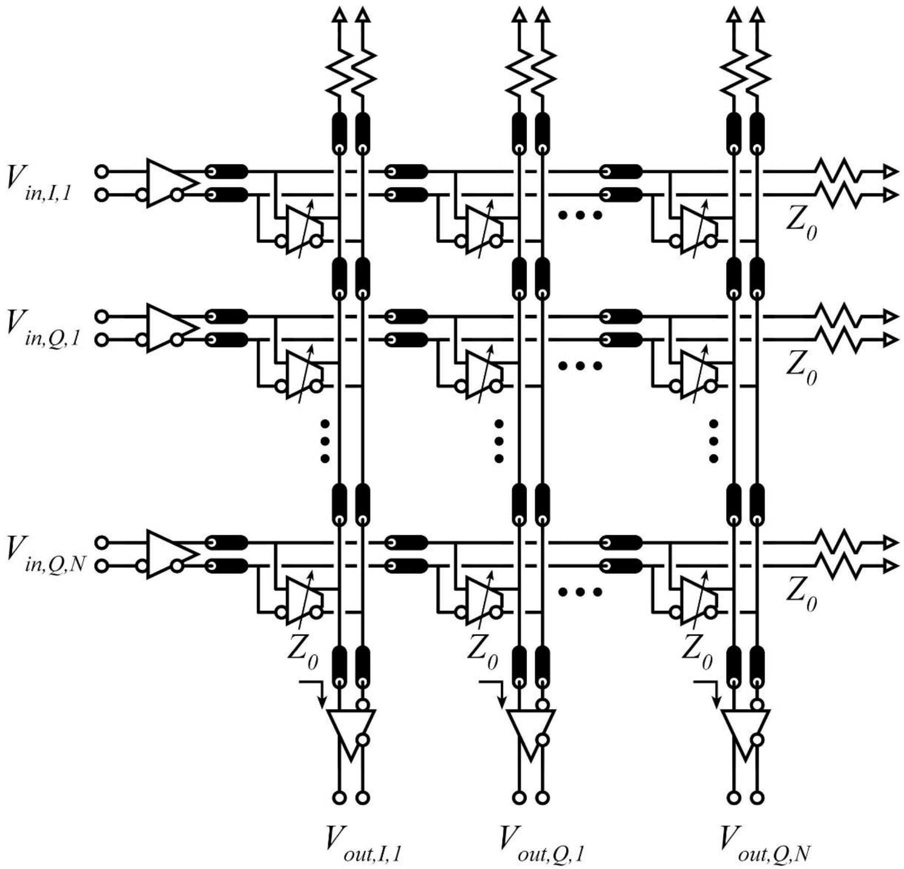
Also for tapeout
140 GHz front-ends for these



Multi-Beam Links: Analog Beamformer Matrix







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I/Q matrix at baseband

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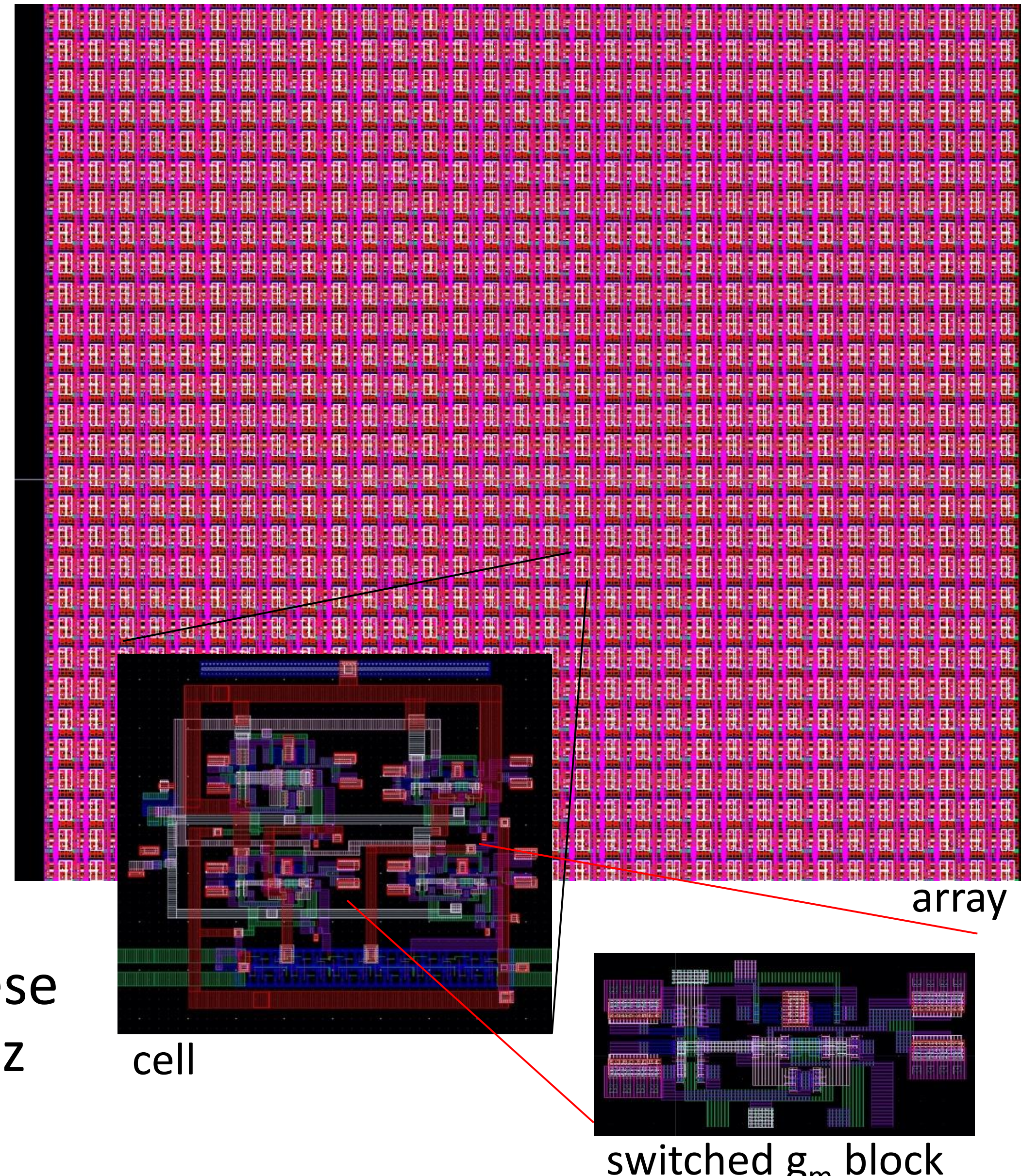
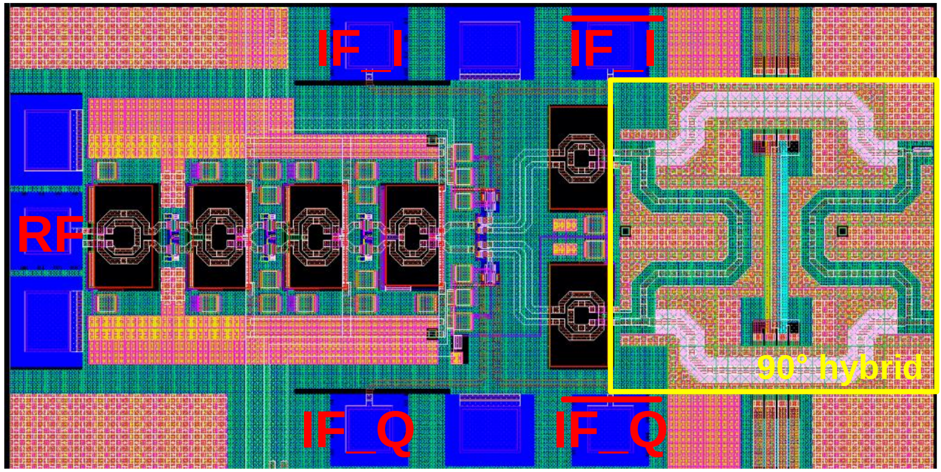
16 beams: 32 x 32 matrix
1024 matrix elements
area: 2.25 mm^2
power: 2.25 W
bandwidth: ~5 GHz ?
aggregate ~160 Gb/s.

Also for tapeout
140 GHz front-ends for these
later: RF for 38GHz, 60 GHz

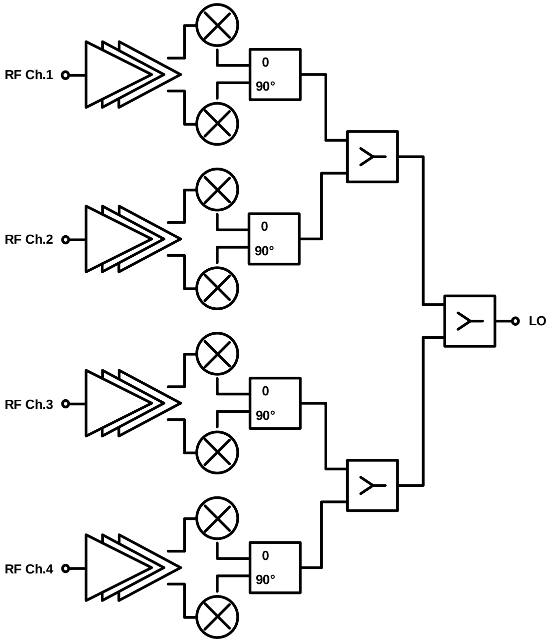


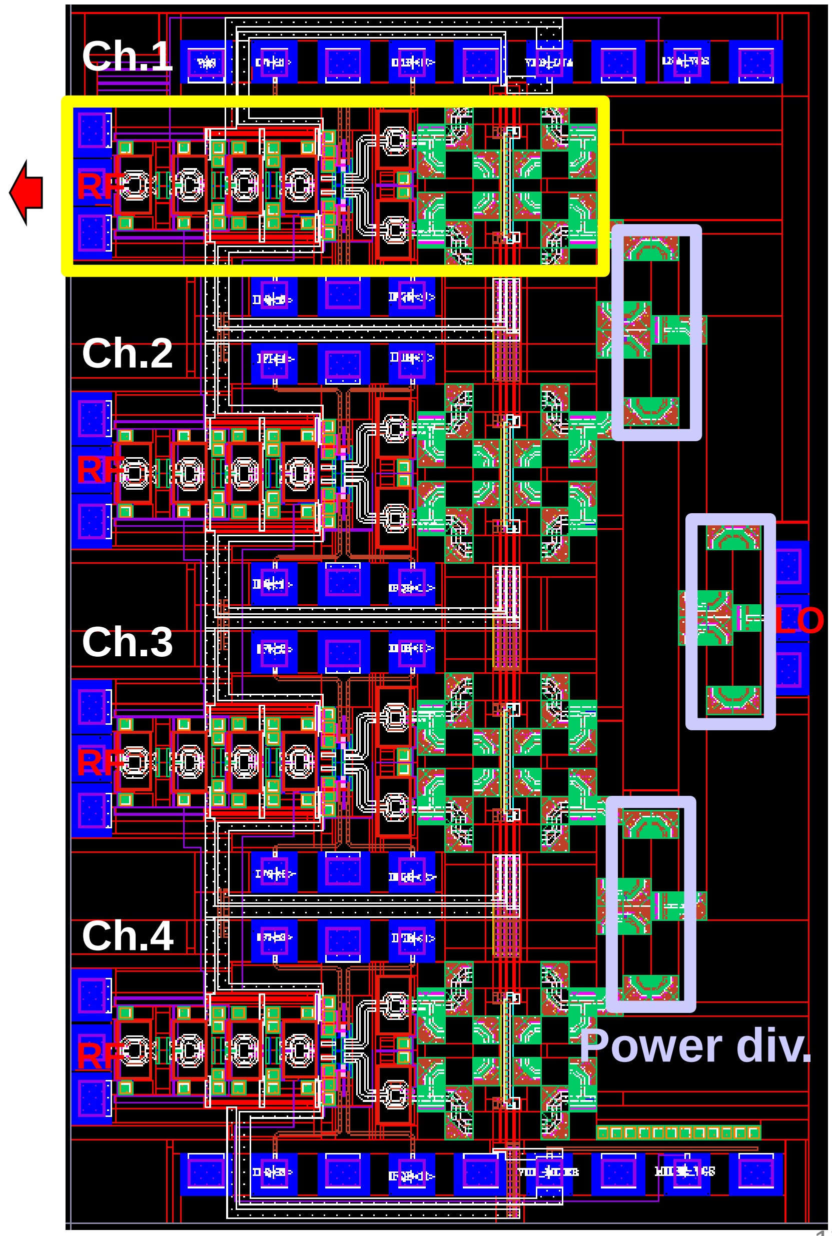
140 GHz MIMO receiver front-end

Size: 1075 x 1760 um²



Single-channel layout



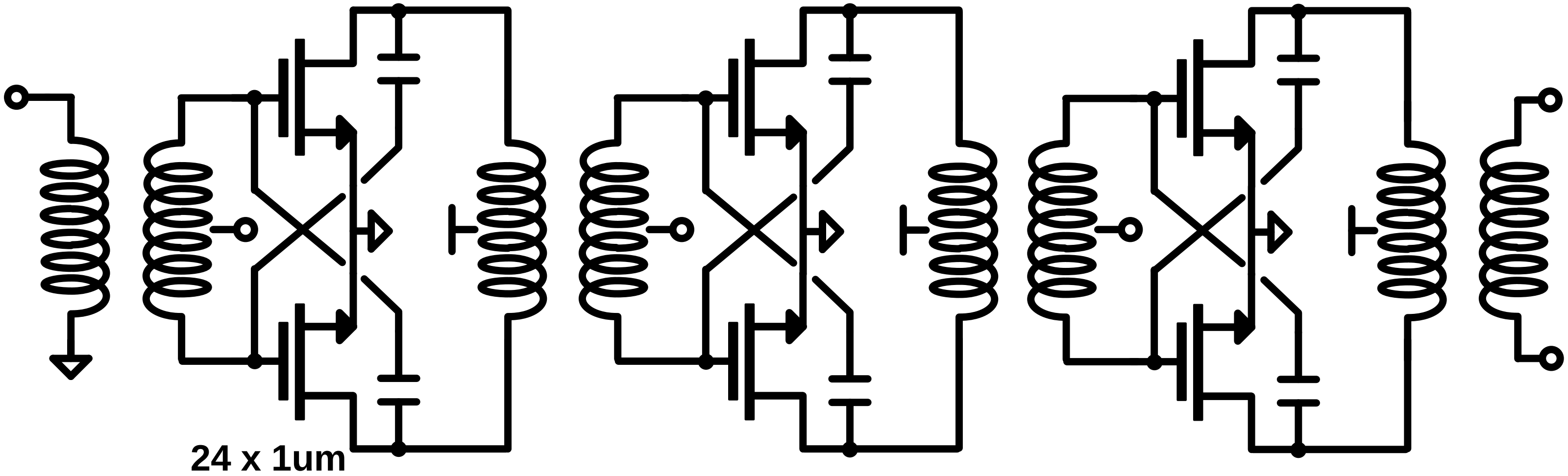


Single-ended vs differential

	Single-ended	Differential
Gain	-	-
Power consumption	Low	High
Design complexity	Low	High (Balun is required)
Isolation (S12) & Stability	Low	High (C_{gd} cancellation)
Power supply (VDD & VSS) immunity	Poor	Good

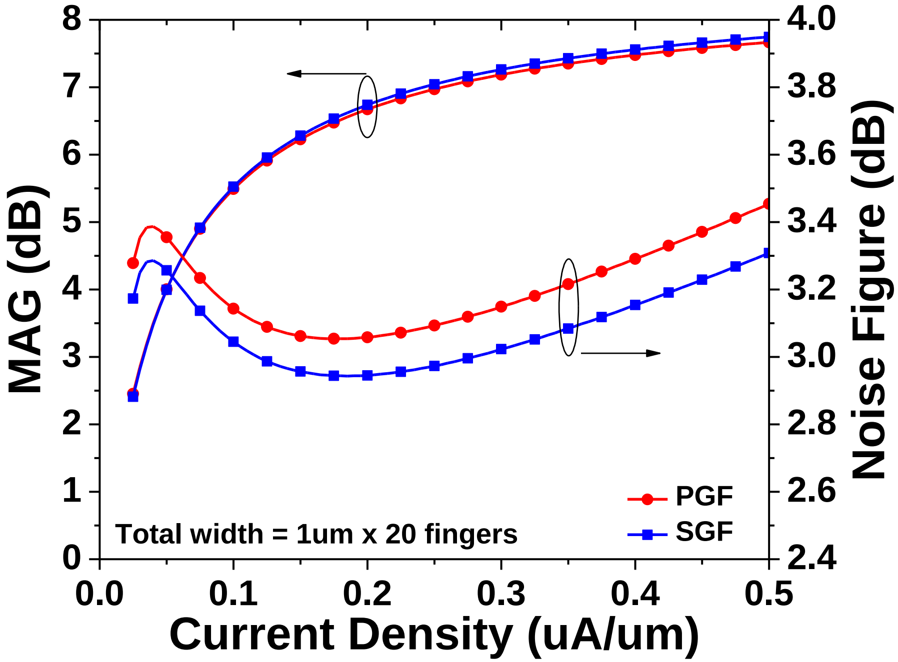
Power supply immunity is critical → differential structure

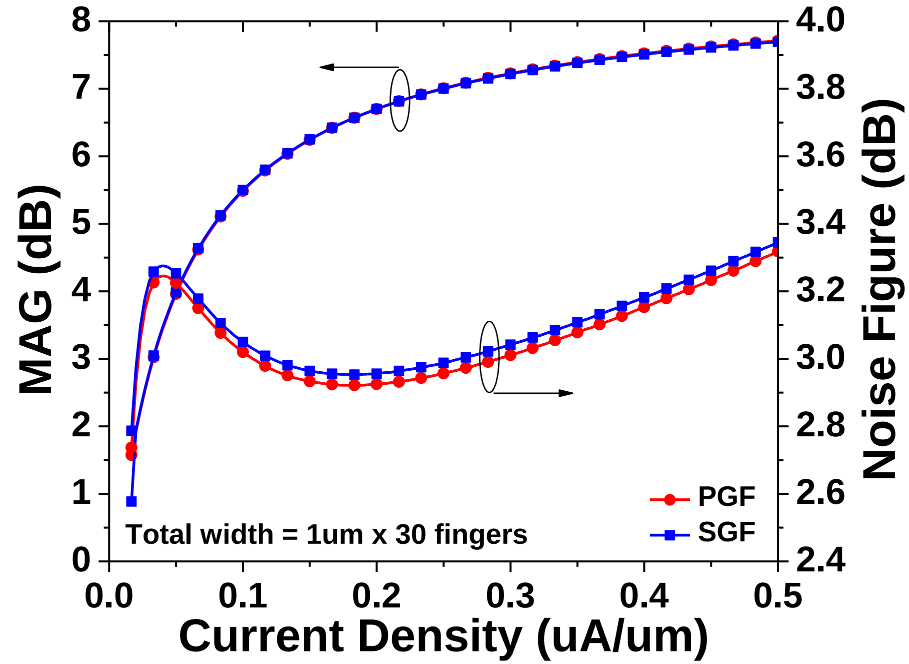
Low noise amplifier



LNA design:
3-stage differential CS amplifier
C_{gd} cancellation
Transformers for matching networks and sing.-to-diff.

SGF vs PGF



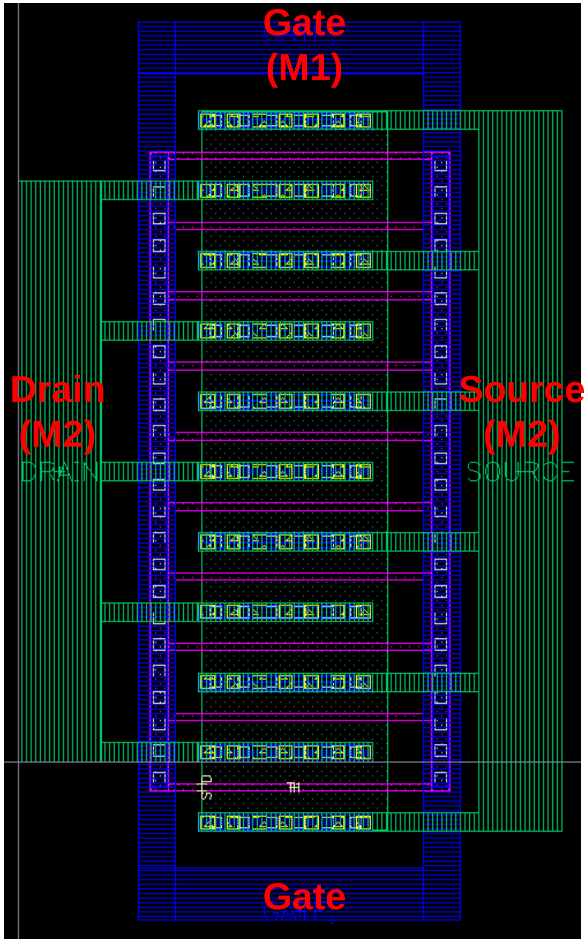


Simulation results includes BSIM model and PEX results

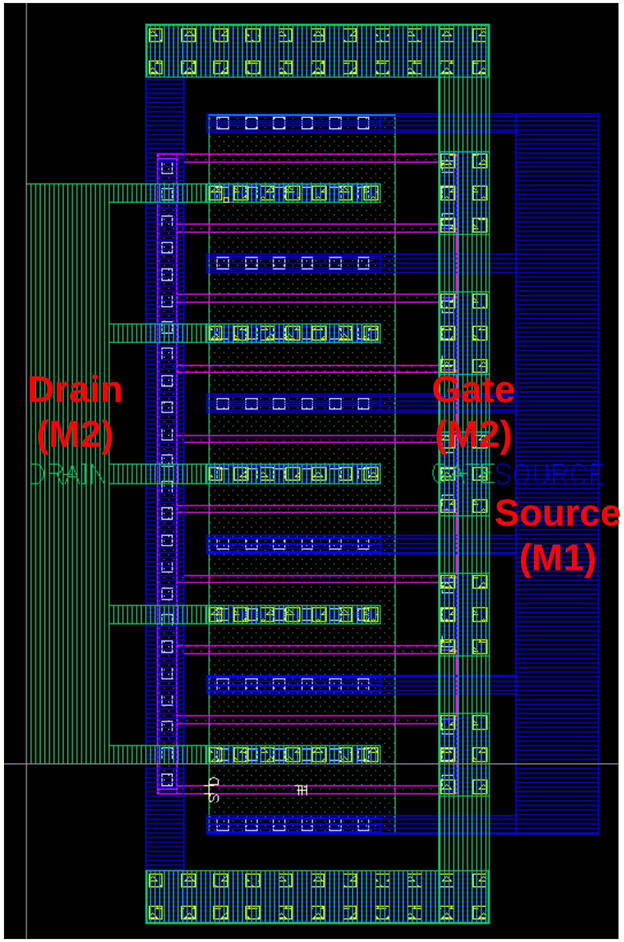
(PEX → capacitance and resistance due to PC, CA and M1)

***PC: poly, CA: connection between poly and metal 1, M1: metal 1**

FET footprint

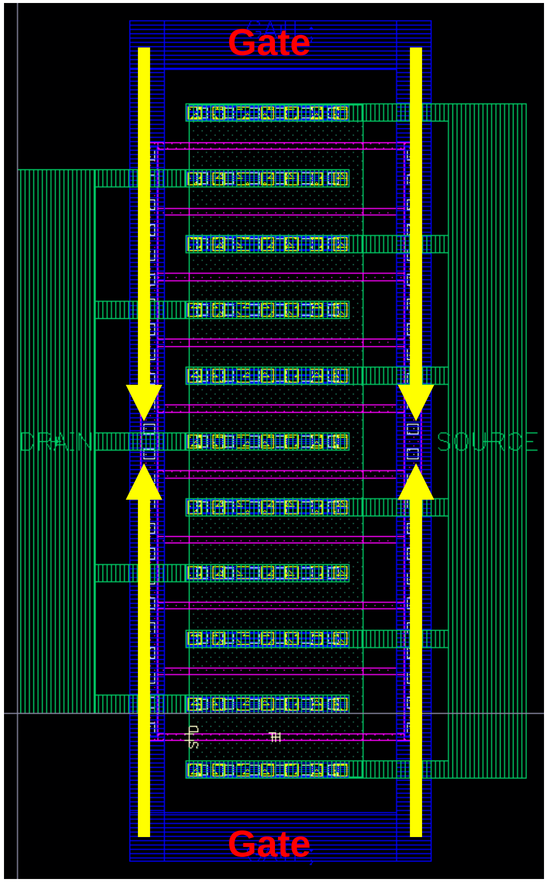


Series gate feeding



Parallel gate feeding

FET footprint - PGF

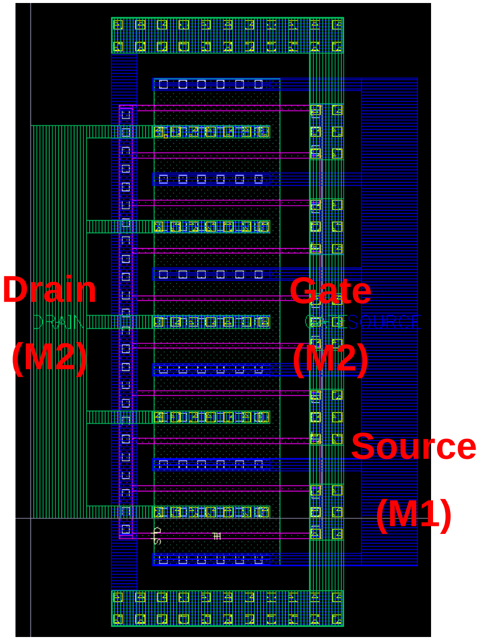


SGF

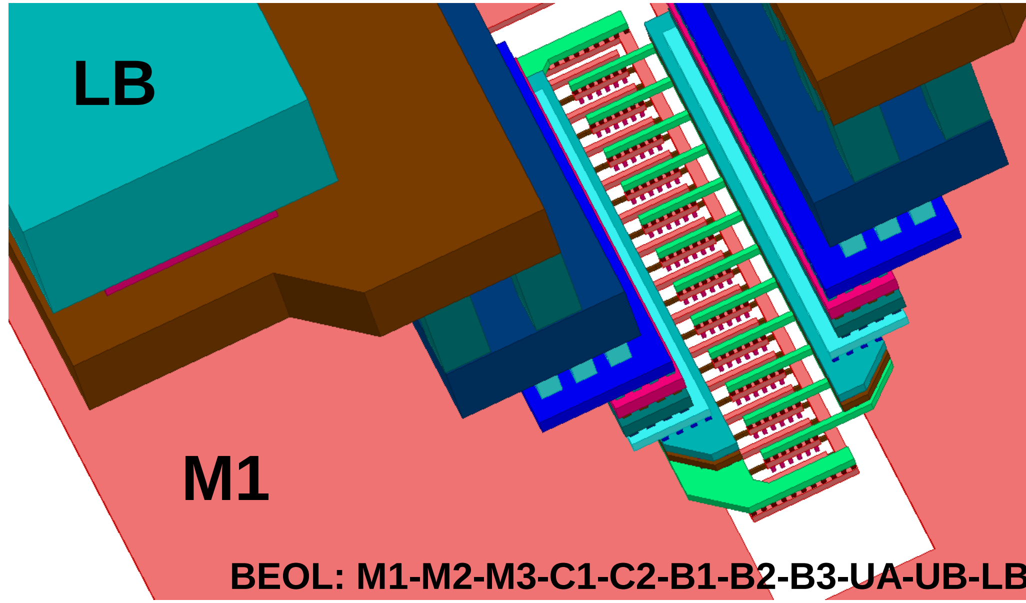
PGF

- **PGF and SGF have similar performances (MSG, NF)**
- **SGF is hard to extract the inductance of the gate feeding line**
- **Source can directly connect to ground (M1 is the ground plane)**

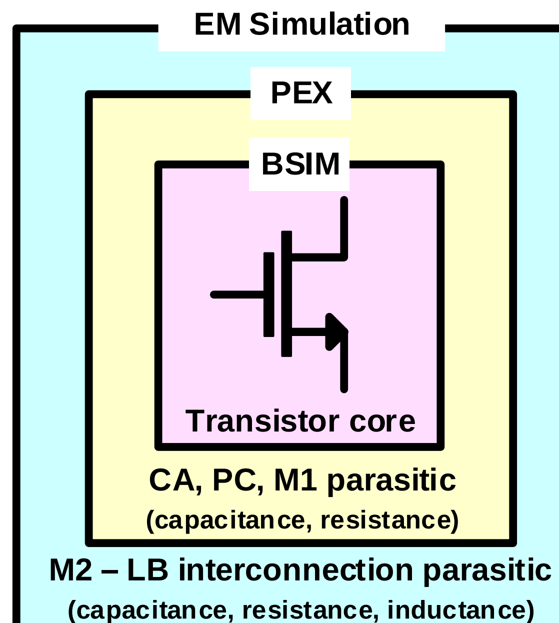
FET modeling



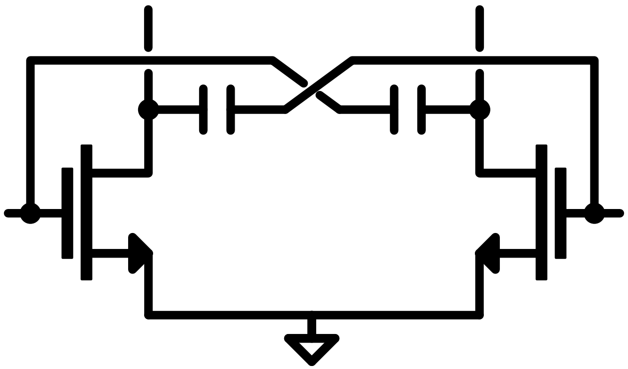
Parallel Gate Feeding

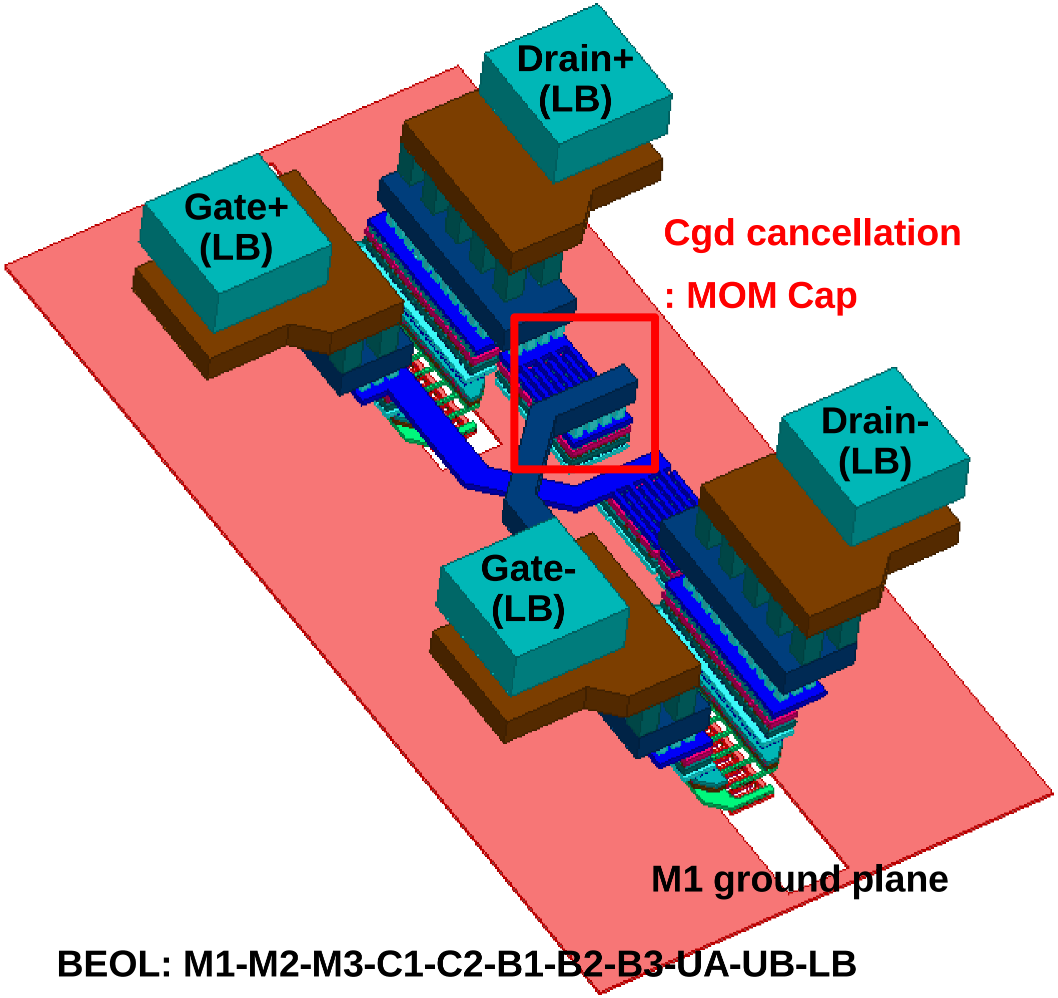


Transistor modeling:
BSIM + PEX + EM simulation
(BSIM & PEX from the foundry)



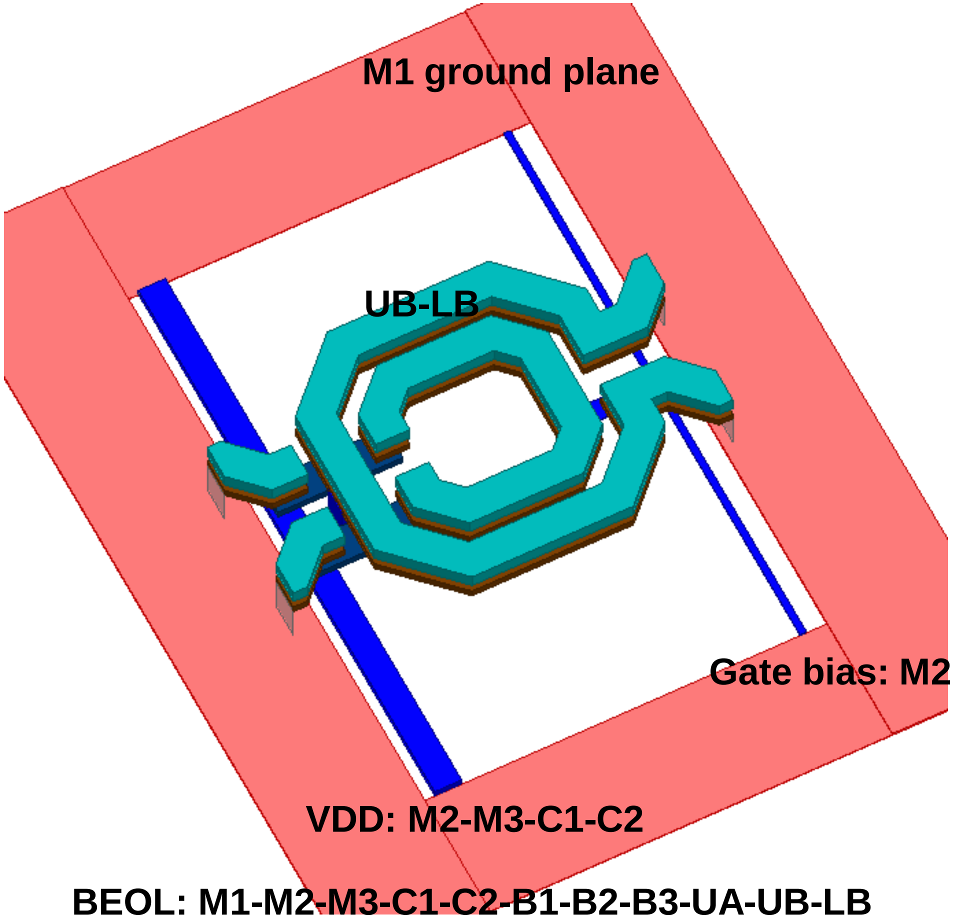
FET differential pair layout





C_{gd} cancellation – better isolation & gain

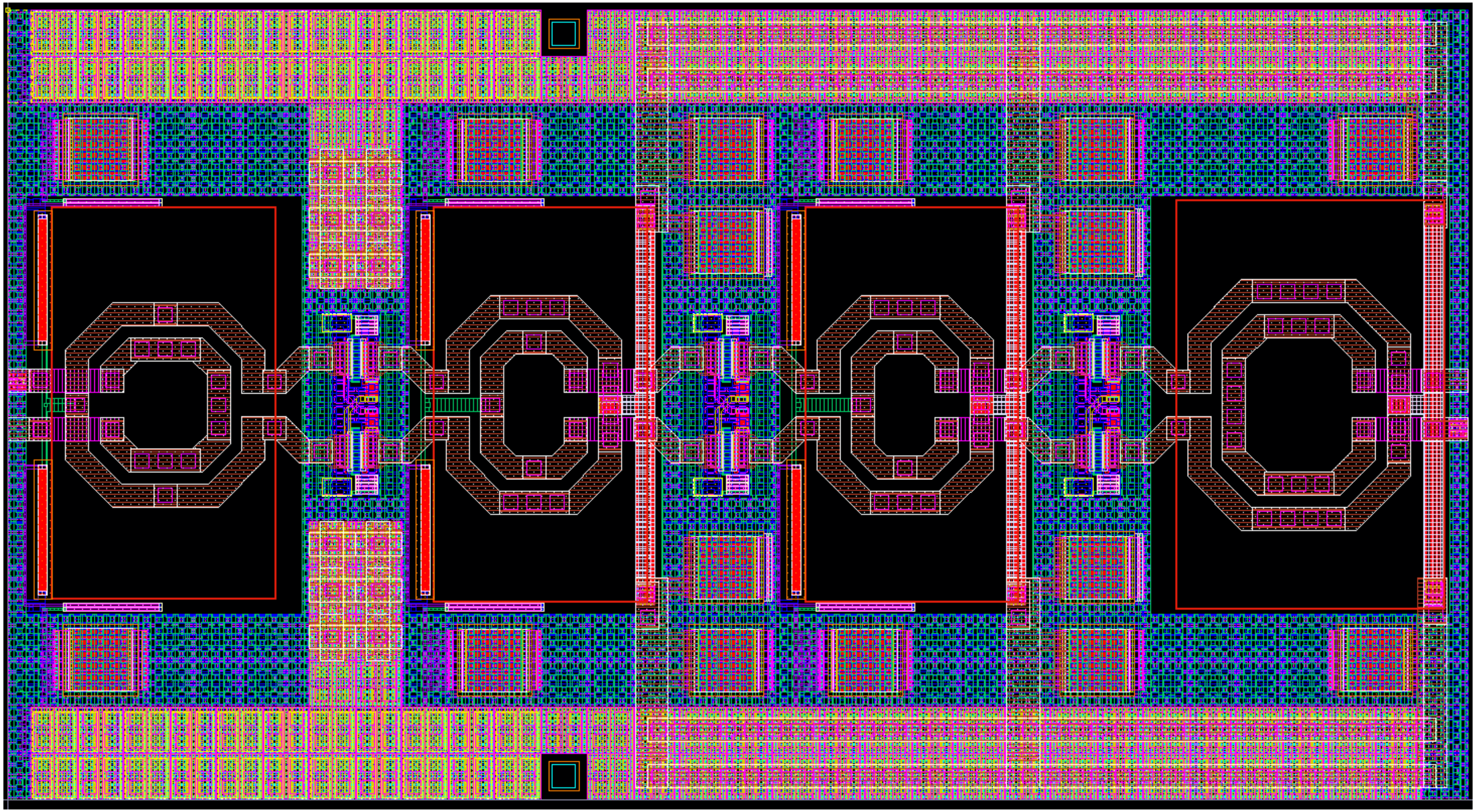
Matching networks



For matching:
Optimize transistor size & transformer diameter

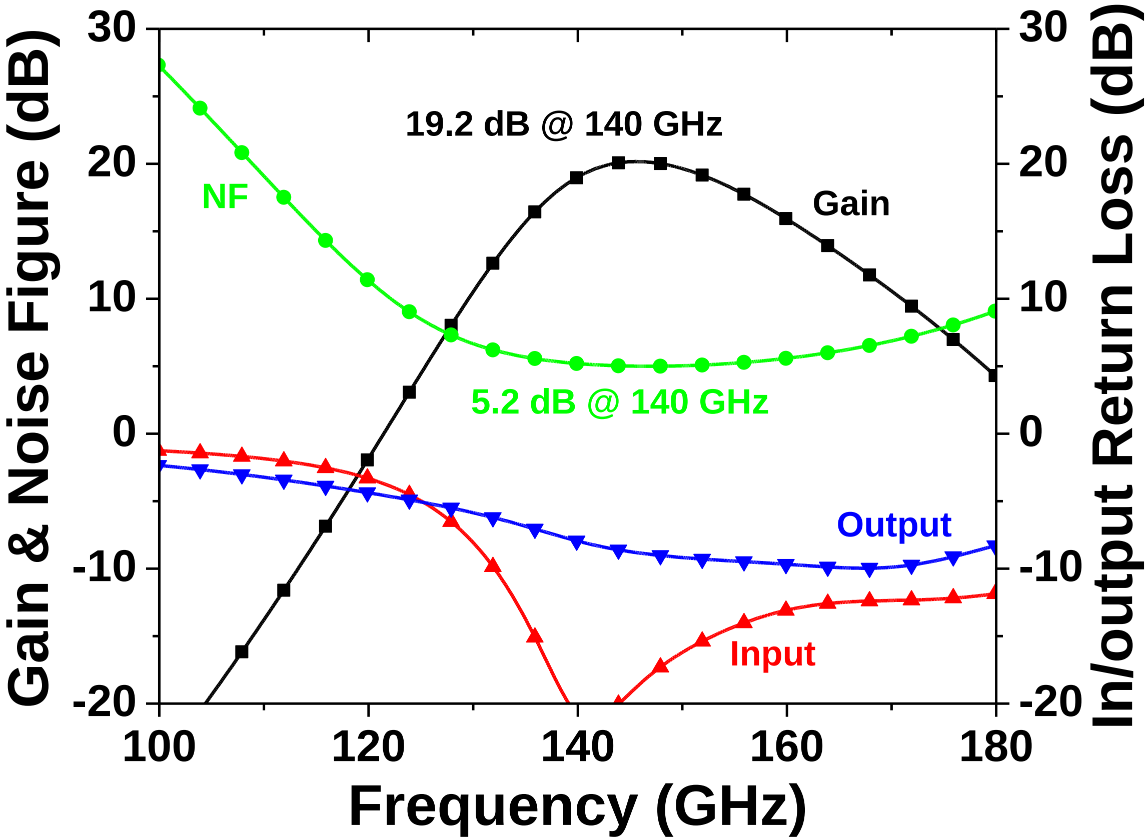
Center-tapped transformer for DC biasing (VDD, VGS)

LNA layout



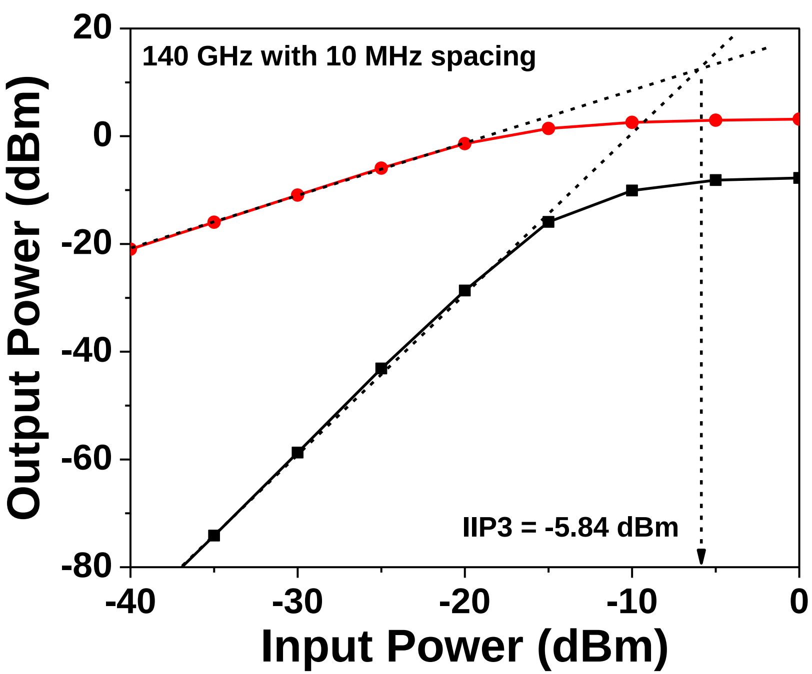
Size: 315 x 170 um^2

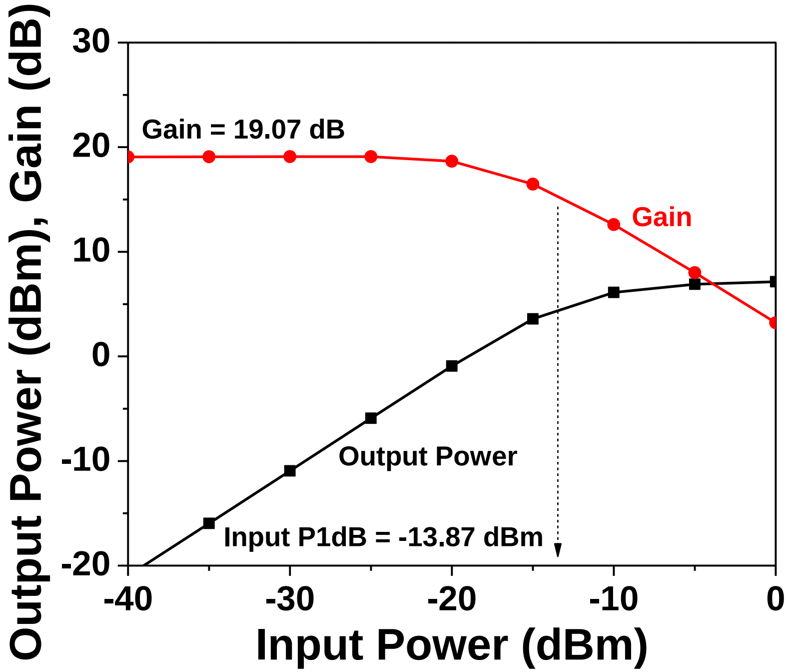
Gain & NF



Gain 19.2 dB (peak gain 20 dB @ 145 GHz)
NF: 5.2 dB

Linearity



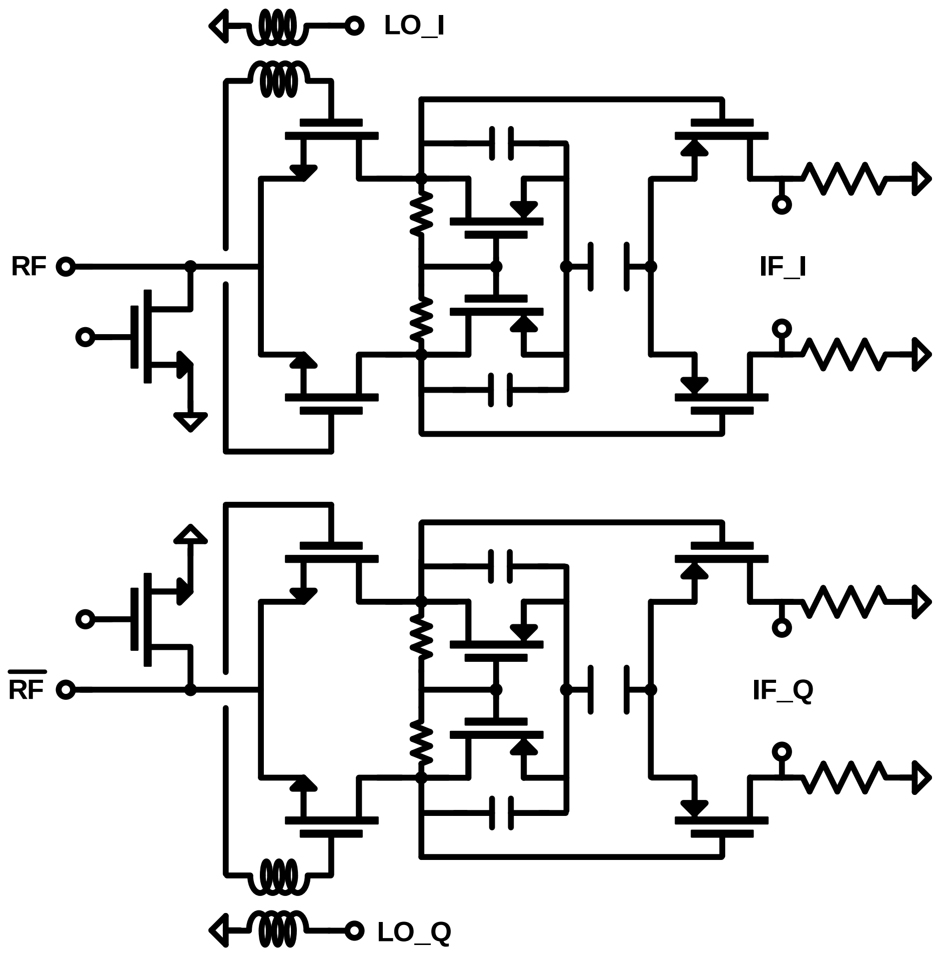


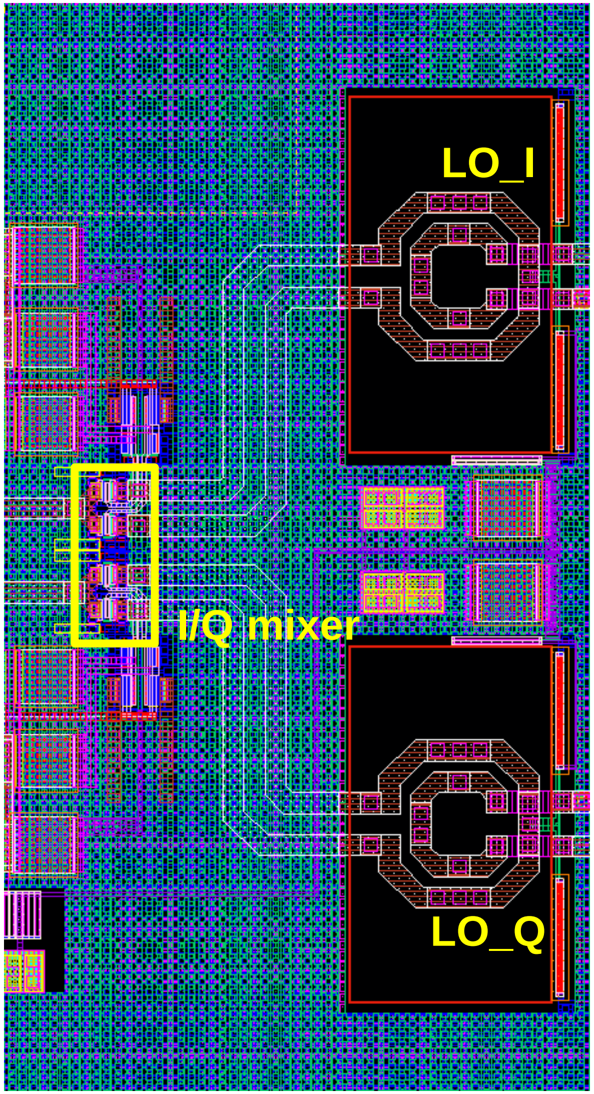
IIP3: -5.84 dBm, Input P1dB: -13.87 dBm

Summary - LNA

Gain	**19.2 dB (Peak 20 dB @ 145 GHz)**
NF	**5.2 dB**
IIP3	**-5.8 dBm**
Input P1dB	**-13.87 dBm**
Power consumption	**41 mA @ 1 V**
Size	**315 x 170 um^2**

Down-conversion mixer

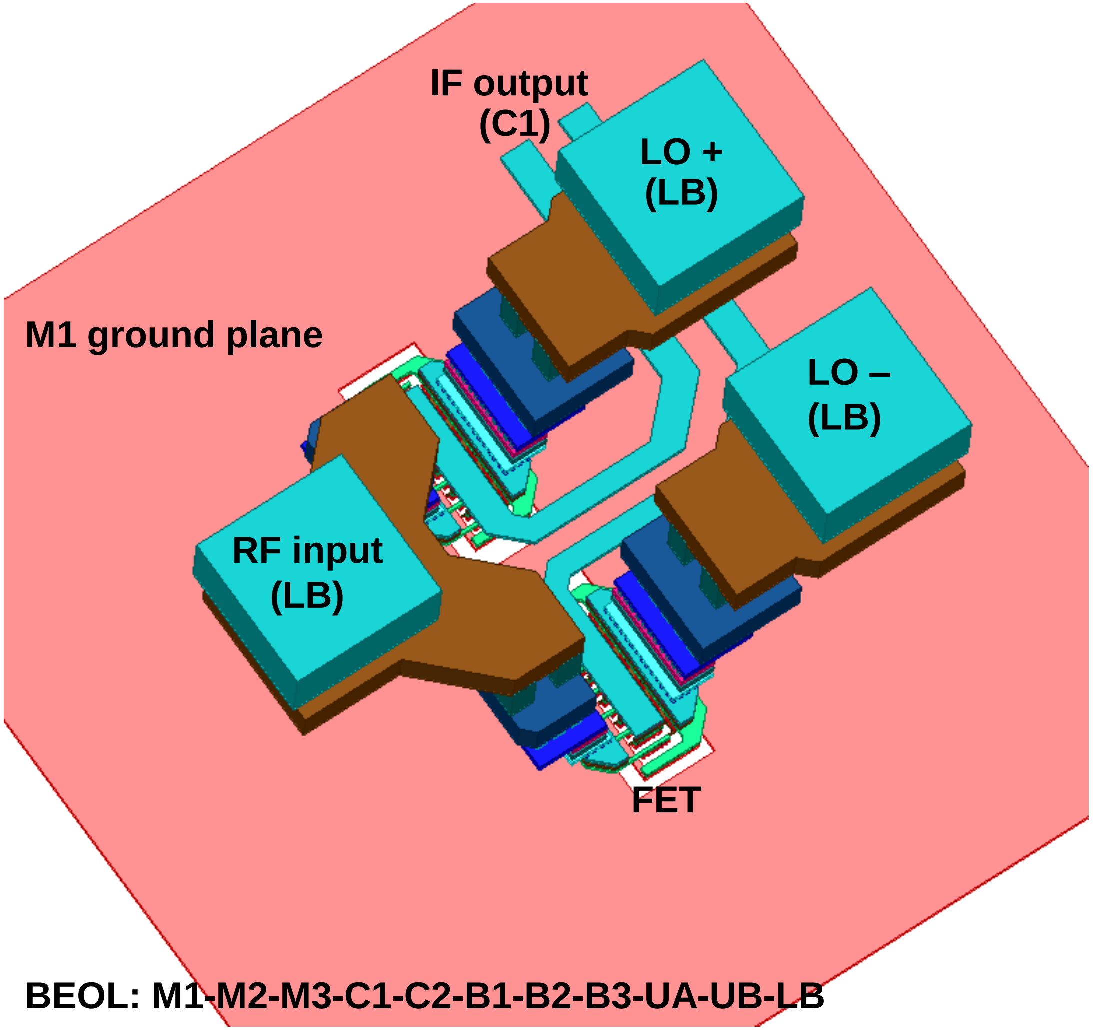




Size: 140 x 230 um^2

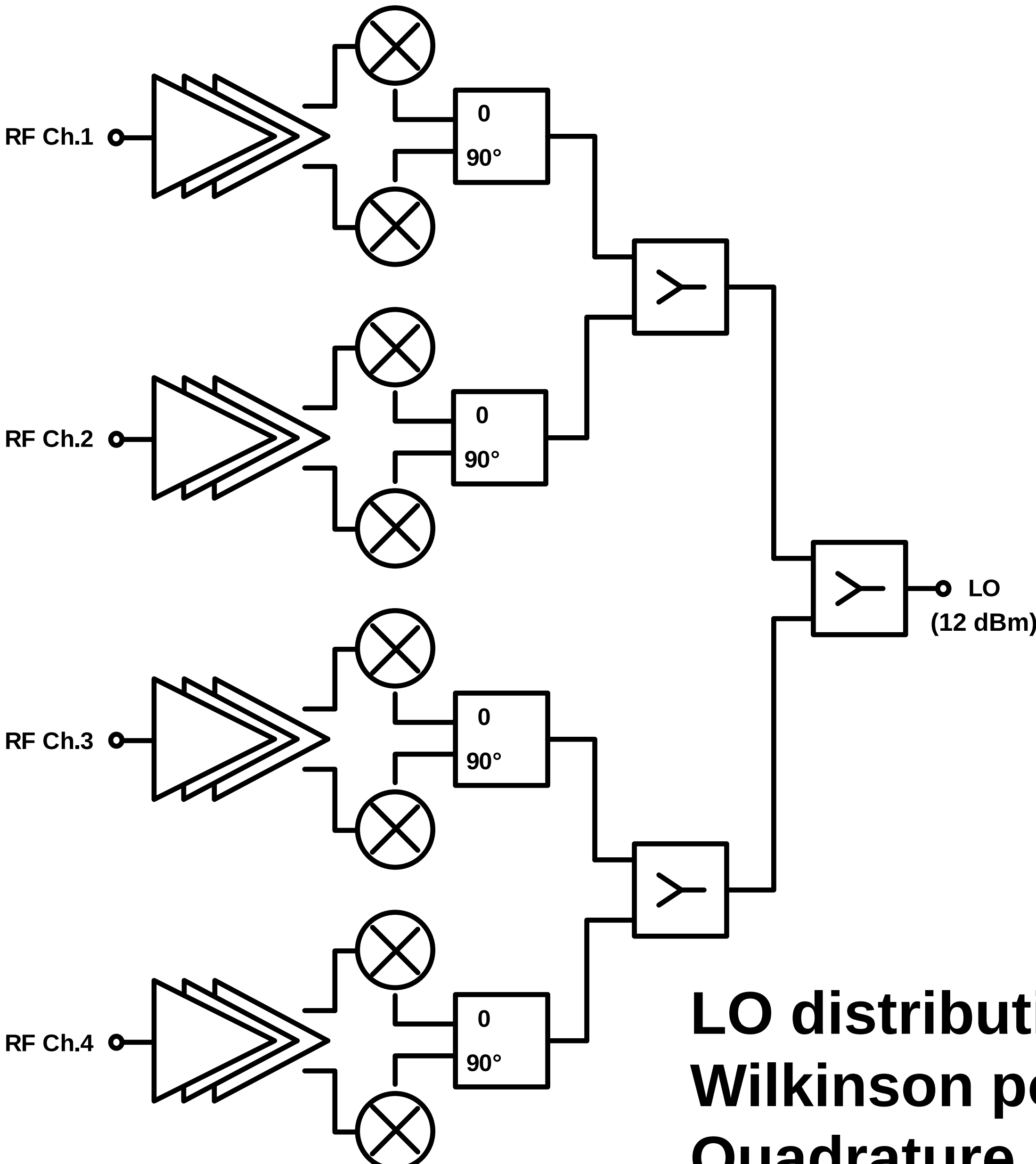
Mixer design:
Single-balanced active I/Q mixer
CS buffer for testing (buffer gain ≈ 1)

Mixer core layout



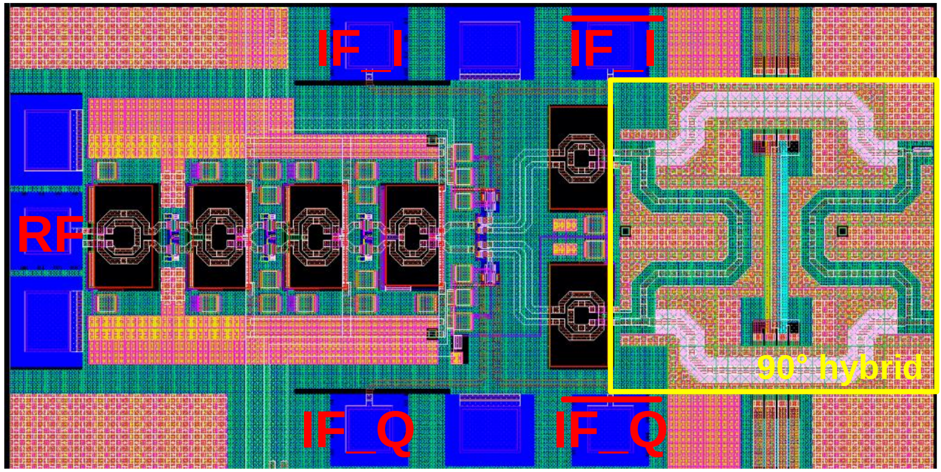
BEOL: M1-M2-M3-C1-C2-B1-B2-B3-UA-UB-LB

Four-channel receiver

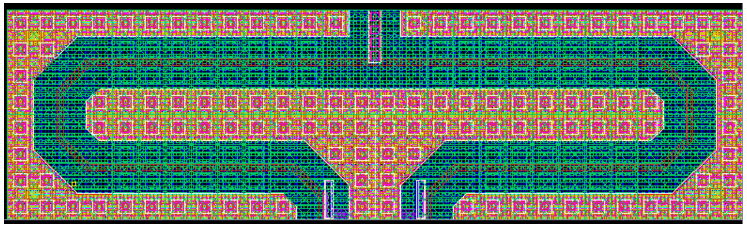


LO distribution network:
Wilkinson power divider
Quadrature hybrid (I/Q generation)

Layout

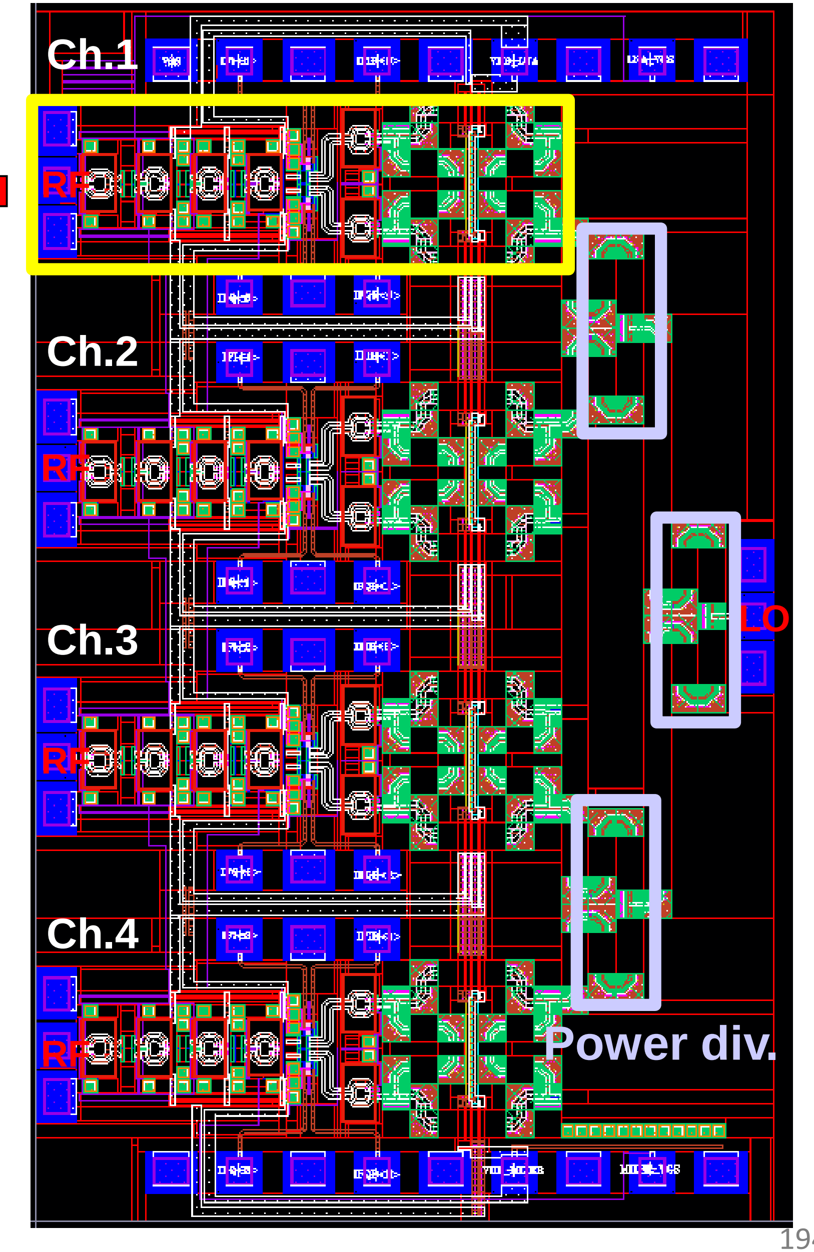


Single-channel layout

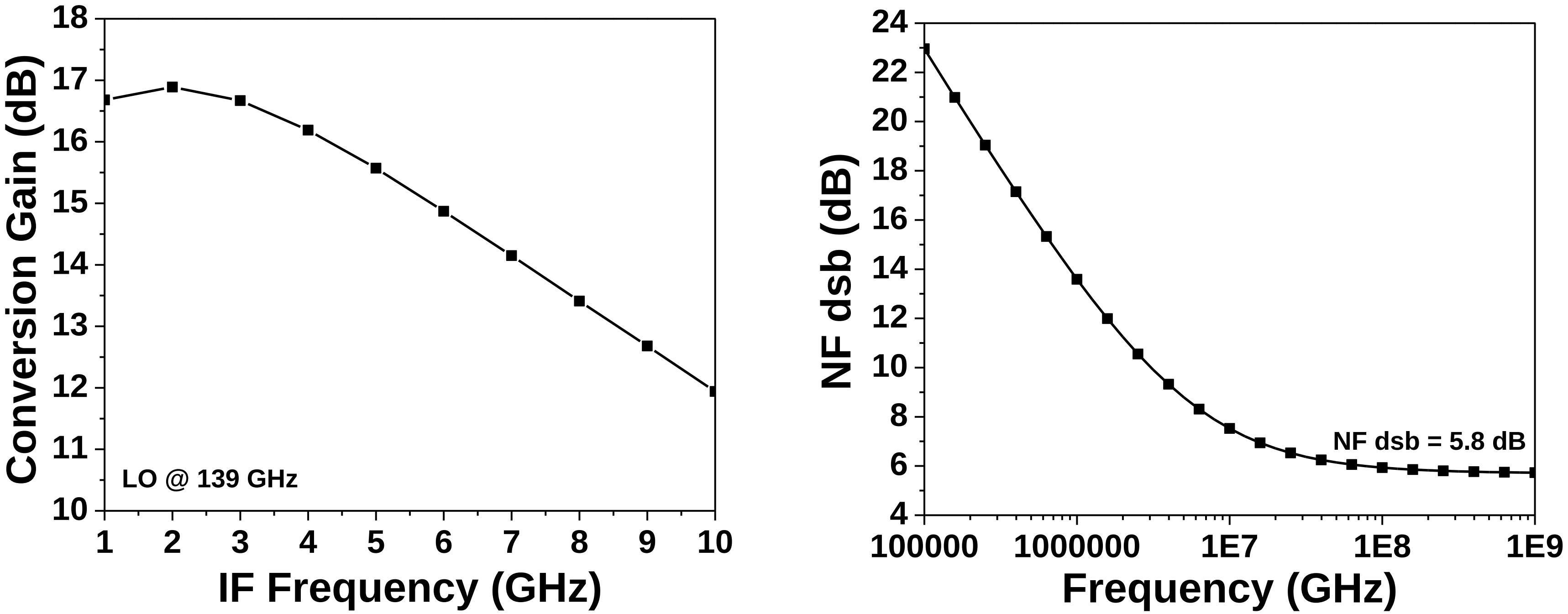


Wilkinson power divider

Size: 1075 x 1760 um²



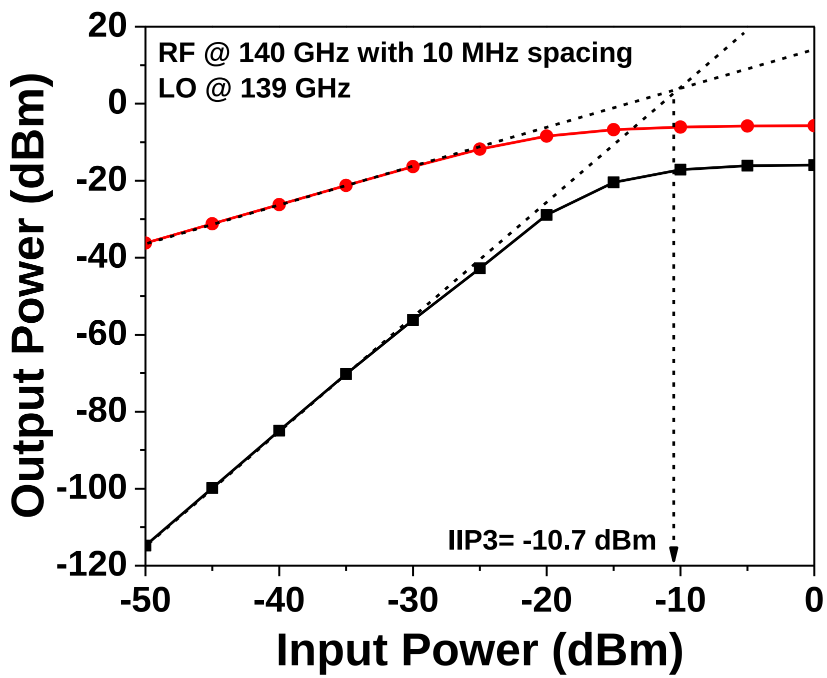
Conversion gain & NF (single-channel)

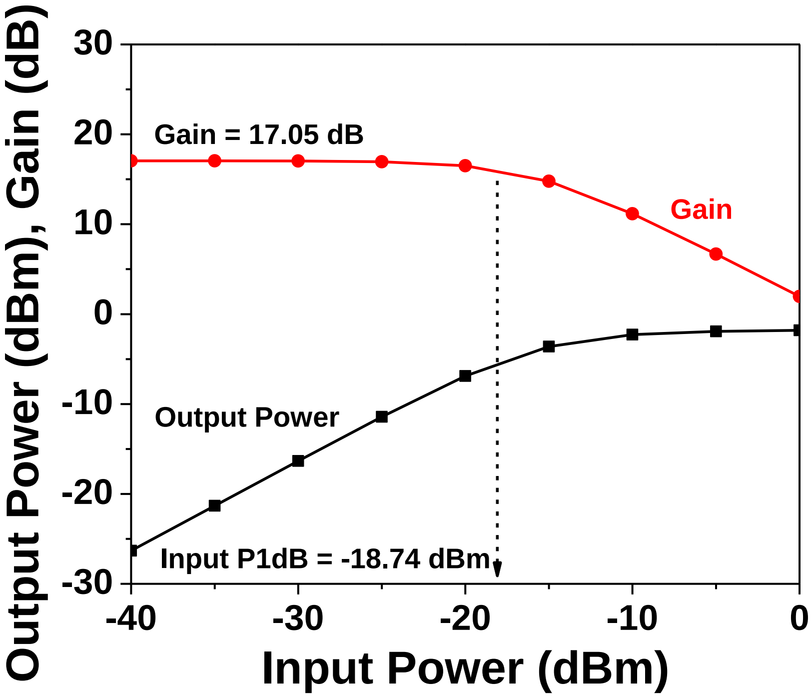


Gain 17 dB (single-channel IF_I output)

NF : 5.8 dB (dsb)

Linearity (single-channel)





IIP3: -10.7 dBm, Input P1dB: -18.74 dBm

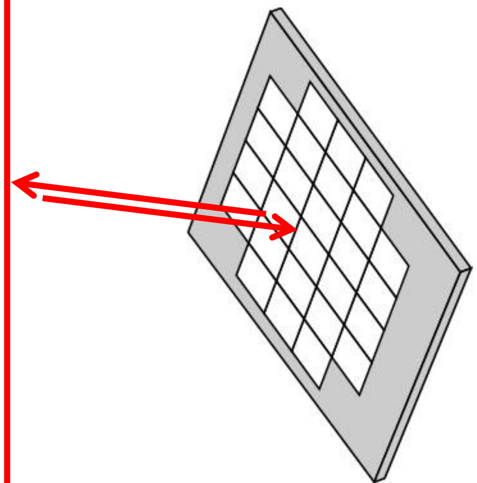
Summary - receiver

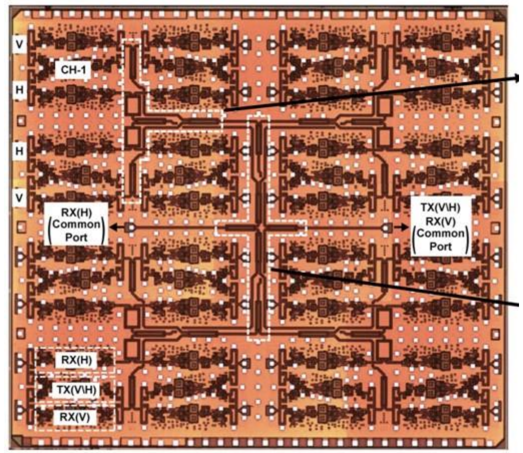
Gain	17 dB (Single-channel IF_I output)
NF	5.8 dB
IIP3	-10. 7 dBm
Input P1dB	-18.7 dBm
Power consumption	41 mA (LNA) + 2 mA (I/Q mixer) + 14 mA (IF-I/Q buffers) @ 1 V (Single-channel)
Size	1075 x 1760 um^2

IC example:
94 GHz
low-power-array

Millimeter-wave imaging

10,000-pixel, 94GHz imaging array→ 10,000 elements





Golcuk: Trans MTT, Aug 2014

Demonstrated:

SiGe (UCSD/Rebeiz)

~1.3kW: 10,000 elements

Lower-power designs:

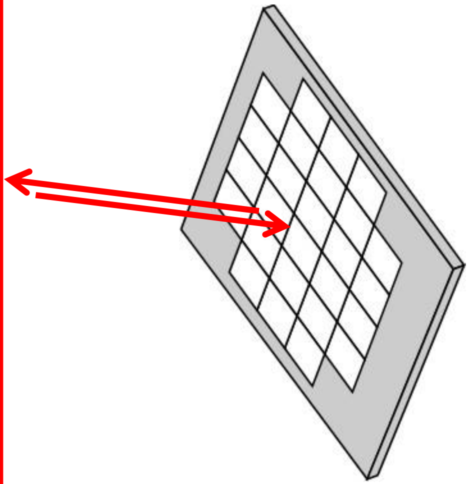
InP, CMOS, SiGe

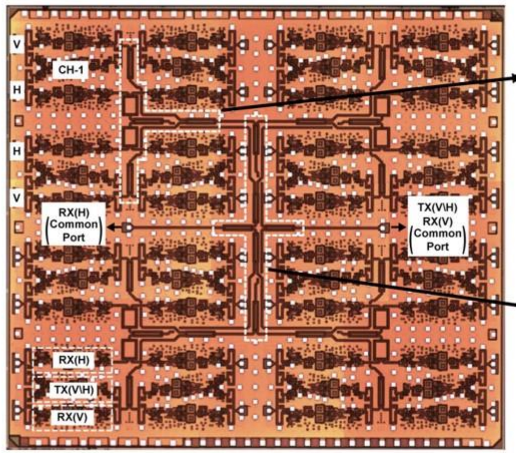
(UCSB, UCSD, Virginia Poly.)

System concept: Bruce Wallace DARPA. 1st ICs (SiGe) Rebeiz, UCSD.

Millimeter-wave imaging

10,000-pixel, 94GHz imaging array→ 10,000 elements





Golcuk: Trans MTT, Aug 2014

Demonstrated:

SiGe (UCSD/Rebeiz)

~1.3kW: 10,000 elements

Lower-power designs:

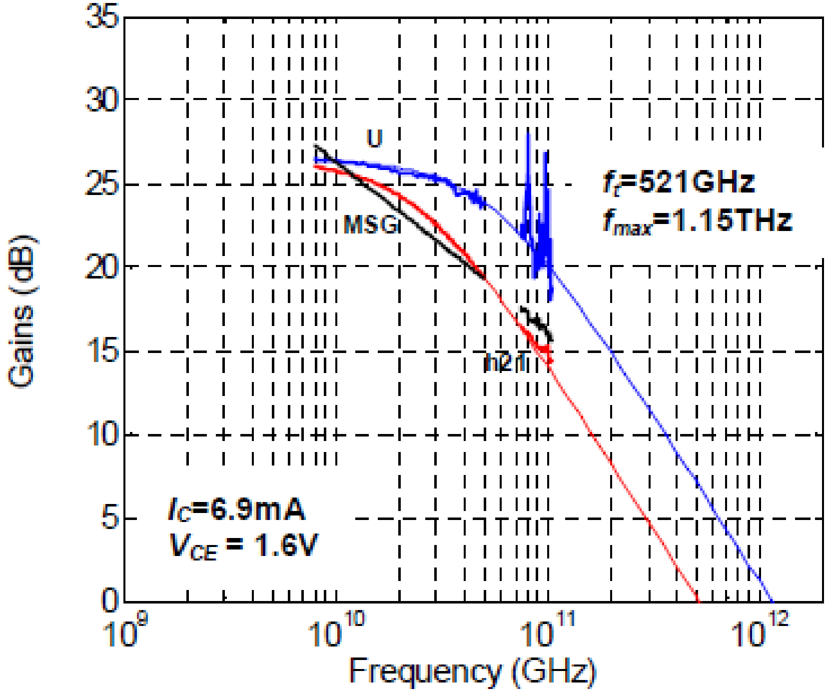
InP, CMOS, SiGe

(UCSB, UCSD, Virginia Poly.)

100 pixel × 100 pixel image→ 10,000 array elements.
~130 mW DC power per element → 1.3 kW system power requirement.
Problem: required size and weight of heat sink.

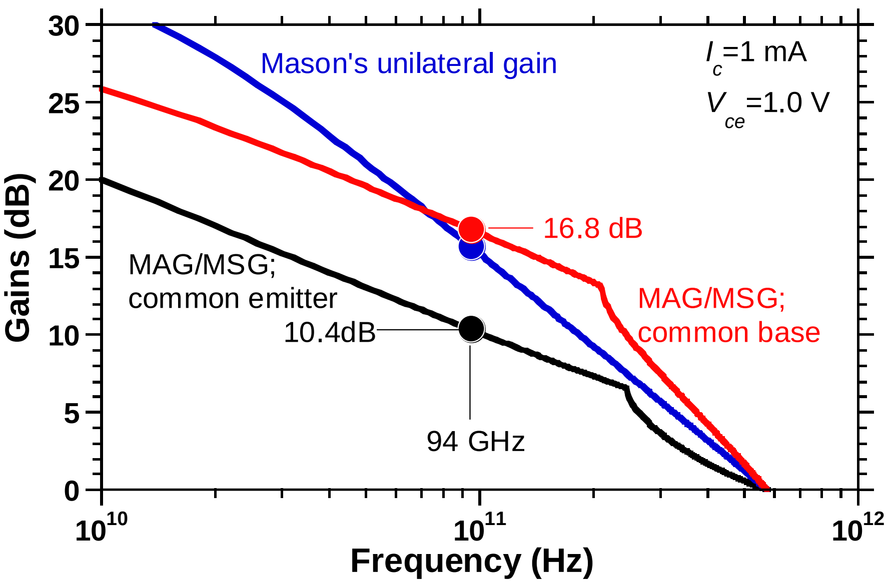
94 GHz low-power IC design: transistors

Teledyne: 130nm InP HBT: high-f_{max} bias



Teledyne: M. Urteaga *et al*: 2011 DRC

Teledyne: 130nm InP HBT: low-power bias

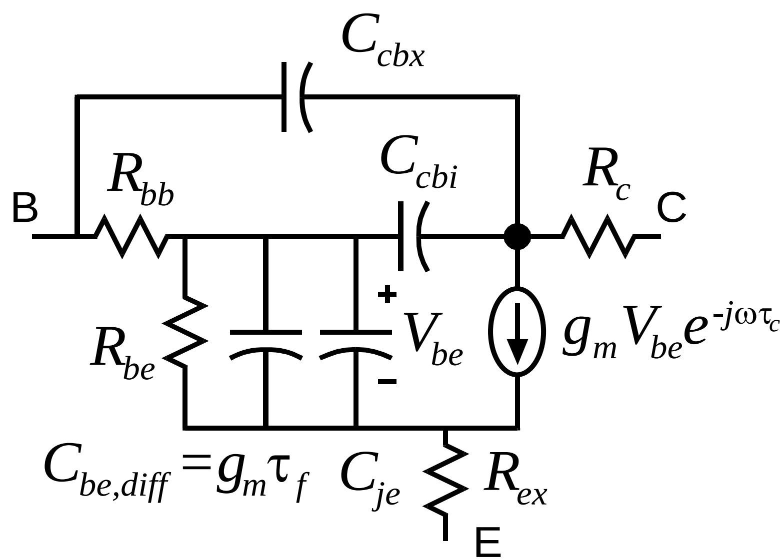


130nm × 3 μm emitter

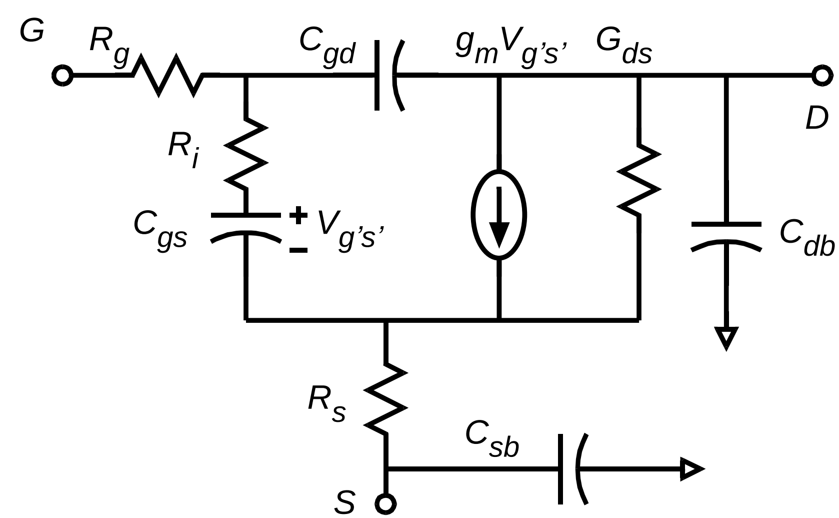
At 1mW dissipation, ~17 dB gain is feasible→ low power ICs.

94 GHz low-power IC design: transistors

BJTs



FETs



$$\text{RF: transistor must be sized to make impedance-matching possible}$$

$$\text{FETs \& BJTs}: Z_{in} \approx R_{g/BB} + (j\omega C_{gs/be})^{-1} \approx (\mathrm{K}/g_m) + (f_\tau / jf)(1/g_m) \propto 1/g_m$$

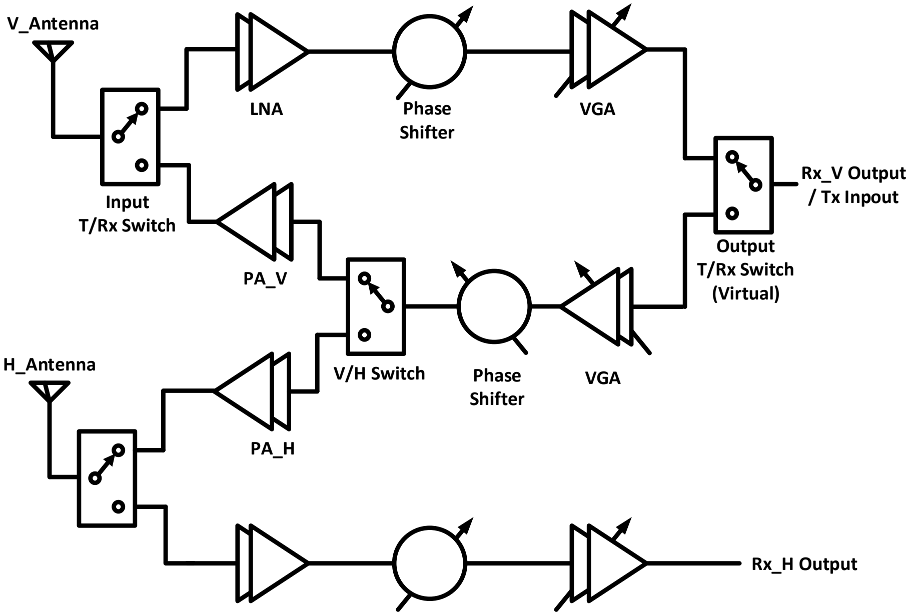
$$\text{BJTs}: g_m \cong I_E / 26\,\text{mV}.$$

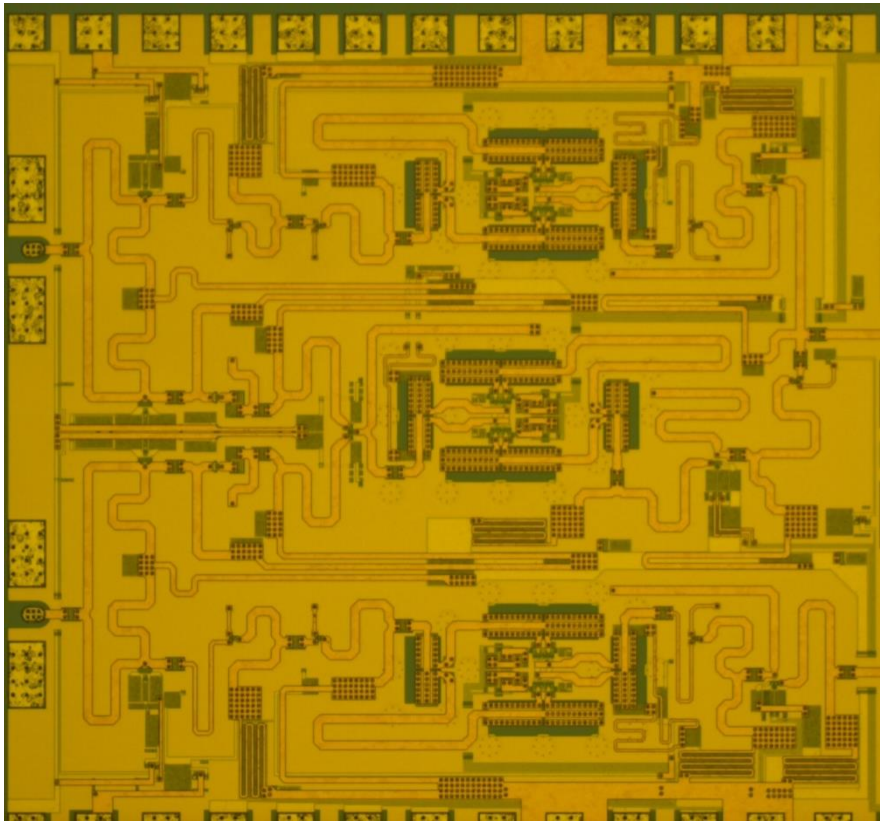
$$\text{FETs}: g_m \sim I_S / 300\,\text{mV}.$$

$$\rightarrow \text{low-power mm-wave ICs should use BJTs}$$

(ignores P_{sat}, IP3 considerations)

Phased array





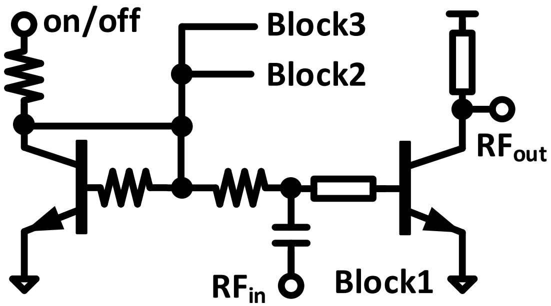
1770 um x 1550 um

IC can transmit on vertical (V) or horizontal (H) polarizations (one at a time)
IC can receive on vertical (V) and horizontal (H) polarizations (simultaneously)
Each mode has phase-shifter, VGA.
Signal distribution on backplane.
InP IC: requires low-speed CMOS digital control IC

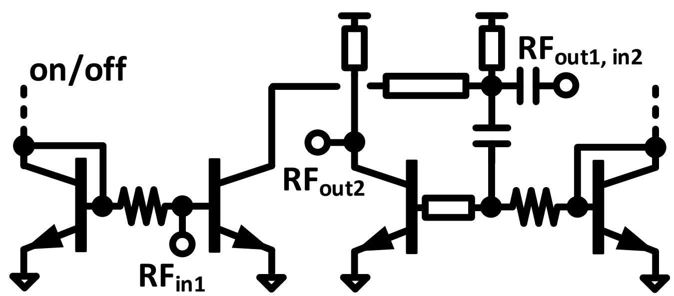
Low-power, low-voltage mm-wave design

Extensive use of current mirrors, translinear techniques

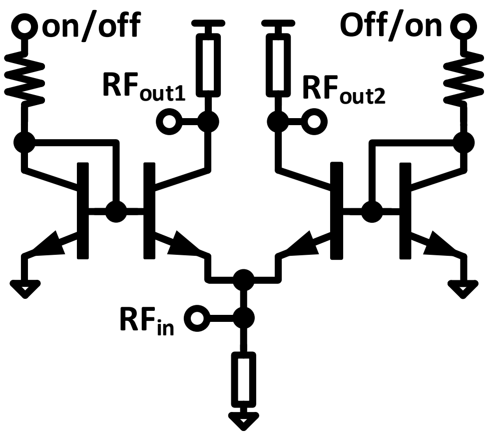
Gain & switching



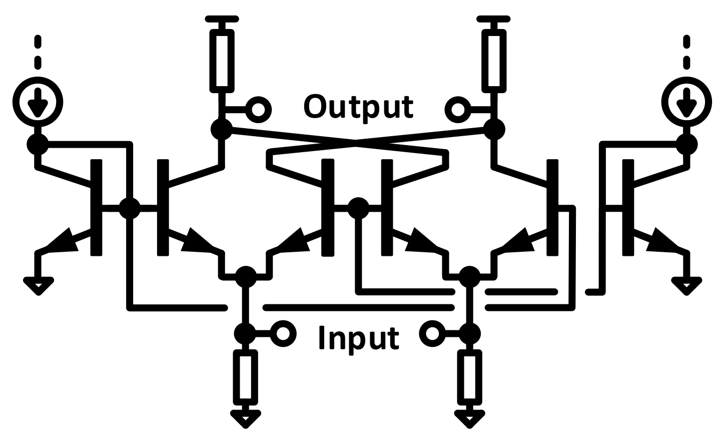
Low-power T/R switching



VGA / switch

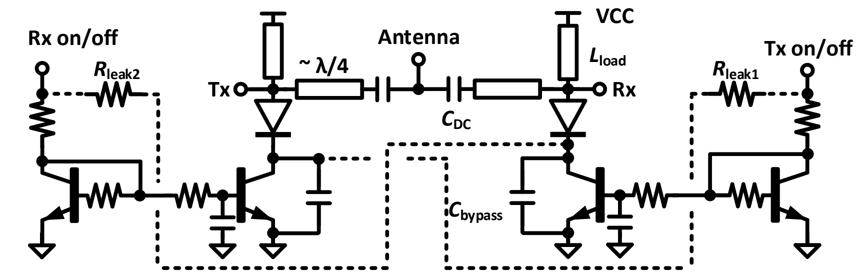


Multiplier→ mixer, modulator, phase-shifter

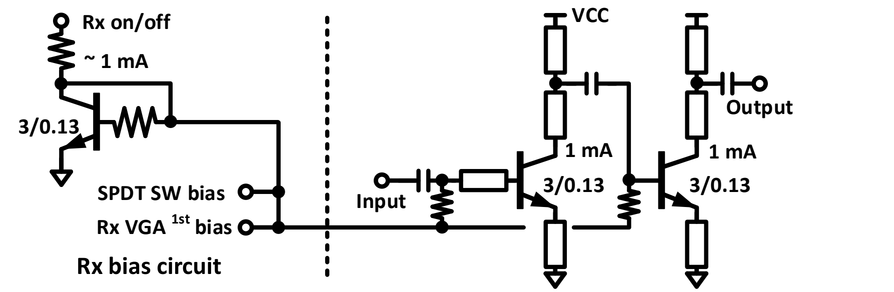


Low-power, low-voltage mm-wave design

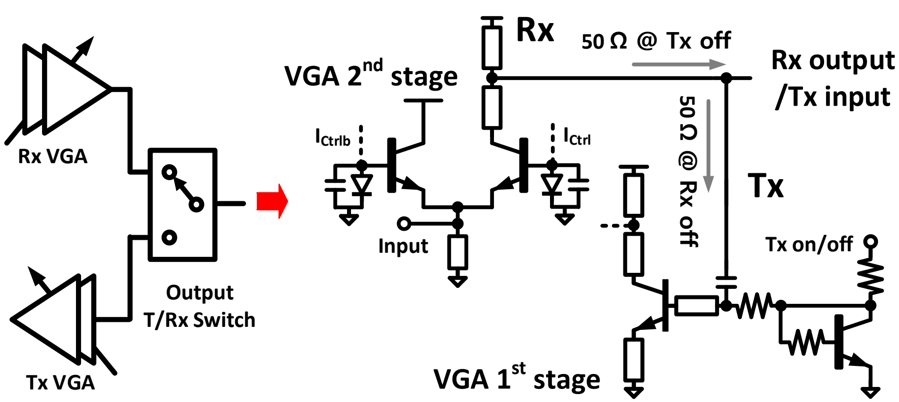
Antenna switch



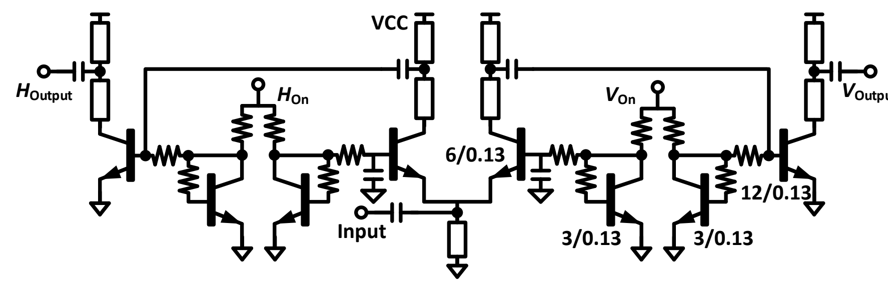
LNA



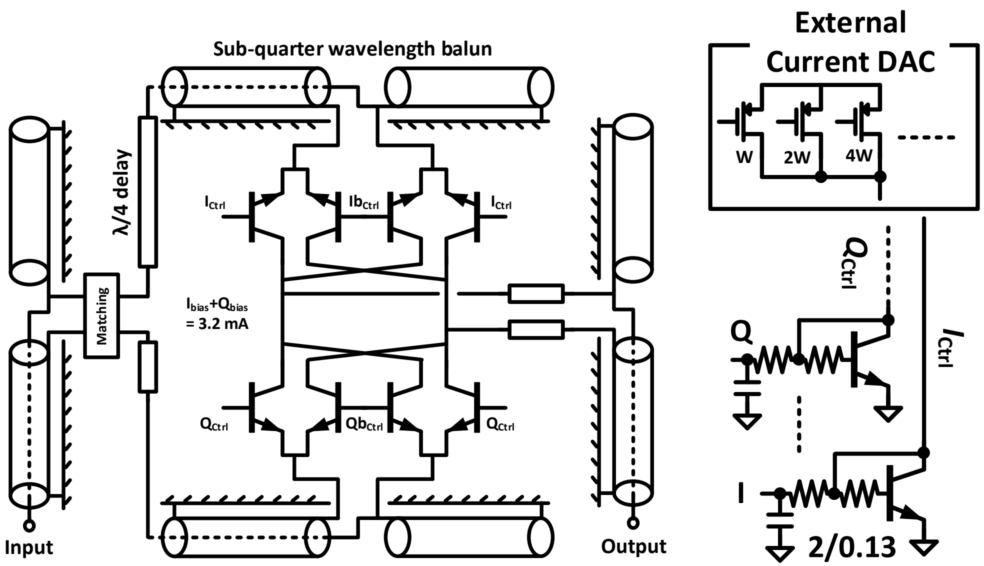
backplane T/R switch

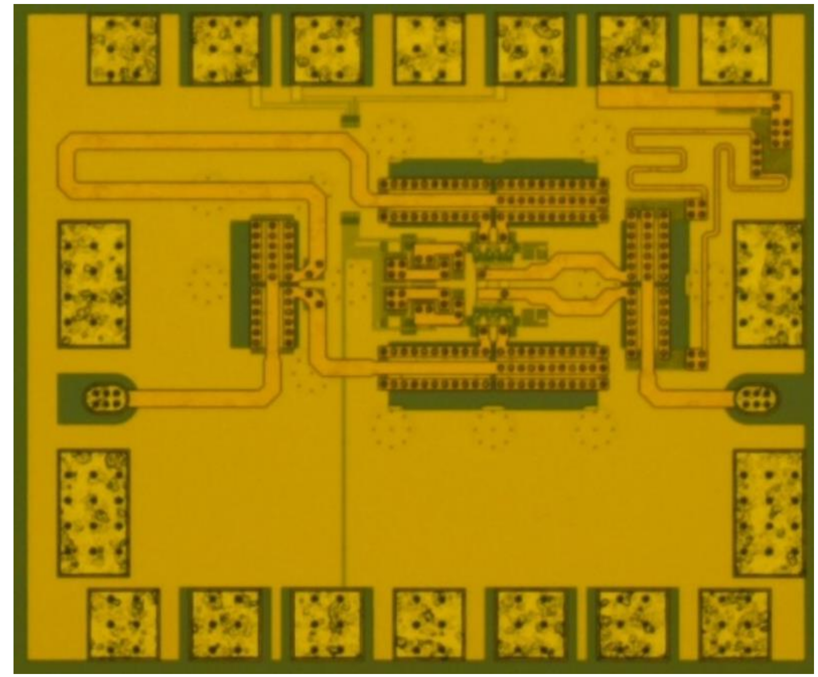


PA & V/H switch



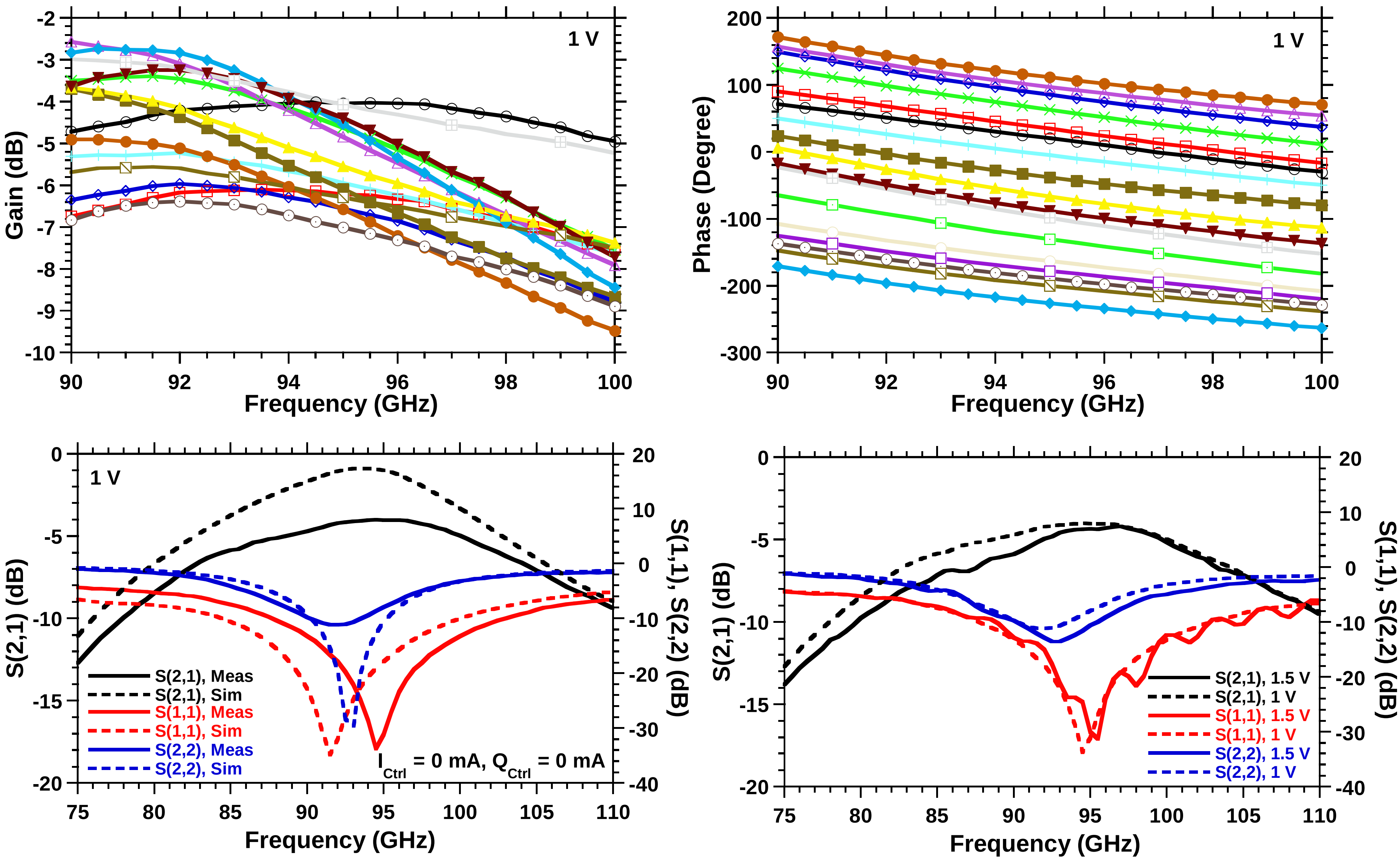
Phase-shifter and control circuits





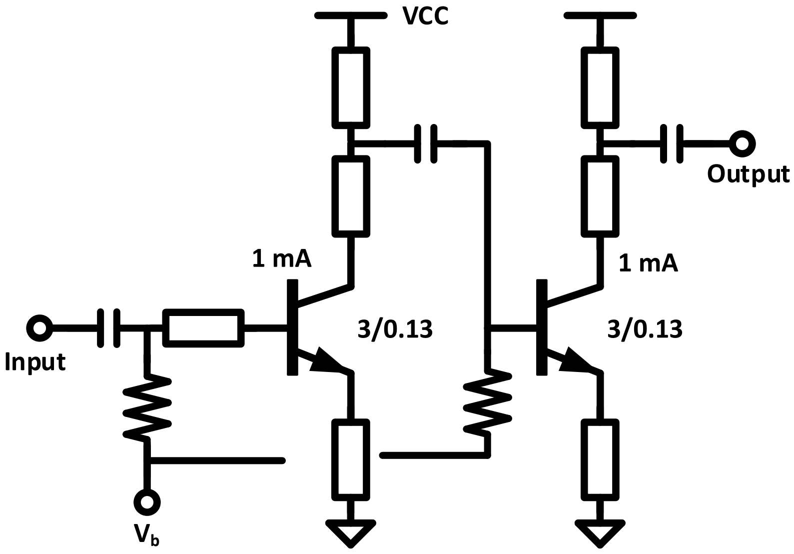
760 um x 640 um

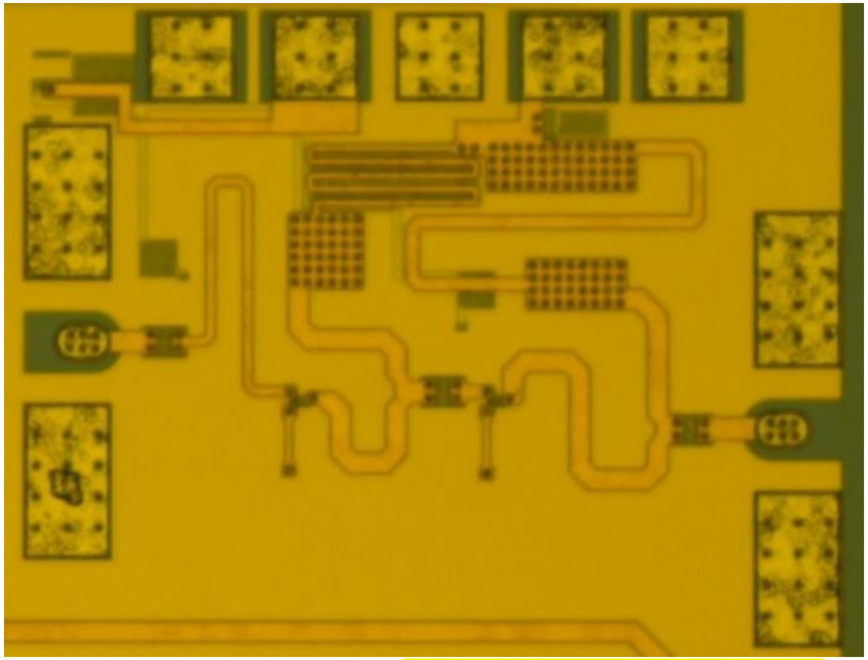
Phase-shifter measurement results (1 V)



Power consumption: 4.2 mA @ 1 V

Low-noise amplifier

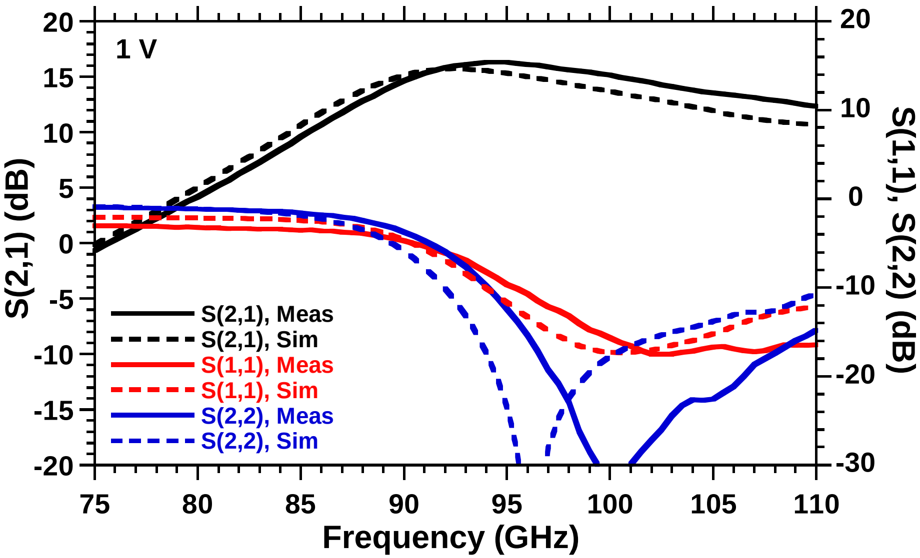


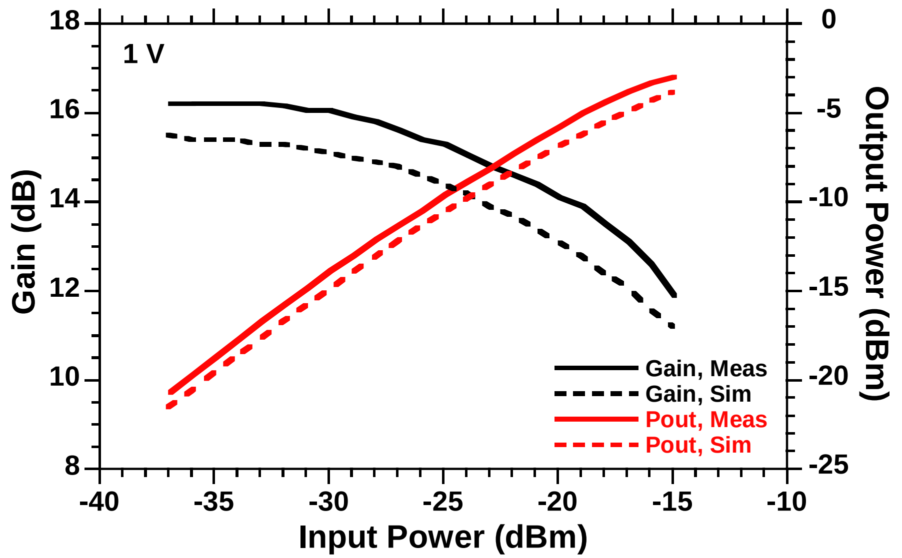


660 um x 510 um

- Noise matching for input
- Conjugate matching for inter-stage
- Gain matching for output
- Power consumption: 2 mA @ 1.5 V

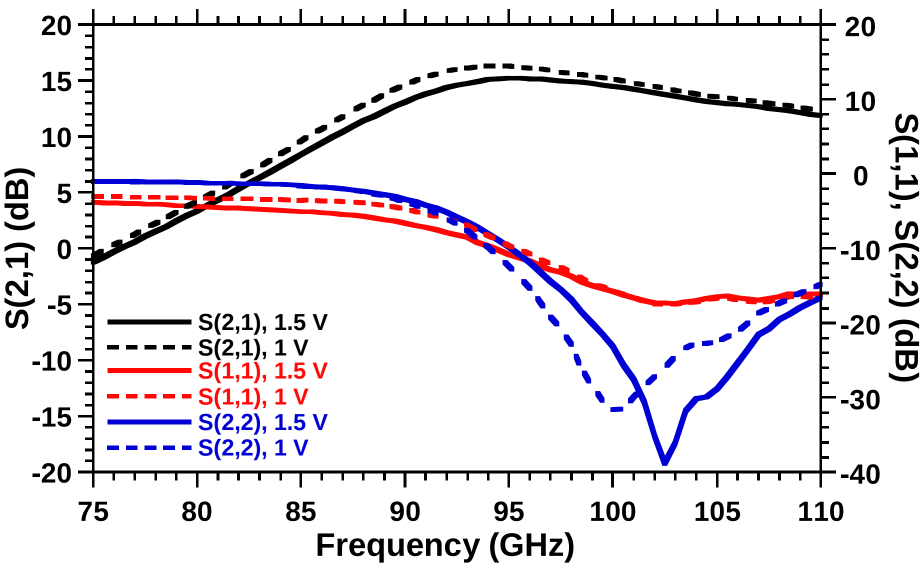
LNA Measurement results (1 V)

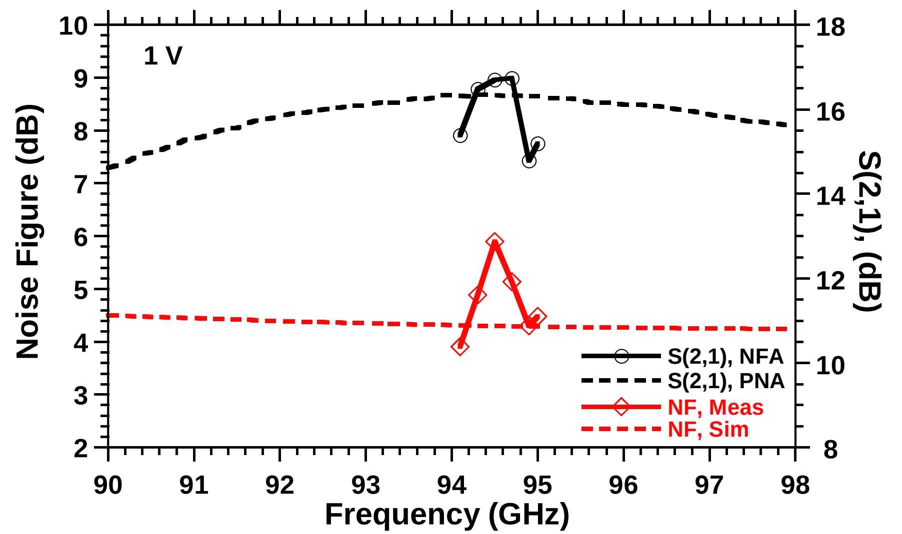




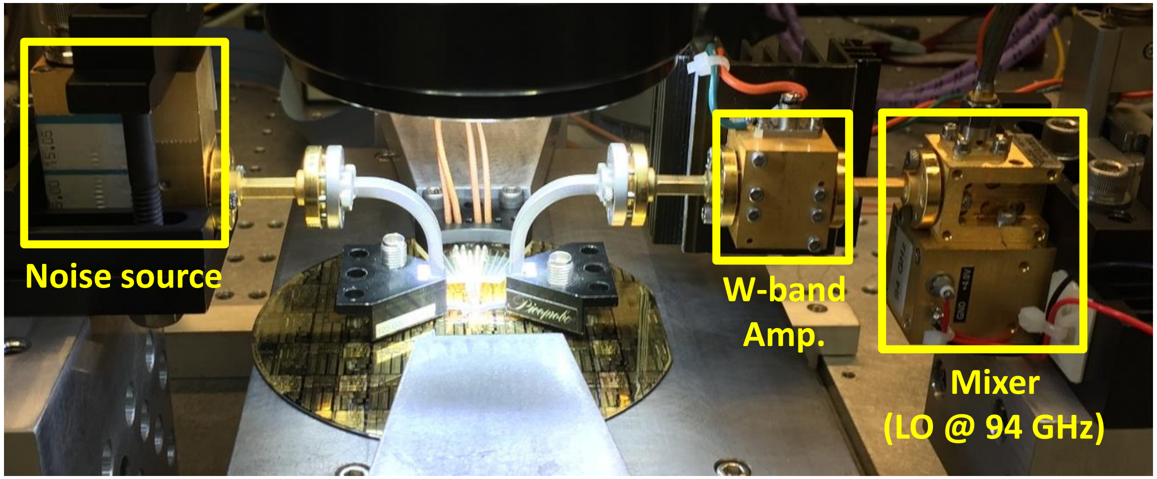
Power consumption: 2.0 mA @ 1 V

Gain: 16.3 dB @ 94 GHz (peak gain)

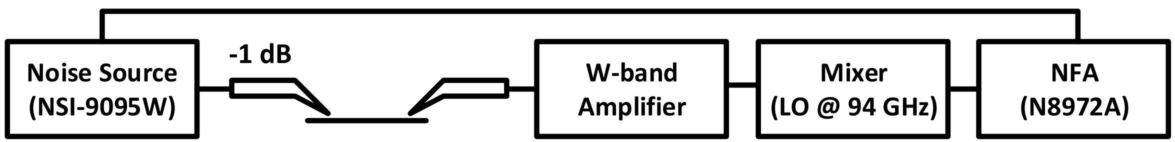




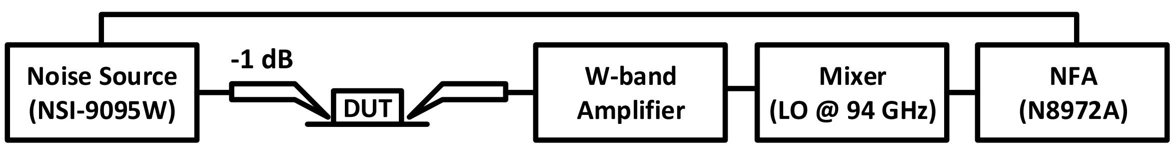
Noise measurement setup



Calibration

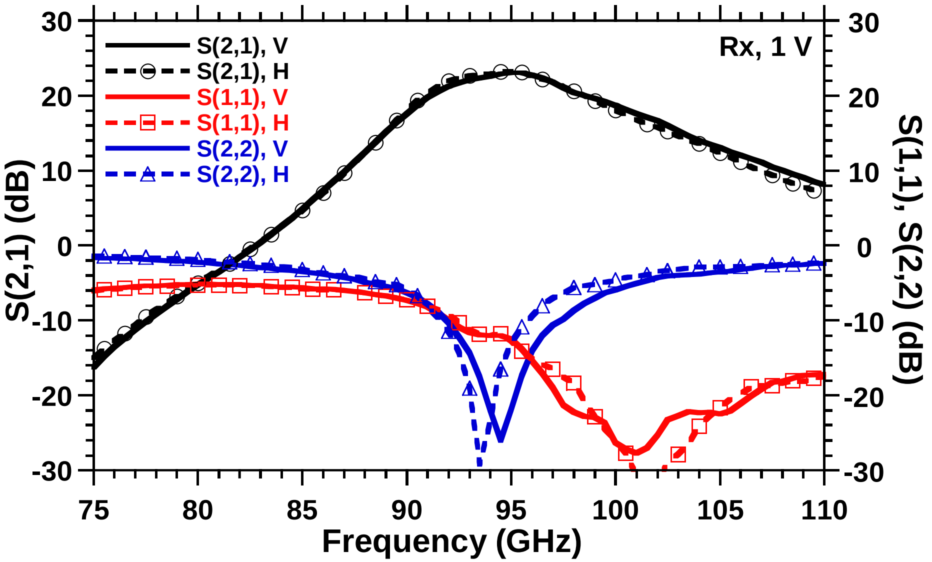


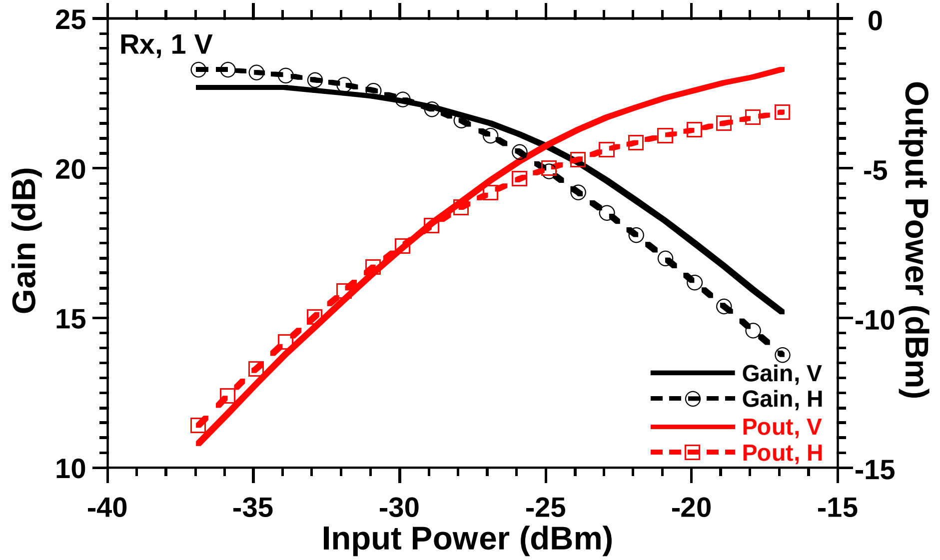
Measurement

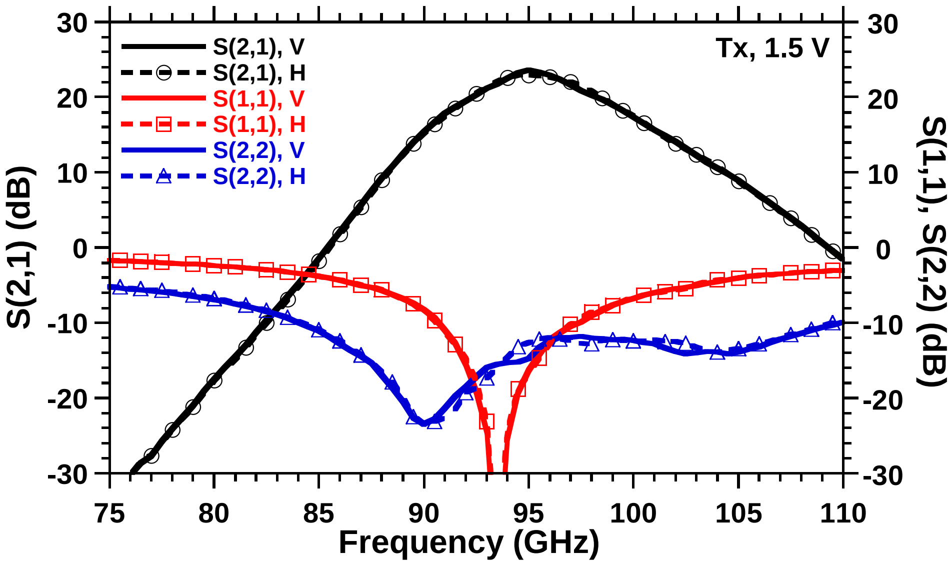


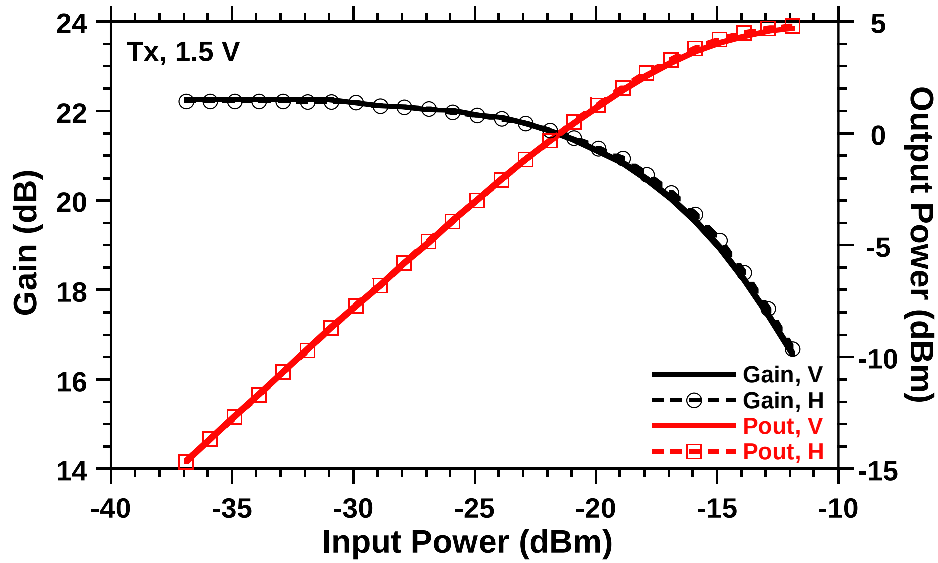
Loss before the DUT: compensated using the NFA's internal function
therefore, measured gain should be subtracted by -1 dB

Transceiver measurement results

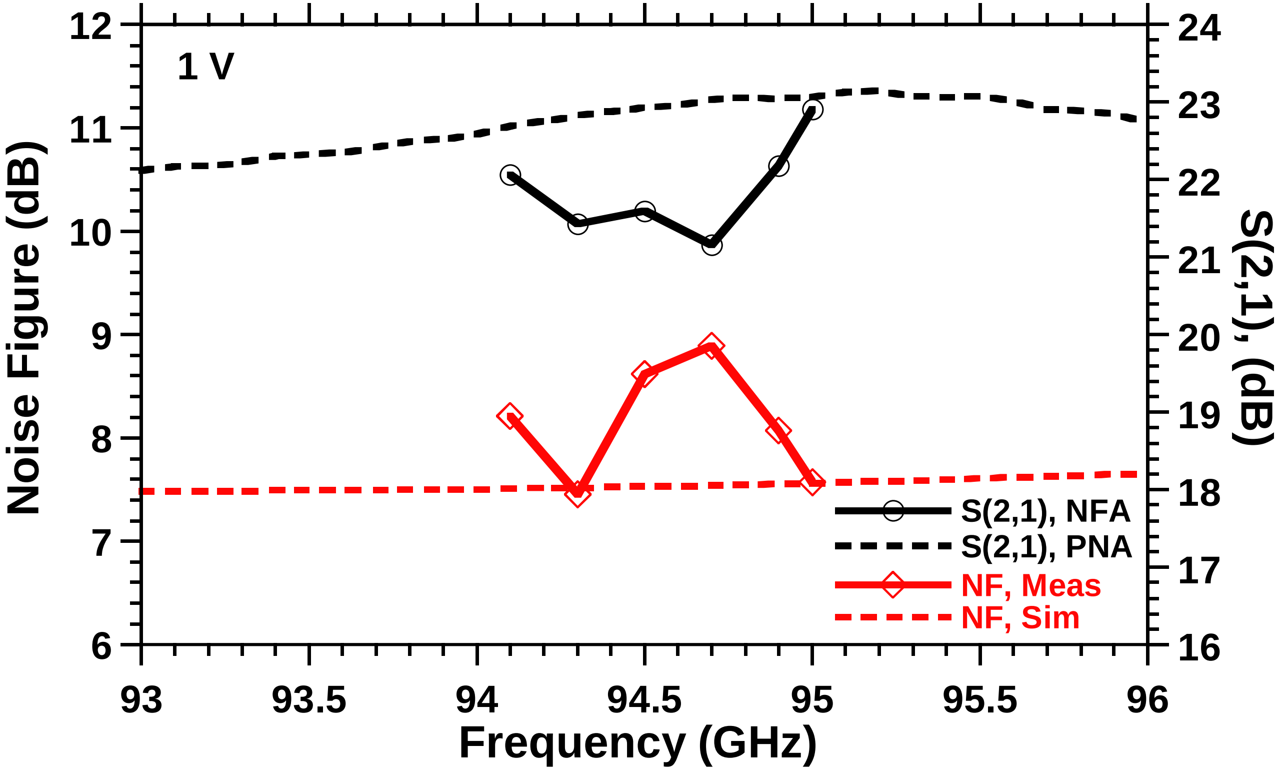




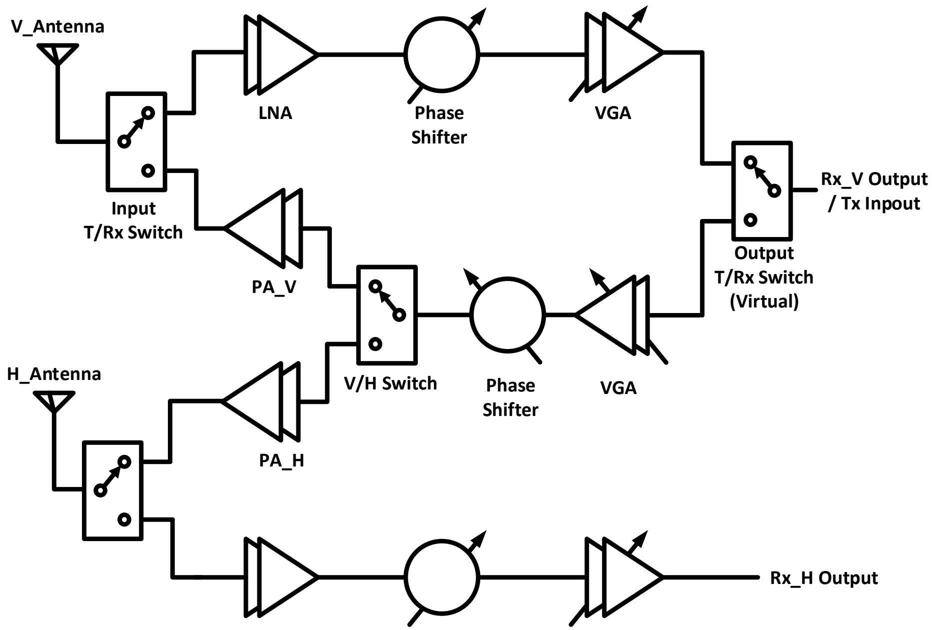




Receiver noise



94 GHz transceiver: performance summary

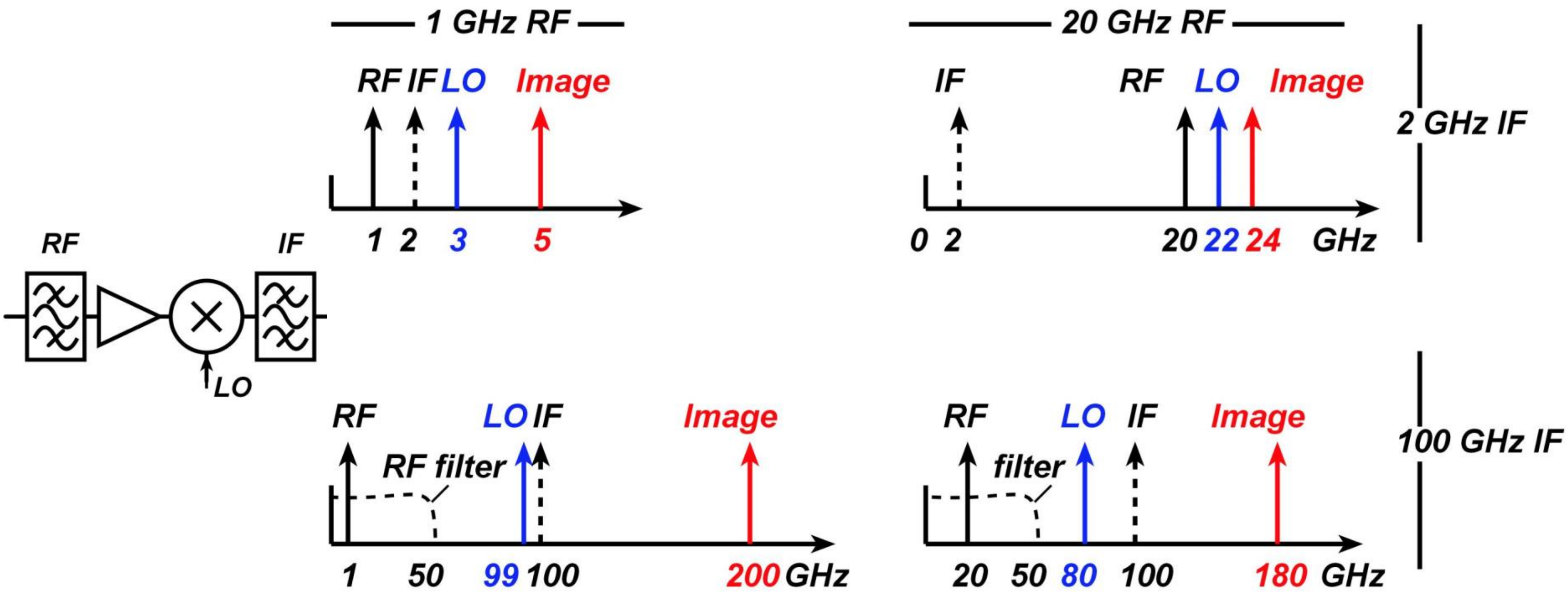


			@Vcc=1.5V	@Vcc=1.0V
Power Amplifier + V/H SW	Output Power P3dB	dBm	6.9	3.5
	Power Gain @P3dB	dB	14	14
	PAE	%	17	12.7
	Pdiss @ P3dB	mW	27.2	16.9
	Pdiss (small-signal)	mW	22.5	16.4
	Pdiss (core exclude bias ckt)	mW	17.55	11.45
	Size (exclude Pads)	µm	475*475	475*475
VGA	Power Gain (Rx/Tx)	dB	12.5/10.9	13.4/11.5
	NF (max gain)	dB	4.8/7.8	4.6/7.7
	NF (max gain - 6dB)	dB	7.1/9.4	6.6/9.3
	Input P1dB	dBm	-12.4/-9.6	-15.9/-15
	OIP3	dBm	6.7/7.6	-1.8/-3
	Pdiss	mW	9	6.4
	Pdiss (core exclude bias ckt)	mW	6.9	4.6
	Size (exclude Pads)	µm	530*900	530*900
LNA	Power Gain	dB	15.1	16.3
	NF	dBm	5	5
	Input P1dB	dBm	-21.9	-24.5
	OIP3	dBm	-1.7	-3
	Pdiss	mW	4.95	3.95
	Pdiss (core exclude bias ckt)	mW	3.5	2
	Size (exclude Pads)	µm	480*280	480*280
Phase Shifter	Power Gain (Rx/Tx)	dB	-5±1.5	-5±1.5
	NF	dB	14.9	14.6
	Input P1dB	dBm	9	6
	OIP3	dB	10.9	2
	Pdiss	mW	6.5	4.2
	Pdiss (core exclude bias ckt)	mW	6.5	4.2
	Size (exclude Pads)	µm	660*340	660*340
SPDT Antenna T/Rx SW	Loss	dB	2	1.8
	Isolation	dB	19.5	18.5
	P1dB	dBm	14	14
	Pdiss	mW	6.8	4.8
	Pdiss (core exclude bias ckt)	mW	4.8	2.8
	Size (exclude Pads)	µm	200*680	200*680
Rx Channel	Power Gain	dB	21	22.7
	NF	dB	8.5	8
	Fractional BW	%	7.6	7.5
	Input P1dB	dBm	-22.9	-27.9
	IIP3	dBm	-16.3	-24.3
	Pdiss	mW	19.2	12.9
	Pdiss (core exclude bias ckt)	mW	17.25	11
Tx Channel	Power Gain	dB	22.2	22.4
	Pout (P3dB)	dBm	3.8	0.1
	Fractional BW	%	6.7	6.7
	Output P1dB	dBm	0.8	-3.4
	OIP3	dBm	10	3.8
	Pdiss	mW	39.7	28.7
	Pdiss (core exclude bias ckt)	mW	31.5	20.5

Simulation

IC example: 1-25 GHz dual-conversion receiver

Dual Conversion: Wide Tuning



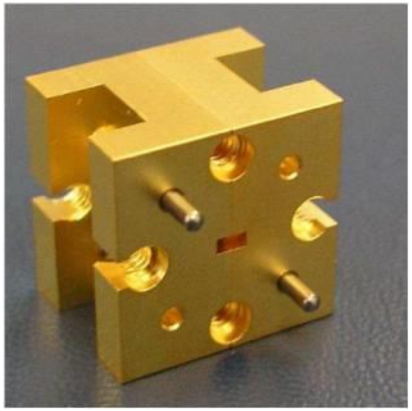
Low (2GHz) IF→ image & LO responses close to RF carrier

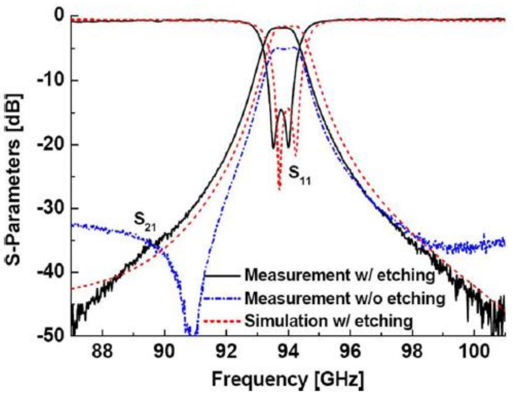
High (100GHz) IF→ image & LO responses far from RF carrier

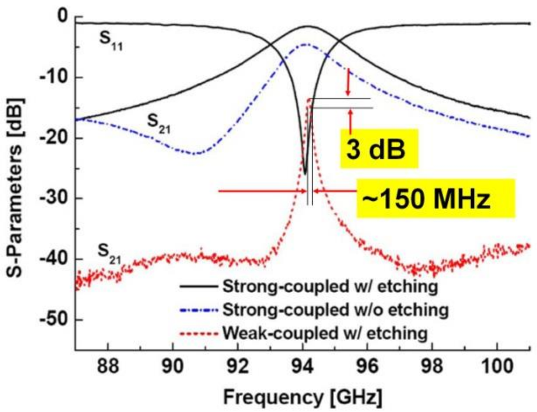
Dual conversion: a standard approach in RF receivers.

Modern THz IC processes→ 100 GHz IF easily feasible
→ Image-response-free 1-50 GHz receiver

W-band Waveguide Filters





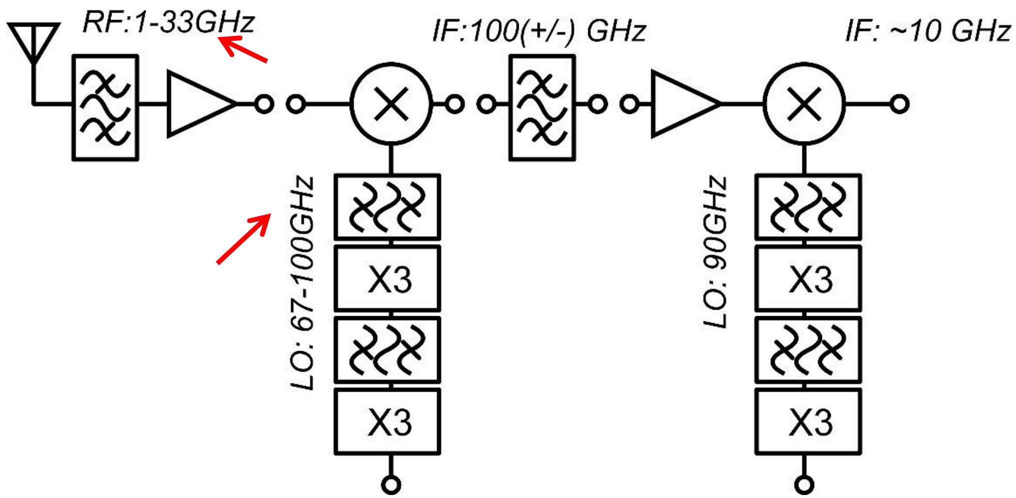


1 GHz filter bandwidth is easy; 100 MHz should be just feasible.

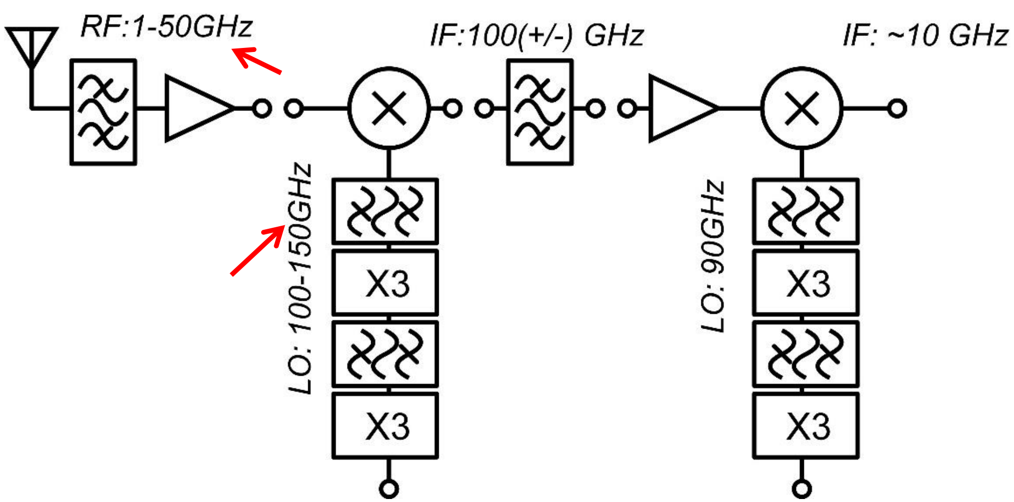
our effort: design the ICs, purchase the filter.

Choice of Frequency Plan

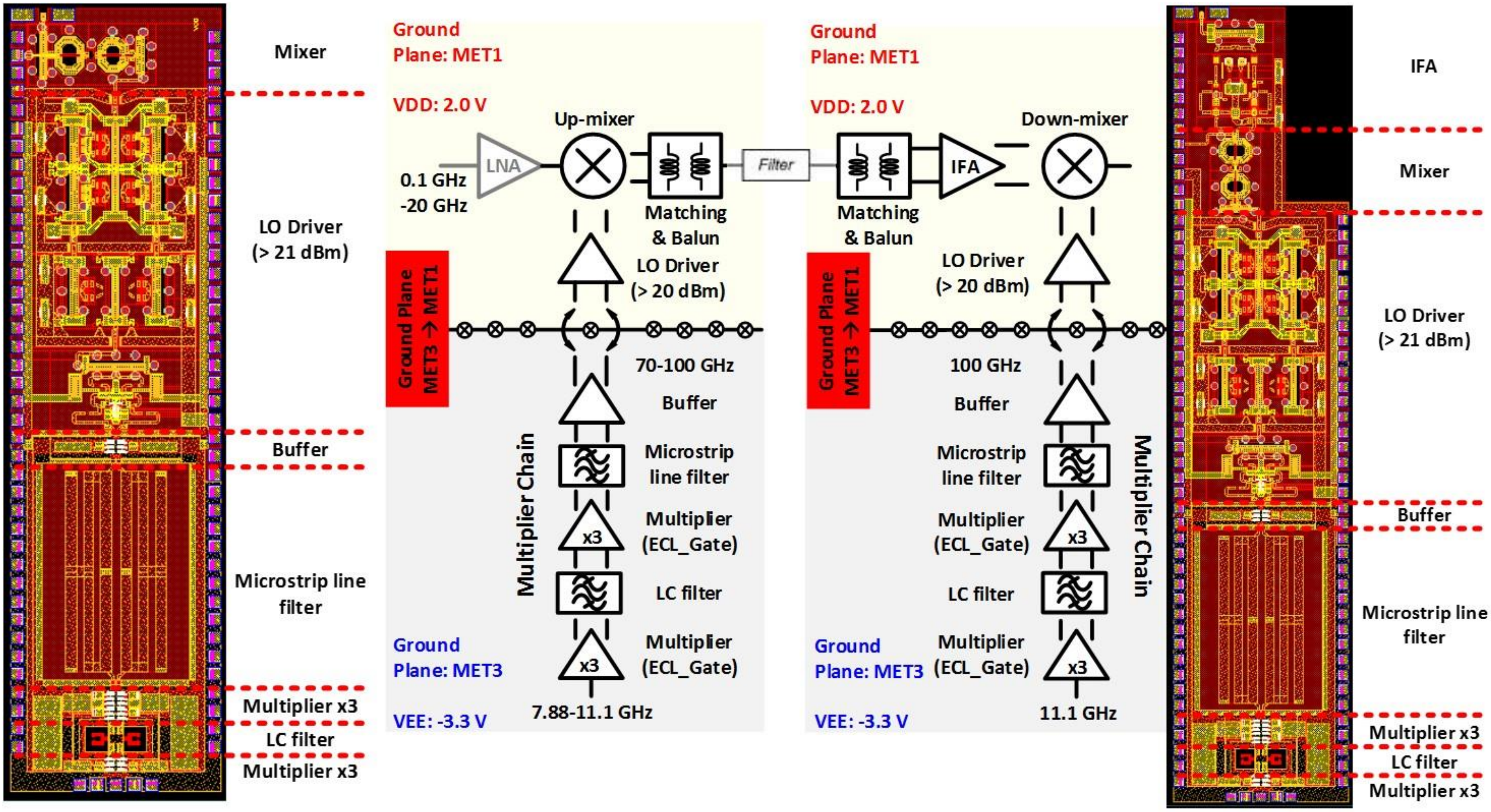
LO below IF:
triplers have residual output @ $2f_{in}$
→ maximum 1.5:1 tuning ratio
→ maximum 67-100 GHz LO tuning
~1-33 GHz RF tuning
Need 67-100GHz LO driver PA
present designs (lower-risk)



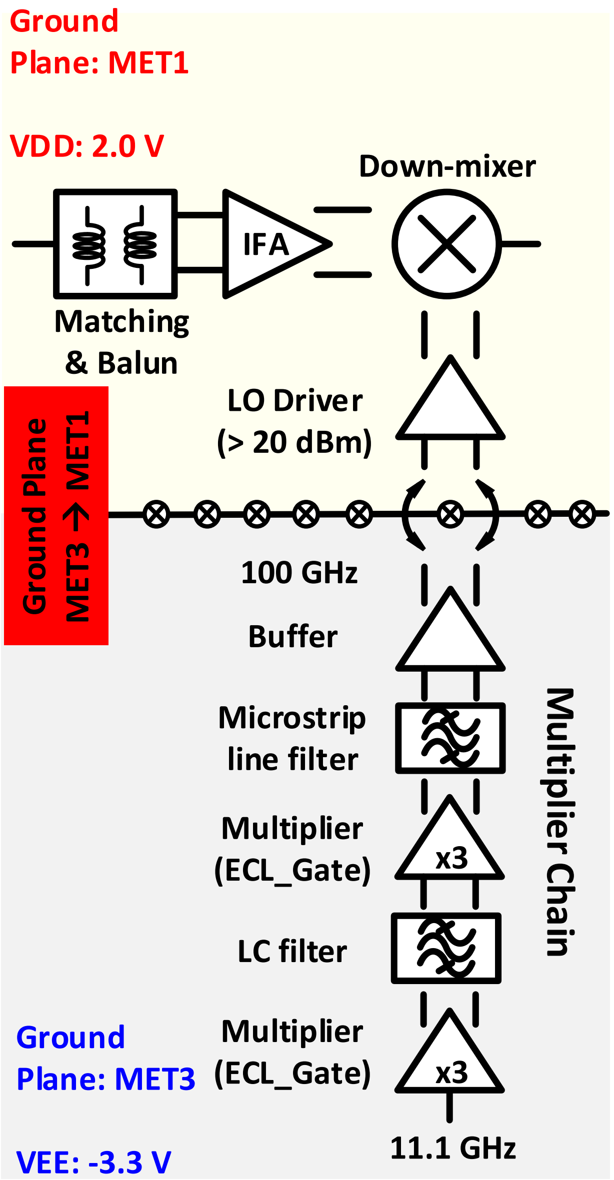
LO above IF:
maximum 100-150 GHz LO tuning
~1-50 GHz RF tuning
Need 100-150GHz LO driver PA
At ~200-300mW output power
higher-risk.

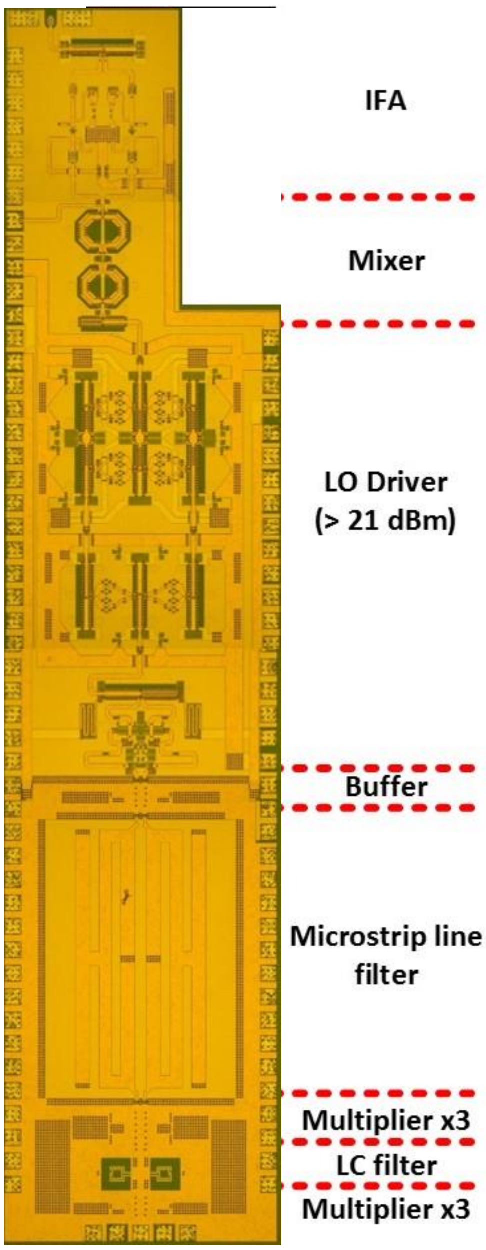


Full receiver configuration: 2 chips to ease testing



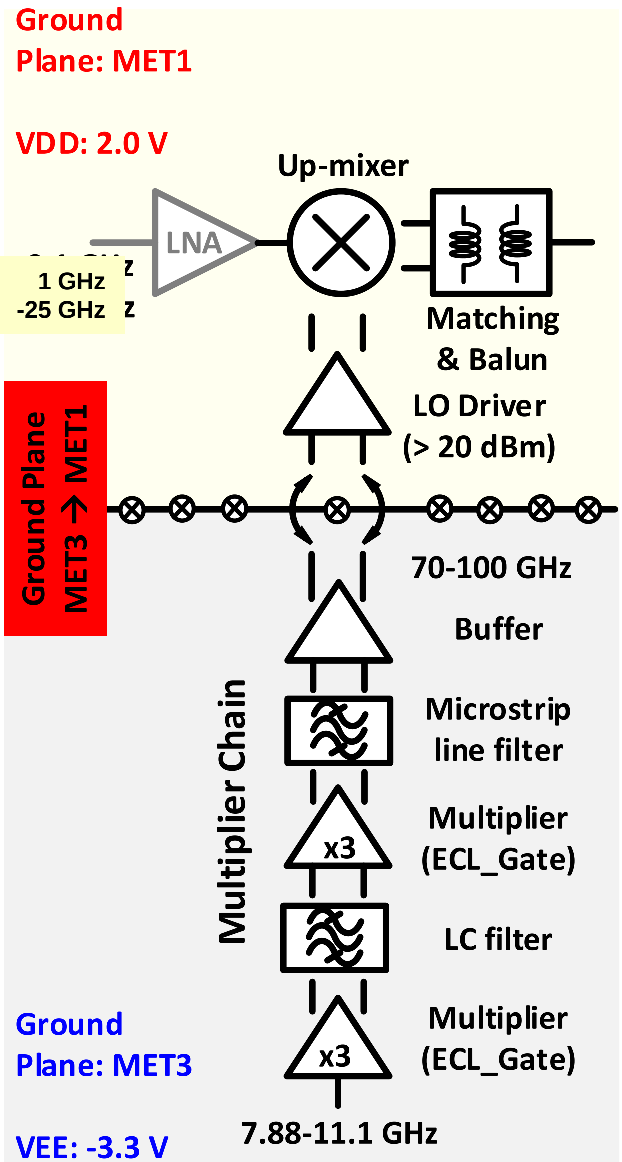
Receiver: down-conversion block



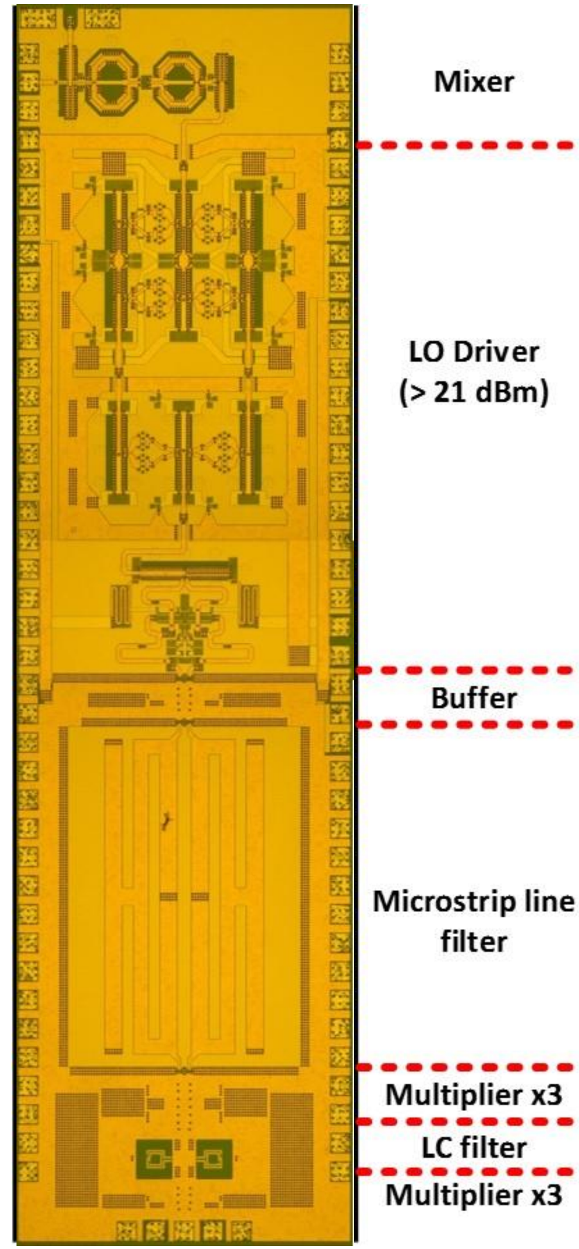


5240 um x 1160 um

Receiver: up-conversion block



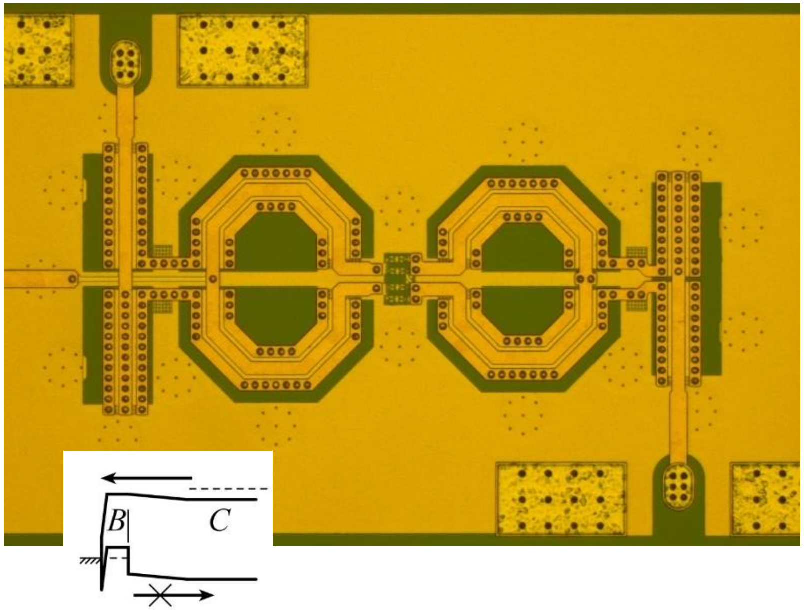
4300 um x 1160 um

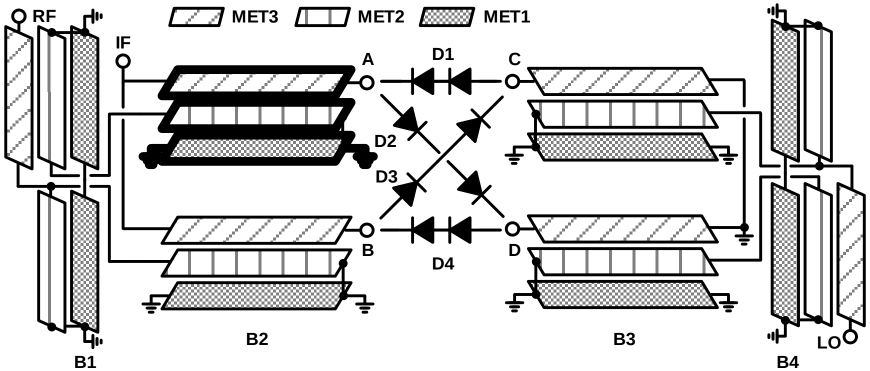


Mixer

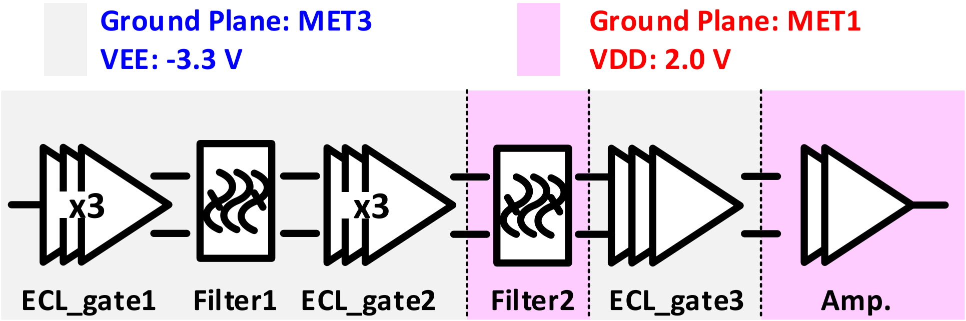
Diode mixer:
High dynamic range.
base-collector diodes: no saturation
series-connected→ high IP3
requires high LO drive power

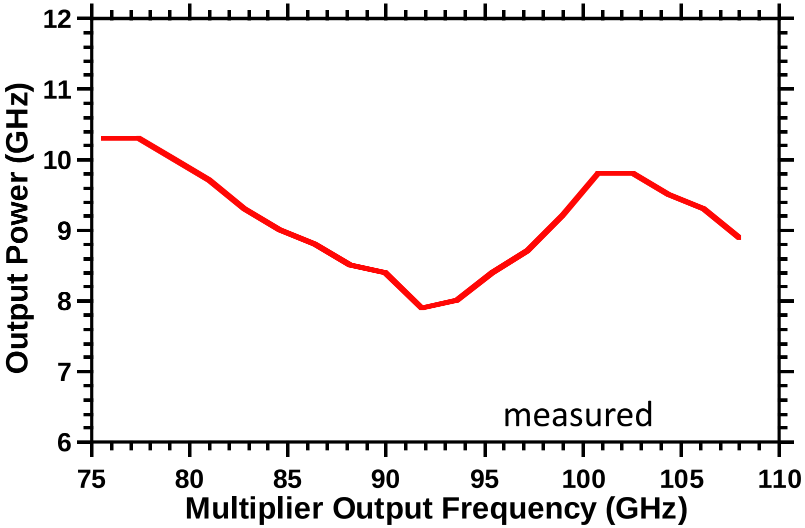
Baluns:
tri-plane design
some are sub-quarter-wavelength



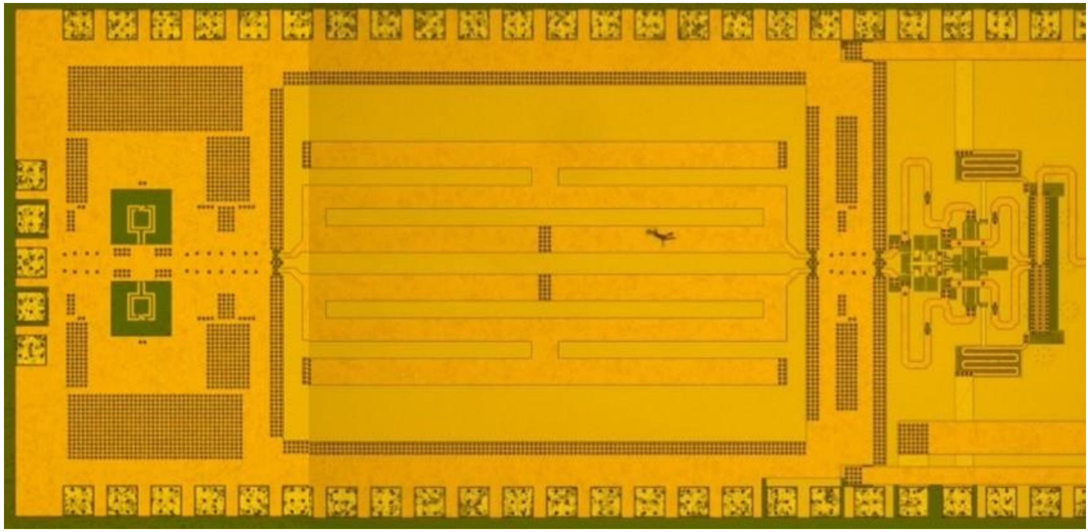


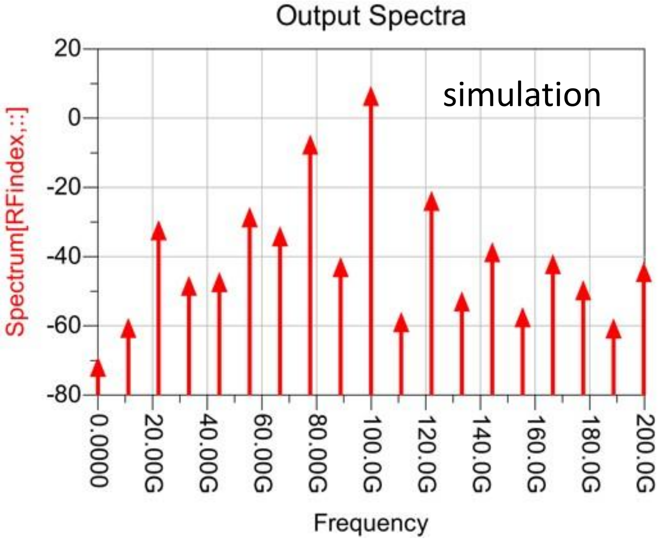
9:1 LO Multiplier





2500 um x 1160 um



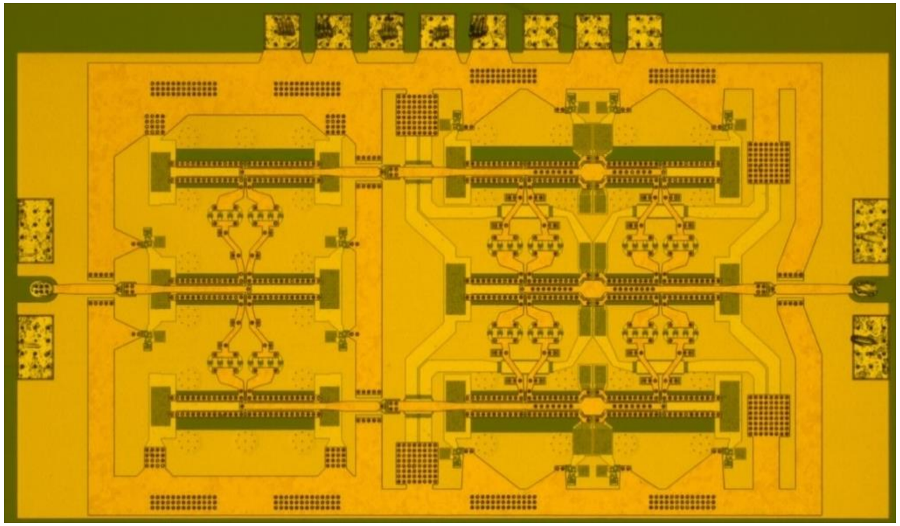


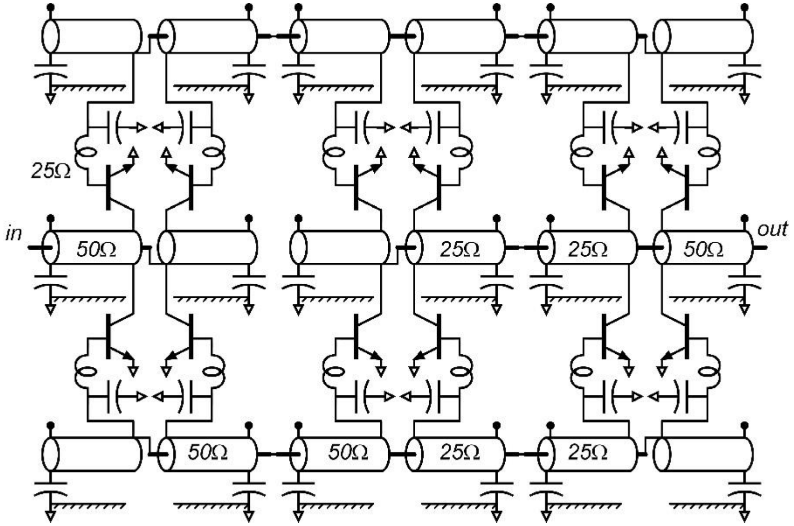
Differential LO Driver Amplifier: 67-100GHz

Ultra-broadband LO driver
limited by 67GHz substrate mode ?
data shows otherwise.

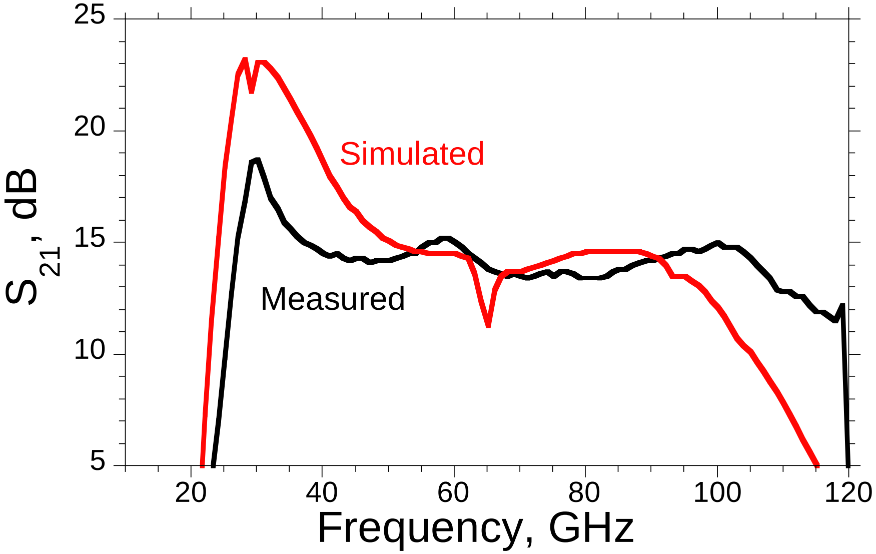
High Power
required by high-IP3 mixer
>100mW over full bandwidth
> 250mW at most frequencies.

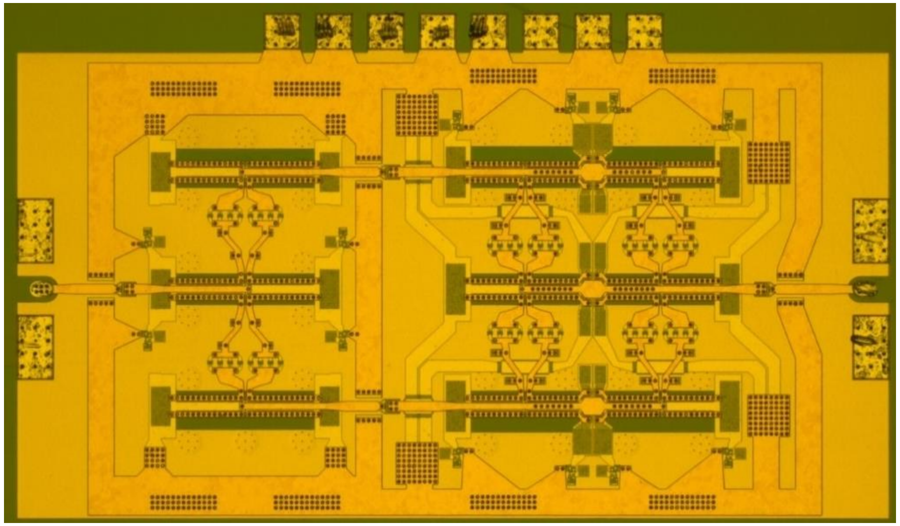
Topology
4:1 series connected by baluns
compact, efficient, ultra-broadband
2 cascaded stages

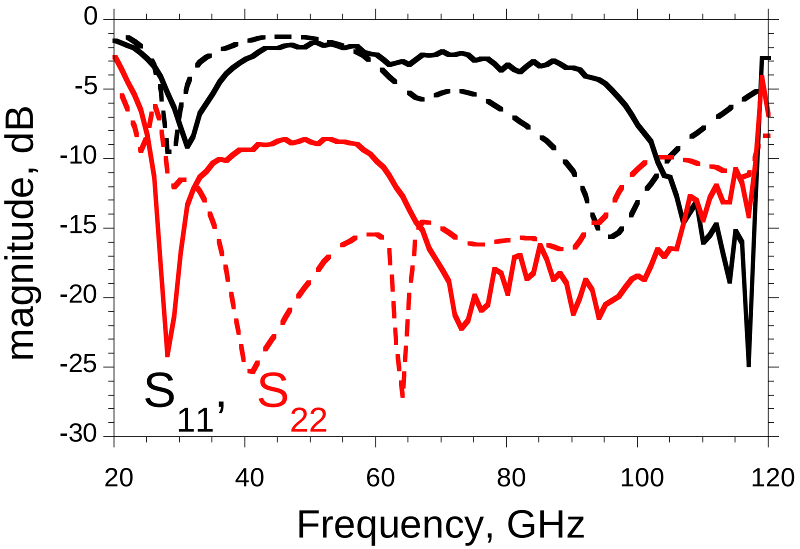


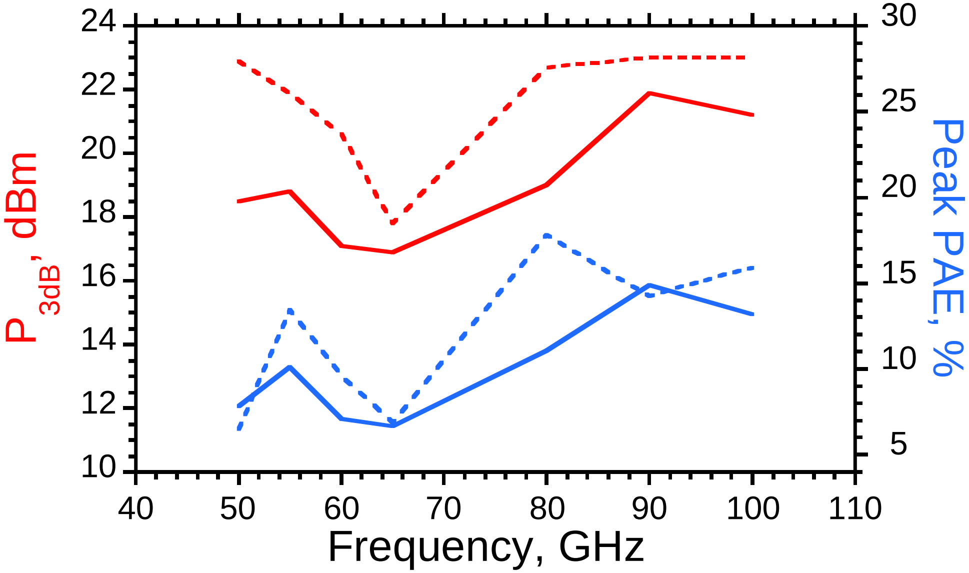


Differential LO Driver Amplifier: 67-100GHz





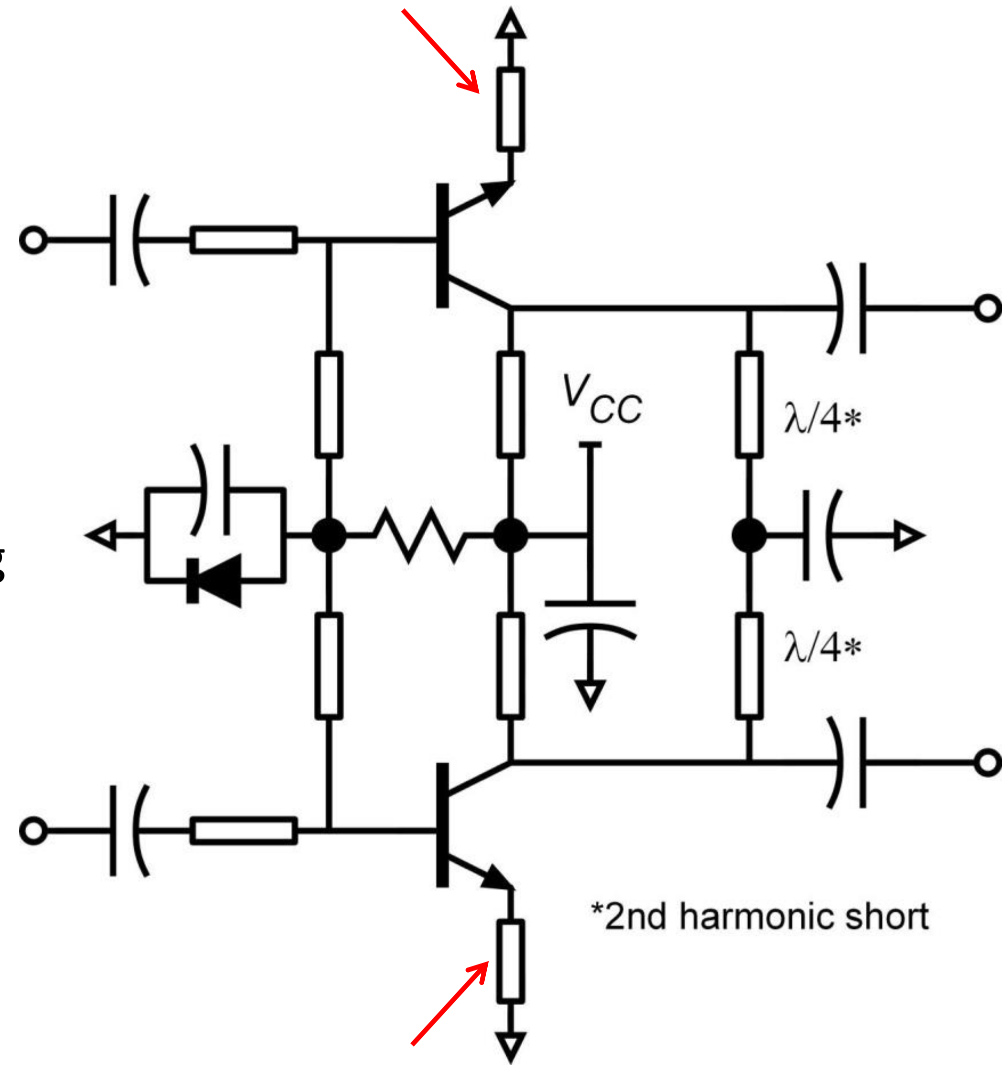




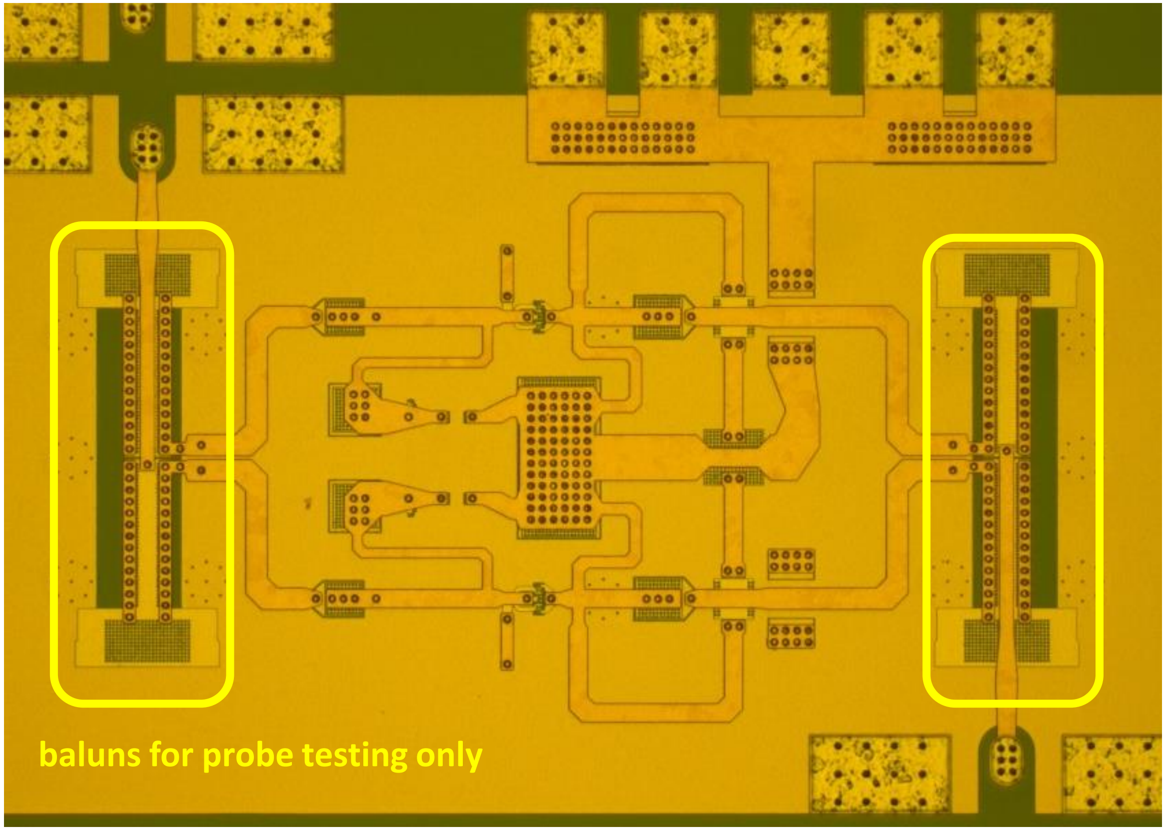
High dynamic range IF amplifier

low noise figure
high third-order intercept
low/moderate gain

Common-emitter
Pseudo-differential
Strong inductive degeneration
- high IP3.
- partly converges noise & S_{11} tuning

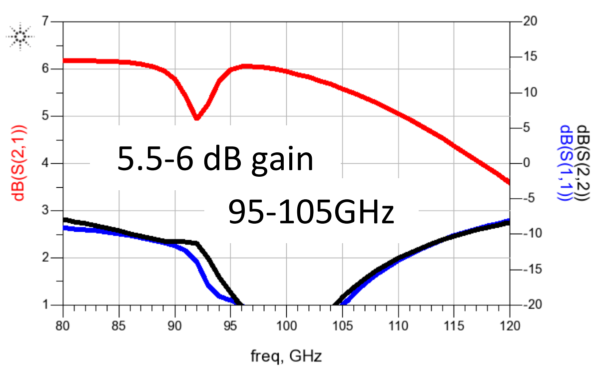


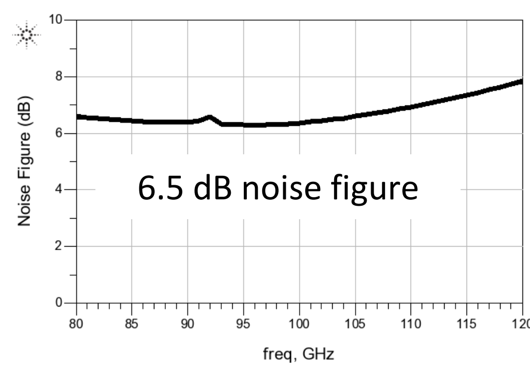
First IF Amplifier

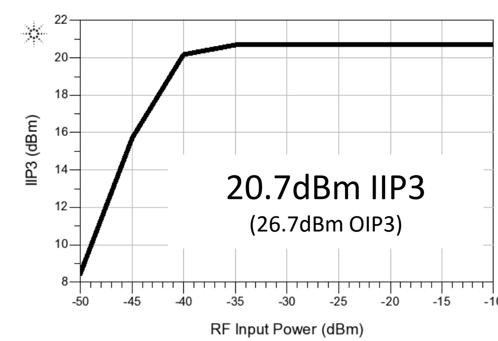


WITHOUT PADS: 551 um X 575 um,
100 mW DC power

Simulations

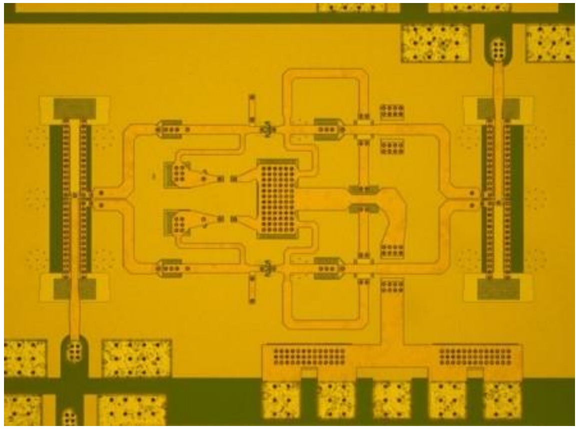


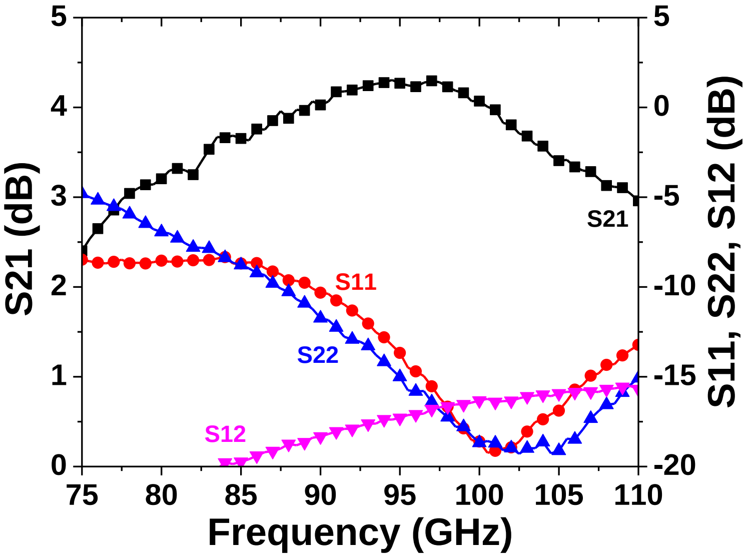




IF Amplifier measurement results

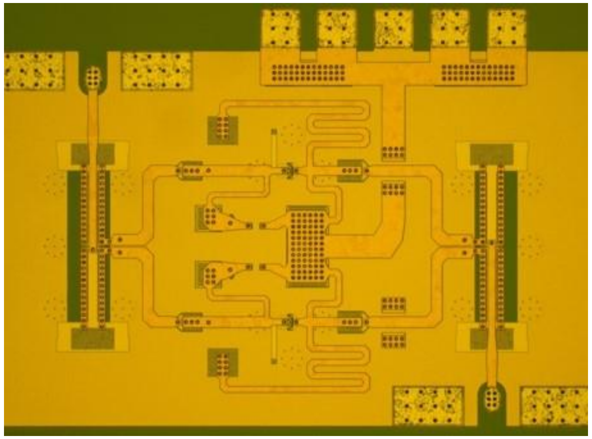
Low-gain (high-IIP3) design

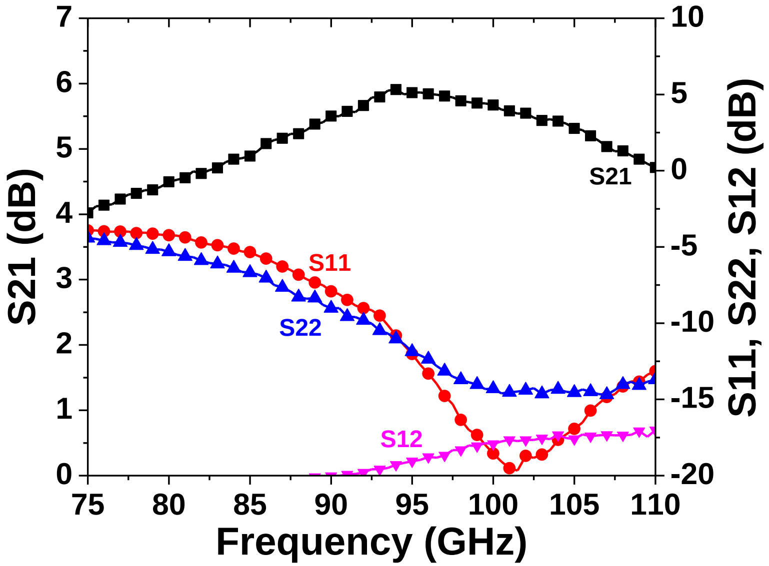




Power consumption: 94 mA @ 2 V
Peak gain: 4.3 dB @ 95 GHz, 4.0 dB @ 100 GHz

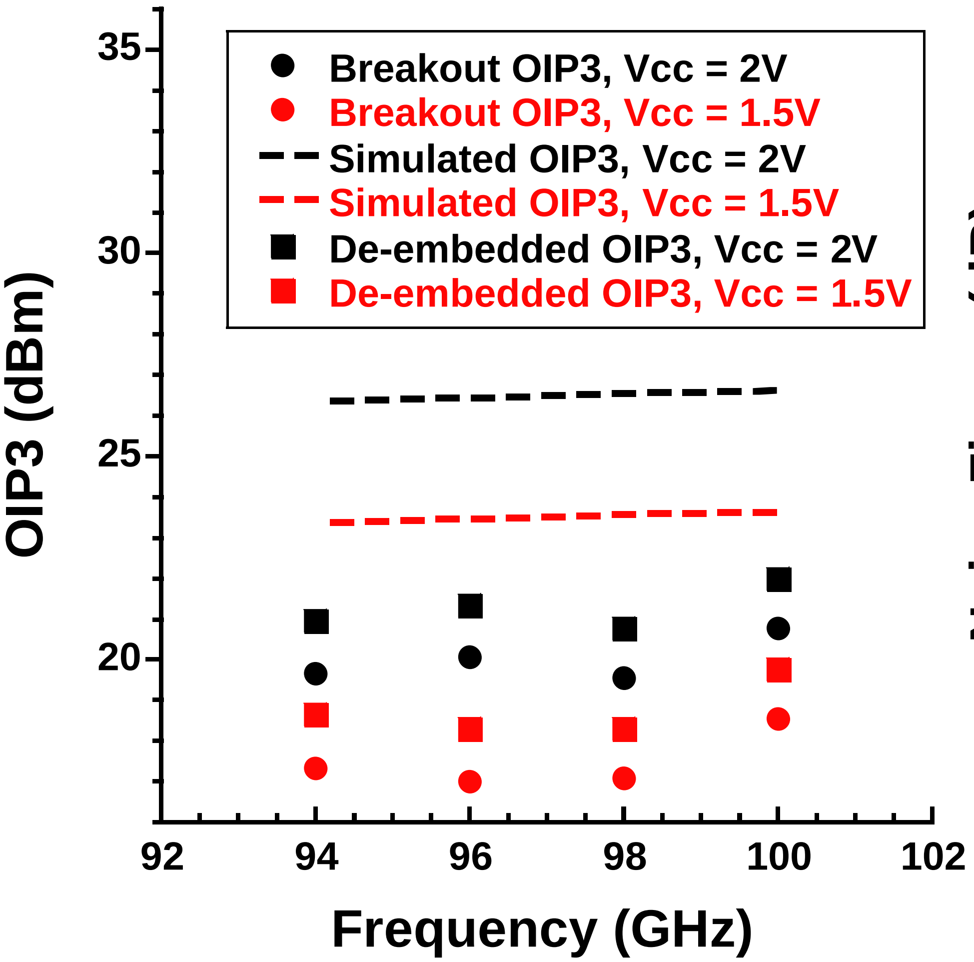
Low-gain (high-IIP3) design

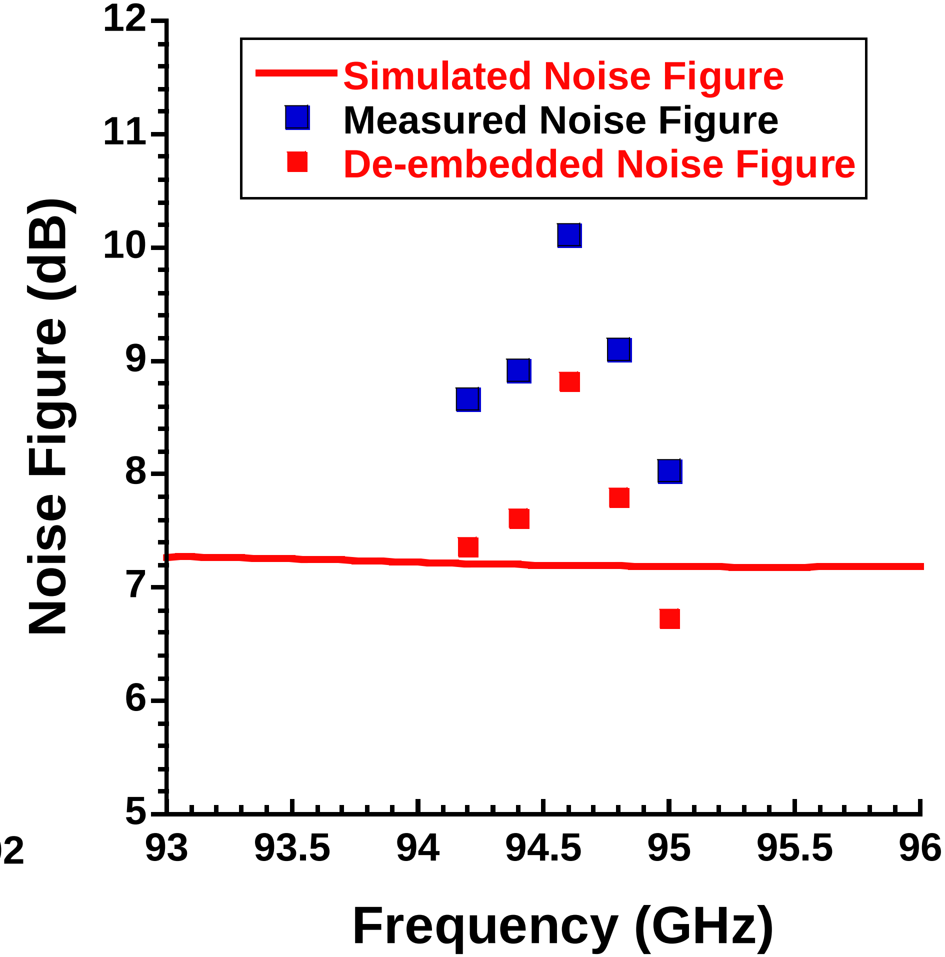




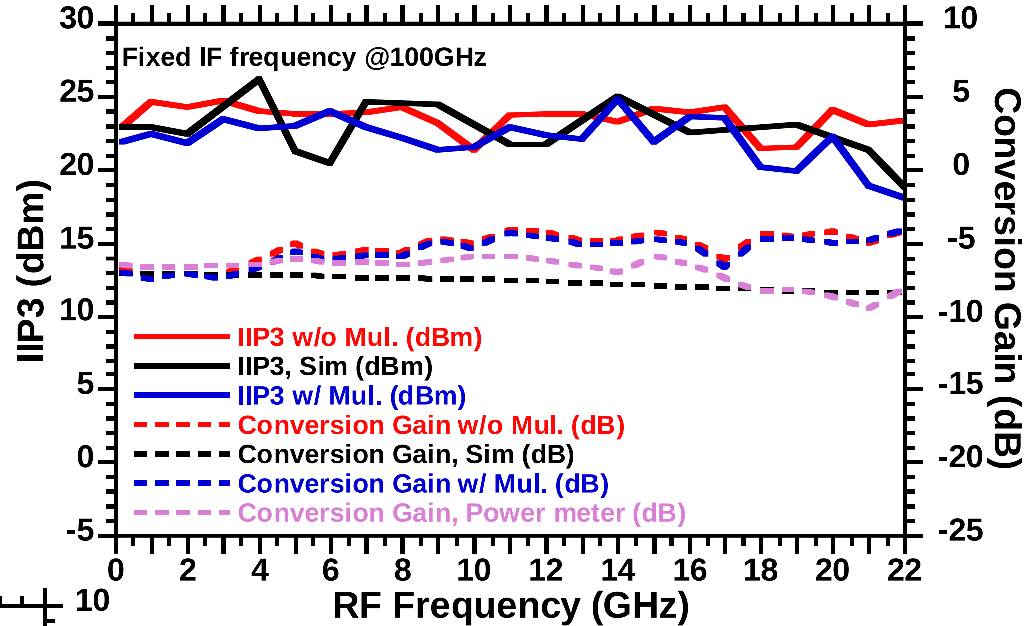
Power consumption: 97 mA @ 2 V
Peak gain: 5.9 dB @ 95 GHz, 5.7 dB @ 100 GHz

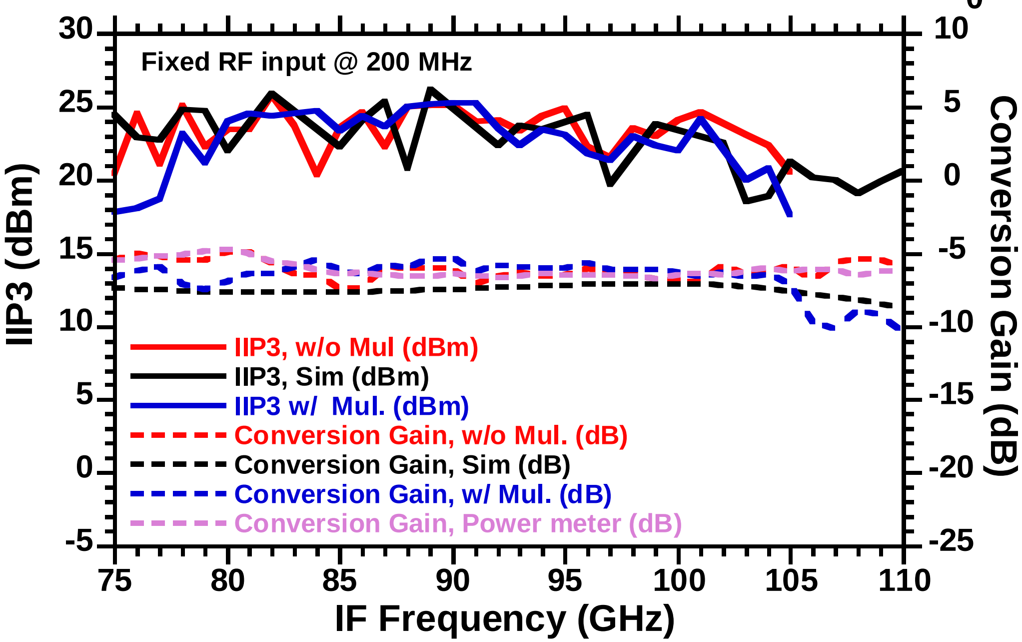
IF Amplifier measurement results



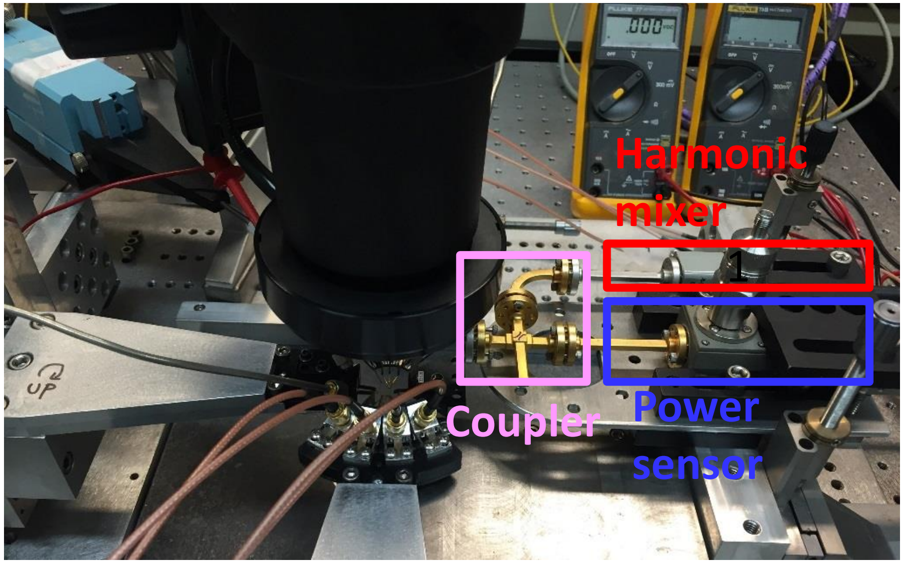


Performance: upconversion block





Upconversion measurement: Gain, IM3

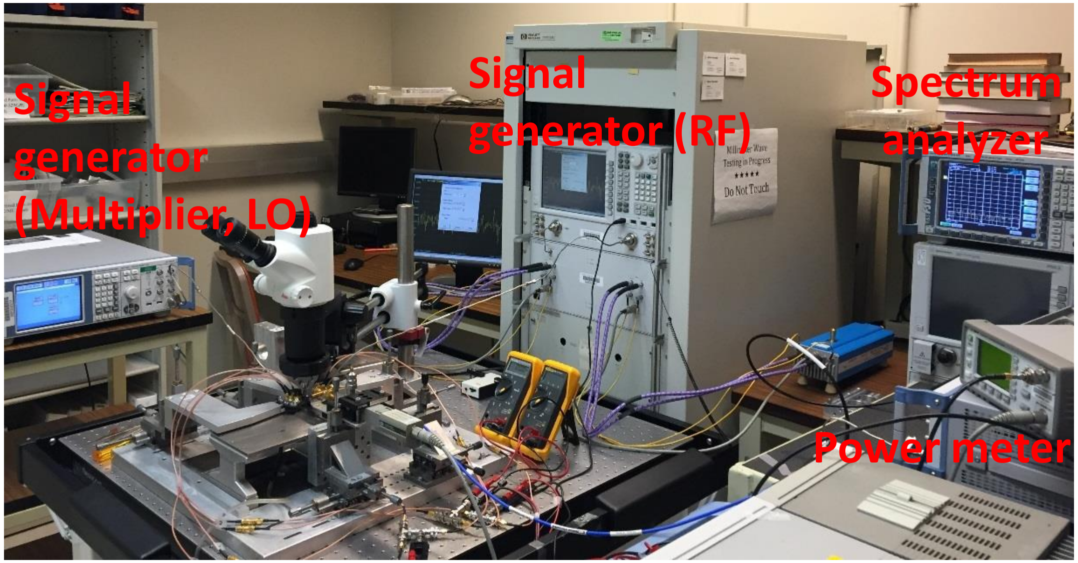


Harmonic mixer
LO = (RF+IF)/n

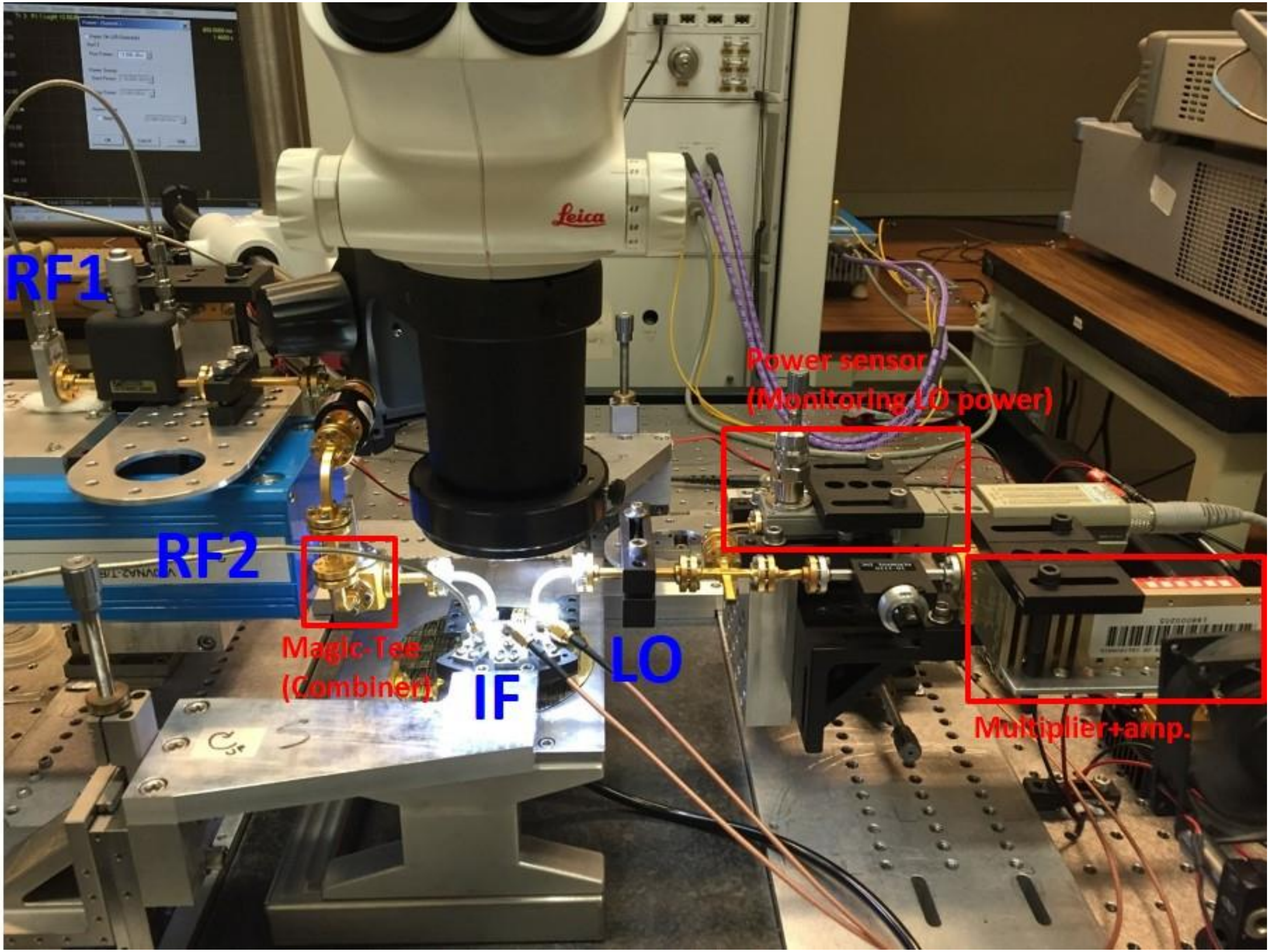
In our test:
n=10 and IF = 1 GHz

Frequency measurement: Harmonic mixer
Power measurement: power meter

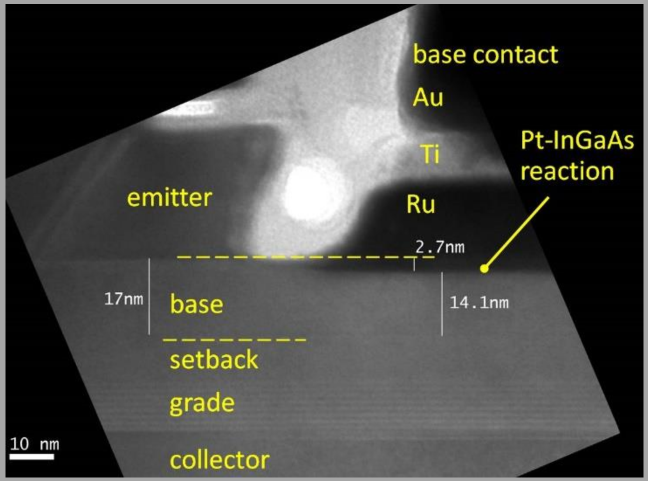
*Harmonic mixer LO frequency was adjusted to measure LO feedthrough (Harmonic mixer IF =1 GHz)

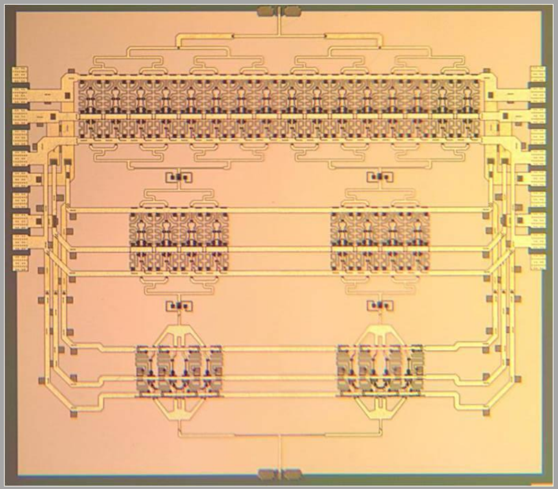


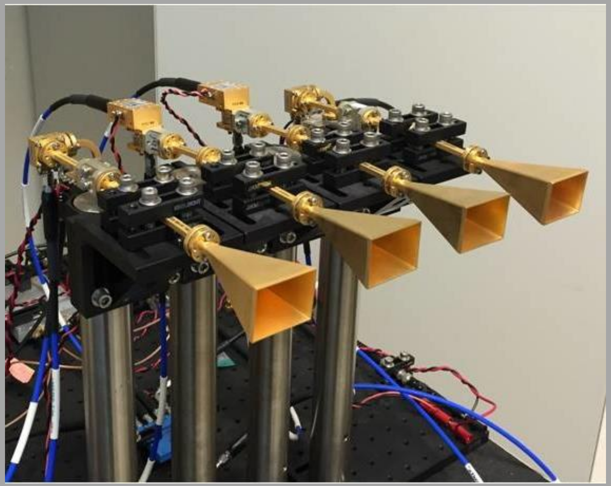
Downconversion measurement: IP3



mm-Wave Wireless

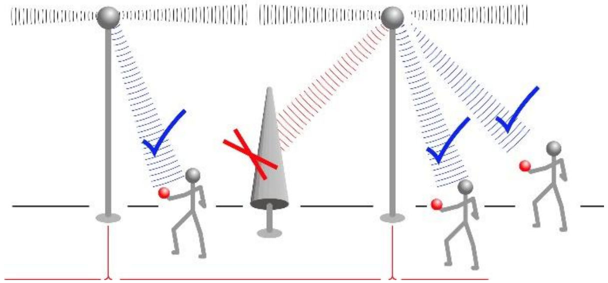


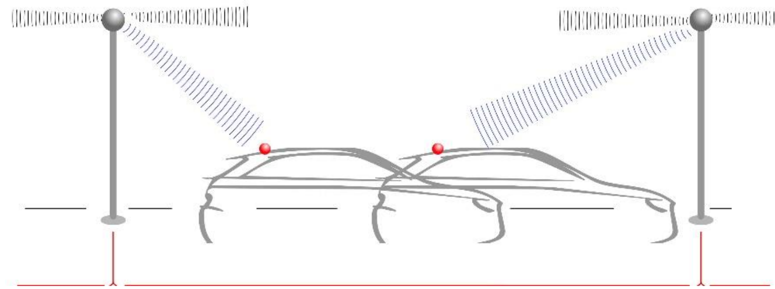




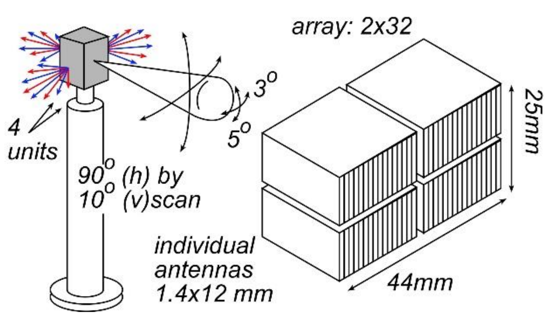
mm-Wave Wireless Electronics

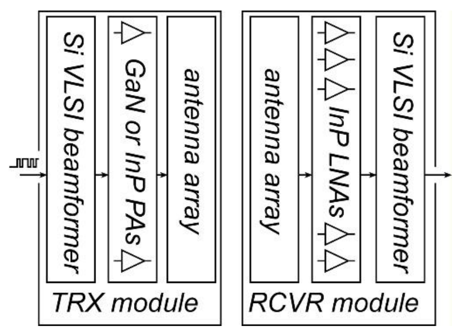
Mobile communication @ 2Gb/s per user, 1 Tb/s per base station





Requires: large arrays, complex signal processing, high P_{out}, low F_{min}





VLSI beamformers
VLSI equalizers
III-V LNAs & PAs (?)

(backup slides follow)