Making better transistors: beyond yet another new materials system

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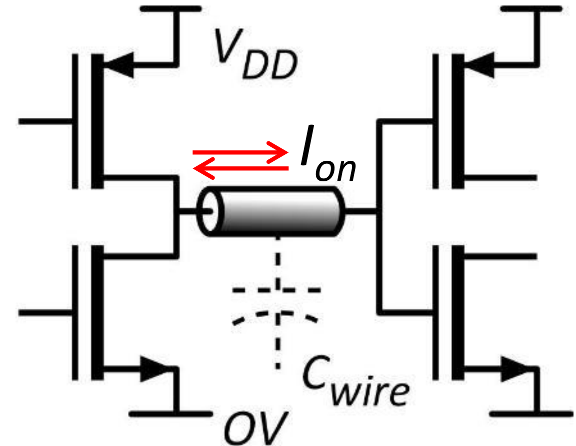
What does VLSI need ?

Small transistors: plentiful, cheap

Small transistors→ short wires

small delay CV_{DD}/I

low switching energy $CV_{DD}^2/2$



Large on-currents

small delay CV_{DD}/I

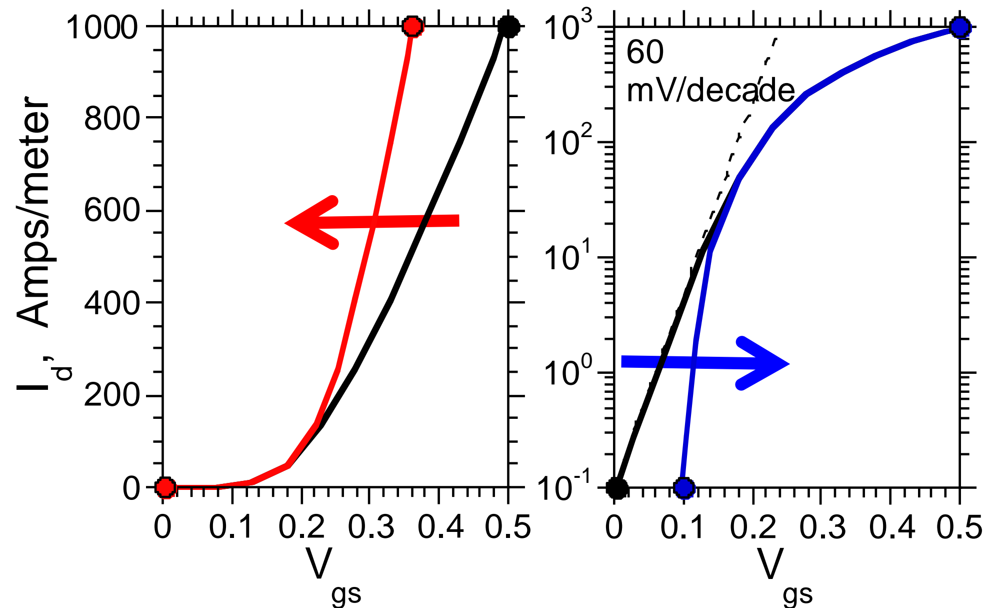
Low supply voltages

low energy $CV_{DD}^2/2$

Low leakage current

thermal: $I_{off} > I_{on}*\exp(-qV_{DD}/kT)$

want low V_{DD} yet low I_{off}.



Transistor Research

Make the switch smaller (scaling)

Make it from different materials

Change its shape

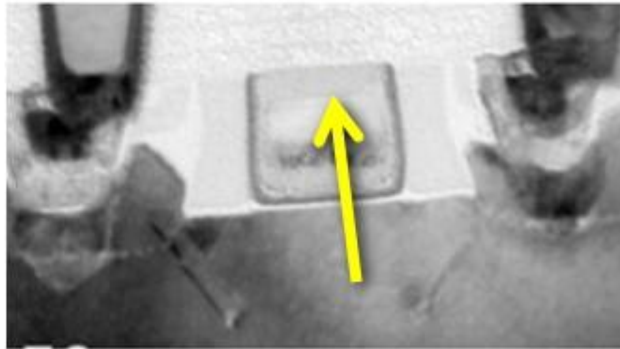
Change its internal operation:

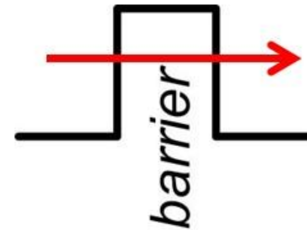
bandgap engineering

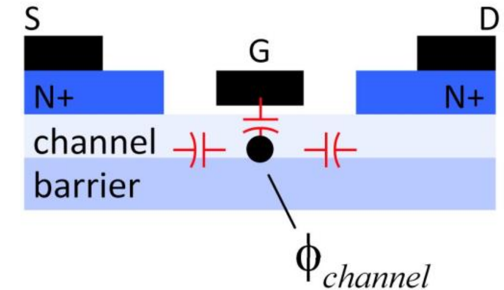
Change what we do with it.

We can't make MOSFETs much smaller

Tunneling: can't make gate insulator any thinner

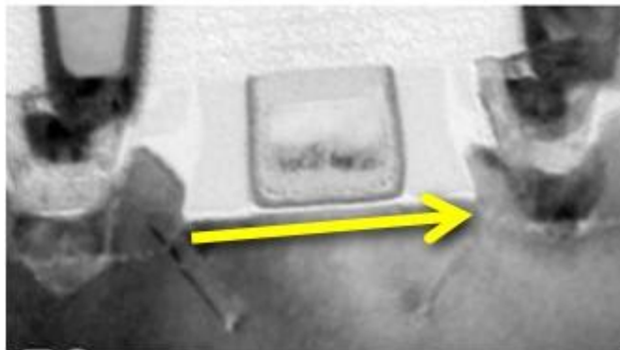


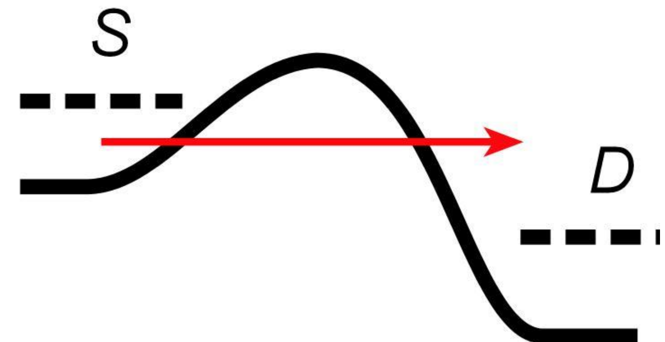




→ smaller devices have poor electrostatic control, don't turn off

Tunneling: can't make channel much shorter





→ smaller devices have high source-drain tunneling, don't turn off

Expensive lithography: EUV, multiple patterning

New Materials: III-V semiconductors ?

S. Lee *et al.*, VLSI Symp. 2014

L_g~25 nm

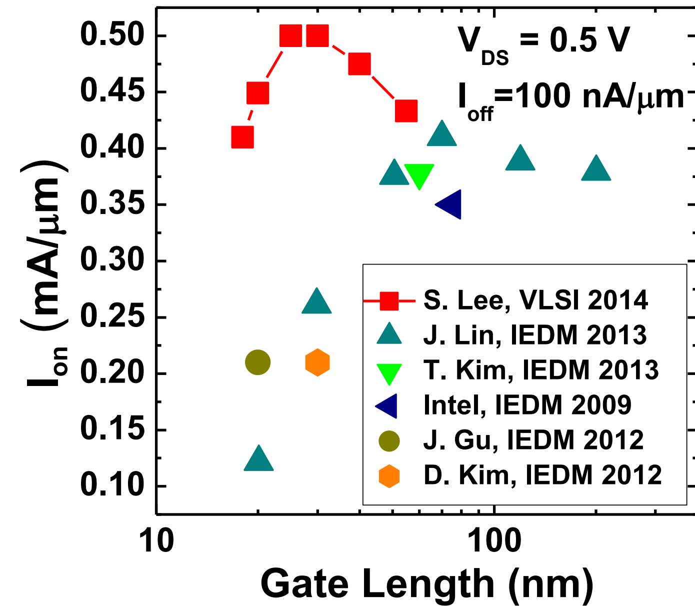
2.7 nm InAs channel (strained)

2.5 nm ZrO_2

1 nm $Al_2O_xN_y$

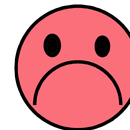
N+ S/D

Vertical Spacer



record for III-V

= best UTB SOI silicon



New Materials: 2-D semiconductors ?

Does 1-atom-thick channel help ?

2D or 3D: the gate oxide won't scale

the oxide sets a minimum gate length

1-atom-thick channels don't help much

If oxides won't scale, we must make fins

with 2D, **can we make fins** ?

later, will need to make nanowires...

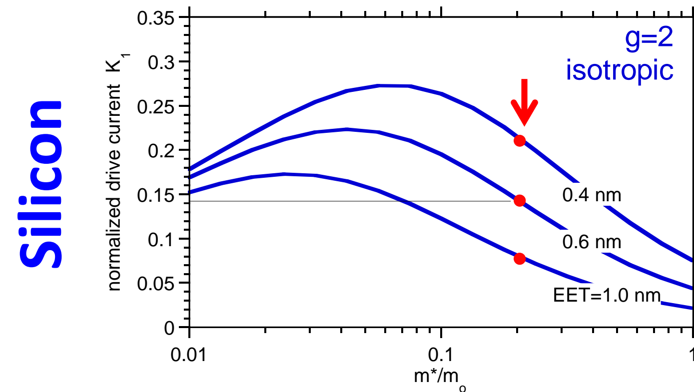
Ballistic drive currents don't win either

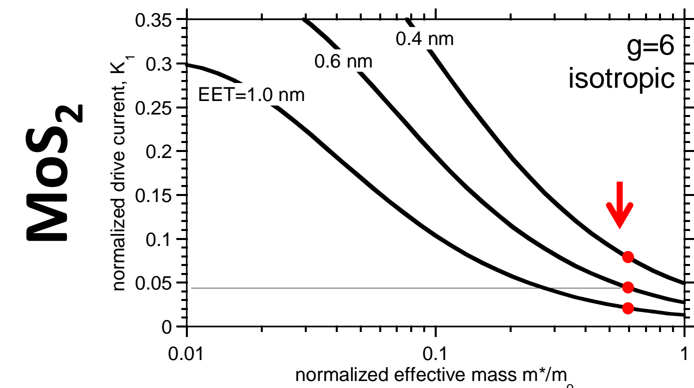
high m*, and/or high DOS

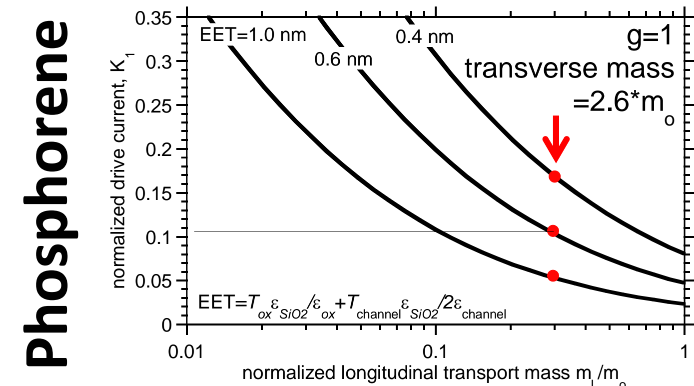
mobility sufficient for ballistic ?

$$J = K \cdot \left(84\frac{\text{mA}}{\mu\text{m}}\right) \cdot \left(\frac{V_{gs} - V_{th}}{1\,\text{V}}\right)^{3/2},$$

$$\text{where } K = \frac{g \cdot (m_\perp^{1/2} / m_o^{1/2})}{\left(1 + (c_{dos,o} / c_{equiv}) \cdot g \cdot (m_\perp^{1/2} m_\parallel^{1/2} / m_o)\right)^{3/2}}$$







When it gets crowded, build vertically

Los Angeles: sprawl

Manhattan: dense

2-D integration:
wire length $\propto$ # gates$^{1/2}$

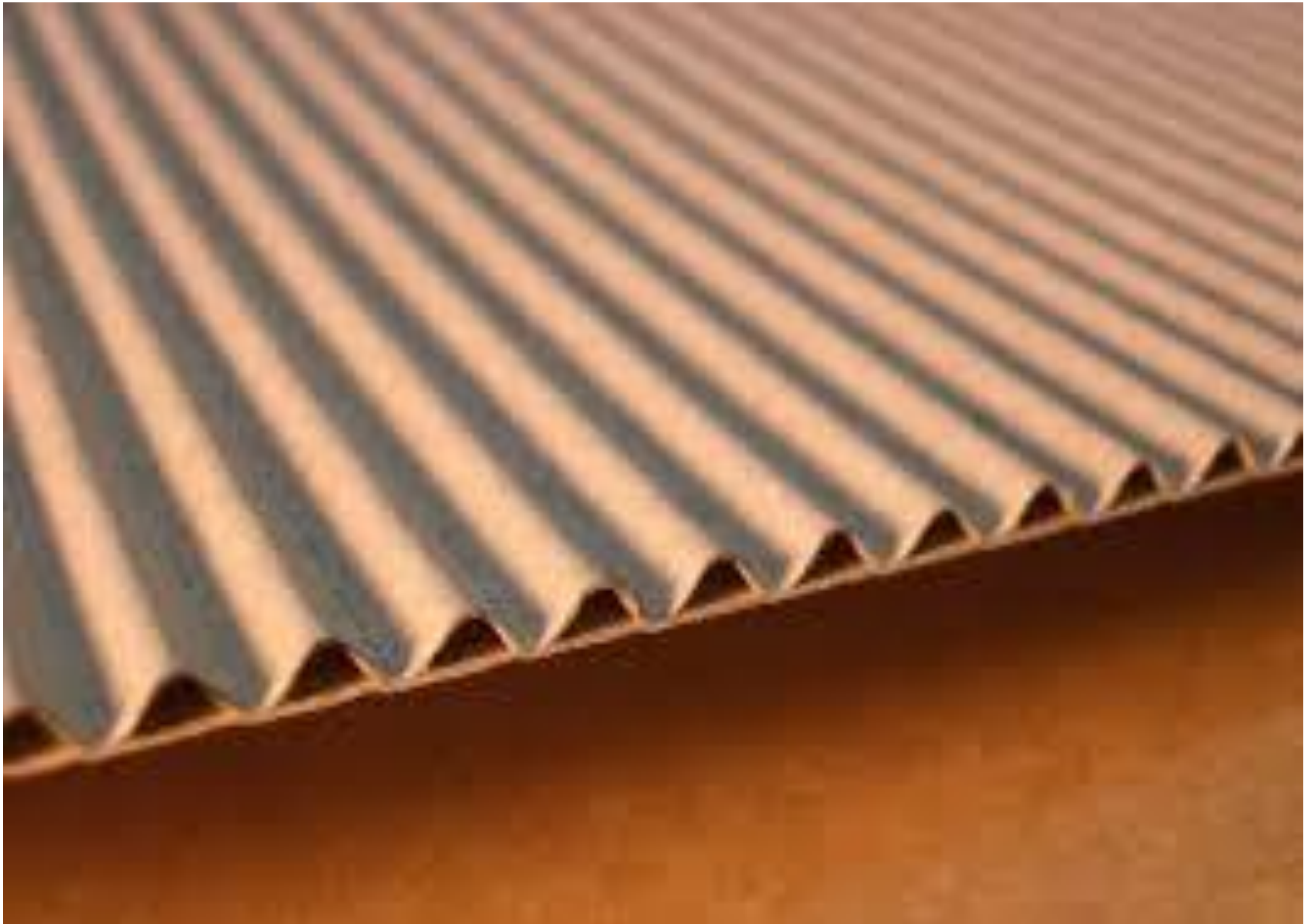
3-D integration:
wire length $\propto$ #gates$^{1/3}$

LA is interconnect-limited

1) Chip stacking (skip)

2) 3D transistors: corrugation (change the shape)

Corrugated surface→ more surface per die area

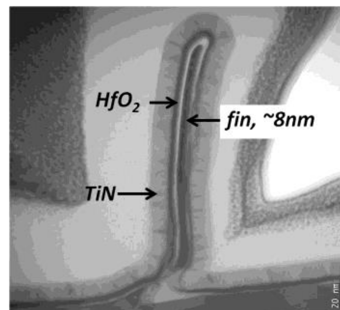


Corrugated surface→ more current per unit area

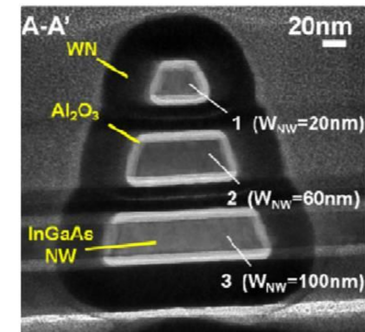
channel
N+ S/D
gate

planar **fin** **tall fin** **"4-D"**

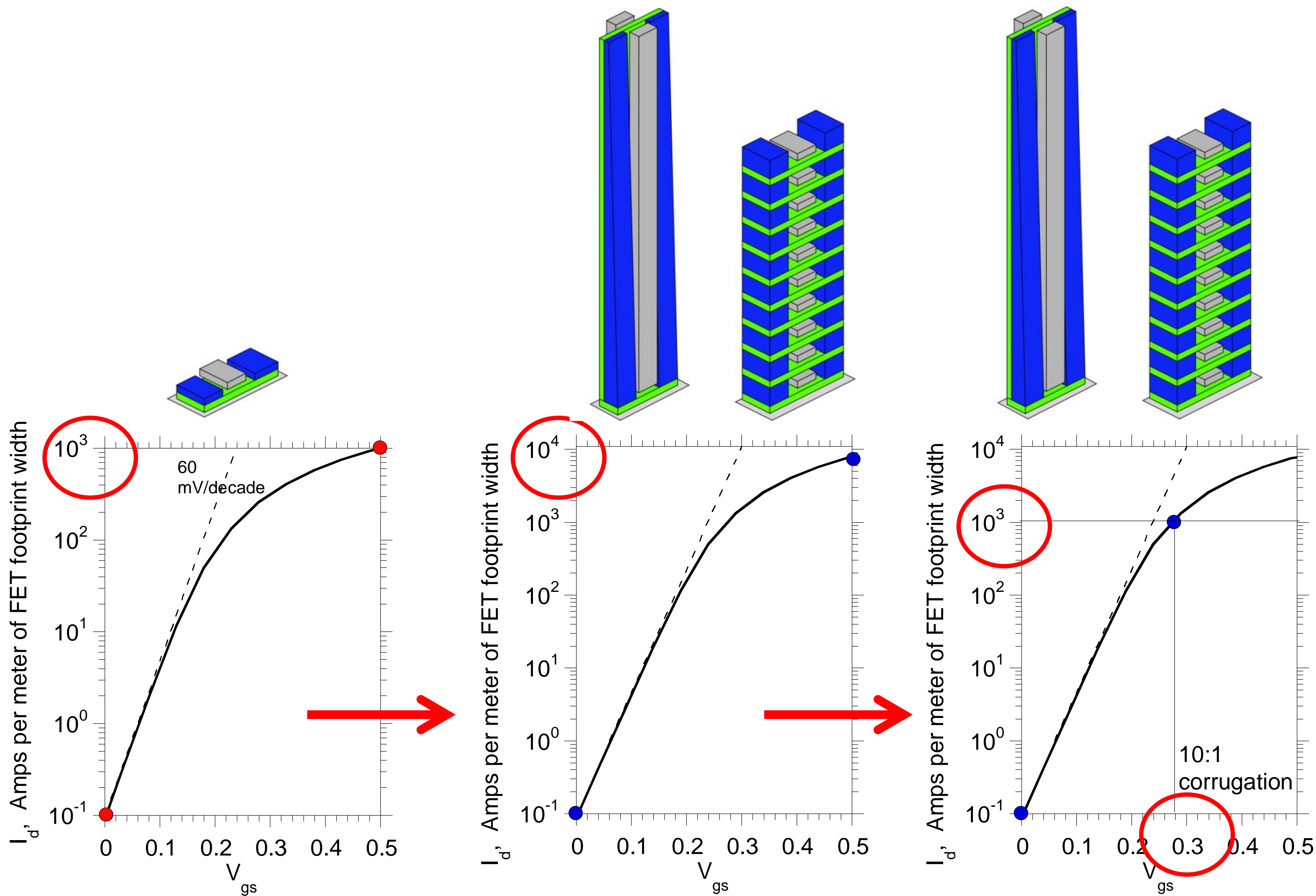
Cohen-Elias *et al.*,
UCSB
2013 DRC



J .J. Gu *et al.*, 2012 DRC,
Purdue
2012 IEDM



Corrugation: same current, less voltage, less CV^2



Forming tall fins by sidewall regrowth (ugly)

fin template
SiN mask
etch stop layer
InP template; (011) facet

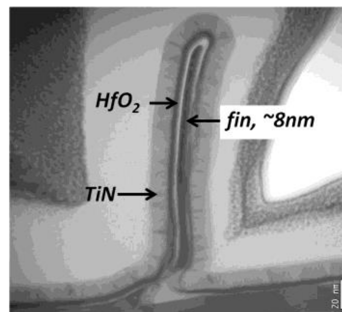
channel ALE
ALE InGaAs

dummy gate
HSQ mask

S/D regrowth
N+ InGaAs source / drain

remove masks

release fins
transistor footprint width
height
fin pitch

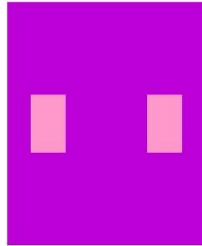


Cohen-Elias *et al.*, 2013 DRC

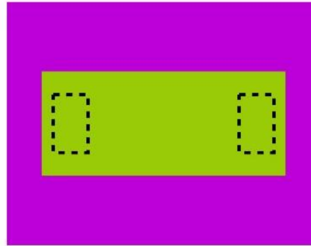
Confined Epitaxial Lateral Overgrowth

blanket SiO_2

holes in SiO_2

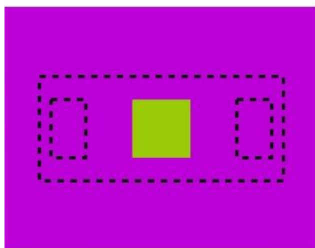


ALD Al_2O_3, pattern

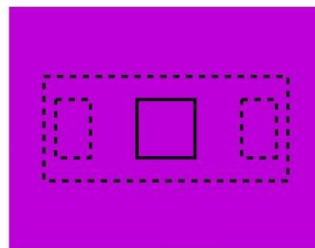


L. Czornomaz et. al, (IBM) 2015 & 2016 VLSI Symposia

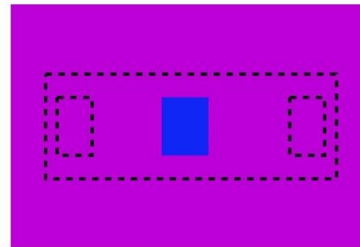
ALD SiO_2, pattern

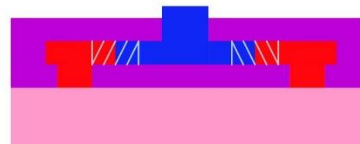


strip Al_2O_3



grow semiconductor

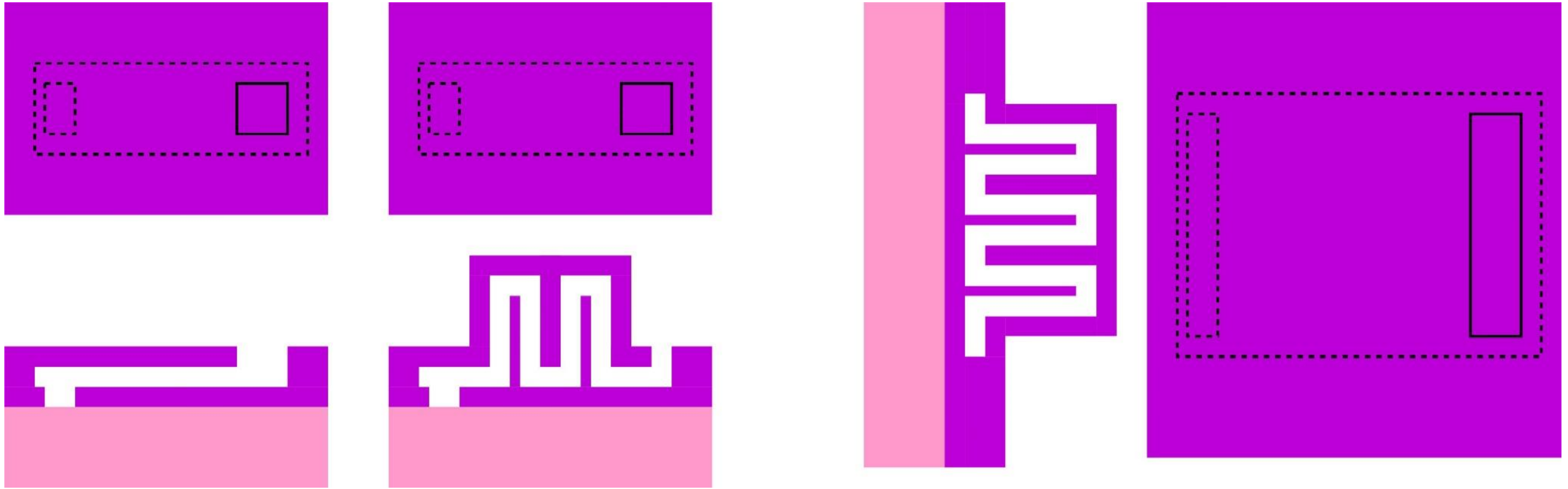




Semiconductor regrowth into hollow glass boxes formed on wafer surface

Semiconductor thicknesses controlled by ALD layer thickness: atomic precision

CELO: Can we grow 3-D structures ?

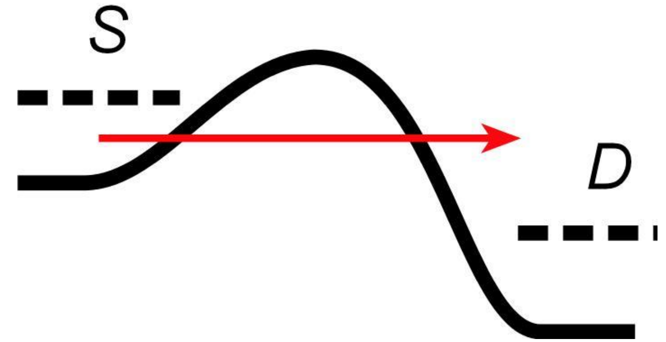


With a few process tricks,
can we make growth templates for 3-D structures ?

Fixing source-drain tunneling by increasing mass ?

Source-drain tunneling leakage:

$$I_{off} \cong \exp(-2\alpha L_g),\ \text{where } \alpha \cong \hbar^{-1}\sqrt{2m^*(qV_{th})}$$

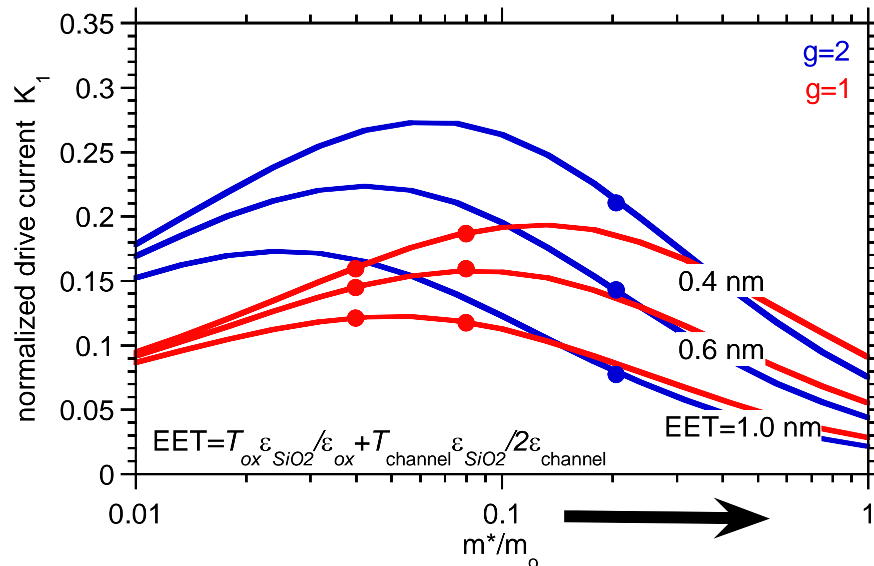


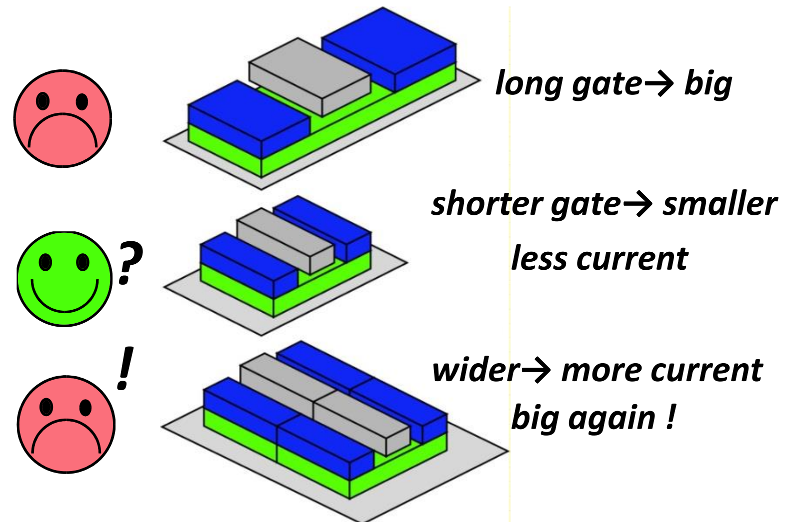
Fix by increasing effective mass ?

$$\alpha L_g = \text{constant} \rightarrow m^* \propto 1/L_g^2$$

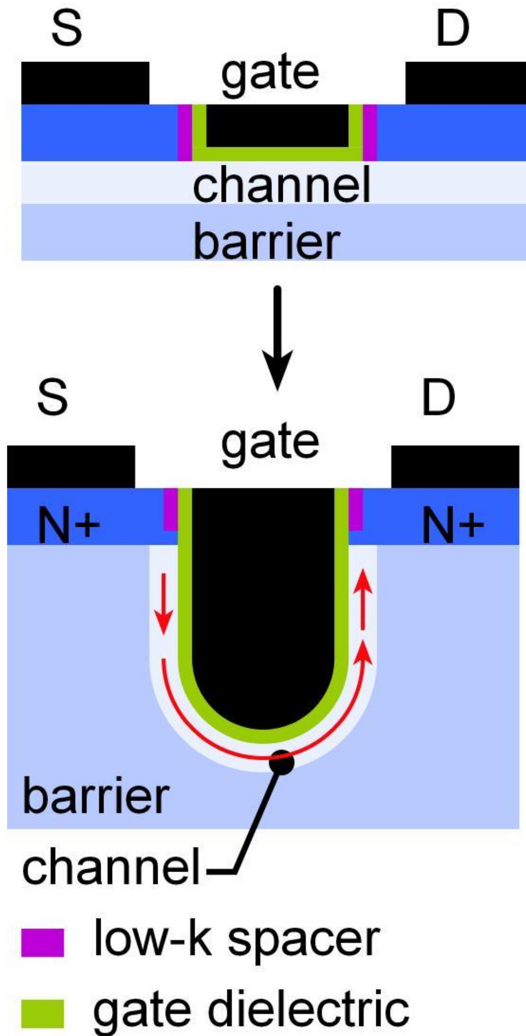
This will decrease the on-current:

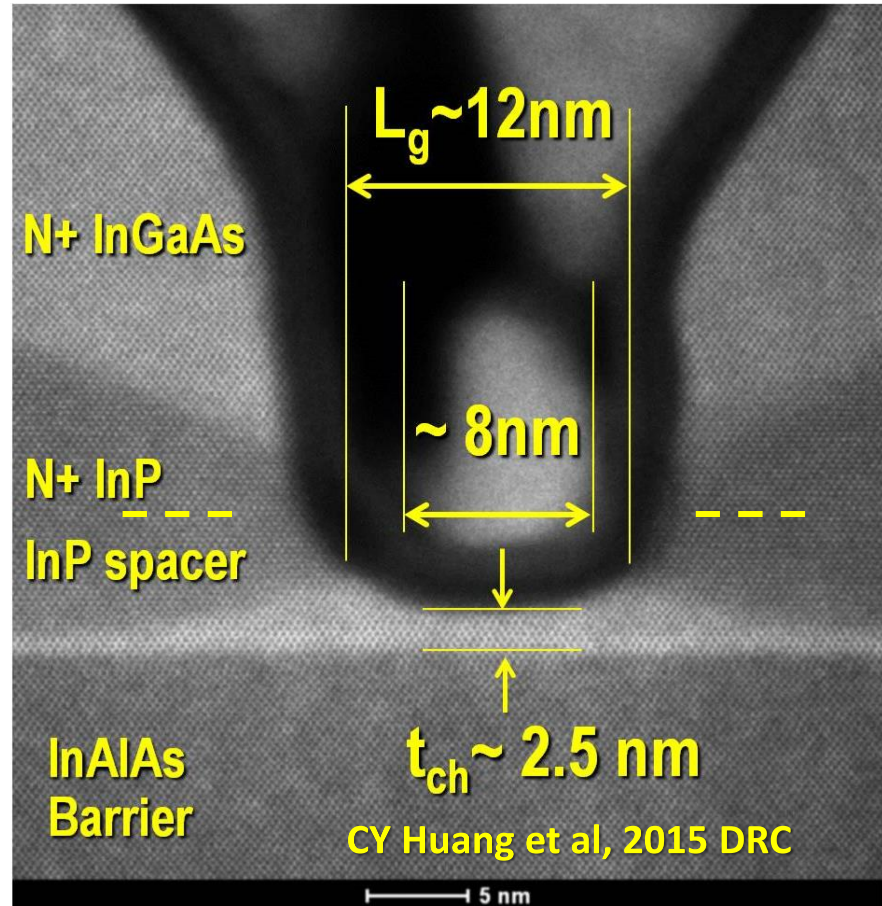
(also increases transit time)





Fixing source-drain tunneling by corrugation





Transport distance > gate footprint length
Only small capacitance increase

Fixing source-drain tunneling by corrugation ?

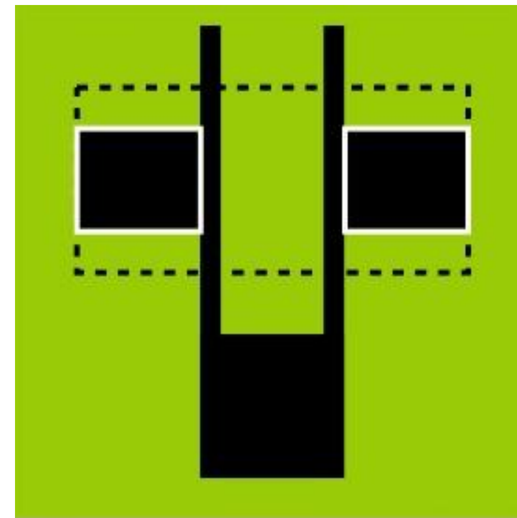
CELO growth over ridge

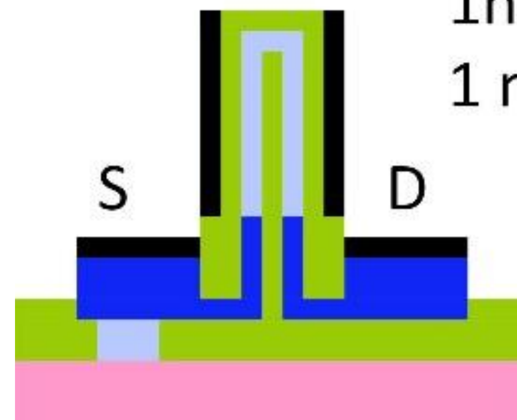
3D structure

transport length >> footprint

improves electrostatics
...like finFET

improves S/D tunneling
...unlike finFET

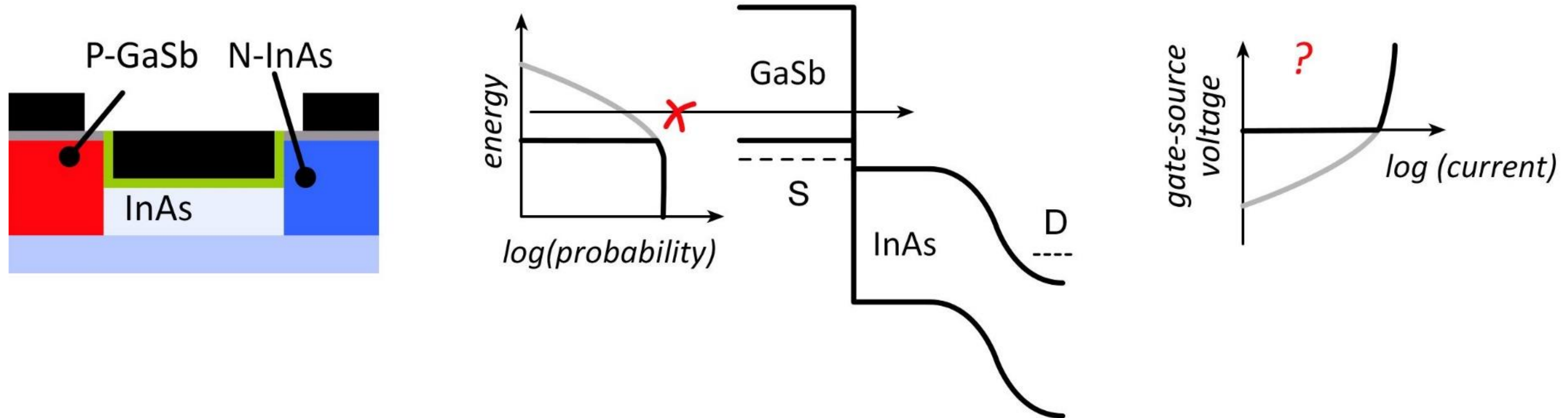




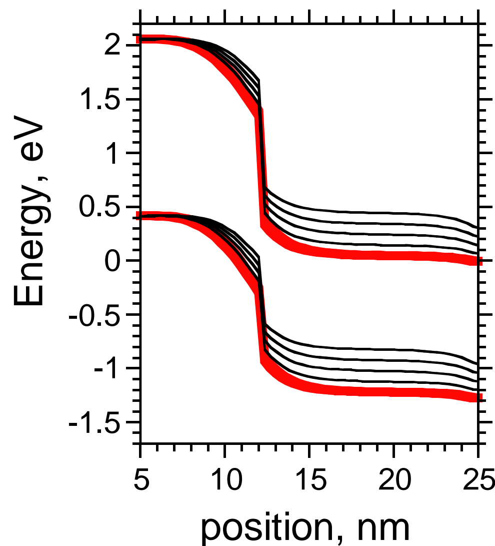
Gate oxide is SiO_xN_y, not HfO_2 → thinner @ given leakage
How to reduce gate footprint below ~5nm ?

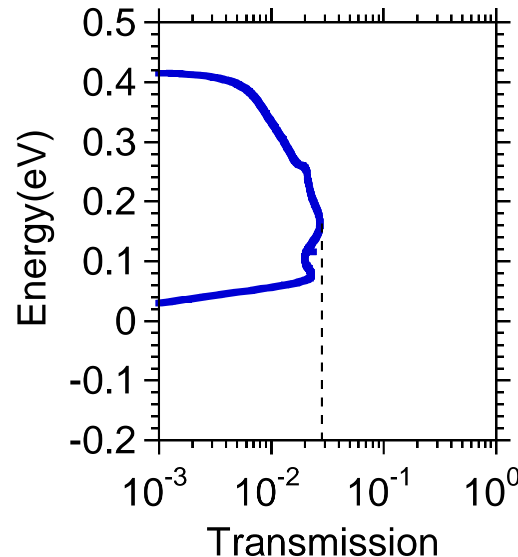
Changing the band structure: tunnel FETs

TFET: bandgap of p-type source truncates source thermal distribution:



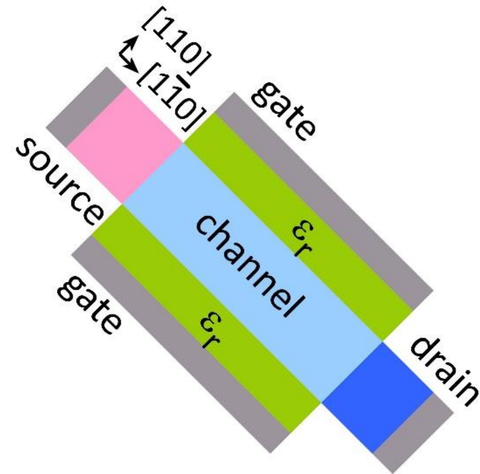
Problem: 4-6nm tunnel barriers→ ~3% tunneling probability→ **very low current**.

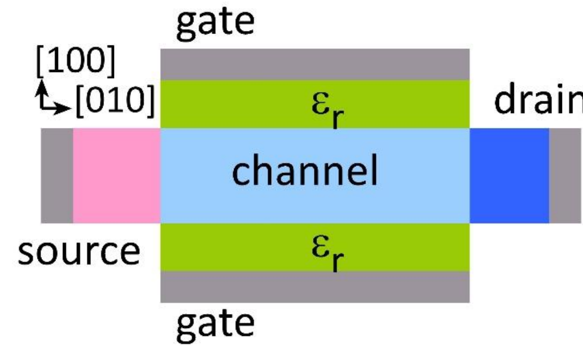


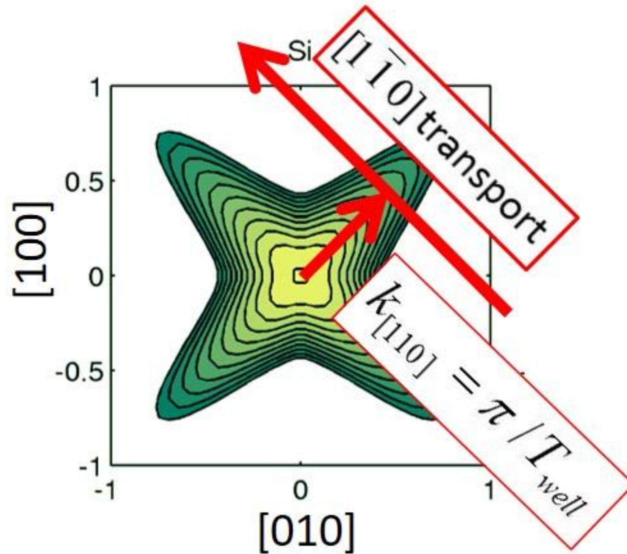


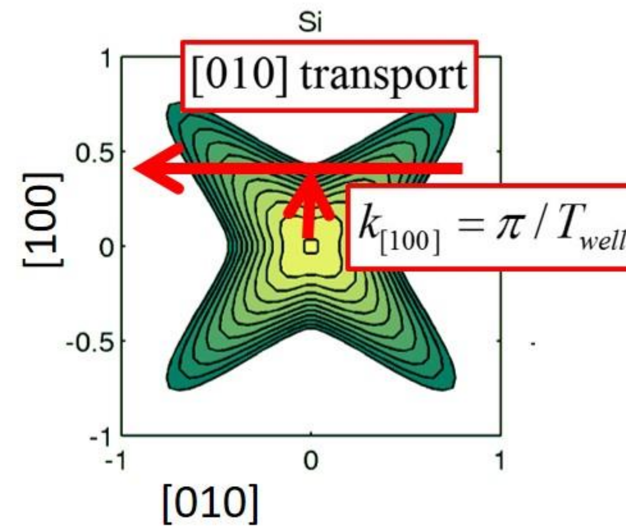
[110] gives more on-current than [100]

P. Long *et al.*, EDL 3/2016









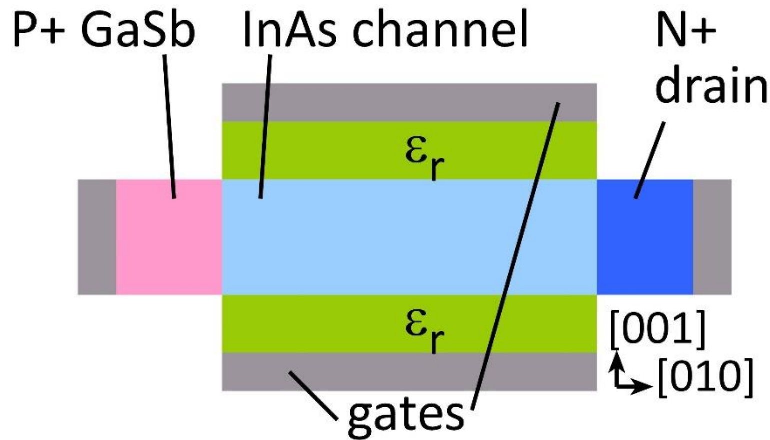
valence band

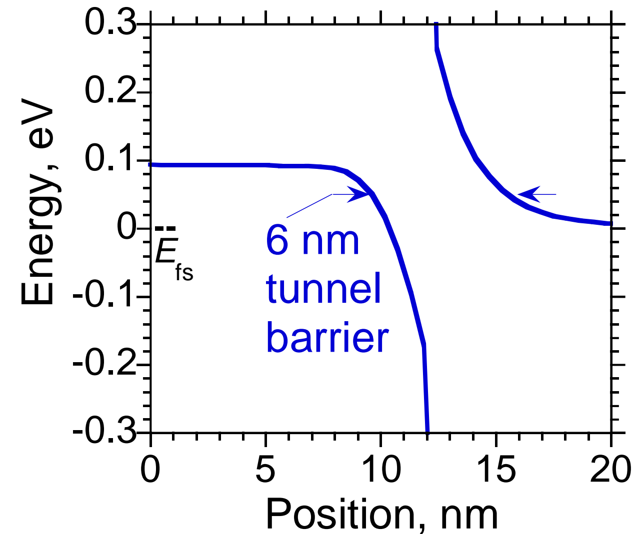
high confinement mass
low transport mass

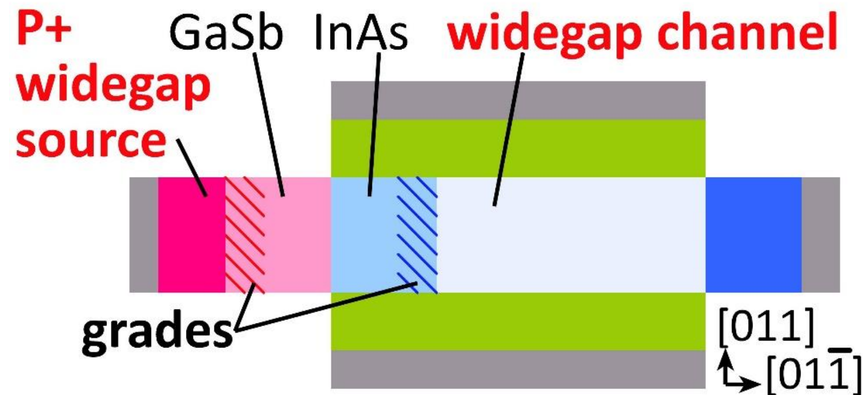
low confinement mass
high transport mass

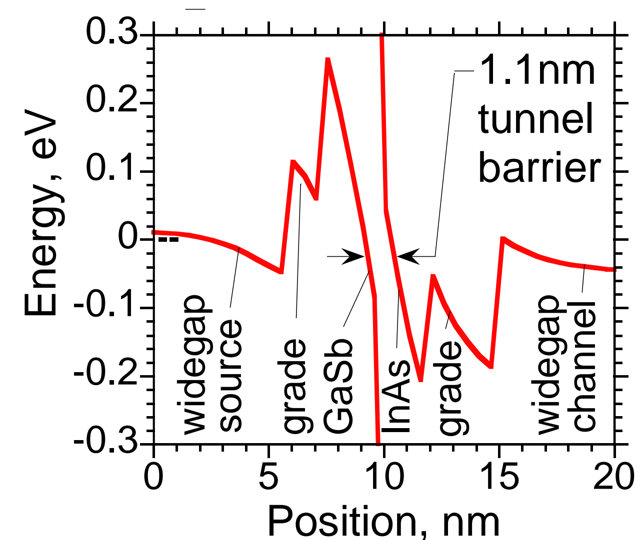
Add more Heterojunctions: much more current.

Source HJ: S. Brocard, *et al*., EDL, 2/2014; Channel HJ: P. Long *et al*., EDL 3/2016



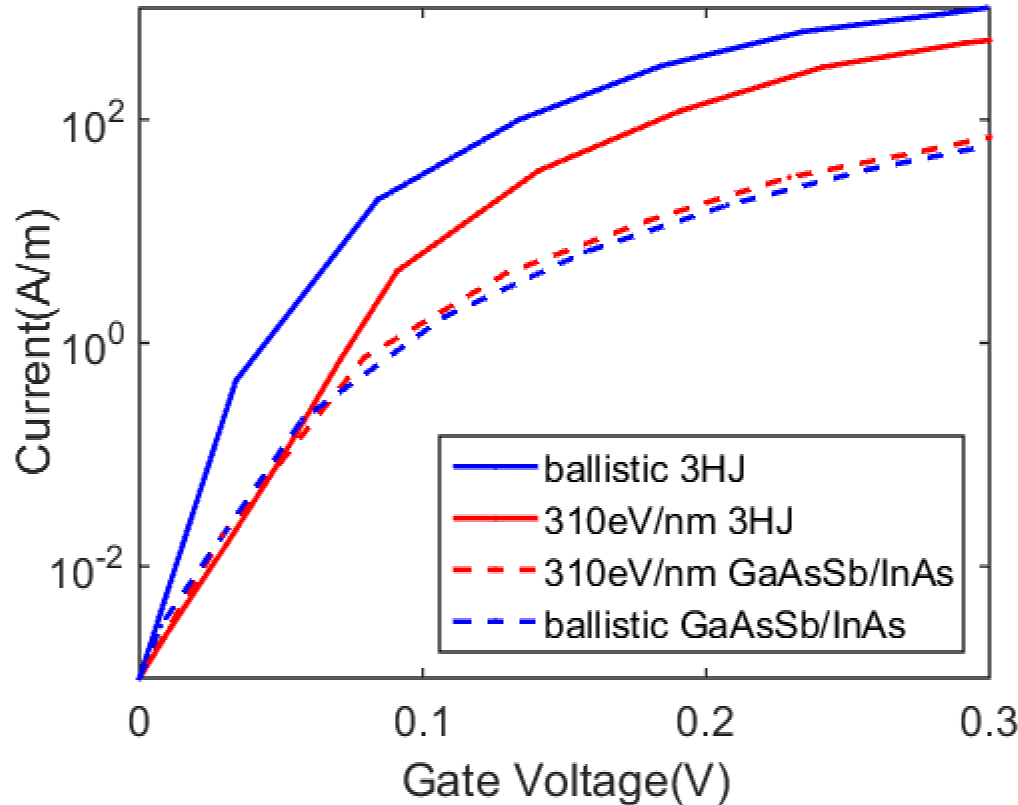






Added heterojunctions→ greater built-in potential→greater field→ thinner barrier → higher tunneling probability (~80%)→ 30:1 more current.

3HJ still have higher ON/OFF ratio than GaAsSb/InAs



3HJ 516A/m

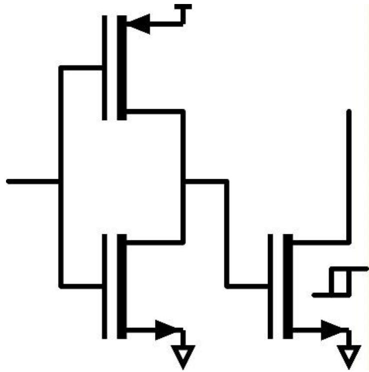
GaAsSb/InAs 75A/m

P. Long, J. Huang,
M. Povolotski: Purdue, Unpublished

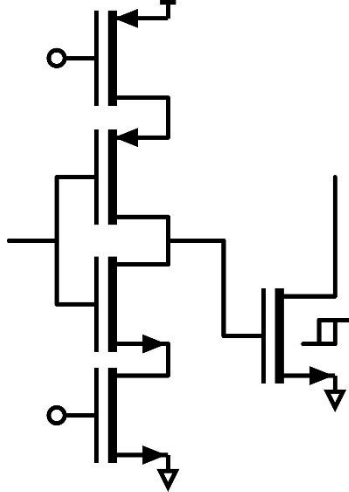
3HJ still have higher ON/OFF ratio than GaAsSb/InAs when acoustic and non-polar optical phonon scattering are considered.

Changing the function: ferroFETs ?

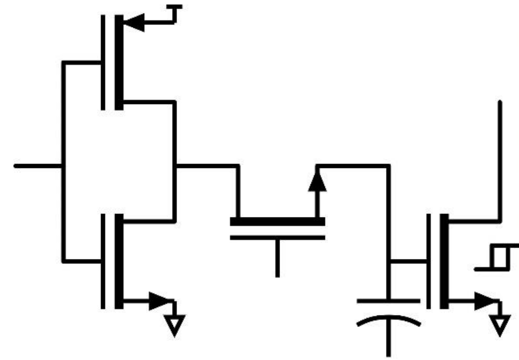
This won't work



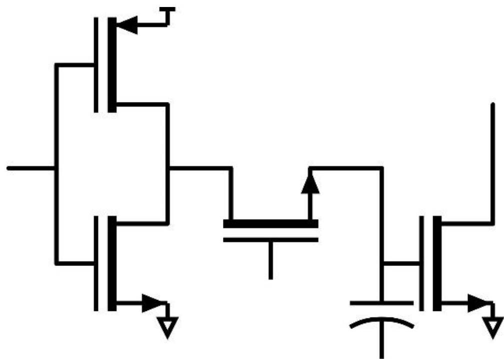
need tri-state driver



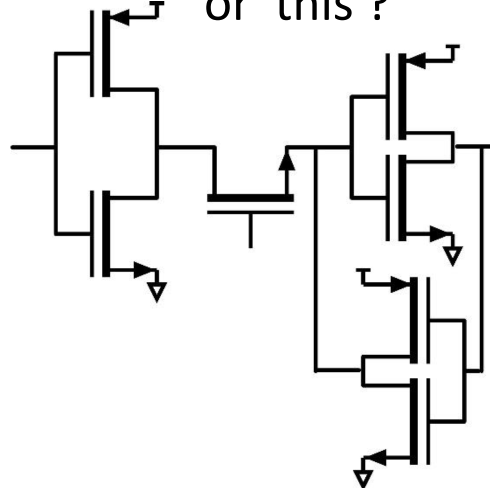
or an input switch.



why not this ?



or this ?



Multiple Supplies for Low-Power Logic

0.2V 0.5V 0.5V 0.5V 0.2V

C_{wire} C_{wire}

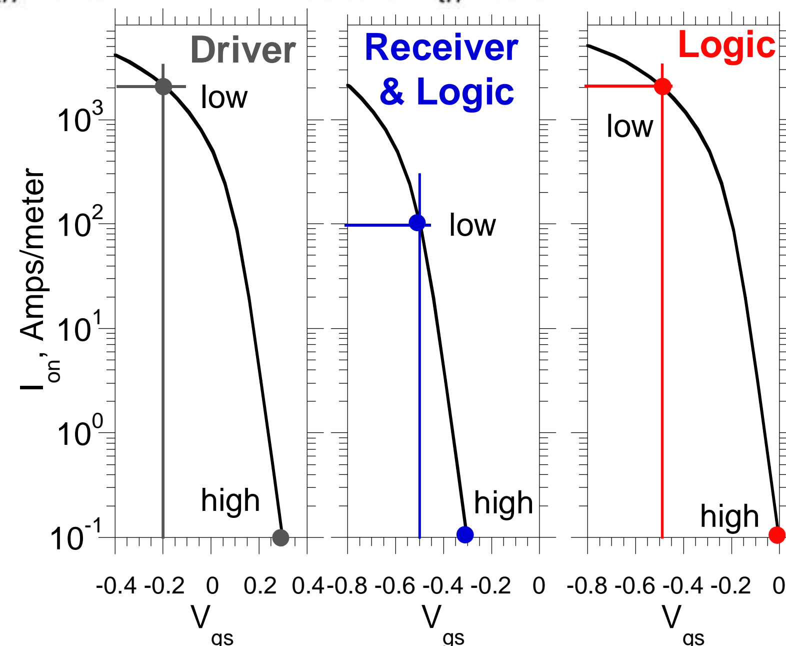
+0.5V 0V | +0.2V 0V | +0.5V 0V | +0.5V 0V | +0.5V 0V | +0.2V 0V

drivers	receiver & logic	logic	driver & logic
PMOS V_{th}=0V	PMOS V_{th}=-0.6V	PMOS V_{th}=-0.3V	PMOS V_{th}=0V
NMOS V_{th}=0.3V	NMOS V_{th}=0.3V	NMOS V_{th}=0.3V	NMOS V_{th}=0.3V

Given 200 mV swings on long interconnects,

Line receivers provide 0.1 mA/μm output with 0.1 μA/μm leakage

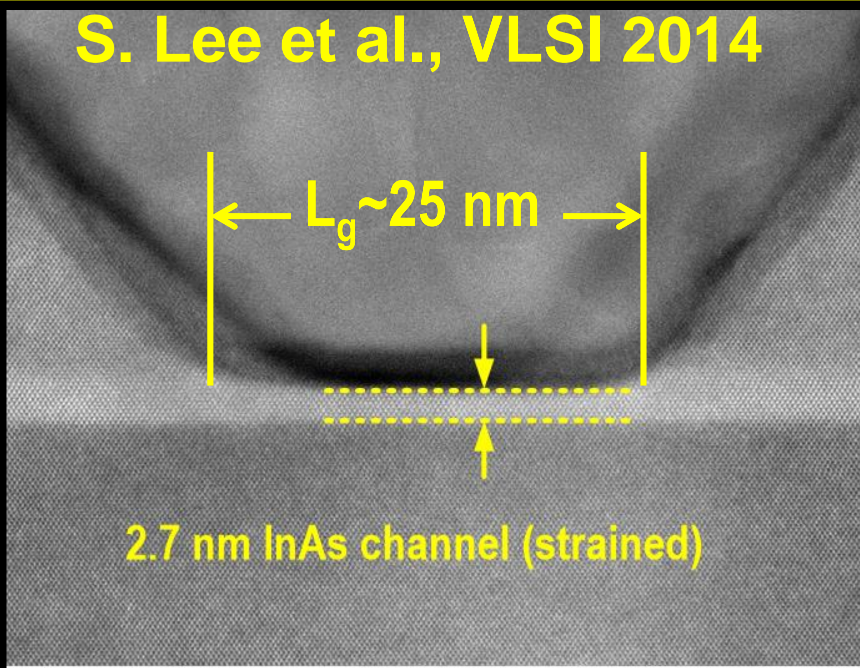
Line drivers, and logic gates provide 3 mA/μm output with 0.1 μA/μm leakage

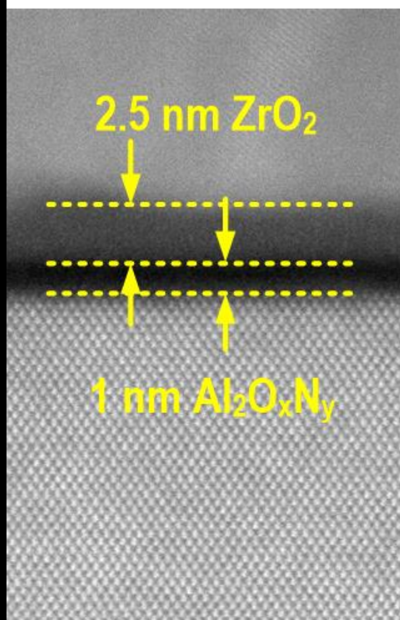


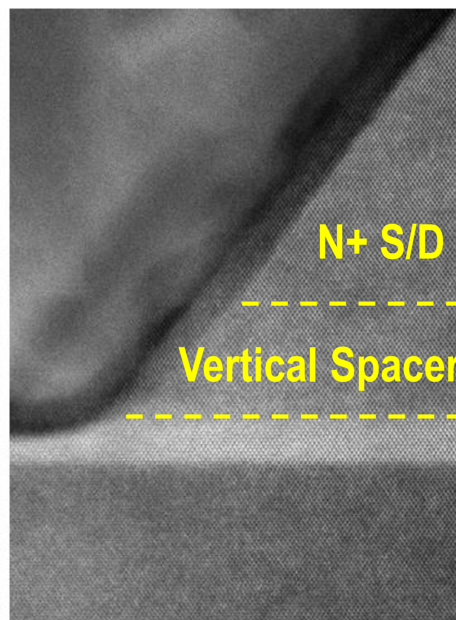
Is cost in added die area acceptable ?

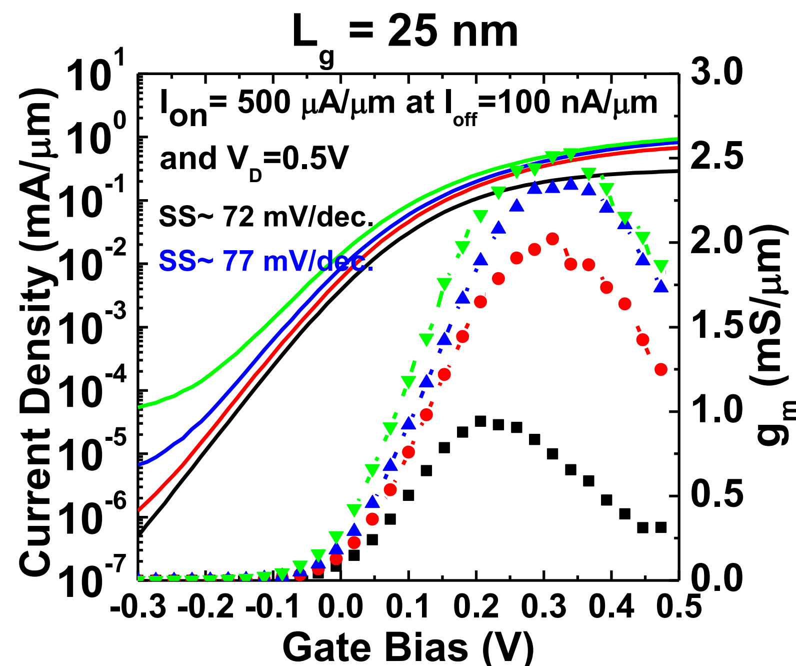
(backup slides follow)

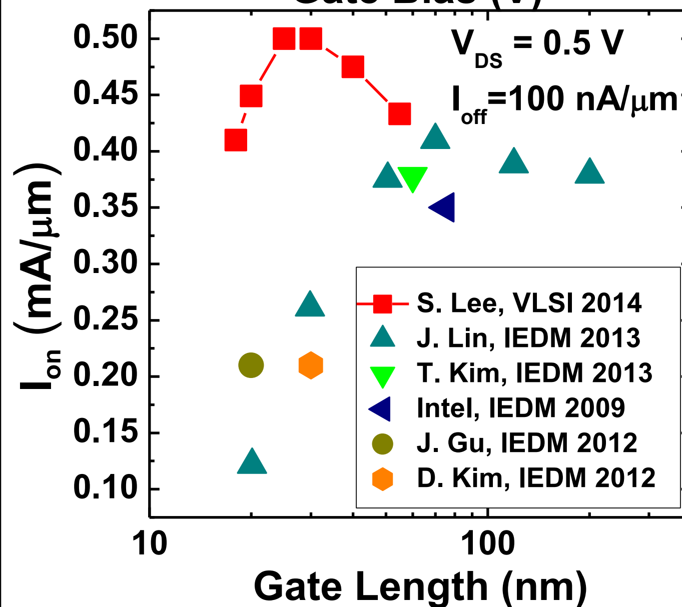
Record III-V MOS











record for III-V

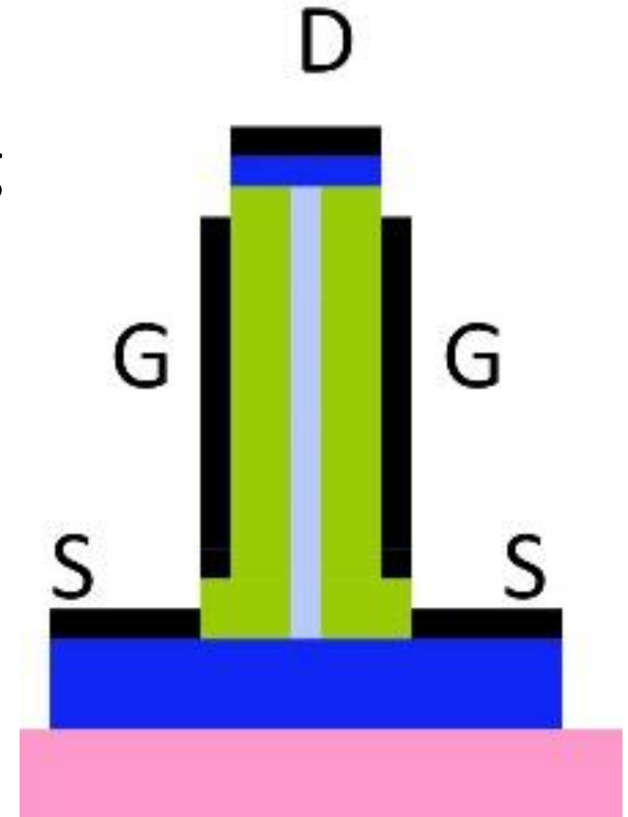
= best UTB SOI silicon

Vertical FETs ????

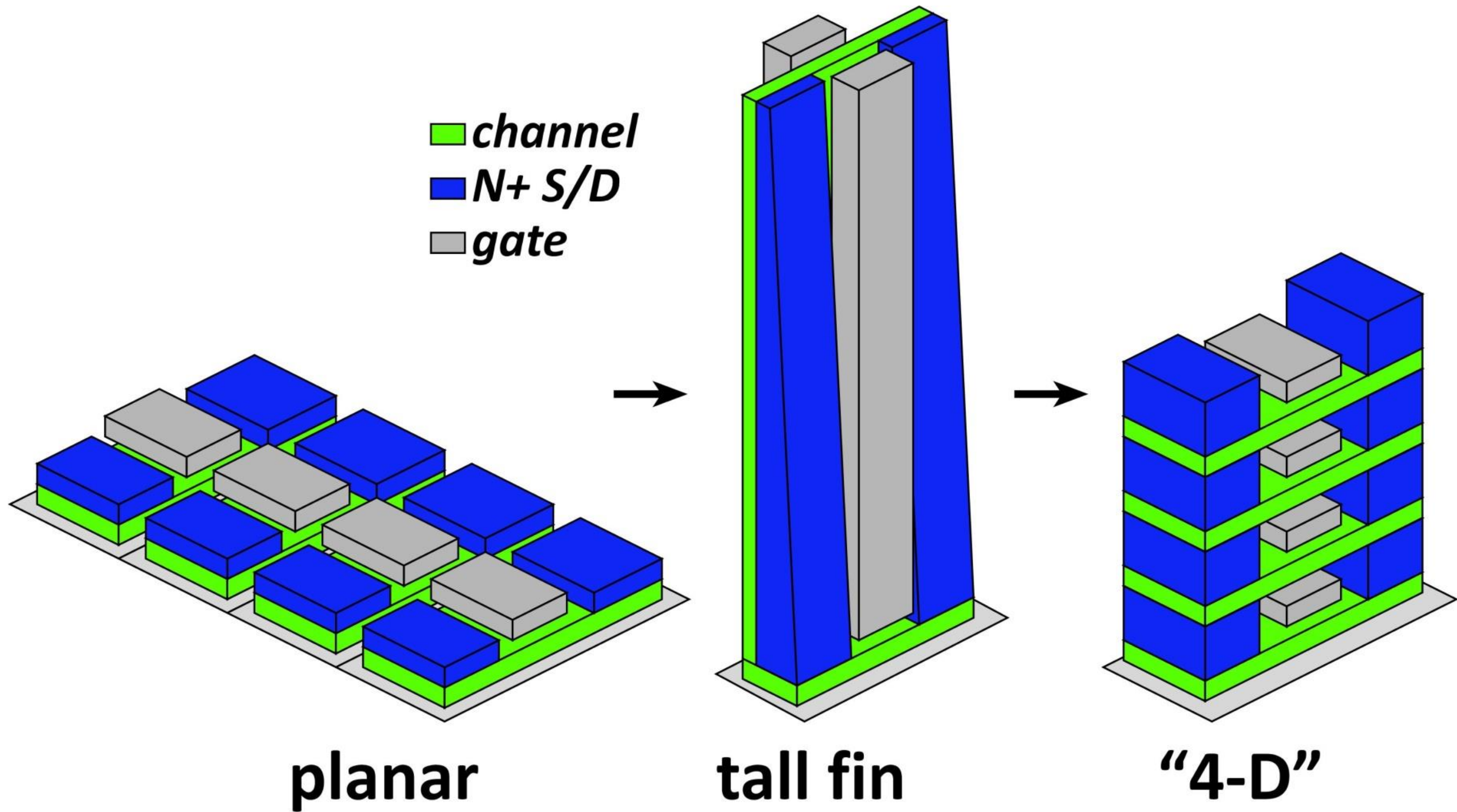
Can have a smaller footprint.

No clue how to make it !

III-V nanowire growth: much too big



3D→shorter wires→less capacitance→less CV^2



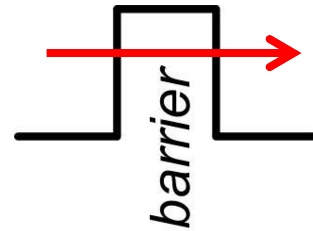
All three have same drive current, same gate width

Tall fin, "4-D": smaller footprint→ shorter wires

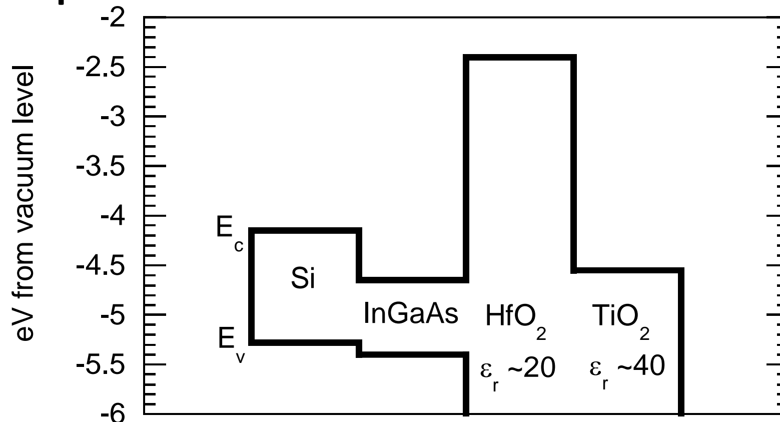
Minimum Dielectric Thickness & Gate Leakage

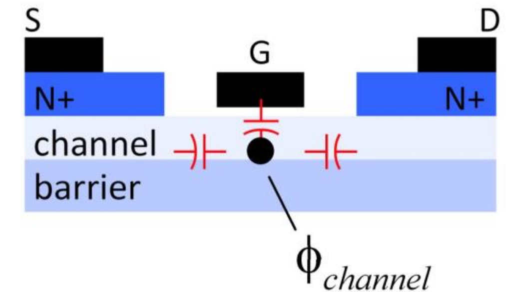
Thin dielectrics are leaky

Transmission Probability $P \cong \exp(-2\alpha T_{\text{barrier}})$, where $\alpha \cong \hbar^{-1}\sqrt{2m^* E_{\text{barrier}}}$



High-ε_r materials have lower barriers



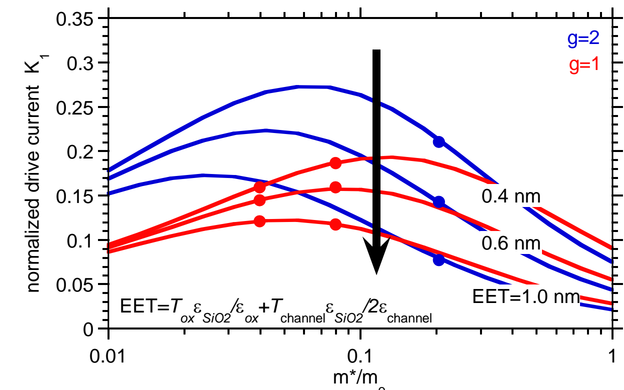


→ 0.5-0.7nm minimum EOT

constrains on-current

electrostatics degrades with scaling

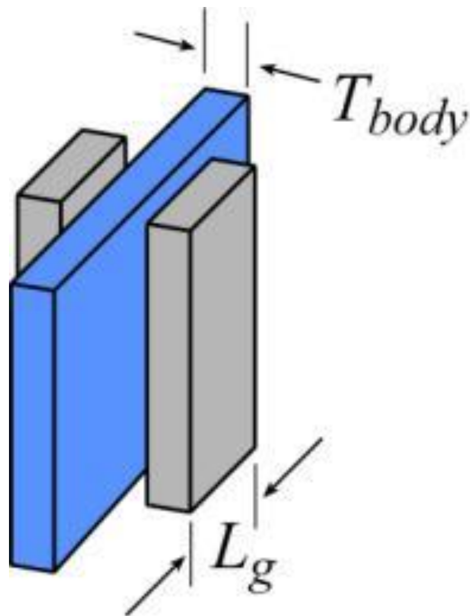
→ fins, nanowires

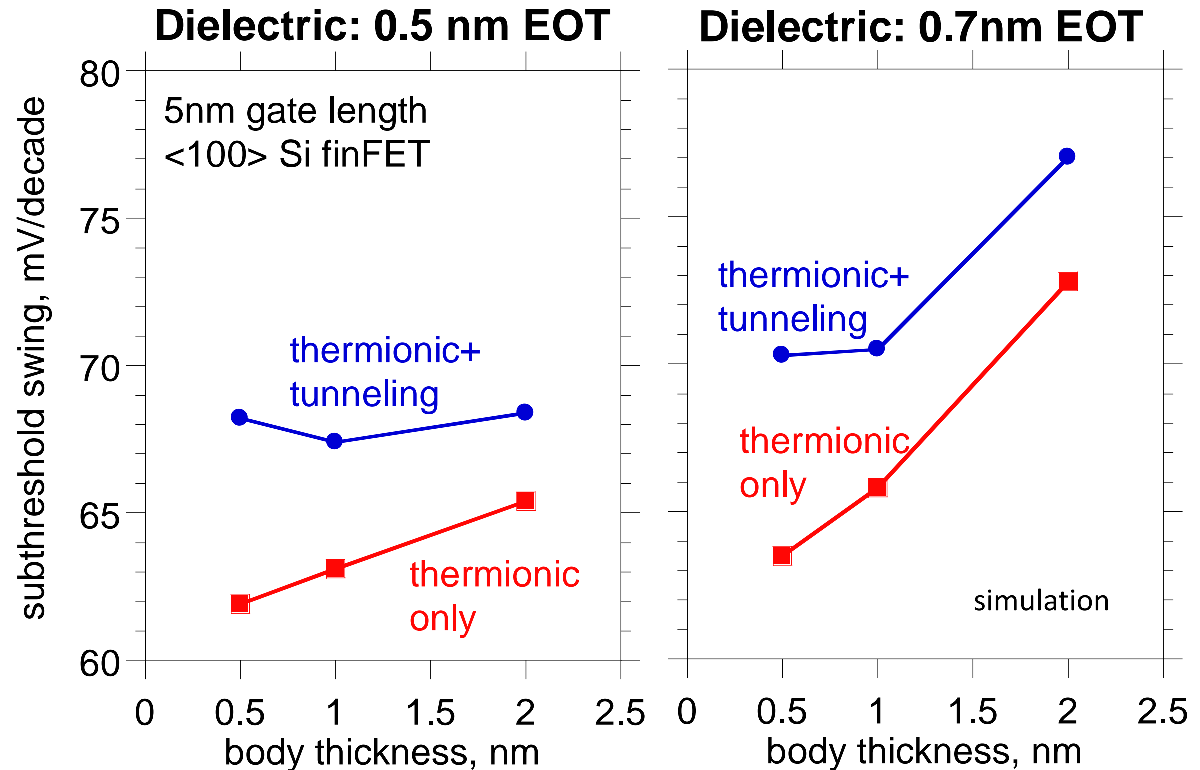


Quick check: scaling limits

NEMO ballistic simulations

finFET: 5 nm physical gate length.
Channel: <100> Si, 0.5, 1, or 2nm thick **dielectric:** ε_r=12.7, 0.5 or 0.7 nm EOT



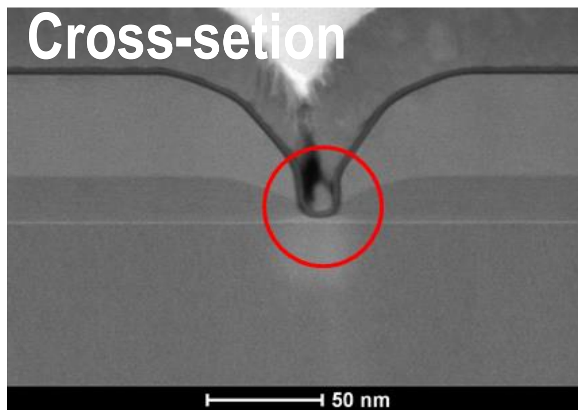


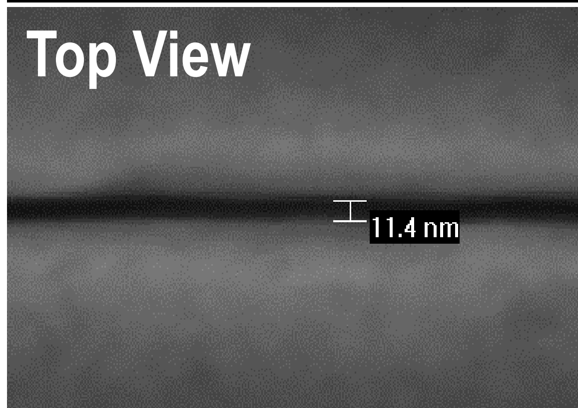
Given EOT limits, ~1.5-2nm body is acceptable.

Source-drain tunneling often dominates leakage.

TEM images of L_g~12 nm devices

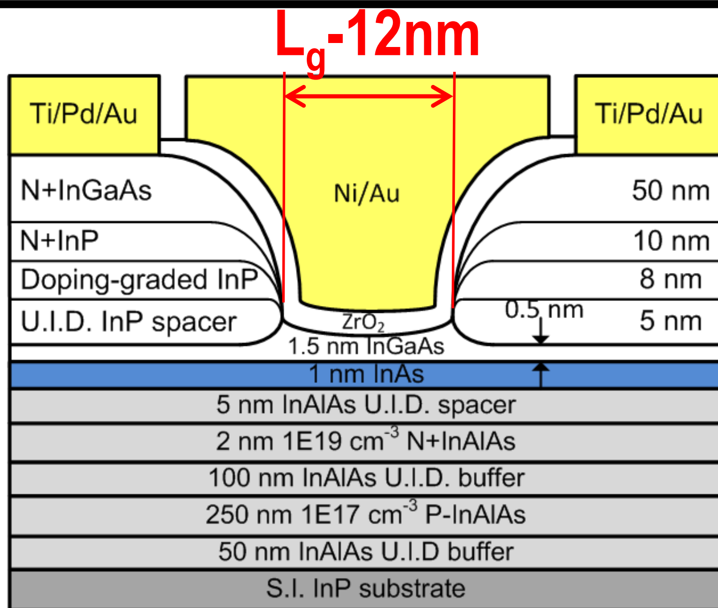
Ti/Pd/Au
Ni/Au
Ti/Pd/Au
N+InGaAs 50 nm
N+InP 10 nm
Doping-graded InP 8 nm
U.I.D. InP spacer 5 nm
ZrO_2
0.5 nm
1.5 nm InGaAs
1 nm InAs
5 nm InAlAs U.I.D. spacer
2 nm 1E19 cm^{-3} N+InAlAs
100 nm InAlAs U.I.D. buffer
250 nm 1E17 cm^{-3} P-InAlAs
50 nm InAlAs U.I.D buffer
S.I. InP substrate

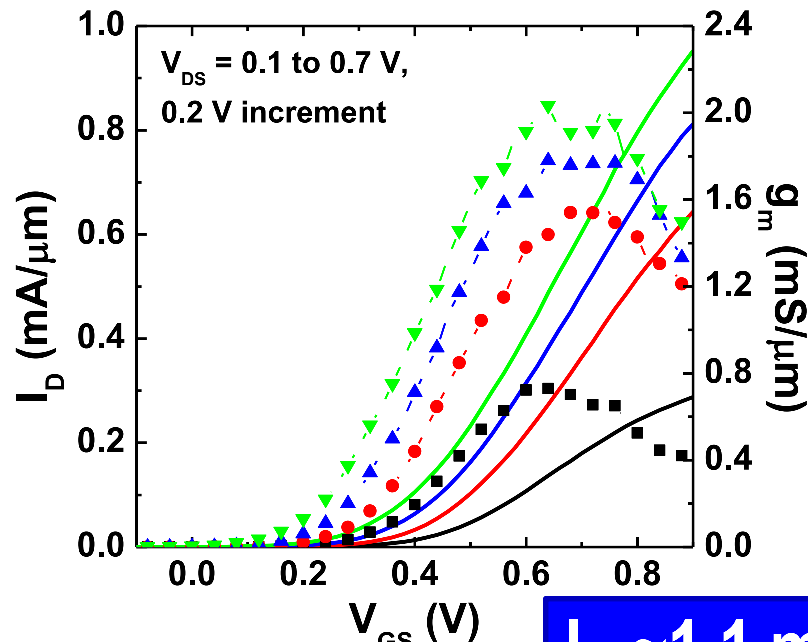


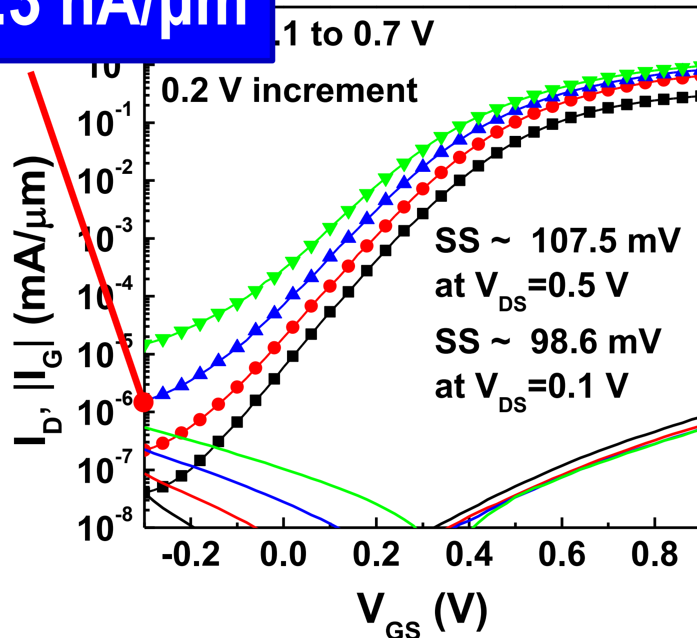


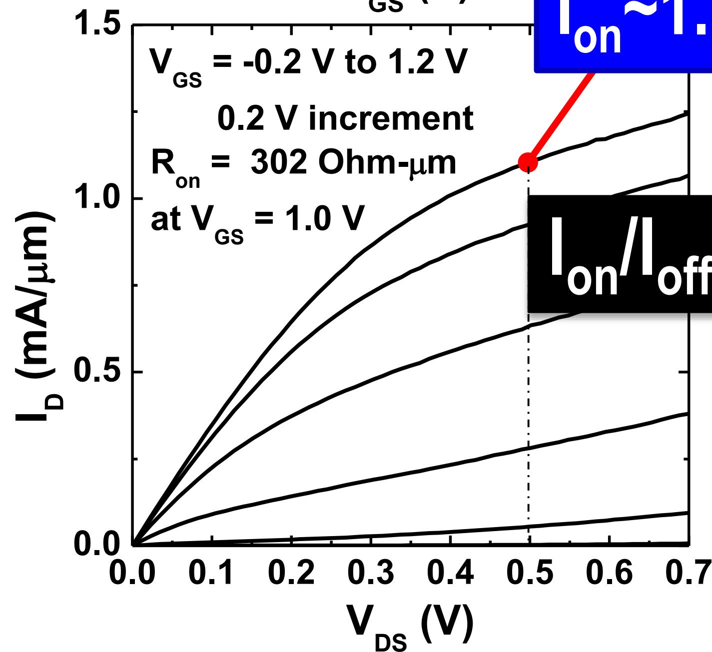
L_g~12nm
~ 8nm
N+InGaAs
N+InP
Ni
InP spacer
InAlAs
Barrier
t_{ch}~ 2.5 nm
(1.5/1 nm InGaAs/InAs)
5 nm

I_D-V_G and I_D-V_D curves of 12nm L_g FETs



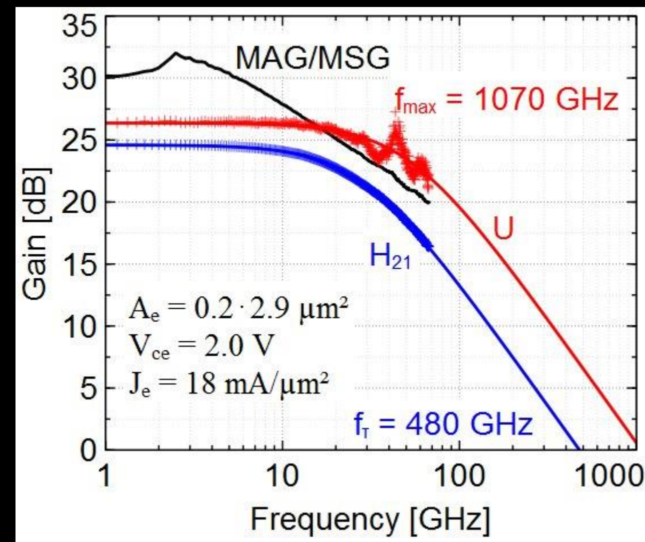


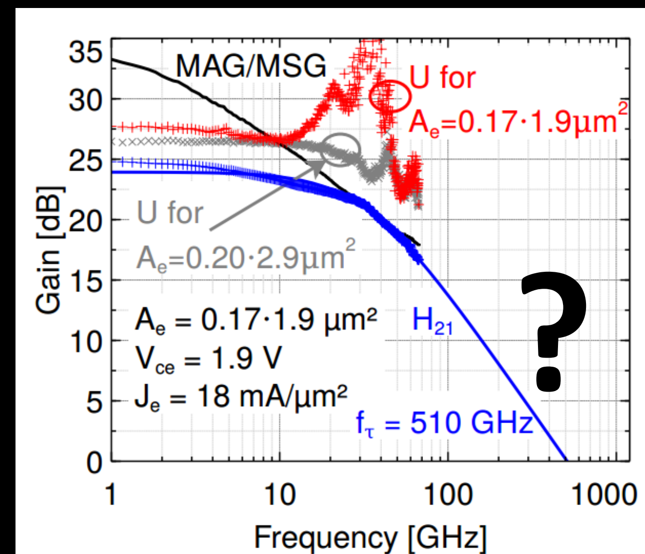




InP HBTs: 1.07 THz @200nm, ?? @ 130nm

base contact
Au
Ti
Pt-InGaAs reaction
emitter
Ru
2.7nm
17nm
base
14.1nm
setback
grade
collector
10 nm



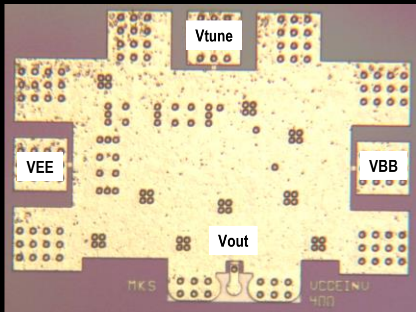


Rode et al., IEEE TED, Aug. 2015

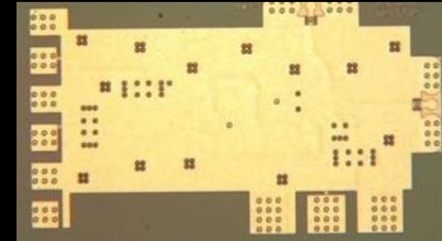
130nm /1.1 THz InP HBT: ICs to 670 GHz

TELEDYNE SCIENTIFIC COMPANY
A Teledyne Technologies Company
UCSB

614 GHz fundamental VCO
M. Seo, TSC / UCSB

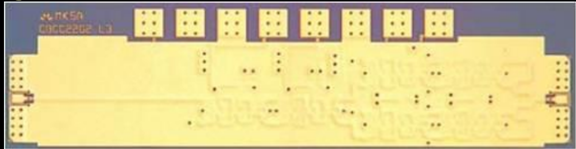


340 GHz dynamic frequency divider
M. Seo, UCSB/TSC
IMS 2010

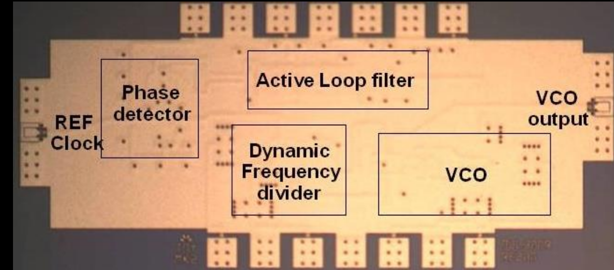


620 GHz, 20 dB gain amplifier
M Seo, TSC
IMS 2013

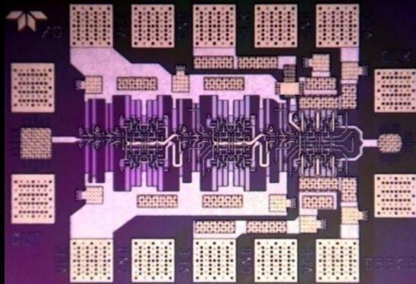
also: 670GHz amplifier
J. Hacker , TSC
IMS 2013 (not shown)



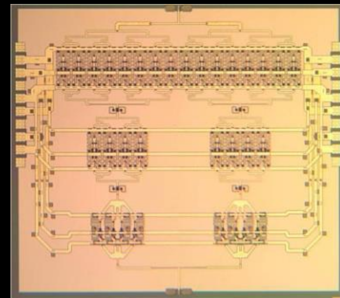
300 GHz fundamental PLL
M. Seo, TSC
IMS 2011



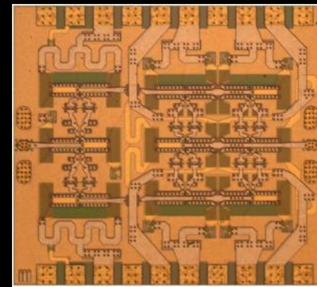
204 GHz static frequency divider (ECL master-slave latch)
Z. Griffith, TSC
CSIC 2010



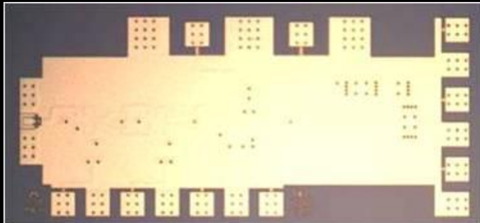
220 GHz 180 mW power amplifier
T. Reed, UCSB
CSICS 2013



81 GHz 470 mW power amplifier
H-C Park UCSB
IMS 2014



Integrated 300/350GHz Receivers:
LNA/Mixer/VCO
M. Seo TSC



600 GHz Integrated Transmitter
PLL + Mixer
M. Seo TSC