# A high-current InP-channel triple heterojunction tunnel transistor design

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VLSI devices are constrained by $CV_{DD}^2/2$ power dissipation. Low power dissipation requires low $V_{DD}$, yet reducing $V_{DD}$ increases $I_{OFF}$. Tunnel FETs (TFETs) have steep subthreshold swings (S.S.) and can operate at low $V_{DD}$, yet their $I_{ON}$ is limited by low tunneling probability. This low $I_{ON}$ results in large $CV_{DD}/I$ delay and slow logic operation. For greatly increased $I_{ON}$, we had proposed a triple-heterojunction (3HJ) TFET design incorporating source and channel heterojunctions (HJ) [1, 2]. The designs of [1, 2] have an InAlAsSb channel, yet no low-trap-density dielectric interfaces to InAlAsSb have been reported. In contrast, low-trap-density dielectric interfaces have been demonstrated to InAs, InGaAs, and InP [3, 4, 5]. Here we propose an InGaAs/GaAsSb/InAs/InP 3HJ TFET design, with growth lattice-matched to InP. The gated channel surface is InAs and InP, and thus can have low trap density. The p-type side of the tunnel junction is GaAsSb, instead of strained GaSb [6], as compressive strain increases the hole transport effective mass, reducing the tunneling probability. In ballistic simulations, with $I_{OFF}$= $10^{-3}$ μA/μm and $V_{DD}$=0.3V, $I_{ON}$ is an extremely high 540μA/μm. Even when simulated assuming incoherent quantum transport, with acoustic and optical phonon scattering modelled, $I_{ON}$ remains very high at 250μA/μm.

The TFETs have double gates (e.g. are FinFETs) with 1.8nm thick gate dielectric ($\varepsilon_{r,ox}$=9), and 30nm long, 3.9nm thick channels. The 3HJ TFET design (Fig. 1b) includes a p-$In_{0.53}Ga_{0.47}As$ source ($N_A=2\times10^{19}cm^{-3}$), a 1.5nm p-$GaAs_{0.73}Sb_{0.27}$ ($N_A=5\times10^{19}cm^{-3}$) grade layer, a 3.0nm p-$GaAs_{0.56}Sb_{0.44}$ ($N_A=5\times10^{19}cm^{-3}$) p-junction layer, a 3.5nm i-InAs channel well, an i-InP channel and n-InP drain ($N_D=5\times10^{19}cm^{-3}$). The $In_{0.53}Ga_{0.47}As$ source and the InP channel are lattice-matched to the InP substrate. The $GaAs_{0.73}Sb_{0.27}$ grade layer further increases the tunnel junction electric field. The 3HJ-TFET design is compared to a GaSb/InAs TFET of identical dimensions (Fig. 1a).

The devices are simulated using the NanoElectronic MOdeling tool NEMO5 [7]. For ballistic transport simulations, the Poisson equation and the open boundary Schrödinger equation are solved self-consistently, employing the strained eight-band k·p method [8, 9]. To explore the incoherent transport behavior between the confined states, acoustic and optical phonon scattering are considered in the non-equilibrium Green's function formalism with the self-consistent Born approximation [10]. To reduce the computation cost, only diagonal terms are considered in the scattering self-energies. Acoustic deformation potential of 5.08eV, optical phonon energy of 30meV and optical deformation constant of 310eV/nm are used [11], leading to $\mu_n(InAs)=1.35\times10^4 cm^2V^{-1}s^{-1}$ and $\mu_p(GaSb)=3\times10^3 cm^2V^{-1}s^{-1}$, which are both close to experimental values.

Fig. 2a) compares the band structures of strained GaSb (lattice-matched to InP) and unstrained $GaAs_{0.56}Sb_{0.44}$ layers of varying thickness. Replacing strained GaSb with unstrained GaAsSb reduces hole $m^*$ from $0.21m_0$ to $0.063m_0$. Increasing $T_{ch}$ of the GaAsSb/InAs TFET from 3.0nm to 3.9nm decreases the tunnel barrier height from 0.52eV to 0.47eV. As a result, the 3.9nm $T_{ch}$ GaAsSb/InAs TFET has the highest ON-state transmission (Fig. 3). Further increasing $T_{ch}$ does not significantly increase $I_{ON}$, but increases $I_{OFF}$.

In the ON-state, the GaAsSb/InAs HJ TFET (Fig. 3a) has 6% peak tunneling probability; the 3HJ TFET (Fig. 3b) has >50% tunneling probability over a 60meV range (Fig. 4a). This is due to both the increased electric field at the tunnel junction and the resonant states in the source and channel quantum wells. The two resonant states form a conduction window over 60meV (Fig. 4b). With fixed $I_{OFF}=10^{-3}$μA/μm and $V_{DD}$=0.3V, the ballistic $I_{ON}$ reaches ~540μA/μm. However, in the OFF-state, phonon scattering couples the two confined states, increasing the leakage current. As a result, $I_{ON}$ degrades from ~540μA/μm to 250μA/μm (Fig. 5a), S.S. degrades from 13mV/dec to 24mV/dec (Fig. 5b), but the 3HJ TFET's $I_{ON}$ is still ~7:1 larger than the GaAsSb/InAs TFET under the same intensity of phonon scattering. Insights into the OFF-state degradation can be gained from the local density of states (LDOS, Fig. 6). The contrast between the ballistic (Fig. 6a) and the scattering (Fig. 6b) cases demonstrates the broadening of the confined states inside the source and channel wells. The current density (Fig. 6c) shows the major energy relaxation is inside the source well. To reduce the phonon scattering leakage, we have experimented with thinner quantum wells to increase the energy separation between the two resonant states. However, the overall $I_{ON}/I_{OFF}$ ratio does not significantly improve because misaligning the resonant states reduces $I_{ON}$.

In summary, a high-current InP-based TFET is proposed and its performance is assessed. Despite the effect of acoustic and optical phonon scattering, $I_{ON}$ of 250μA/μm at $I_{OFF}=10^{-3}$μA/μm and $V_{DD}$=0.3V is obtained, making it a promising candidate for low voltage logic applications.

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Acknowledgements: The nanoHUB.org computational resources funded by the US NSF grant Nos. EEC-0228390, EEC-1227110, EEC-0634750, OCI-0438246, OCI-0832623 and OCI-0721680. This work is supported by the NSF Grant ECCS-1509394, ECCS-1639958 & SRC 2016-EP-2694-C. NEMO5 developments were critically supported by an NSF Peta-Apps award OCI-0749140, SRC's GRC Task 2653 and by Intel Corp.

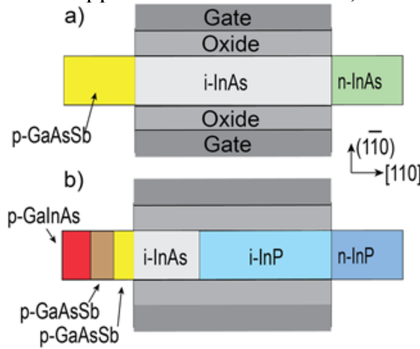


**Fig. 1.** Device cross sections of a GaAsSb/InAs HJ TFET a) and a GaInAs/GaAsSb/InAs/InP 3HJ TFET (b). In (b), the source HJ is graded.

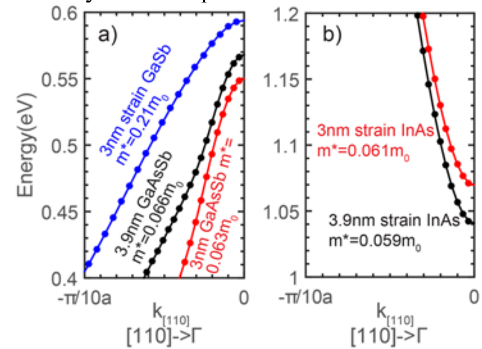


**Fig. 2.** Top valence band of confined GaSb and GaAsSb a) and bottom conduction band of confined InAs b).They are $(1\bar{1}0)$ confined. The transport is along [110]. Replacing the strained GaSb with the unstrained GaAsSb yields a smaller hole $m^*$. Increasing the $T_{ch}$ to 3.9nm decreases the tunnel barrier height.

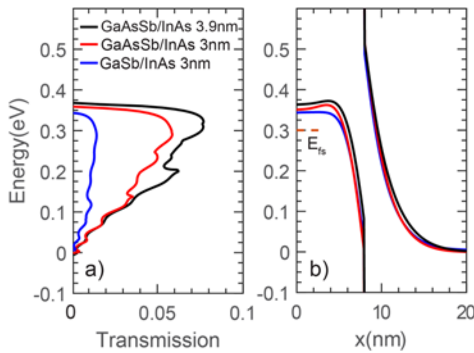


**Fig. 3.** Transmission probability a) and band diagram b) (same bias of a) of HJ TFETs with GaSb or GaAsSb source and 3nm/3.9nm body thickness. Using the GaAsSb source and increasing the $T_{ch}$ to 3.9nm increase the transmission probability (given the same conduction band alignment).

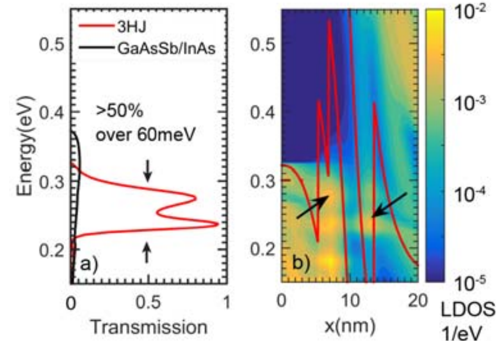


**Fig. 4.** Transmission probability a) and LDOS b) of the 3HJ TFET in the ON-state. The two resonant states in the source and channel form a conduction window of over 60meV with >50% transmission.

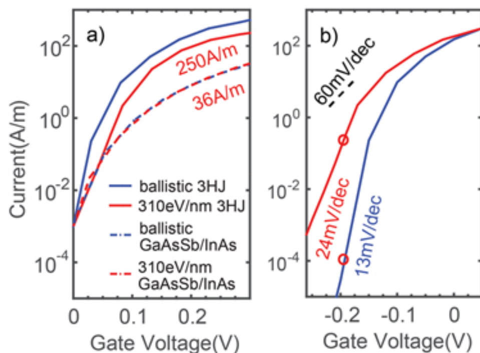


**Fig. 5.** Transfer characteristics with fixed $I_{OFF}$=$10^{-3}$μA/μm a) and when $V_{th}$ is held constant b). Phonon scattering degrades $I_{ON}$ from ~540μA/μm to 250μA/μm, S.S. from 13mV/dec to 24mV/dec, but $I_{ON}$ is still higher than the GaAsSb/InAs TFET (a). The red dots in b) show the bias of Fig. 6.

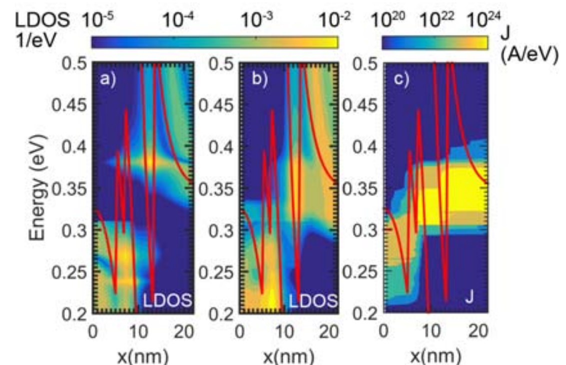


**Fig. 6.** Ballistic LDOS a), scattering LDOS b) and energy resolved current density (J) of the 3HJ TFET c). The resonant states in the source and channel are broadened when phonon scattering is included. The energy resolved current relaxes primarily in the source well when $V_G$=−0.18V (the red dots of Fig. 5b).

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