8.6-13.6 mW Series-Connected Power Amplifiers Designed at 325 GHz using 130 nm InP HBT Technology

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***Abstract*— We report two 325 GHz series-connected power amplifiers (PAs) using 130 nm InP HBT technology. The unit cell, using two series-connected transistors, produces 8.6 mW at 325 GHz and consumes 243 mW DC power. The PA has a 4.3 dB compressed gain and 2.2% power added efficiency (PAE). Two of these cells are then power-combined, and two further cells are used as driver stages, to form the second design, which produces 11.36 mW at 325 GHz with 9.4 dB compressed gain and 1.09% PAE. The peak small signal gain is 16.6 dB at 325 GHz, and the 3-dB bandwidth is 9 GHz. The total power consumed is 1.12 W and the dimensions including the pads are 0.98 mm × 0.98 mm.**

Keywords—Stacked power amplifier; H-band power amplifier; mm-wave; Indium Phosphide.

I. INTRODUCTION

At high mm-wave and sub-mm-wave frequencies, wavelengths are short, and even small phased arrays can contain many elements and hence can transmit or receive many simultaneous beams. Such massive spatial multiplexing, plus the wide available spectrum, will permit massive capacity short-range wireless links. Atmospheric attenuation and (λ^2/R^2) are high, and moderate-power amplifiers are required for acceptable transmission range.

Millimeter-wave power-combining is challenging, with interconnect losses limiting the maximum number of power-combined transistor fingers. Reported designs at 250-340 GHz include [1-6]. Series-connected transistors [7-9] are one technique for compact, efficient power-combining. Extending upon design approaches [9] based on nodal analysis given defined equivalent-circuit models of transistors and passive elements, we had earlier reported design of 204 GHz [10] series-connected amplifiers using 130 nm InP HBT technology [11]. These were designed using 2-port and load-pull parameters, the procedure permitting design from an arbitrary transistor model combined with the N-port parameters of the amplifier's interconnects and passive elements determined from electromagnetic simulation [10]. This facilitates design at very high frequencies.

Here we introduce similar series-connected amplifiers operating at 325 GHz. The first design (the unit cell) connects two transistors in series and produces 9.4 dBm saturated output power with 2.2% PAE and 4.3 dB compressed gain at 243 mW DC power consumption. It has 10 dB small signal gain and the 3-dB bandwidth extends from 311-325 GHz. The saturated output power is at least 4 mW over a 323-340 GHz bandwidth.

In the second amplifier, a transmission-line network combines two of these cells, and two further cells serve as driver stages. This PA produces 11.4 dBm saturated output power with 1.09% PAE at 9.4 dB gain driven. The 3-dB bandwidth extends from 316 GHz to 325 GHz.

II. SINGLE CELL POWER AMPLIFIER DESIGN

The amplifier is designed using 130 nm InP HBT technology. This has a 1.1 THz power-gain cutoff frequency ($f_{\max}$), a 3.5 V breakdown, and a maximum ~3 mA current per μm emitter finger length. The Au interconnect stack has three layers, with 1 μm BCB (ε_r=2.7) between metal 1 and metal 2, and 5 μm BCB between metal 2 and metal 3. 50Ω microstrip lines between metal 1 and metal 3 have 1.4 dB/mm loss (0.9 dB per guide wavelength) at 300GHz. There are 0.3fF/μm^2 MIM capacitors and 50Ω/square thin-film resistors.

The amplifier unit cell (Fig. 1) has two stacked 8-finger transistors, each of 5 μm emitter finger length. The transistors are biased at 1.3 mA/μm, with current under RF drive then varying from zero to 2.6 mA/μm. Microstrip lines serve as interconnects and for impedance-matching; these use a metal 1 ground plane and metal 3 signal lines.

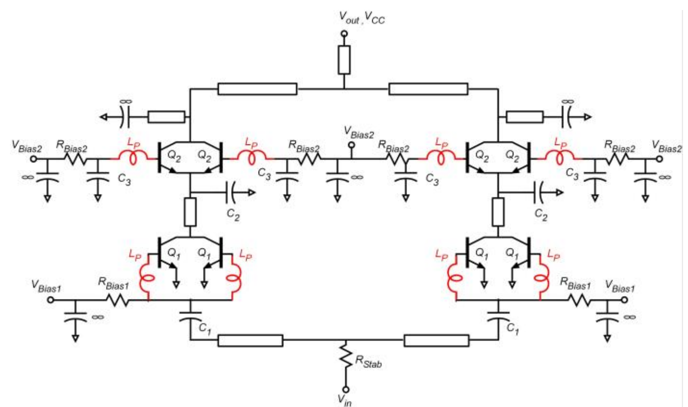

Fig. 1: PA unit cell (two stacked HBTs with matching circuits). Q_1 and Q_2 are two finger transistors each 5μm emitter length. The inductors (red) are added to represent the base inductance model and are not real inductors.

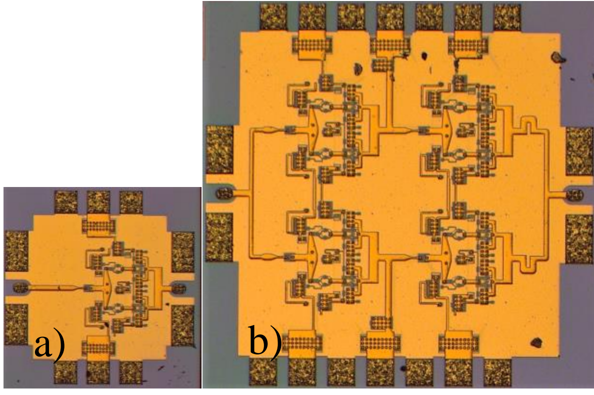

Fig. 2. Chip micrograph of the power amplifiers: a) Design #1 (dimensions = 600 μm × 585 μm) b) Design #2 (dimensions = 0.98 mm ×1 mm)

The power cell has input matching to 50 Ω, output tuning providing the optimum large-signal loadline to Q_2 given an external 50Ω load, a capacitor C_3 controlling the RF voltage distribution between the two transistors, and an interstage network ensuring equal RF currents in the two transistors. Resistors provide out-of-band stabilization. Amplifiers are designed according to the procedures of [10]. Interconnects, matching and power supply lines, and MIM capacitors are simulated using a ADS momentum, a 2.5D tool.

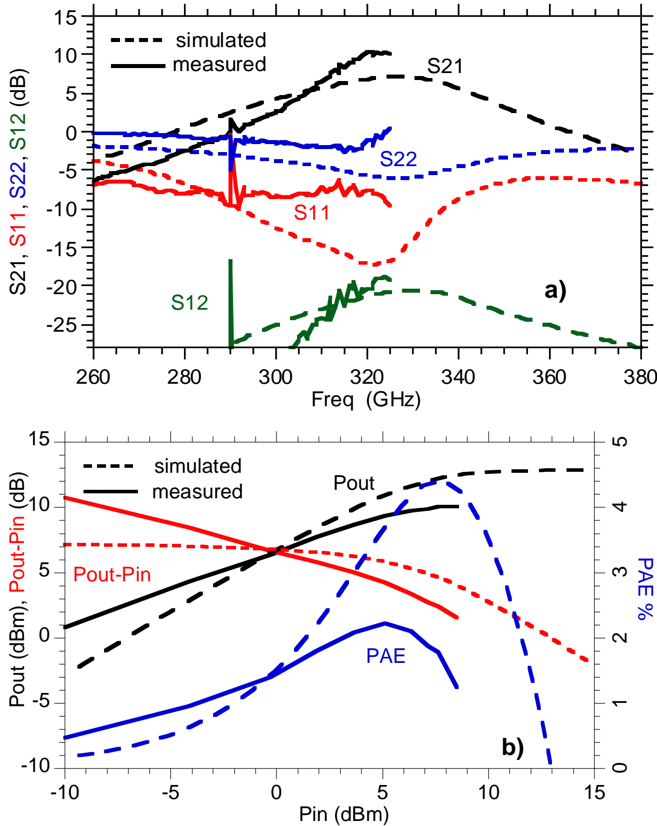

Fig. 3: Simulated and measured s-parameters (a) and power transfer characteristics @325GHz (b) of the unit-cell design.

III. 2:1 Power-Combined Design

For increased output power, transmission-lines combine the outputs of two unit cells and match these to 50Ω (Fig. 2b). Two additional unit cells serve as predrivers. These increase the IC gain and provide the necessary input power for the final stage, at the expense of increasing the total power dissipation. Quarter-wave transmission lines provide DC bias to the driver stages; DC bias pads have *RC* bypass networks to prevent resonance with external probe inductances.

IV. Measurement Results

Fig. 2 shows the IC photographs. The output (V_{CC}) is biased at 3.6V and the DC collector current, equal to the total IC DC current, is 68mA. The base bias voltage of the Q_2 is 2.3V. The collector to emitter voltage (V_{CE}) of transistors (Q_1) is smaller than the V_{CE} of the common base transistors (Q_2) to reduce the total power dissipation and optimize the PAE. Separate bias resistors are provided to the two parallel common-emitter transistors, preventing thermal competition for the DC bias current. 220-325 GHz S-parameters are measured using an HP vector network analyzer with Oleson mm-wave frequency extenders and waveguide-coupled wafer probes. Calibration is to the probe tips using an external LRRM calibration standard substrate. Fig. 3a compares the simulated and measured S-parameters of the unit cell. The measured peak gain is 10 dB at 325 GHz while the simulated peak gain is 5.5 dB at 330 GHz. The spikes at ~290GHz occur due to the frequency extension modules and they are not related to the circuit itself.

For power measurements, a 330 GHz VDI frequency multiplier generates the input signal and an Ericson THz power meter measures the output power. Wafer probe losses were determined by a through measurement, and were de-embedded from the power measurements. Fig. 3b shows the simulated and measured output power, the PAE, and the gain, as a function of the input power at 325 GHz. The PA has 9.4 dBm saturated output power at 4.3 dB compressed gain and 2.2% PAE.

There is considerable discrepancy between the simulated and measured small-signal and power characteristics of the unit cell power amplifier. The HBT model, established from RF characterization of single-finger devices, includes 2.7pH per 5 μm emitter finger. In a 2-finger power cell, the aggregate inductance of the base feed network is considerably larger. Although the base feed network and its parasitics were modeled during design, this is a complex network without an underlying ground plane providing a clear path for the ground-return currents; modeling of the interconnect inductance within the multifinger HBT is therefore difficult. To attempt to resolve the difference between measurement and simulation, the amplifier was re-simulated with a variable base feed inductance for all multifinger HBTs. A 3.5 pH (L_P in Fig. 1) inductance provides the best fit between measurement and simulation for both the small-signal and power data (Fig. 4). This inductance is approximately that of a 5 μm length conductor.

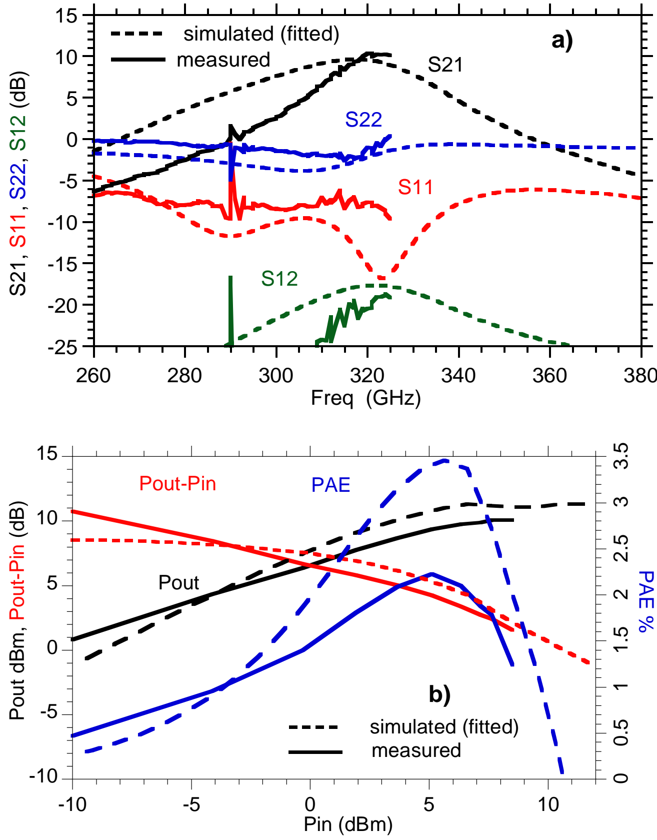

Fig. 4. Comparison of measured and resimulated s-parameters (a) and power transfer characteristics @325GHz (b) of the unit-cell design assuming an additional 3.5 pH base feed inductance per two-finger each 5 µm emitter length HBT.

Fig. 2b shows the micrograph of the second design. The PA combines two-unit cells using transmission lines. The bias conditions of all the cells are identical and similar to design 1 (V_{CC}=3.6 V, V_{Bias2}=2.3 V) and the total DC current is 290 mA. Fig. 5a shows the measured and simulated S-parameters. The measured peak small signal gain is 16.6dB at 325 GHz, while the simulated peak gain is 8.25 dB at 330 GHz. The measured 3-dB bandwidth extends from 316 GHz to beyond the 325 GHz measurement limit of the network analyzer's frequency converters. Fig. 5b shows the power transfer characteristics at 325GHz. The amplifier has a 11.4 dBm saturated output power at 9.4 dB associated gain and 1.09% PAE.

Fig. 6 shows the input-output power characteristics as a function of frequency for the single-cell (Fig. 6a) and 2:1 power-combined amplifiers (Fig. 6b).

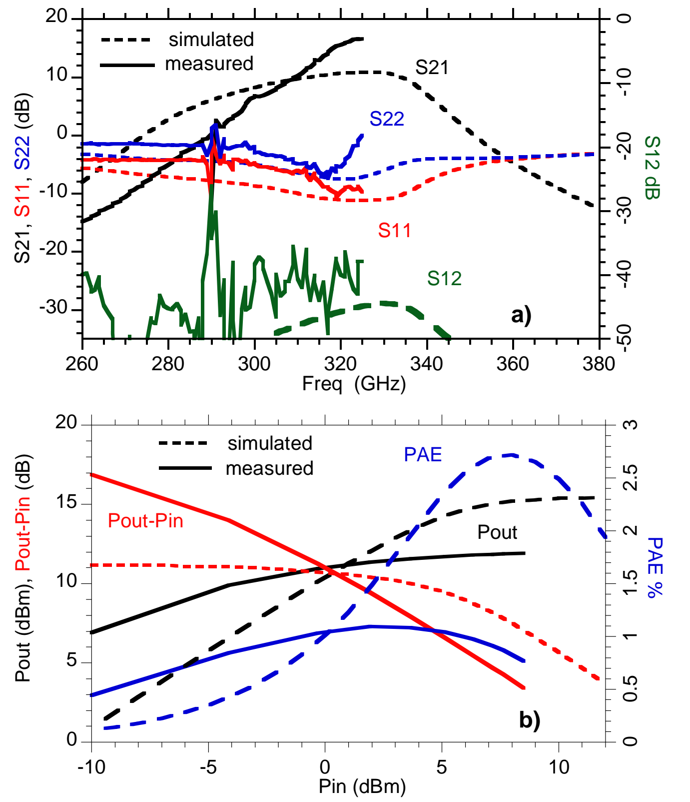

Fig. 5: Simulated and measured s-parameters (a) and power transfer characteristics (b) of the 2:1 power-combined design.

V. Conclusion

The paper presented the series-connected power amplifiers operating above 300 GHz. The single-cell design produces 8.6 mW output power at 2.2 % PAE, while the 2:1 power-combined amplifier produces 13.6 mW output power at 1.09% PAE. The die areas are 600 μm × 585 μm and 0.98 mm ×1 mm for design #1 and design #2 respectively which show compact area. Table 1 summarize the state-of-the art power amplifiers above 300 GHz. The presented stacked designs have competitive saturated output power, efficiency and compact size compared to the previously reported amplifiers at these frequencies.

Table 1. Comparison between stat-of-the-art designs

Freq GHz	Tech.	S21 dB	PDC W	Pout, mW	PAE %	Dimensions mm×mm	Ref
290-307.5	250nm InP HBT	20-23.5	0.85	6-10	1.1	1.45×0.44	[1]
338	Sub-50nm HEMT	14.6	0.29	13.5	3.5	1.1×0.45	[6]
300	250nm InP HBT	21.5	0.72	8.9	1.1	-	[7]
301	250nm InP HBT	35	-	22.3	-	0.67×0.68	[8]
325	**130nm HBT**	**10**	**0.24**	**8.6**	**2.2**	**0.6×0.58**	**This work**
325	**130nm HBT**	**16.6**	**1.12**	**13.6**	**1.09**	**0.98×1**	**This work**

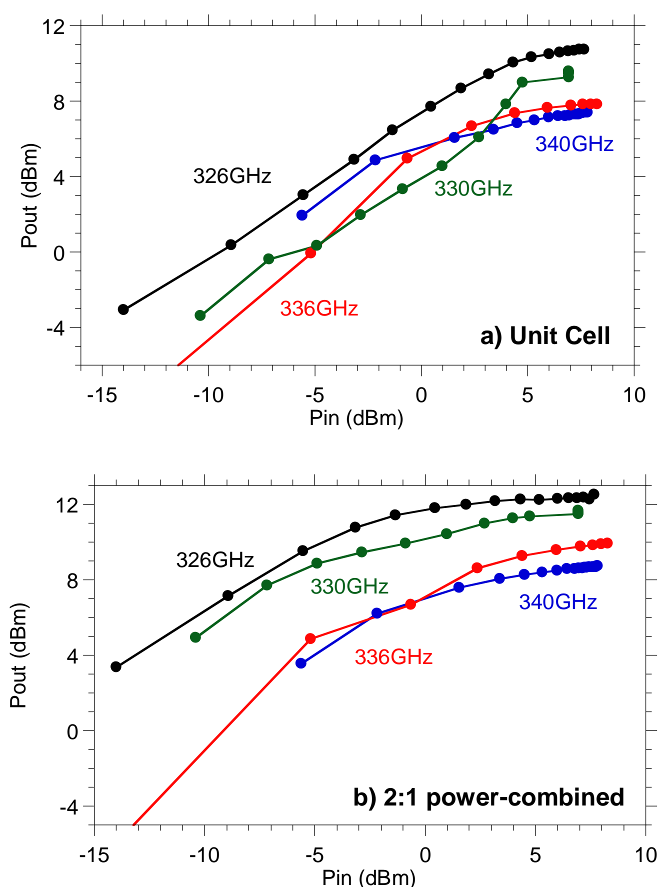

Fig. 6. Measred output power at different frequencies vs the input power for a) design#1 and b) design #2

Acknowledgment

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