A 140 GHz MIMO Transceiver in 45 nm SOI CMOS

Arda Simsek[1], Seong-Kyun Kim[2], and Mark J. W. Rodwell[1]

[1]University of California, Santa Barbara, USA

[2]Teledyne Scientific and Imaging, USA

Acknowledgements

Contact support: NSF Giganets program.

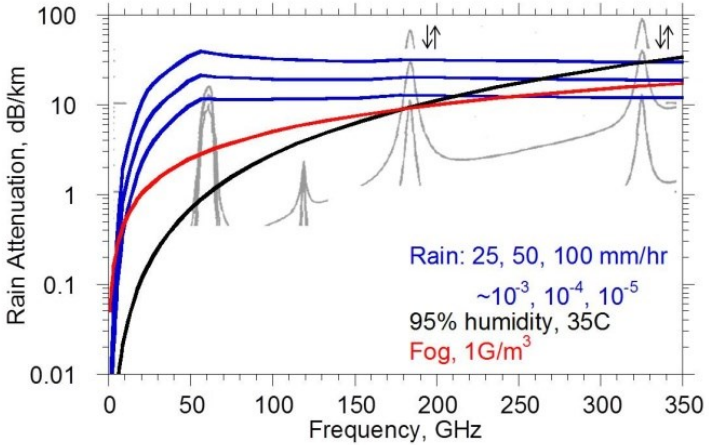
IC Fabrication: Global Foundries. 45nm SOI

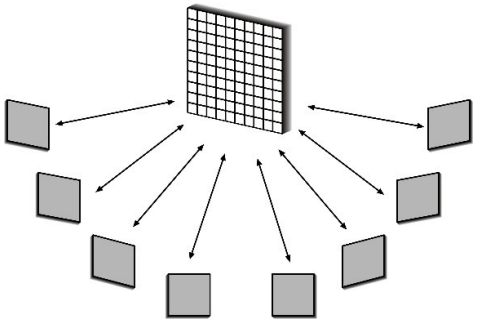
Motivation

Large available spectrum at mm-waves

Shorter wavelength – small IC, antenna arrays

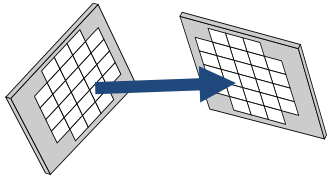
Massive # of parallel channels – multiple independent beams



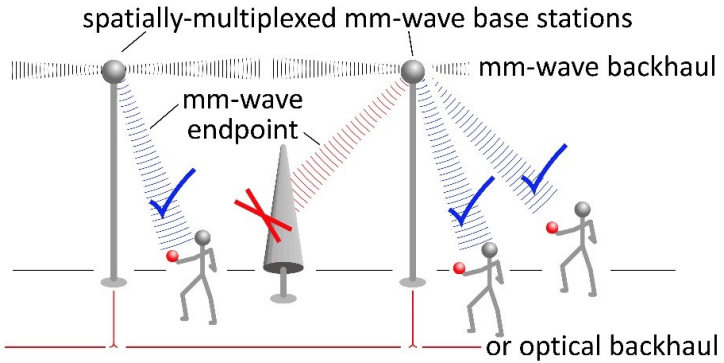


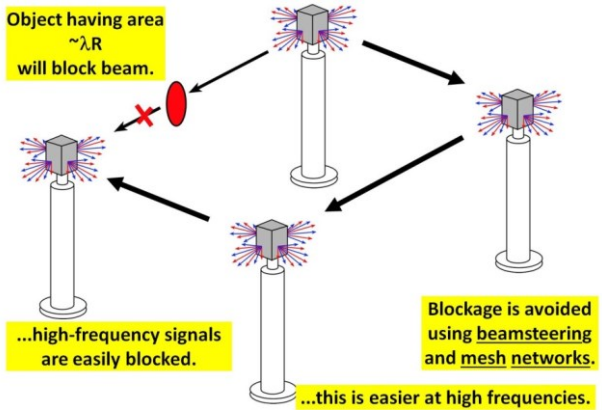
Applications and Challenges

High capacity mobile communications



Problems:	**Solutions:**
▪ High attenuation	Phased arrays
▪ High blockage	Mesh networks & beam steering



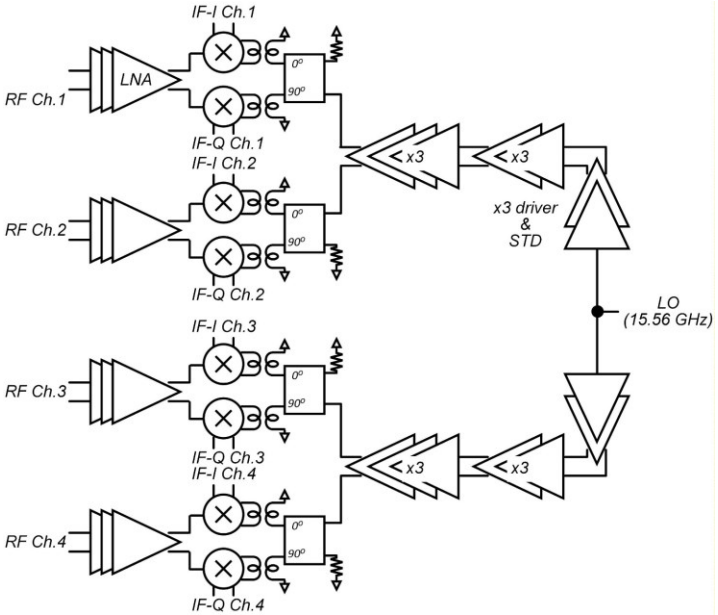


4-Channel MIMO Receiver

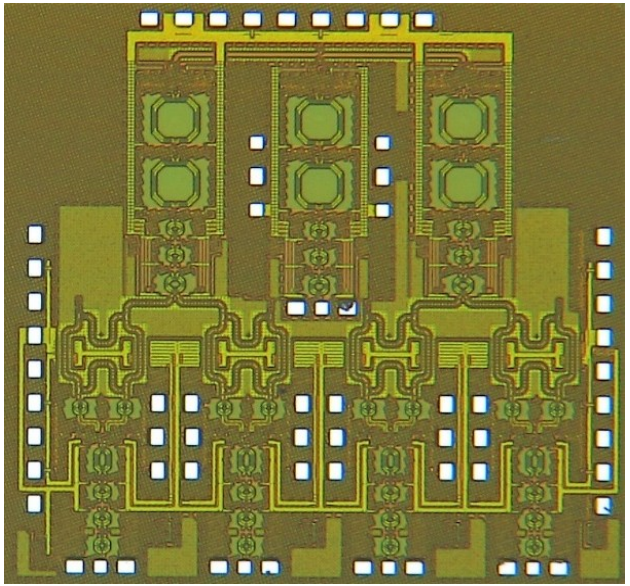
Direct conversion receiver

140 GHz LNA, double balanced passive mixer

LO distribution through two x9 multipliers from common LO port



1.69 mm x 1.76 mm

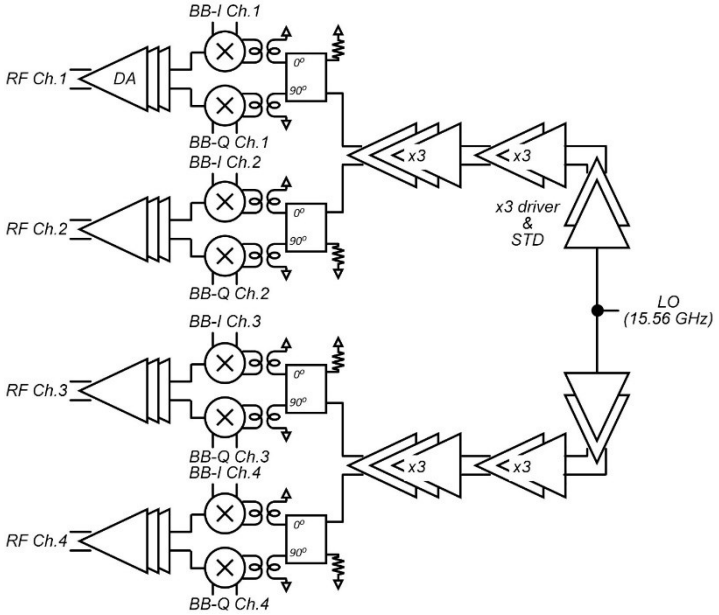


4-Channel MIMO Transmitter

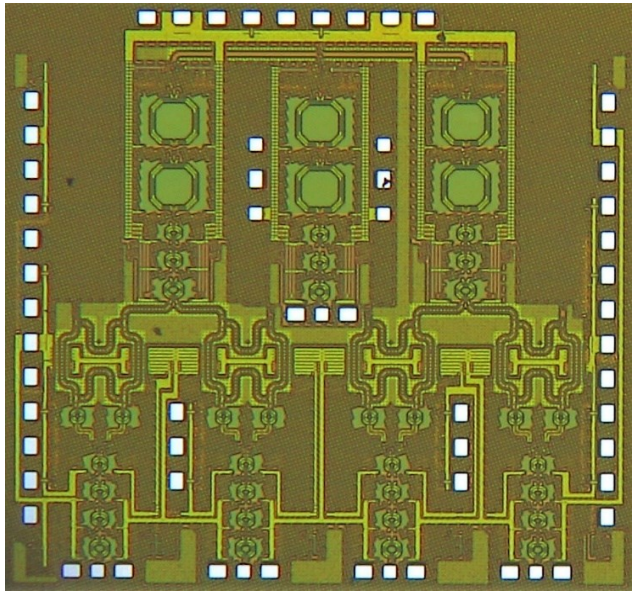
Direct conversion transmitter

140 GHz PA (same with LNA), I/Q Gilbert Cell Active Mixer

LO distribution thru two x9 multiplier from common LO port

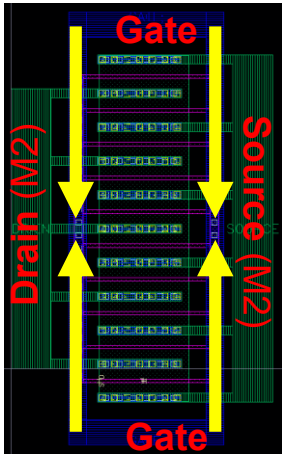


1.67 mm x 1.76 mm

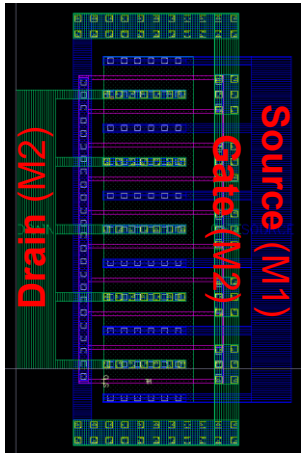


Design Details – Transistor Modeling

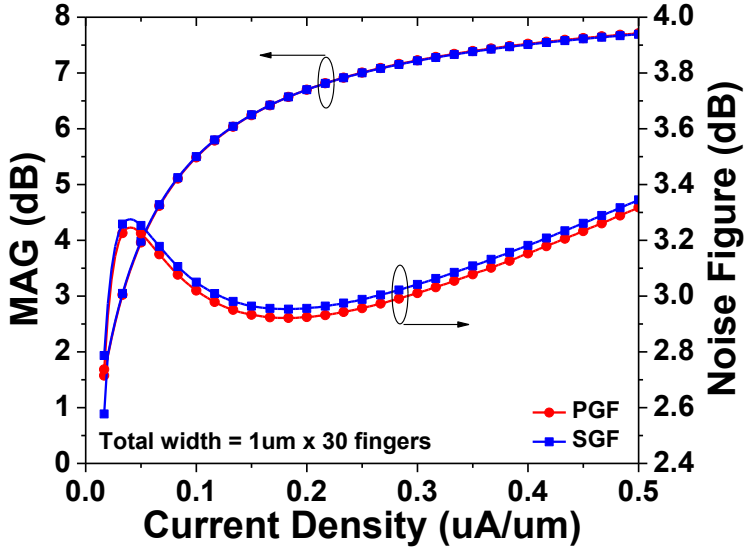
45 nm CMOS SOI



Series Gate Feeding



Parallel Gate Feeding



Similar performances (MSG, NF)

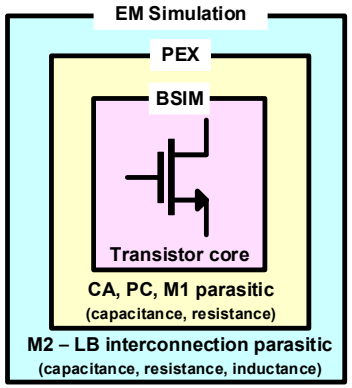
SGF is hard to extract the gate inductance

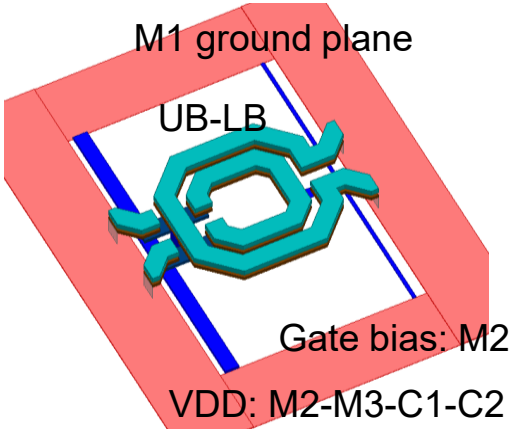
PGF - Source can directly connect to ground

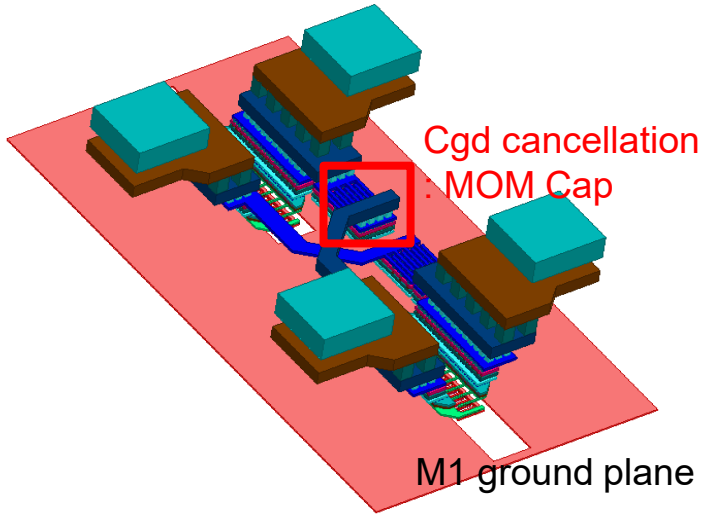
BSIM f_{max} > 400 GHz,
measured f_{max} = 213 GHz
(30x1um single gate contact device)
(Inac et al, 2014)

Design Details – Transistor and Matching Modeling

45 nm CMOS SOI

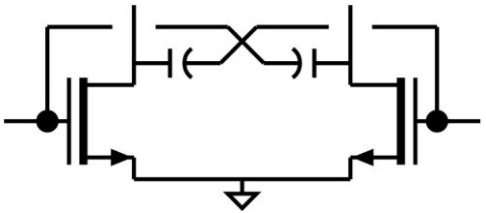




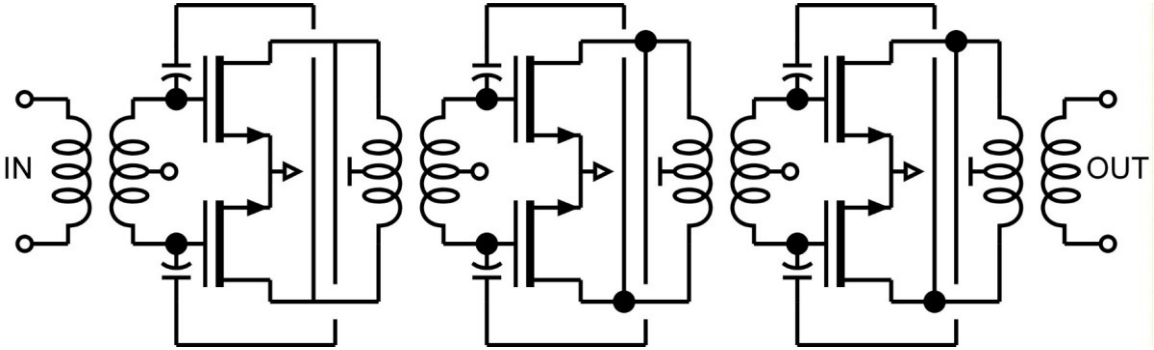


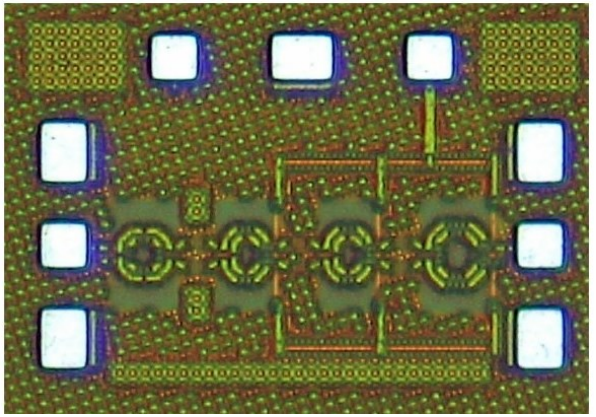
BSIM + PEX + EM simulation
(BSIM & PEX from the foundry, HFSS for EM)

C_{gd} cancellation – better isolation & gain



Design Details – Low Noise Amplifier (LNA)

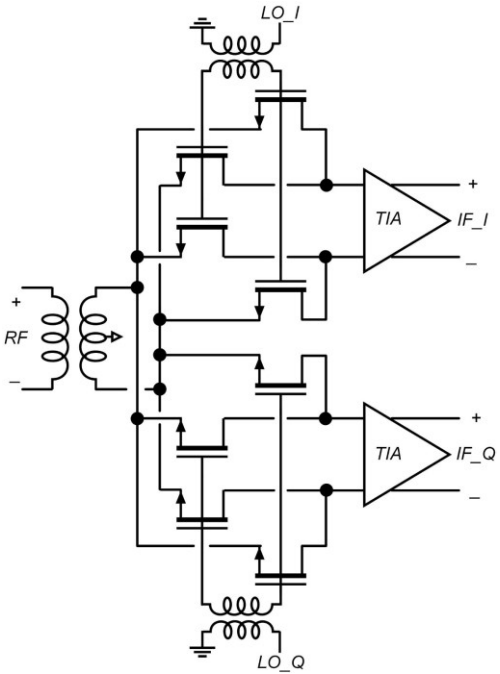


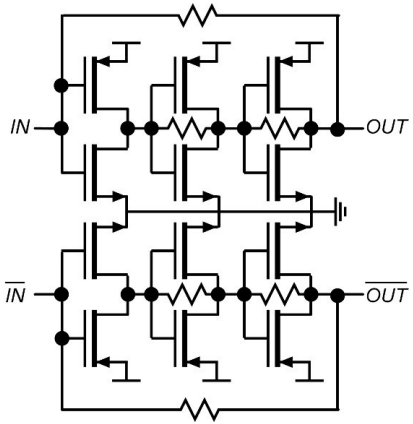


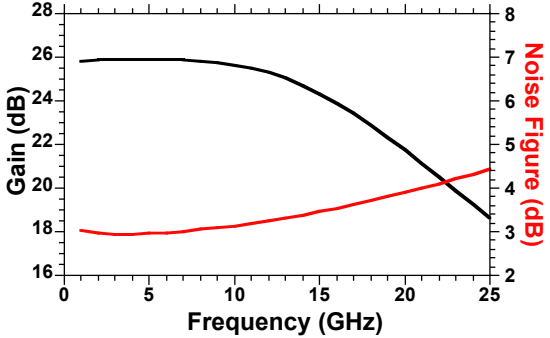
315 x 170 um^2 without pads
~ 415 x 370 um^2 with pads

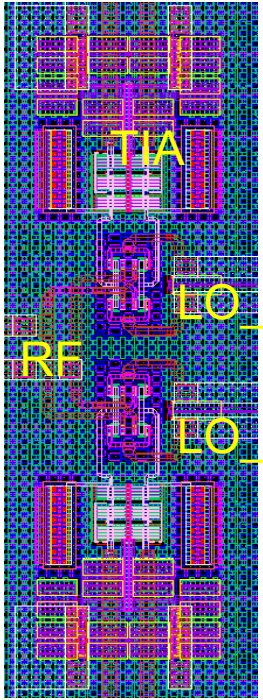
3-stage differential CS amplifier
C_{gd} cancellation
Transformers for matching networks and sing.-to-diff.

Design Details – Down-conversion Mixer









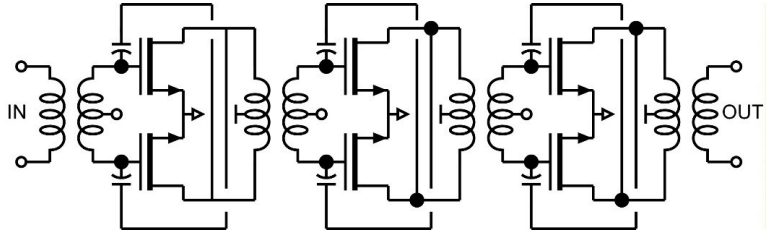
Double balanced passive mixer

Better linearity and low flicker noise

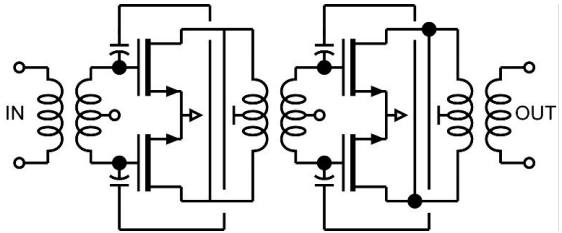
Pseudo-differential TIA

Total width of each transistor (TIA) = 30 μm

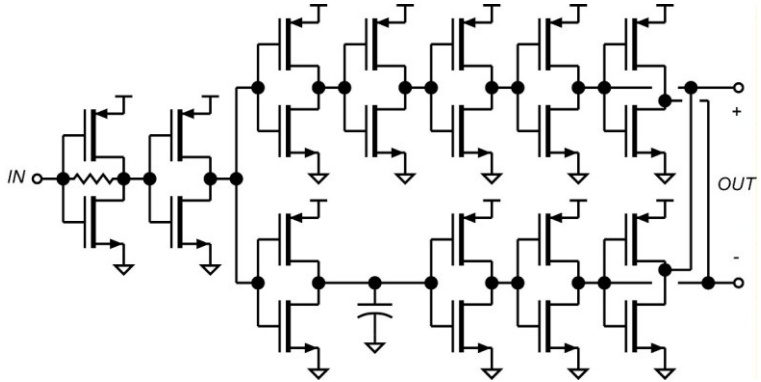
Design Details – x9 Multiplier



X3 (140 GHz)

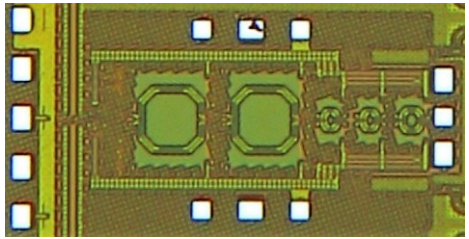


X3 (47 GHz)



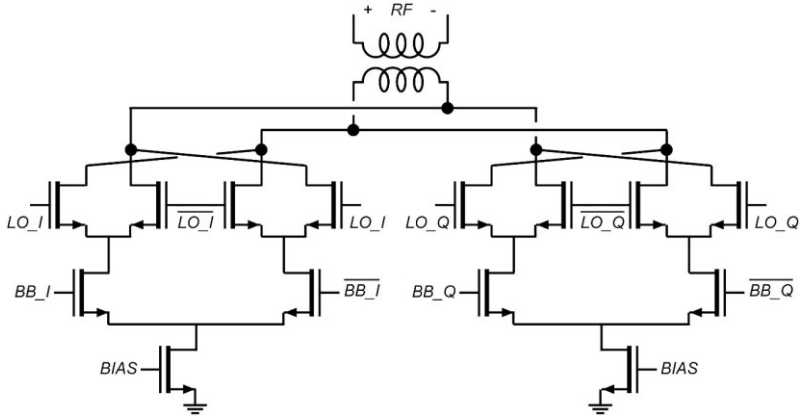
LO Input stage

- Inverter based single-to-differential conversion & 3rd harmonic generation
- 47 GHz and 140 GHz triplers use similar topology with LNA

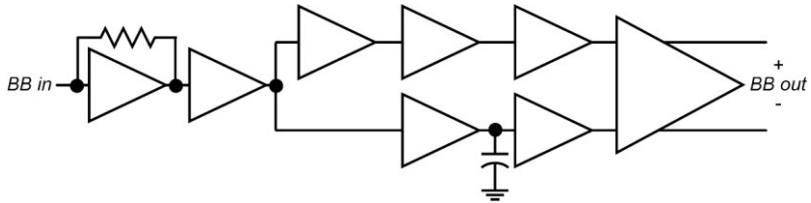


- 80 mA @ 1V

Design Details – Up-conversion Mixer / DA

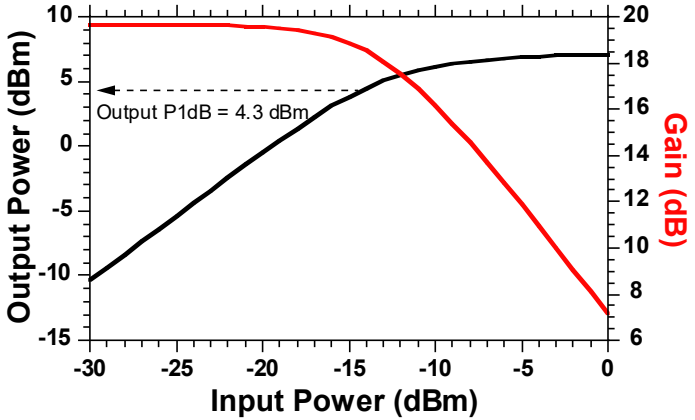


IQ modulator



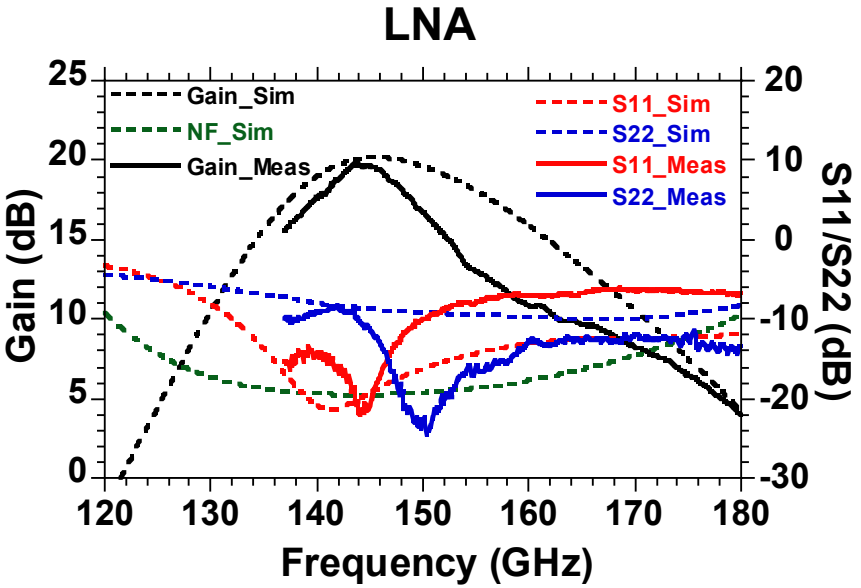
BB input stage

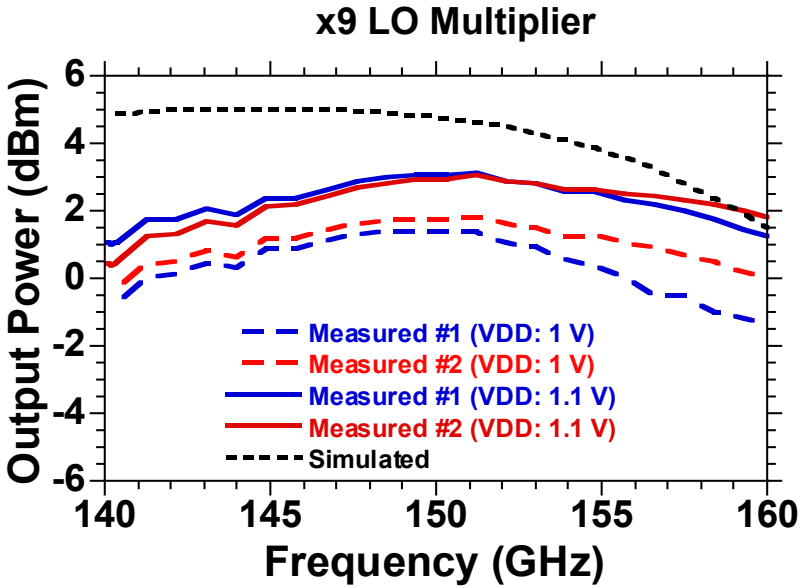
- Active double balanced Gilbert cell design
- Lower conversion loss
- Digital baseband inputs - Limited to QPSK
- DA is same with LNA



Output power: 5 dBm
P1dB = 4.3 dBm

Measurements – Circuit Blocks

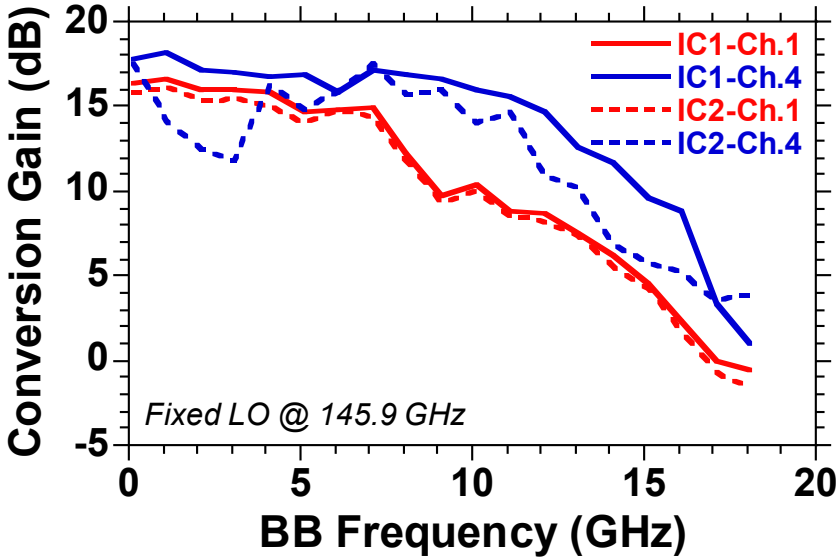


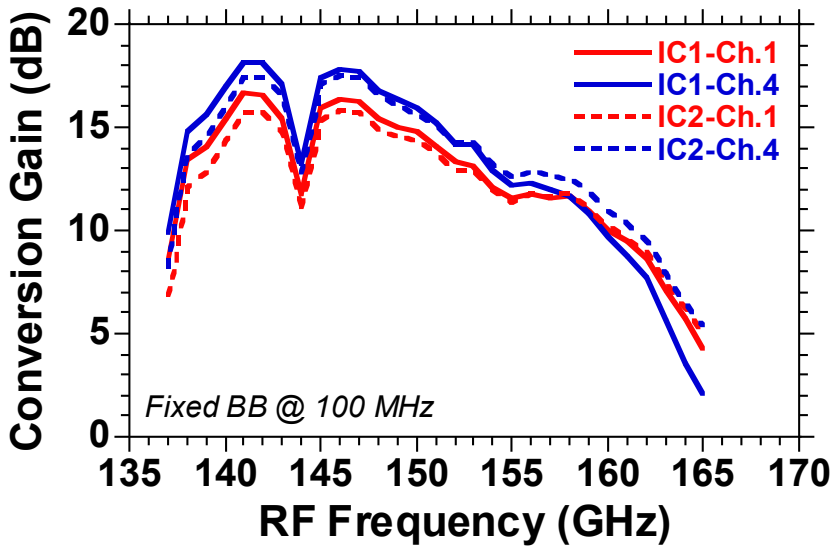


41 mA @ 1V
Peak Gain = 19.9 dB @ 145 GHz
3-dB BW = 10GHz

98 mA @ 1V
Peak output power = 1.5 dBm @ 148 GHz

Measurements – Receiver Channel





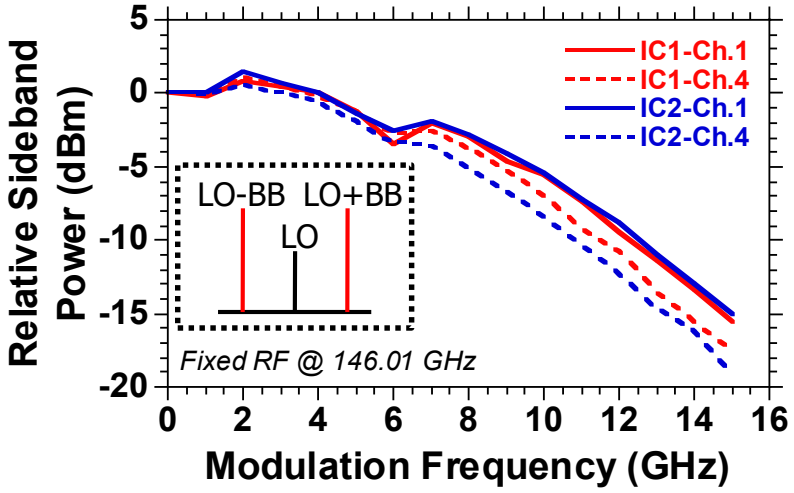
18 dB conversion gain

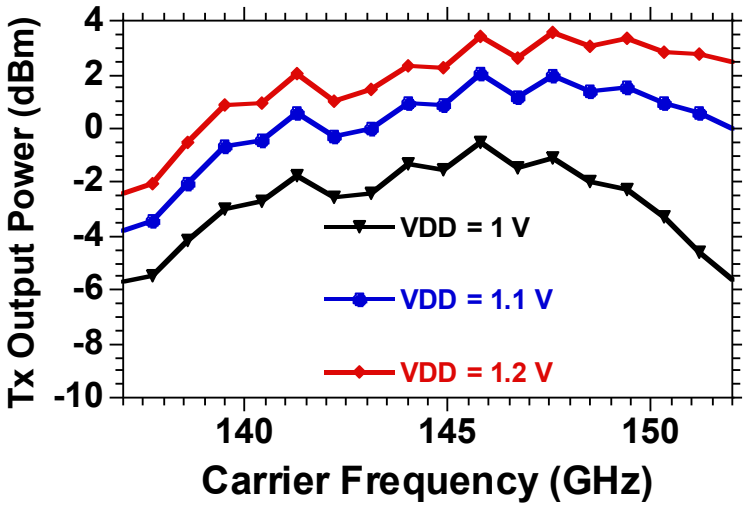
12 GHz 3-dB BW

Narrow-band notch in RF response - limits the data rate

163 mA + 109 mA + 223 mA = **495 mA @ 1V**

Measurements – Transmitter Channel





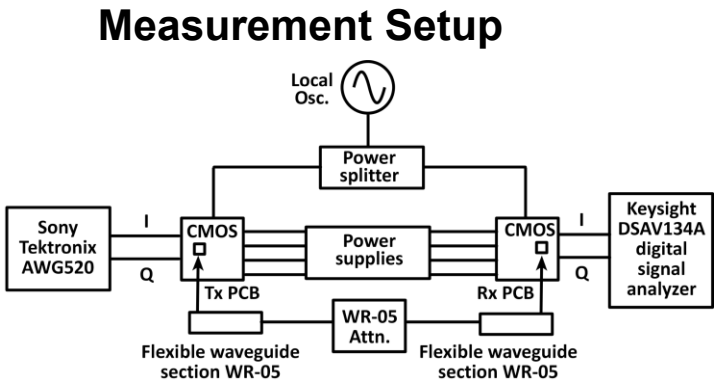
3-dB modulation bandwidth ~ 6 - 8 GHz

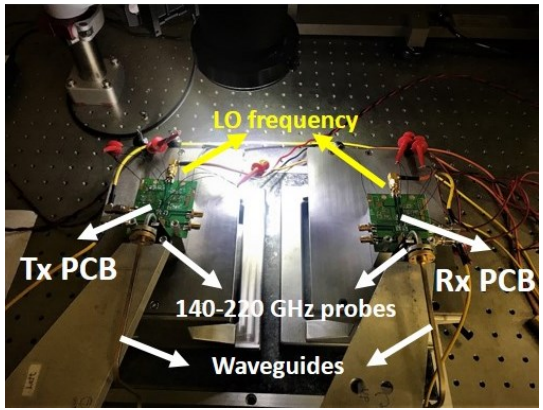
Total transmitter output power: -2 dBm with 1 V supply,

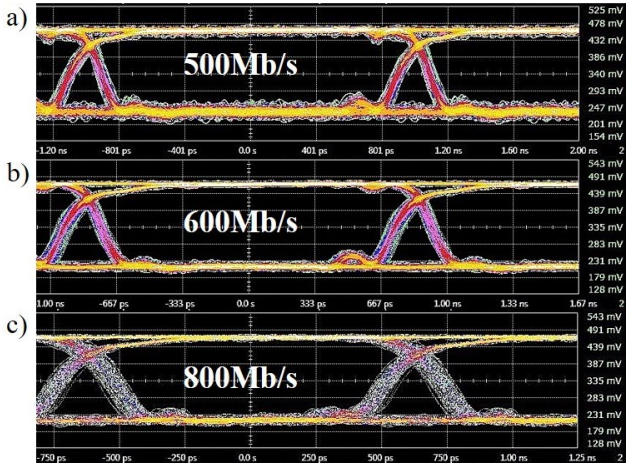
3 dBm with 1.2 V supply **@ 145 GHz**

161 mA + 94 mA + 208 mA = **463 mA @ 1V**

Measurements – Link Experiment







Wired link: G-band (140-220 GHz) waveguide probes, ~1 meter waveguide connection and a waveguide attenuator (20 dB)
common 16.6 GHz LO subharmonic drive signal
mm-wave carrier is at 16.6 x 9 = 149.4 GHz

State of the Art Transceivers

	UC Berkeley (2014)	Tel Aviv Uni. (2016)	UCSD (2014)	Chalmers Uni. (2016)	This Work (UCSB)
Technology	65nm CMOS	28nm CMOS	45nm CMOS	250nm InP DHBT	**45nm CMOS**
Freq. [GHz]	240	102-128	155	110-170	**140**
Gain [dB]	25	36-39	23	26	**18**
NF [dB]	15#	8.4-10.4	20*	9.5	**5.5***
Pdc [mW]	260 (1 TRx)	51 (1 Rx)	345 (1 TRx)	357 (1 TRx)	**958 (4 TRx)**
Area [mm^2]	2 (1 TRx)	0.89 (1 Rx)	3.92 (1 TRx)	3.64 (1 TRx)	**5.91 (4 TRx)**
Integration	Full	Rx Front End	Tx/Rx	Tx/Rx	**Tx/Rx**

*: simulated

#: calculated from measureremements

Conclusion and Future Work

A 140 GHz QPSK transceiver front-end
with four channels per IC to support MIMO

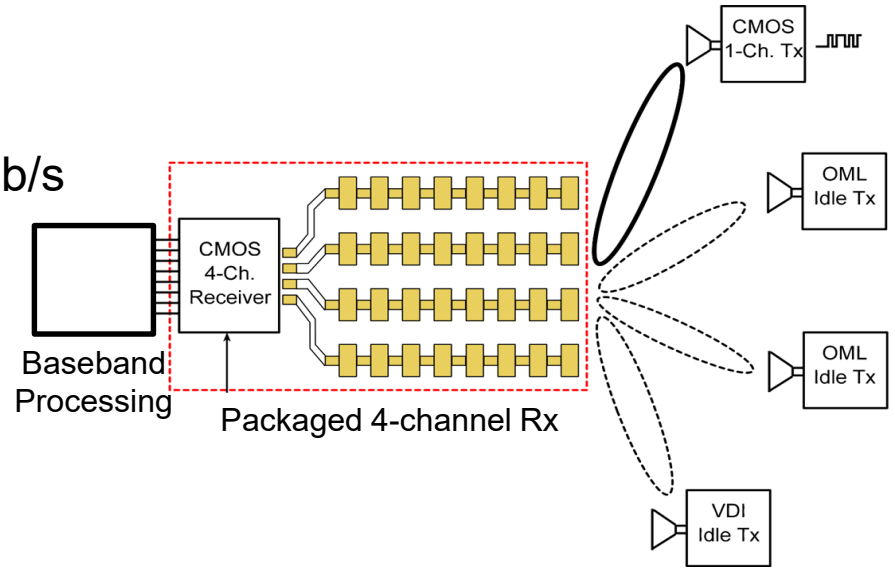
One channel transceiver measurements

Initial link experiment results up to 800 Mb/s

Work in Progress
Wireless link measurements
with higher data rate

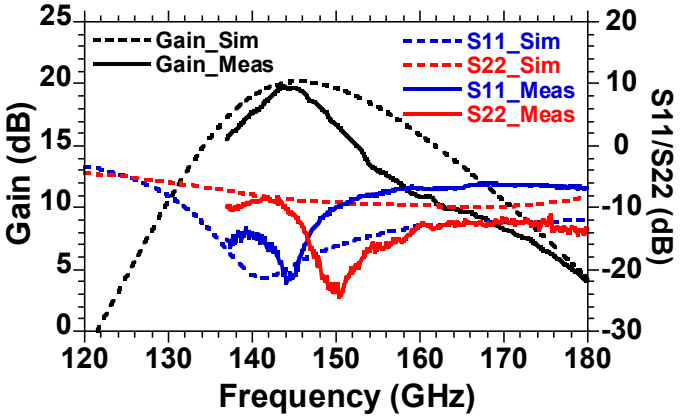
Antenna and package designs

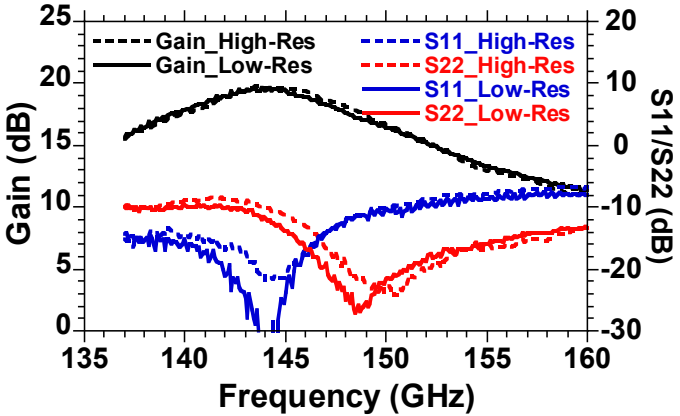
4-channel MIMO receiver hub experiment.



Backup Slides

LNA Measurements



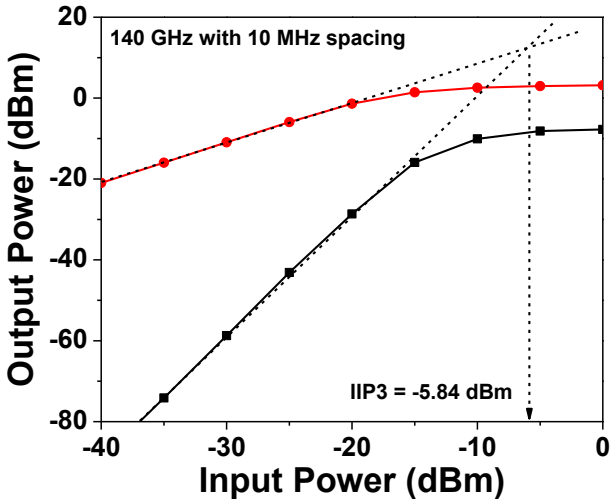


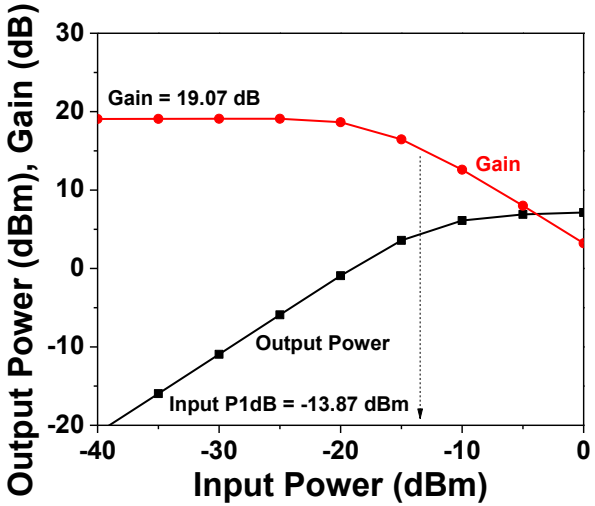
Simulation vs Measurements (trap-rich) Substrate: High (trap-rich) vs Low resistivity

3-dB bandwidth: 11 GHz (138 – 149 GHz)

Power consumption: Trap-rich 42.4 mW @ 1 V
Low-res. 41.7 mW @ 1 V

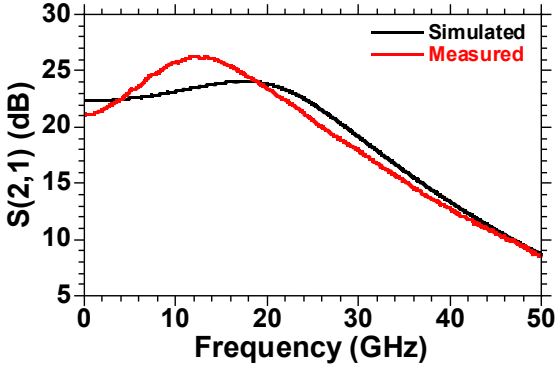
LNA Linearity Simulations



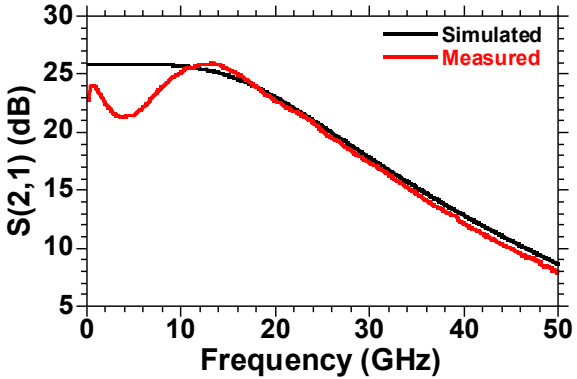


IIP3: -5.84 dBm, Input P1dB: -13.87 dBm

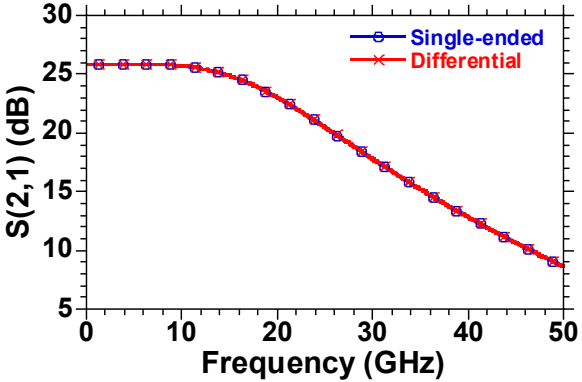
TIA Breakout measurements



*TIA: total width of each transistor: 30 um



Simulation: Ideal
Measurement: VDD without 50 Ω termination

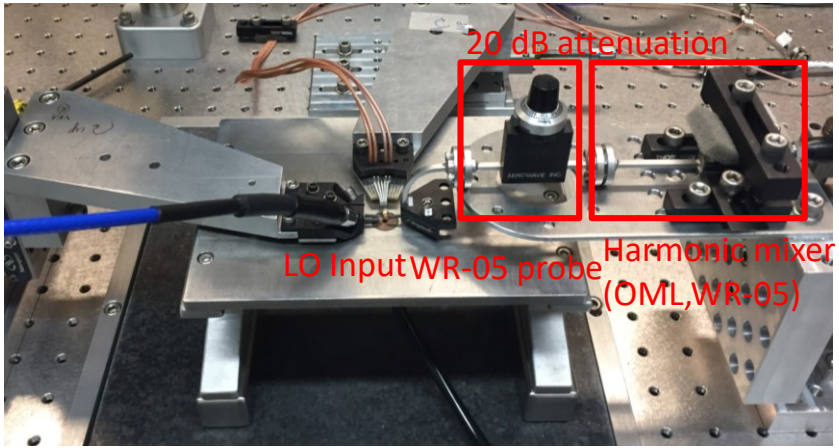


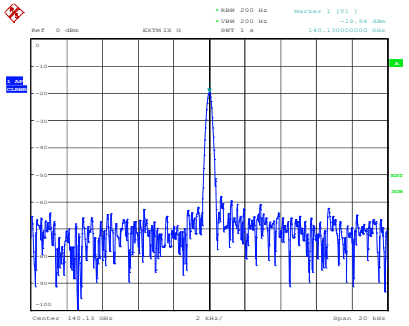
Simulation: Ideal
Measurement: VDD with 50 Ω termination

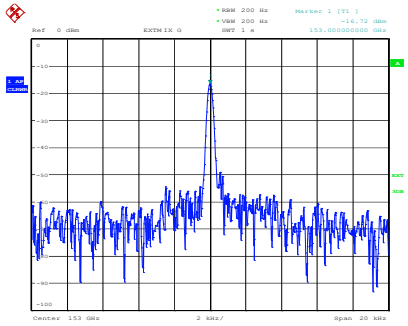
Power consumption
- Simulation 12 mA @ 1 V
- Measurement 11.9 mA @ 1 V

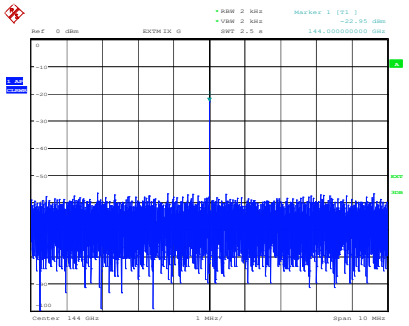
In/output feeding lines are not de-embedded in the measurement
Simulation results doesn't include the feeding lines
Notch due to the bias network (next slide)

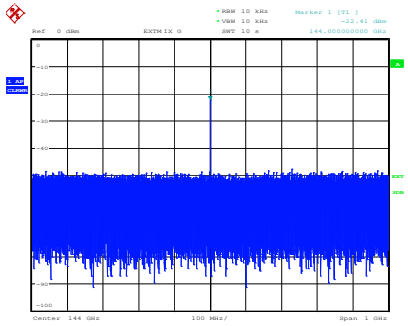
Multiplier chain (x9) measurement setup







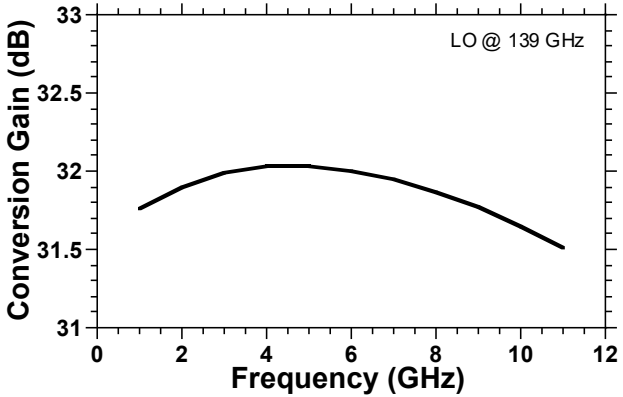


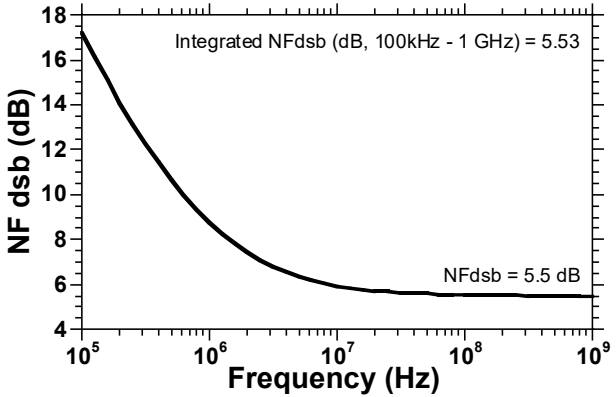


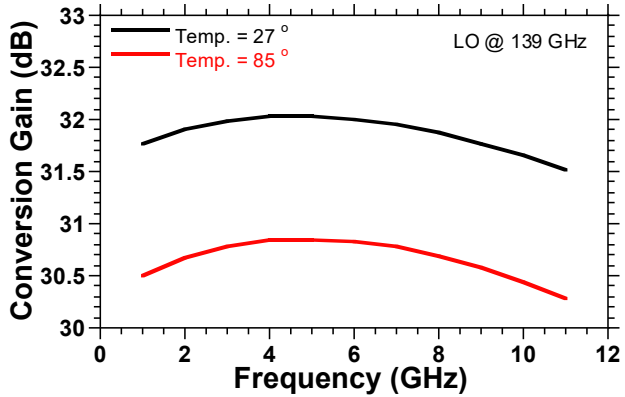
Harmonic mixer:

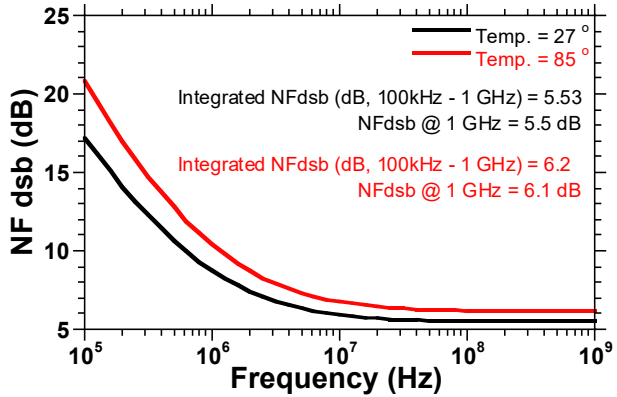
- Harmonic number: 16, IF @ 404.4 MHz

Receiver Simulations

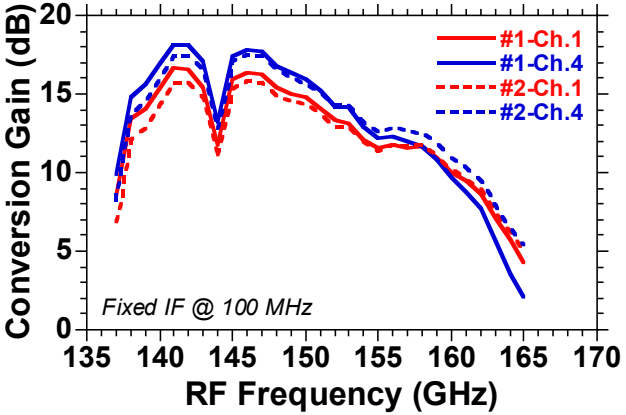


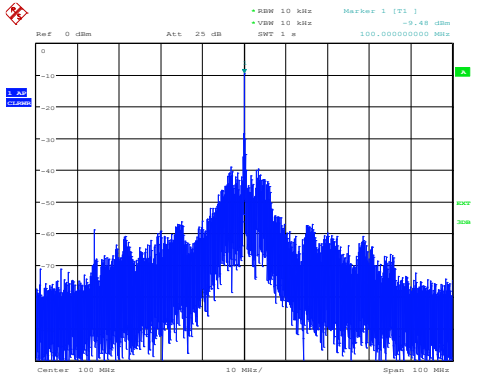




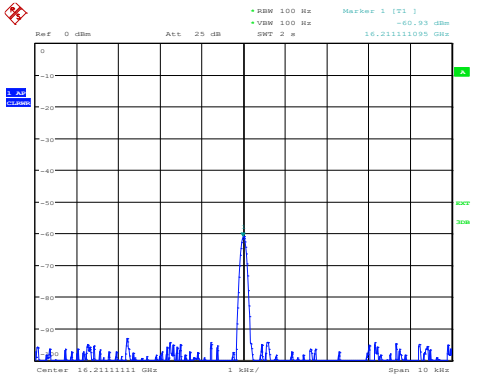


Receiver measurements

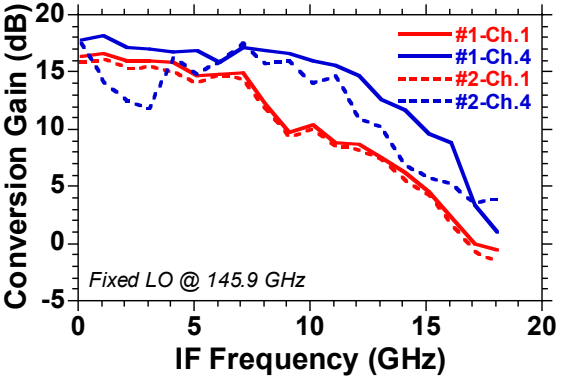


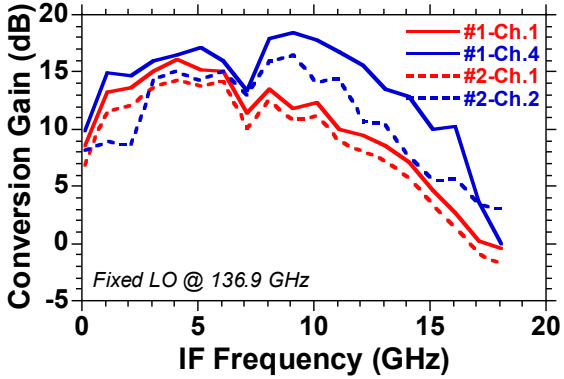


IF spectrum: span 100 MHz

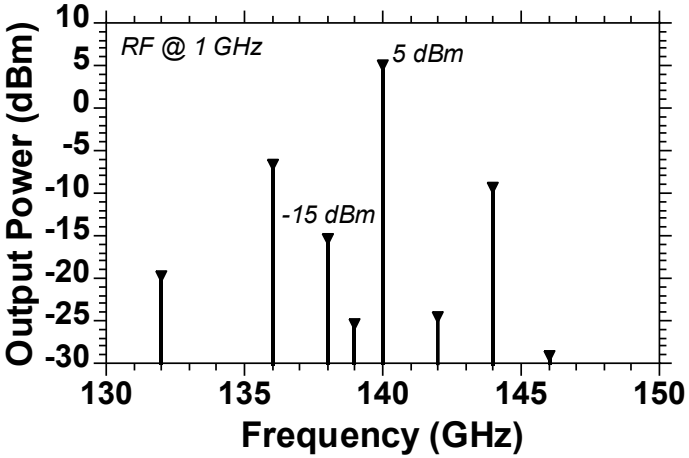


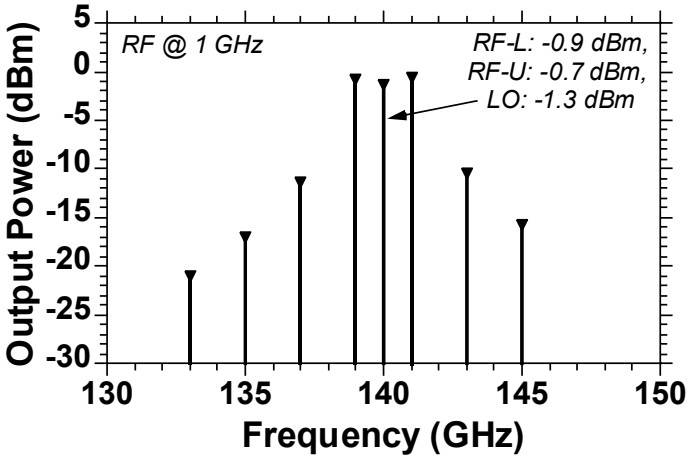
LO feedthrough





Transmitter Simulations

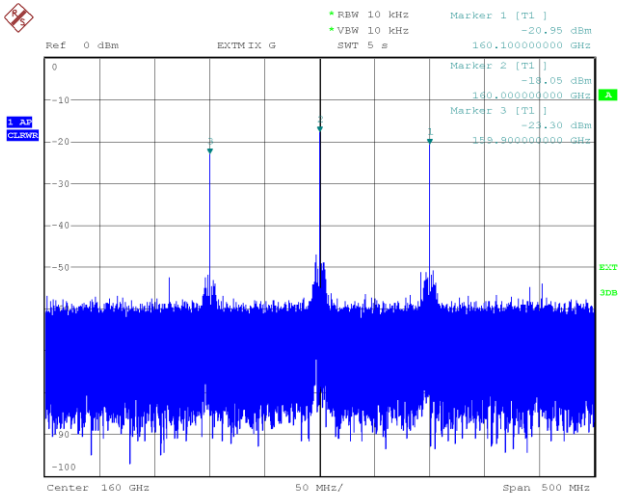




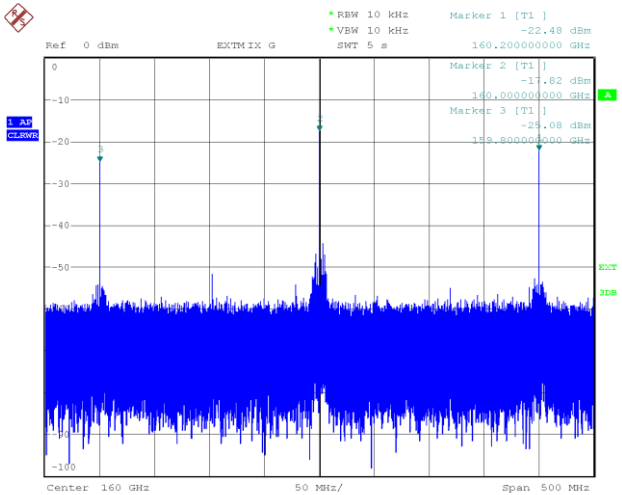
LO feedthrough: Q-mixer is unbalanced
Lower output power ~ 6 dB

0 V quadrature input

Transmitter measurements



BB @ 0.1 GHz, LO @ 160 GHz



BB @ 0.2 GHz, LO @ 160 GHz

BIAS	VDD (V)	Current (mA)	
		Chip1	Chip2
Driver amp.	1	160	161
Mixer	1	89	94
Multiplier chain	1	204	208

Measurement setup: BB-I input is open, all channels are in the on state

Transmitter measurements