A High-Spurious-Harmonic-Rejection 32-53 GHz and 50-106 GHz Frequency Doublers using Digital Logic and DC Negative Feedback

Seong-Kyun Kim[*#], Arda Simsek[*],
Miguel Urteaga[#], Mark J.W. Rodwell[*]

[*]University of California at Santa Barbara, USA
[#]Teledyne Scientific and Imaging, USA

UCSB
UNIVERSITY OF CALIFORNIA
SANTA BARBARA

TELEDYNE
SCIENTIFIC & IMAGING
Everywhereyoulook™

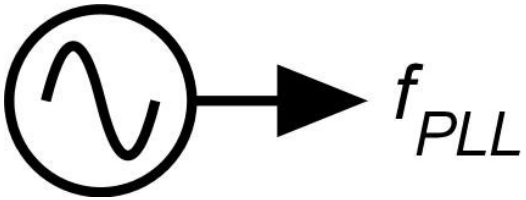
48TH EUROPEAN MICROWAVE CONFERENCE 2018
The 48th European Microwave Conference

EuMIC 2018
The 13th European Microwave Integrated Circuits Conference

EuRAD 2018
The 15th European Radar Conference

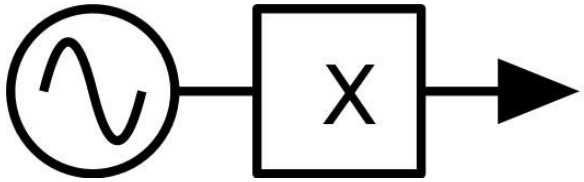
mm-wave LO Generation

mm-wave systems for military systems and mobile wireless
→ Require low-phase-noise mm-wave LO



Considerable phase noise
-low-Q passive devices at mm-wave

Moderate tuning range

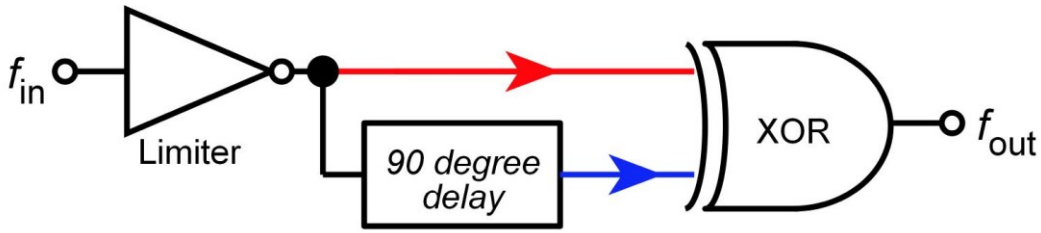


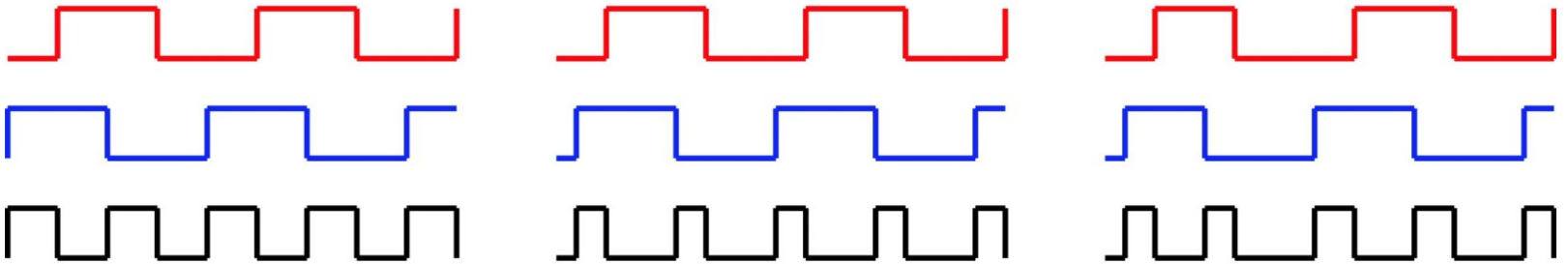
Lower phase noise
- GHz-range PLL with high-Q devices

Wide tuning range

Spurious harmonics
- generate out-of-band interference

Problems of Conventional Design





<u>Limiter DC offsets</u>

Spurious outputs at DC, $2f_{in}$, $4f_{in}$, …

→ spurious XOR outputs at f_{in}, $3f_{in}$, $5f_{in}$, …

<u>Delay ≠ 90 degree</u>

Spurious XOR outputs at DC, 4fin, ...

<u>High-Q filters are required</u>

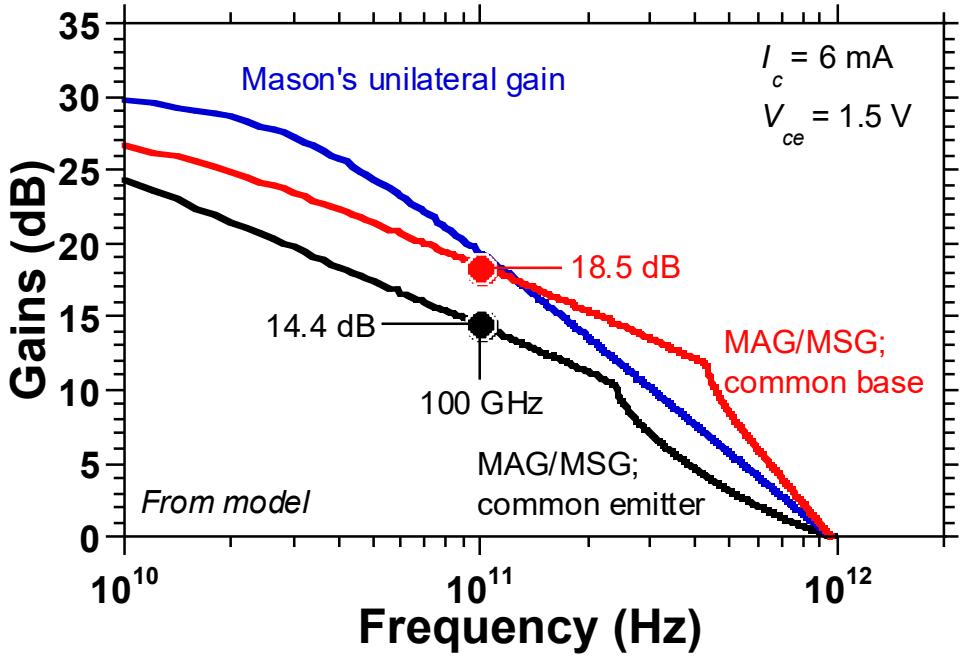
large die area

poor out-of-band rejection

<u>CMOS digital logic</u>

Cannot operate > 100 GHz

THz HBTs → Digital logic at > 100 GHz



Teledyne 130 nm InP HBT

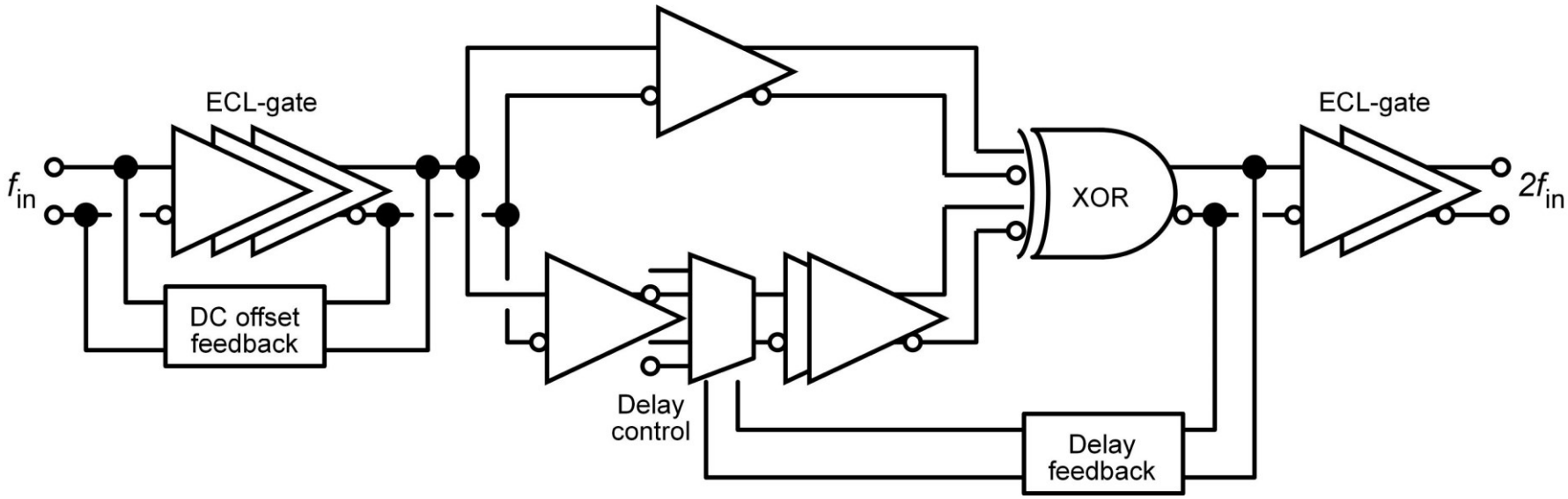
1.1 THz f_{max}.

CE: 14.4 dB MSG @100 GHz

CB: 18.5 dB MSG @100 GHz

THz transistors enable a broadband frequency multiplier architecture using digital logic at > 100 GHz

Proposed Frequency Doubler



DC offset feedback

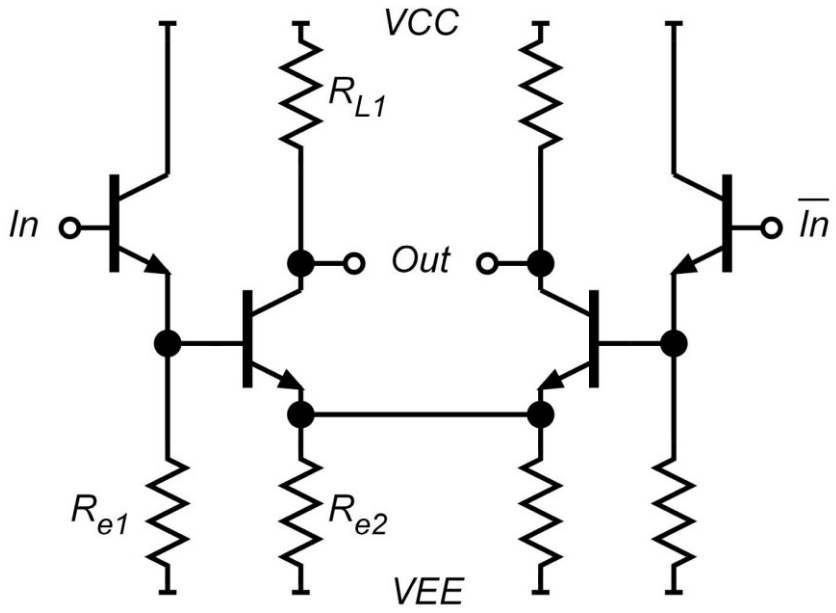
Minimize dc offset of the ECL limiter output

Delay feedback

The phase shifter (delay circuit) to 90 degree delay

→ ***Suppress spurious harmonics***

In/Output-stage: ECL-gate



Input

Converts a sinusoidal input into a square-wave

Input can be driven single-endedly

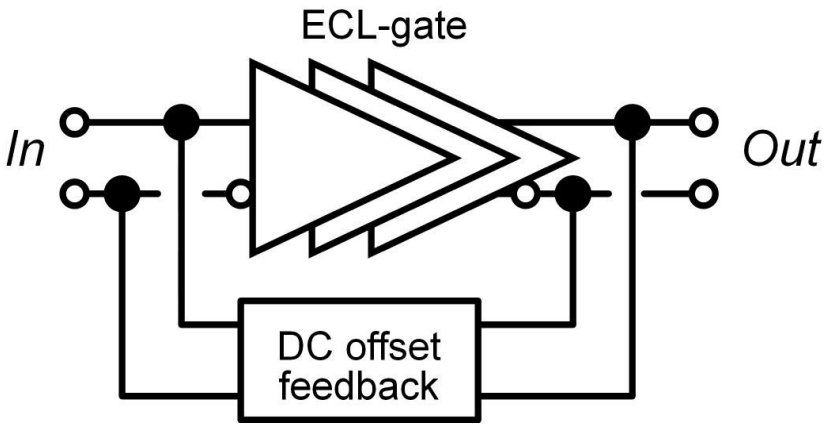
Low input signal (-3 dbm) can drive

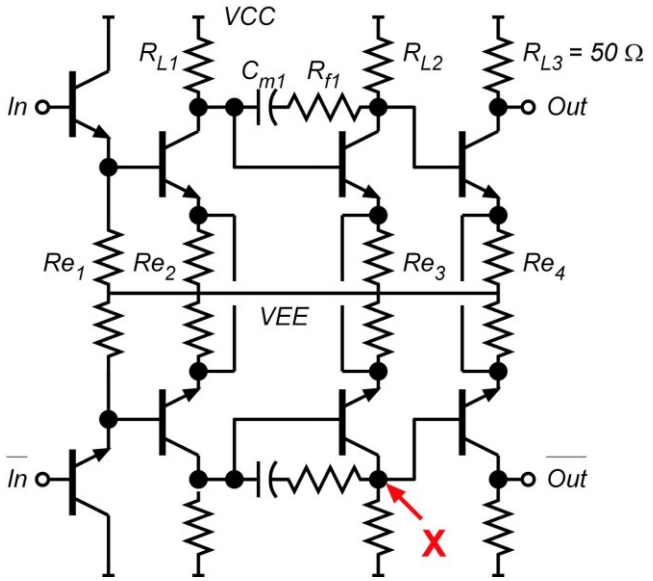
Output

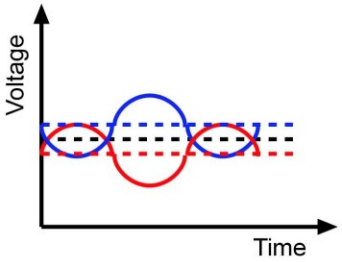
Driver 50 Ω output load

ECL-gate can operate at > 100 GHz

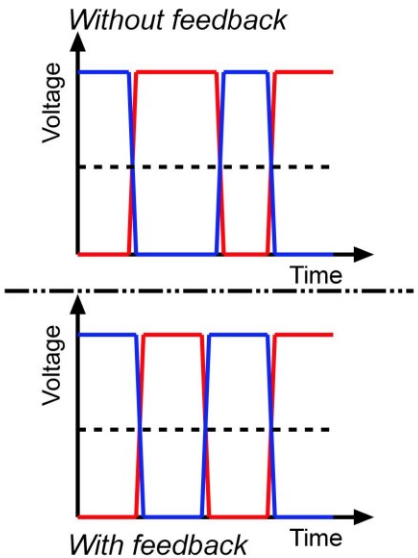
DC-offset Cancellation



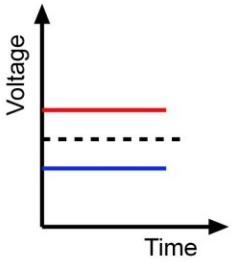




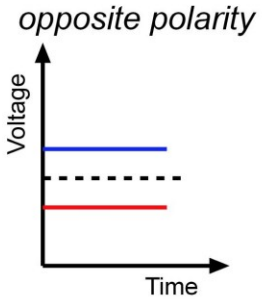
In



Out
(Feedback Input)



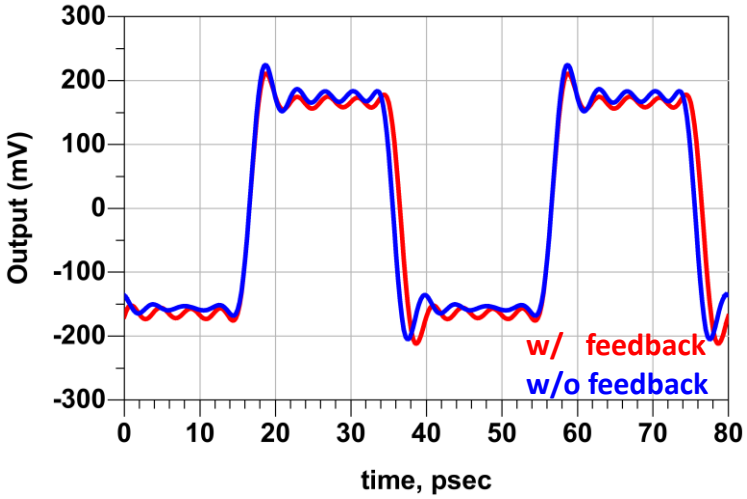
Node X

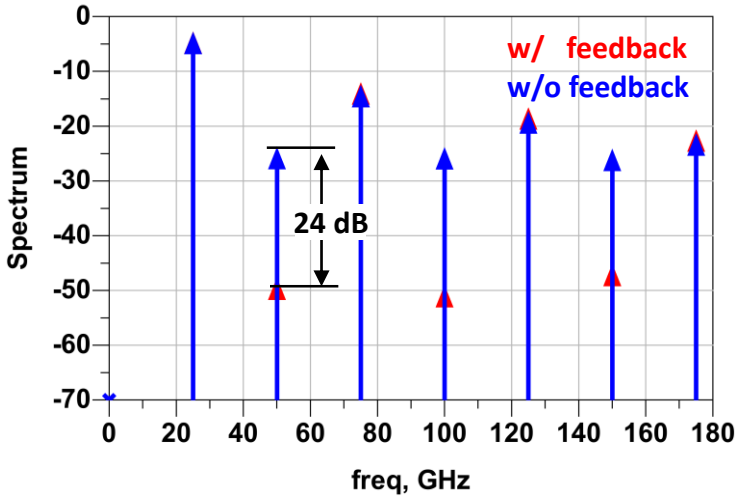


Feedback Output
(Connected to In)

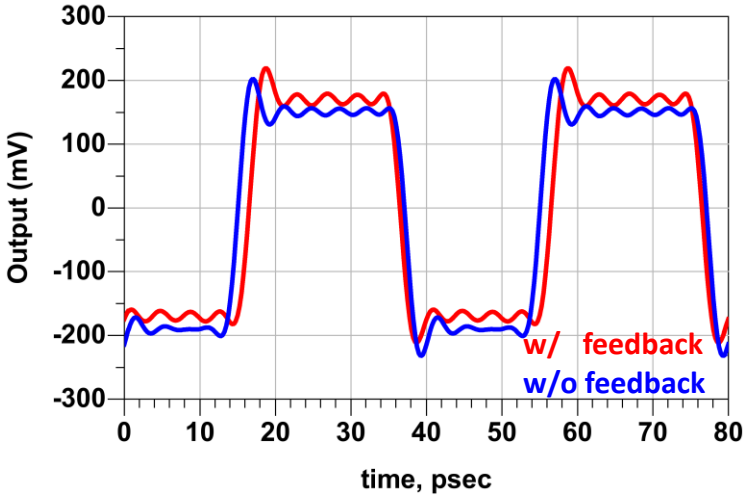
Simulation results: Input 25 GHz

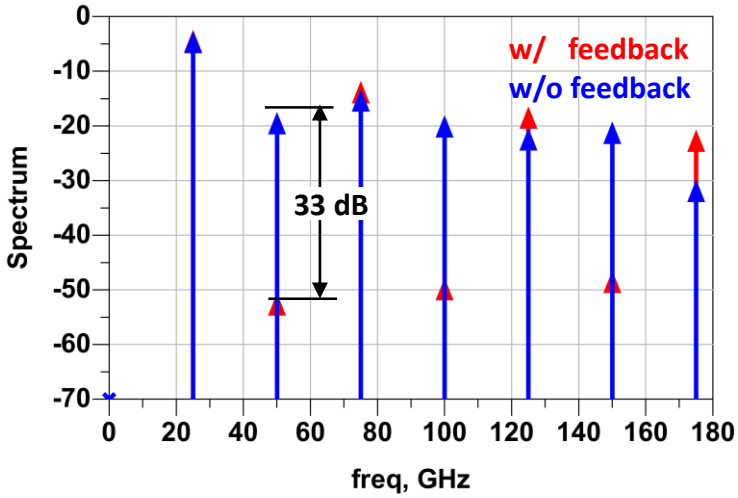
The second ECL-gate has 100 mV offset voltage



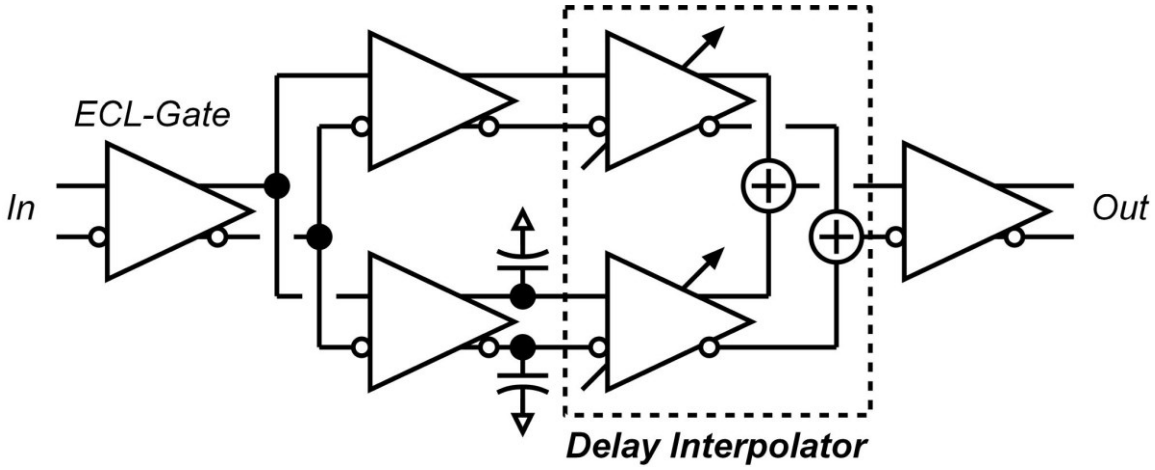


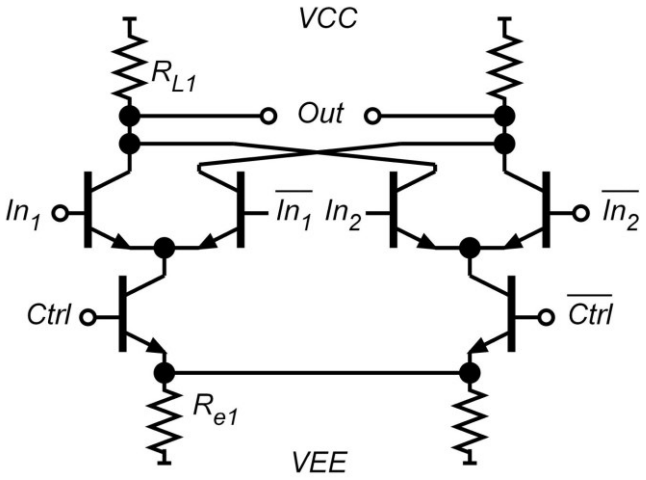
Each ECL-gate has 100 mV offset voltage





Delay Control

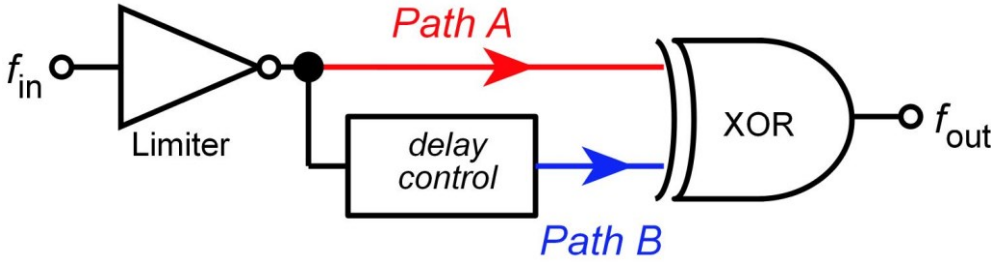


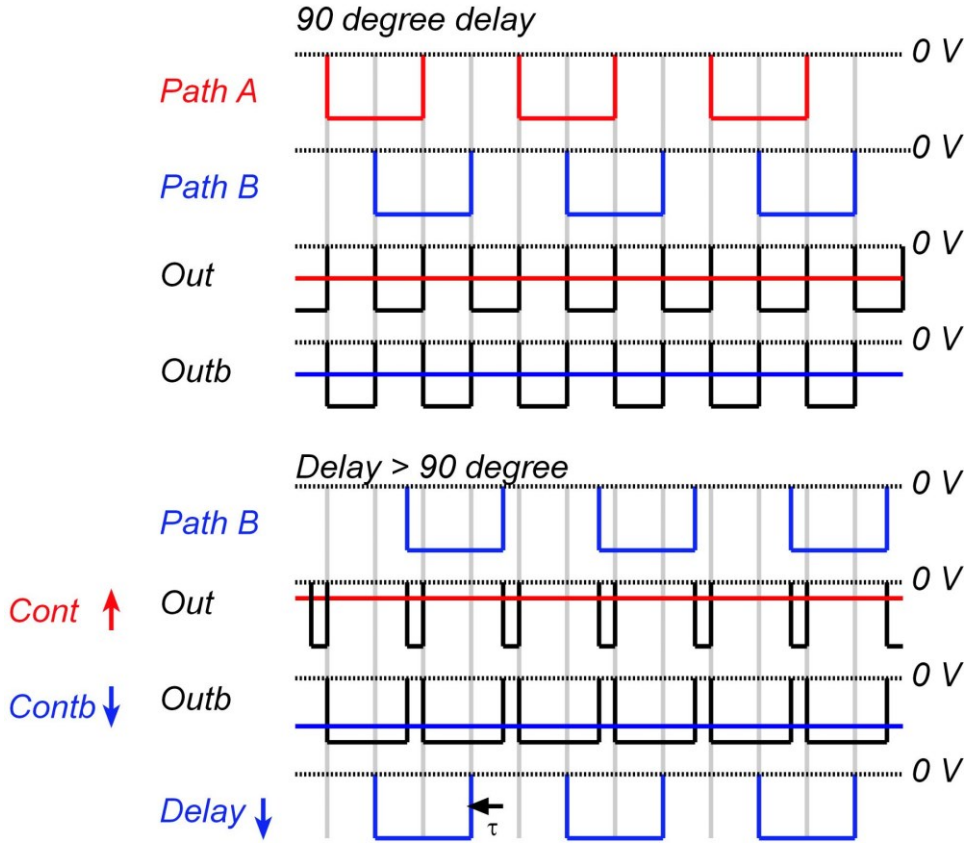


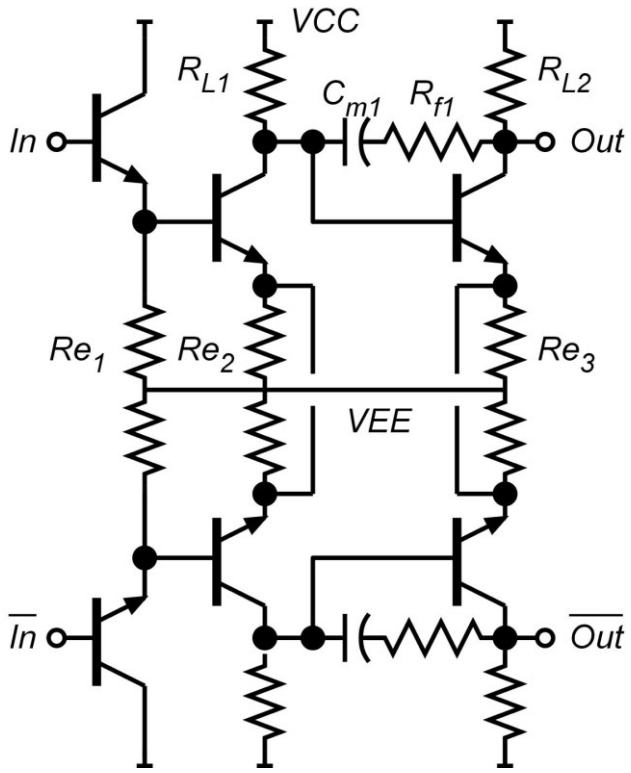
Delay interpolator

Optimum operating range is limited by the tunable delay range
XOR has same topology as the delay interpolator

Delay Feedback & Operation



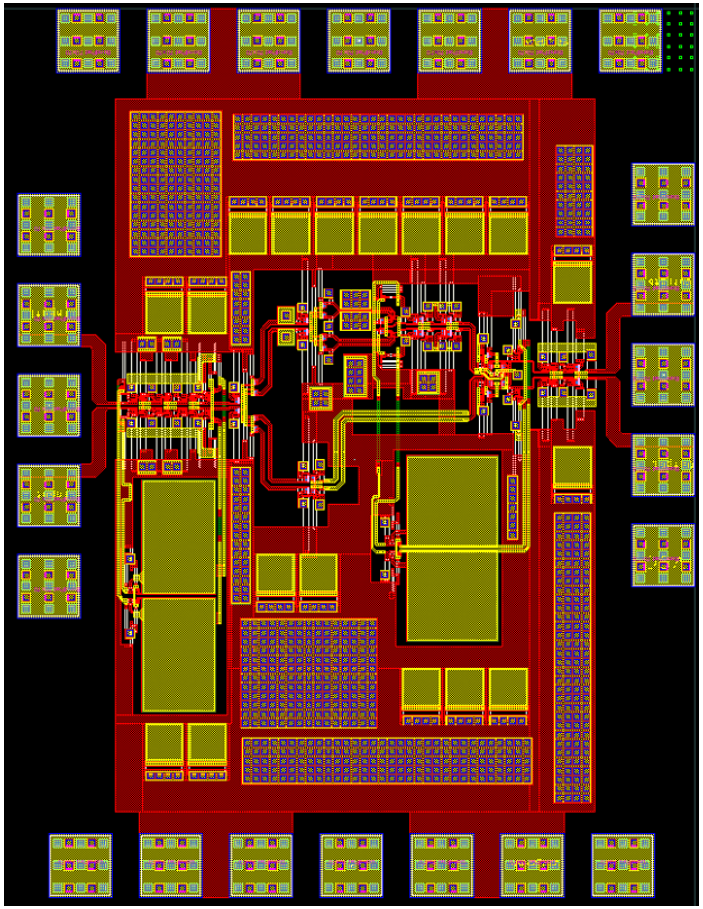


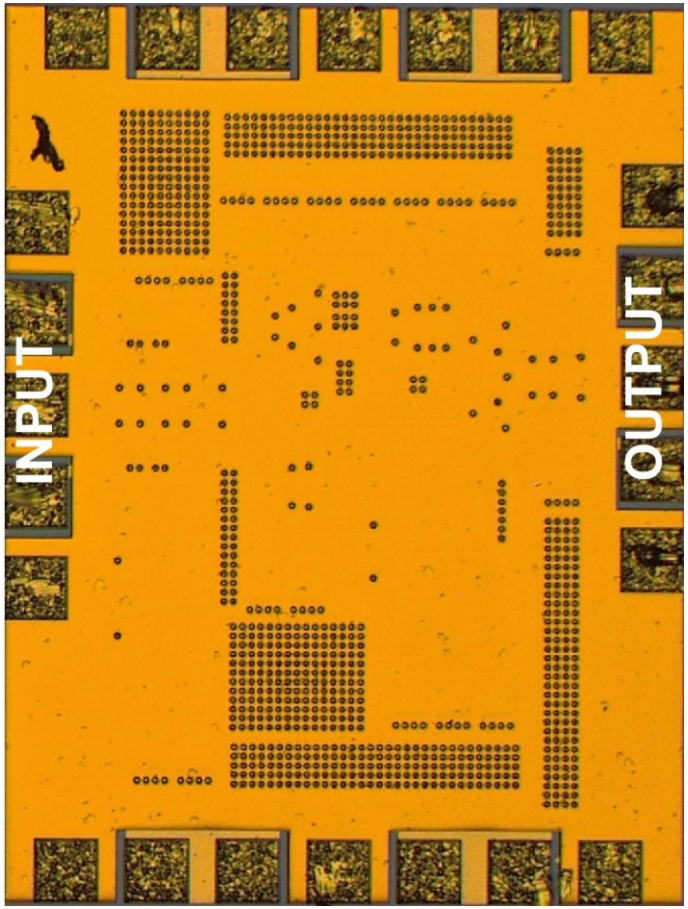


Input is connected to XOR outputs

Outputs are connected to Ctrl of the delay interpolator

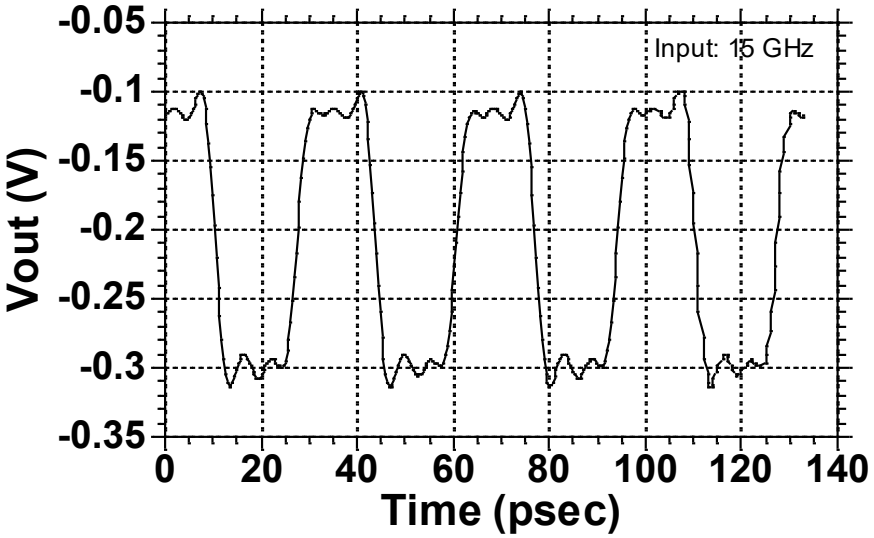
Layout & Chip Photo



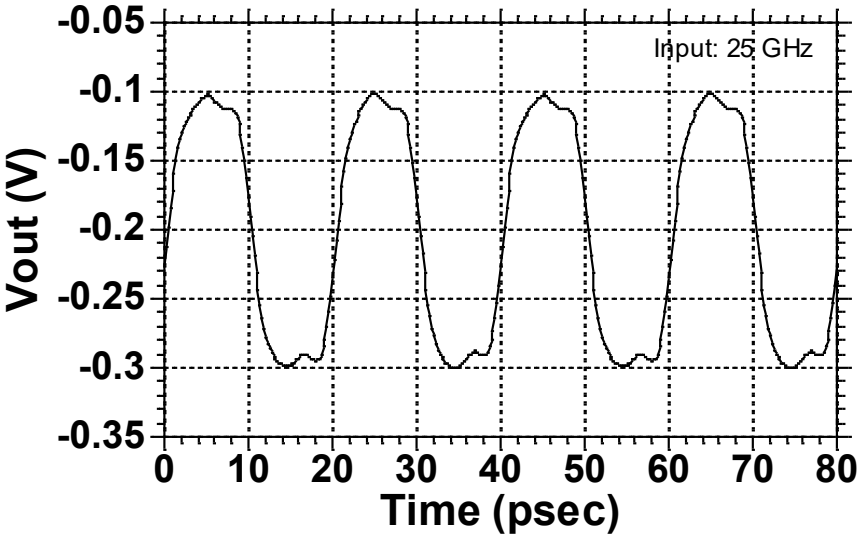


Chip size: 750 × 990 um^2 (area encloses active devices: 540 x 280 um^2)
Power consumption: 284 mA (32 – 53 GHz), 324 mA (60-100 GHz) @ 3.3 V

Simulation: Time-domain



Input 15 GHz → Output 30 GHz



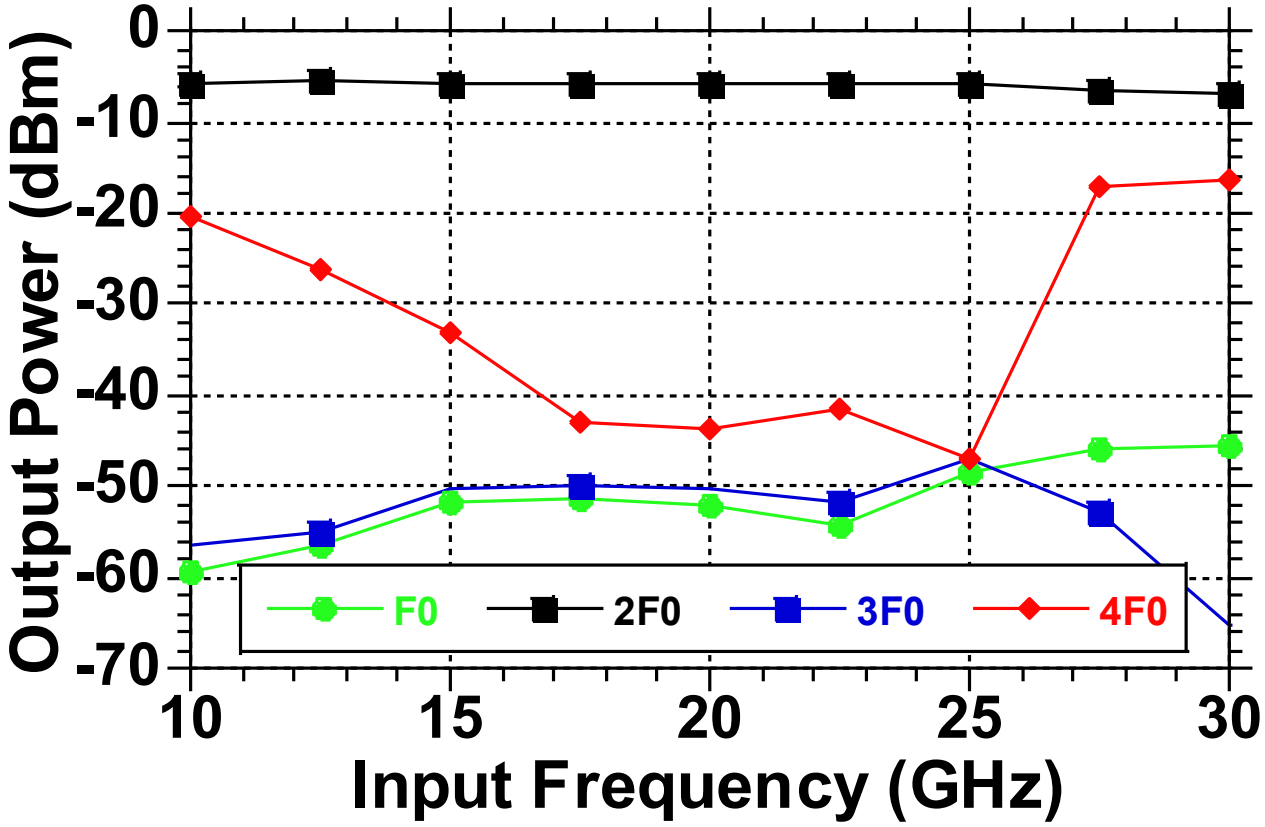
Input 25 GHz → Output 50 GHz

** single-ended simulation results*

Waveforms have 50 % output duty-cycle

The amplitude correspond to digital logic level in the design

Simulation: Frequency-domain

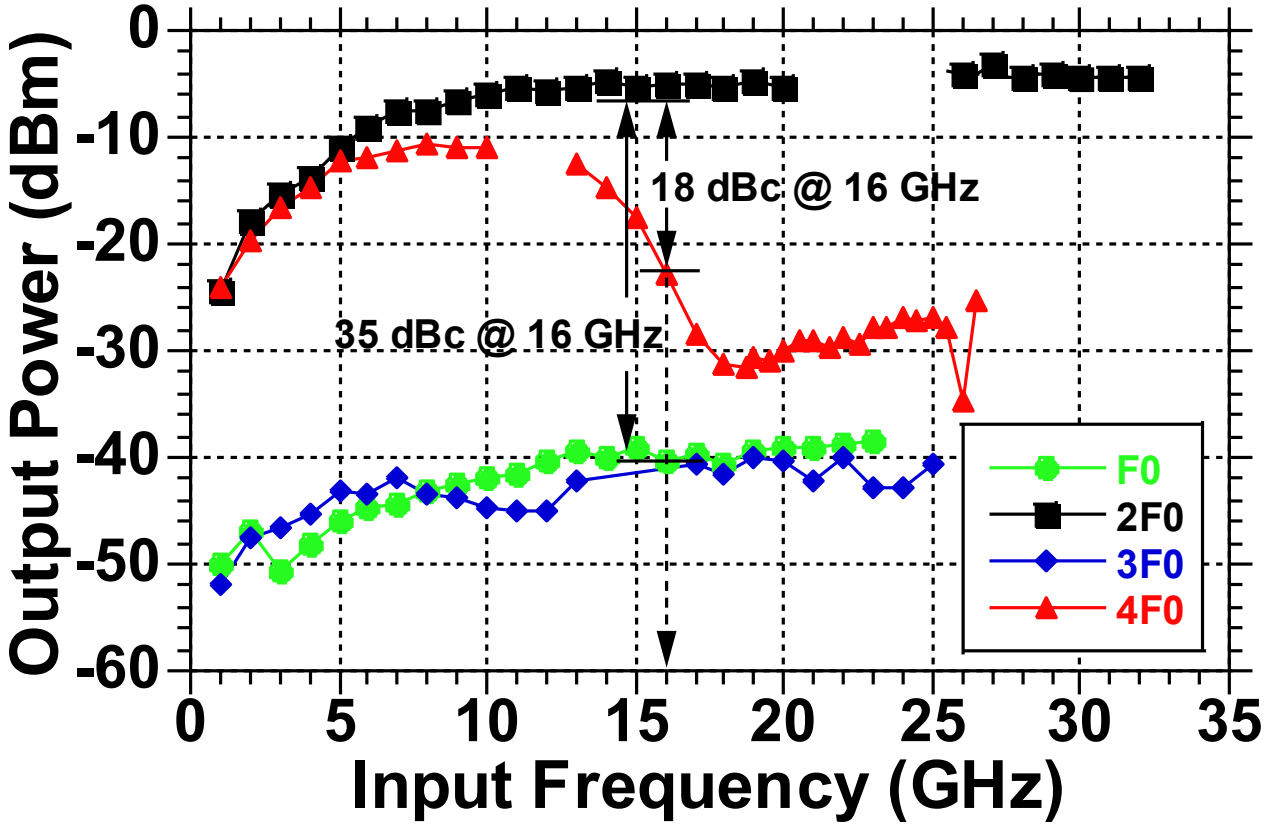


2nd harmonic output power: -8 – -5 dBm

1st & 3nd harmonic rejection > 40 dBc

4th harmonic rejection > 30 dBc

Doubler: 32 – 53 GHz Output

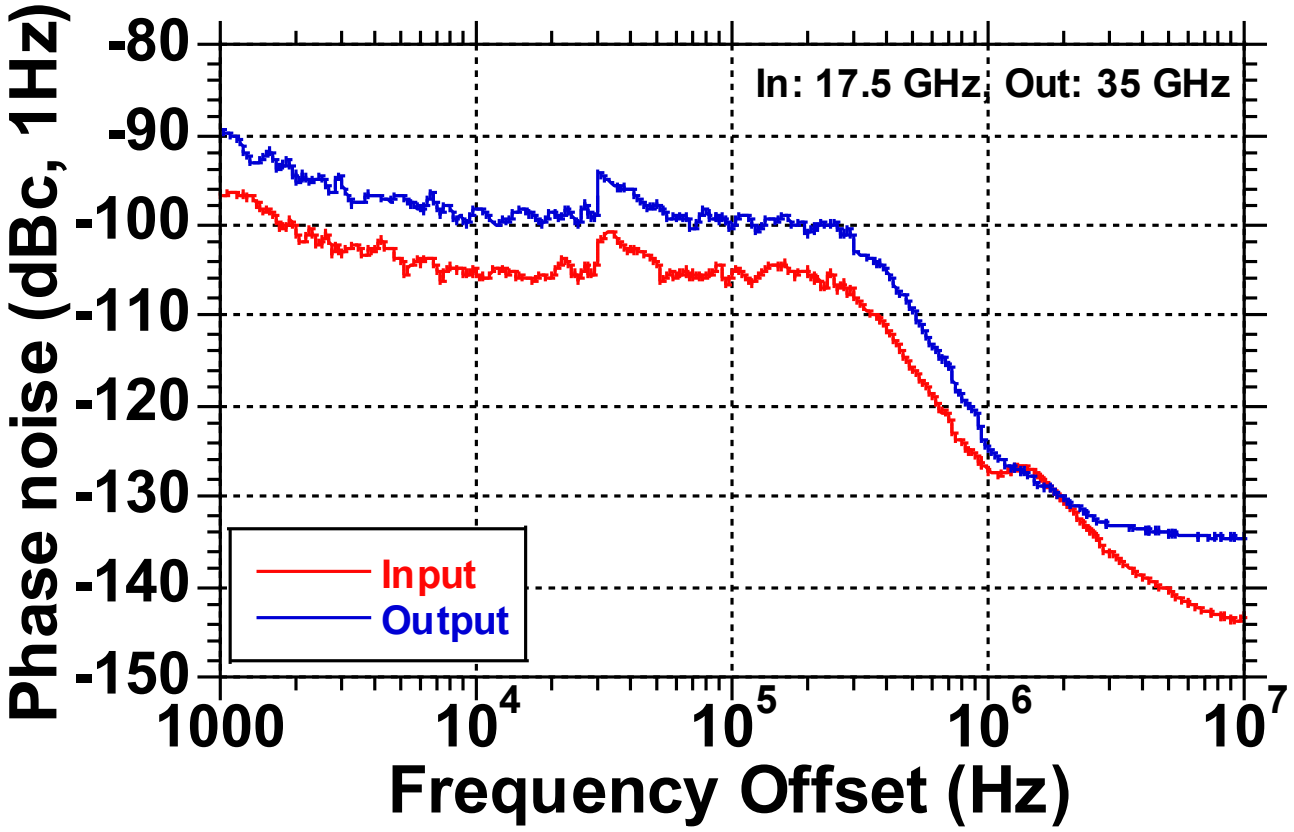


2nd harmonic output power: -5 – -8 dBm

1st & 3rd harmonics rejection > 30 dBc.

4th harmonic rejection > 18 dBc within the delay tuning range (16 – 26.5 GHz)

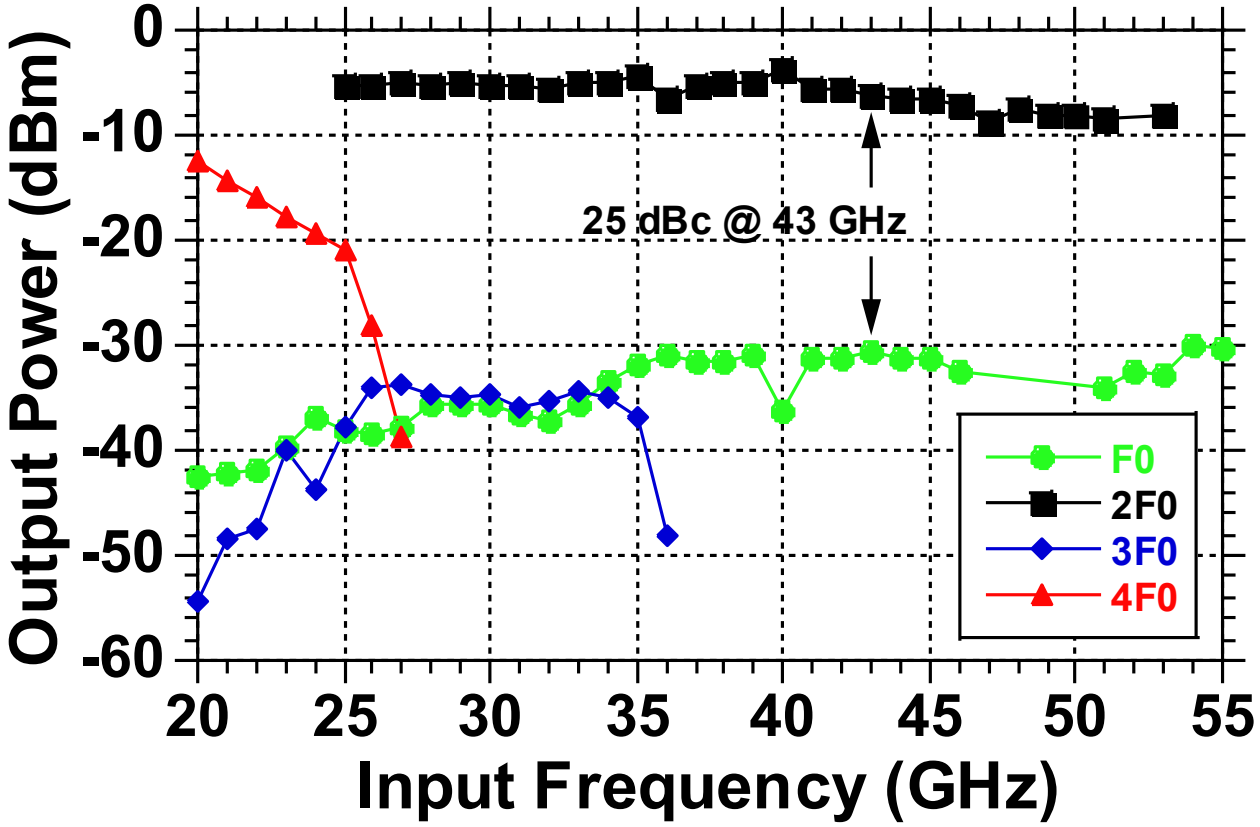
Phase Noise Measurements



Input: 17.5 GHz, Output 35 GHz

Added phase noise: 6 – 7 dB (*ideal multiplier: 20*log(N)*)

Doubler: 60 – 100 GHz Output



2nd harmonic output power: -5 – -8 dBm

1st & 3rd harmonics rejection > 25 dBc.

4th harmonic rejection: similar behaviour as the lower frequency doubler

*limited results at high frequency due to the available test equipment

Performance of the proposed

	[4]	[5]	[6]	[7]	This work	This work
Technology	0.18 um SiGe BiCMOS	90 nm CMOS	0.2 um InP DHBT	0.13 um SiGe BiCMOS	0.13 um InP DHBT	0.13 um InP DHBT
Topology Input / Output	Differential Differential	Single Single	Differential Single	Single Single	Diff./Single Differential	Diff./Single Differential
Output BW (GHz)	36 – 80	42 – 90	DC – 100	27 – 41	32 – 53*	50 – 106*
Input Power (dBm)	-7 @ 66 GHz 1 @ 80 GHz	5	-5 @ 60 GHz	-15.5	-3#	-3#
Output Power (dBm)	1.7 @ 66 GHz -3.9 @ 80 GHz	-6 – -3	-10 @ 60 GHz	1.3 – 4.3	-5#	-5 – -8#
Pdc (mW) @ V_{DC}	137 @ 3.3	20 @ 1	730 @ -4.5	17-22 @ 2	937 @ -3.3	1069 @ -3.3
Fundamental Suppression (dB)	20 - 36	20 – 48	24 – 32	25.7 – 33	35	25
3rd order Suppression (dB)	N/A	N/A	N/A	N/A	35	29+
4th order Suppression (dB)	N/A	> 14	N/A	N/A	>18	>15
Area (mm^2)	0.27	0.33	2.24	0.34	0.74	0.74

Note that, to demonstrate the harmonic rejection performance of the present work, no output band-pass filter have been used. Filtering will improve harmonic rejection.

* The doubler can work at higher input frequencies; harmonic rejection at such input frequencies was not tested because of the available test equipment.

Single-ended measurement results.

+ Only up to 36 GHz input frequency range due to the available test equipment.

High-Spurious-Harmonic Rejection Doubler

Broadband frequency doublers with 32 GHz to 53 GHz
and 50 GHz to 106 GHz output frequencies

Output power: -5 – -8 dBm
DC offset and delay feedback loops suppress spurious harmonics

THz transistors enable digital logic can operate at > 100 GHz

We thank Teledyne Scientific & Imaging for IC fabrication

Thank you

UCSB
UNIVERSITY OF CALIFORNIA
SANTA BARBARA

TELEDYNE
SCIENTIFIC & IMAGING
Everywhereyoulook™

48TH EUROPEAN MICROWAVE CONFERENCE 2018
The 48th European Microwave Conference

EuMIC 2018
The 13th European Microwave Integrated Circuits Conference

EuRAD 2018
The 15th European Radar Conference