204GHz Stacked-Power Amplifiers Designed by a Novel Two-Port Technique

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***Abstract* —We report stacked mm-wave power amplifiers designed by a novel 2-port technique. Two power amplifiers designed into 130-nm InP HBT to verify the technique. The first design (unit cell) biased at 436mW Pdc produces 34.6mW saturated output power with 5.8% PAE at 204GHz. The amplifier has a 13.9dB peak small signal gain at 236GHz and 27 GHz 3-dB bandwidth. The chip size is 0.63mm×0.54mm including the pads. The second design combines two cells in parallel with an additional gain stage. The design consumes 1.18W Pdc and it shows a 63mW saturated output power with 4.8%PAE at 204GHz. The amplifier has a 22.7dB peak small signal gain at 230GHz and larger than 25GHz 3-dB bandwidth. The chip size is 0.7mm×1.3mm including the pads. The paper reports the first stacked power amplifier designed in a rigorous way at mm-wave frequencies.**

***Keywords* — stacked power amplifier, 2-port network, InP HBT, compact area.**

I. INTRODUCTION

Emerging mm-wave radar and wireless communications systems require efficient medium-power and high-power amplifiers. Such power amplifiers combine the output power of many individual transistor fingers, typically using corporate transmission-line combiners. The resulting combining losses limit the maximum feasible output power and reduce the power-added efficiency. Seeking reduced losses, several series power-combining techniques have been explored, including distributed active transformers [1], sub-quarter-wavelength baluns [2], and direct series transistor connection [3, 4, 5, 6]. Direct series connection is particularly attractive because, with only short line sections needed between transistors, die size is small and combining losses potentially very small.

The direct series connection design procedures described in [7] use equivalent-circuit analysis, and, like any such technique, must be re-derived if the device model is changed or if more complex interconnect parasitics are added. This is a difficulty at higher mm-wave frequencies, where even very short interconnects have substantial effect and for which robust IC design consequently requires electromagnetic simulation of all interconnects. Given complex device and interconnect models, 2-port design procedures are more flexible and more general.

Here we report two stacked power amplifiers, each implemented in a 130nm (1.1THz fmax) InP HBT technology [8], operating at 204GHz. The amplifiers were designed using a two-port synthesis procedure that computes the required transistor input, load, and common-lead impedances from the available input power and from the transistor two-port terminal voltages and currents required for efficient large-signal operation. A first PA (design 1) using 3:1 series connection, with one gain-matched and two power-matched transistors, produced 11.7 dB large signal gain and 15.1 dBm saturated output power at 204 GHz. A second PA (design 2) consists of two-unit cells, with input and output 2:1 transmission-line power-combiners, plus a pre-driver stage. This design produced 16.5 dB large signal gain and 18 dBm output power at 204 GHz.

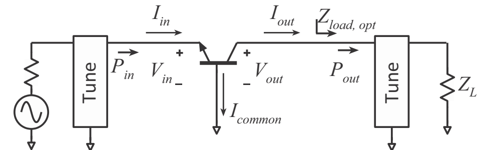

Fig. 1. Common-base transistor operating at saturation with input and output voltages, currents, and powers, V_{in}, V_{out}, I_{in}, I_{out} P_{in}, and P_{out}.

II. TWO-PORT SYNTHESIS

For high efficiency in a series-connected amplifier, given an input power which drives the amplifier output to the onset of clipping, each transistor cell within the stack must operate with its maximum (clipping) AC collector-emitter voltage V_{ce}, its maximum (clipping) AC collector-current I_c, and with the correct phase relationship between them. Stated colloquially, each transistor must be presented with the correct large-signal load impedance, and, as the input power is increased, each transistor must reach its voltage and current clipping limits simultaneously. Given significant transistor and interconnect parasitics, impedance compensation or tuning is necessary.

We develop the design procedure to obtain this. We first simulate a common-base transistor operating large-signal (Fig. 1) with its optimum large-signal load impedance $Z_{load,opt}$. The absolute AC magnitudes and phases of the input and output voltages and currents V_{in}, V_{out}, I_{in}, and I_{out} are recorded, as is the real added power $P_{added} = real\ (P_{out} - P_{in})$.

Fig. 2. shows a 3:1 series-connected power amplifier. To ensure that each device reaches its voltage and current clipping limits simultaneously, the amplifier provides interstage tuning networks plus common-lead impedances for the common-base stages. The common-emitter stage Q_1 provides its *common-emitter* saturated output power and must be provided with *common-emitter* optimum large-signal load impedance Z_{load1}.

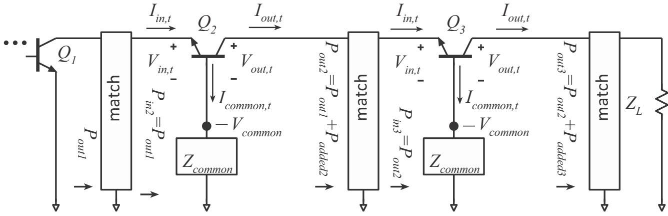

Fig. 2. Three-element series-connected power amplifier. Common-lead impedances Z_{common} and interstage tuning networks ensure that each device reaches its voltage and current clipping limits simultaneously.

Transistor Q_2 must operate with voltages and currents V_{in2}, V_{out2}, I_{in2}, I_{out2} and $I_{common2}$, differing only by a constant phase factor $\exp(j\phi_2)$ from the voltages and currents V_{in}, V_{out}, I_{in}, I_{out} and I_{common} of the common-base power amplifier of Fig. 1. The output power of Q_2 would then be $P_{out2} = P_{added} + P_{out1}$. Similarly, transistor Q_3 must operate with voltages and currents V_{in3}, V_{out3}, I_{in3}, I_{out3} and $I_{common3}$, differing only by a constant phase factor $\exp(j\phi_3)$ from V_{in}, V_{out}, I_{in}, I_{out} and I_{common}. The output power of Q_3 would then be $P_{out3} = P_{added} + P_{out2}$. Z_{common} must be lossless, i.e. pure imaginary.

Generalizing to a N-element design, the required common-lead impedance of the nth cell is

$$Z_{common(n)} = 2j(n-1)P_{added}/(X_1 X_2 \sin(Y_2 - Y_1)), \quad (1)$$

the required load impedance of the nth cell is

$$Z_{L(n)} = (V_{out} + Z_{common(n)}(I_{in} - I_{out}))/I_{out}, \quad (2)$$

and the input impedance of the nth cell is

$$Z_{in(n)} = (V_{in} + Z_{common(n)}(I_{in} - I_{out}))/I_{in}, \quad (3)$$

where X_1 is the magnitude of I_{in}, X_2 is the magnitude of I_{out}, Y_1 is the angle of I_{in} in radians, and Y_2 is the angle of I_{out} in radians. Given that the common-lead, input and required load impedances are now known for all cells, we can design tuning networks to match between stages, i.e. between $Z_{in(n)}$ and $Z_{L(n-1)}$. Although in principal $Z_{common(n)}$ could be inductive or capacitive, typical numbers in the design showed that $Z_{common(n)}$ is capacitive which matches the previous work done by circuit analysis [7]

III. Experimental Designs

To demonstrate this synthesize procedure, PAs were designed at 204GHz in a 130nm InP HBT technology [8]. This has a 1.1 THz power-gain cutoff frequency (f_{max}), a 3.5 V breakdown, and a maximum ~3 mA current per μm emitter finger length. The Au interconnect stack has three layers, with 1 μm BCB (ε_r=3.8) between metal 1 and metal 2, and 5 μm BCB between metal 2 and metal 3. There are 0.3fF/μm^2 MIM capacitors and 50 Ω /square thin-film resistors. High-performance 220GHz [8] PAs, using corporate combiners, have been reported in 130nm and 250nm InP HBT technology.

Fig. 3a show a schematic of a 204 GHz design (Design 1) using a 3: 1 stack. In this design, all the transistors ($Q_1, Q_2, and\ Q_3$) are divided into two clusters each is 4 fingers with 5 μm emitter length. This will simplify the matching circuits and ballast resistors could be added to each cluster or less to prevent thermal stability problem. The input transistor is tuned for maximum gain, and the upper two transistors are tuned for maximum saturated output power. From the transistor

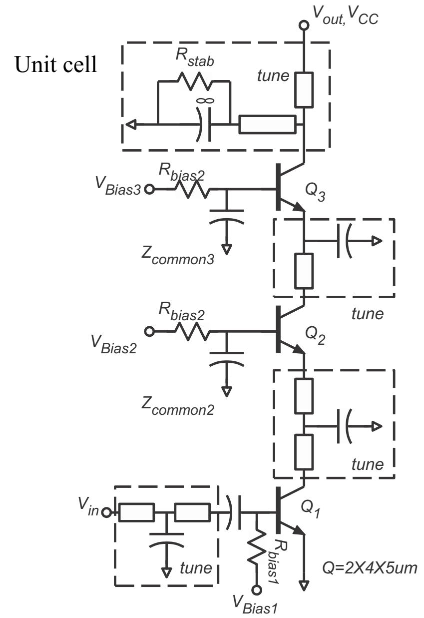

Fig. 3. Simplified schematic diagrams of a 204GHz, 3:1 series connected stack with gain-matching on Q_1 and power-matching on Q_2 and Q_3.

design kit model, a large signal CB load pull simulation (Fig. 1) was first performed to determine the required transistor terminal voltages and currents under efficient large-signal operation. The input, load, and common-lead impedances Z_{in}, Z_L, and Z_{common}, were computed from (1,2,3), and, from these, the interstage tuning networks designs. The interstage matching circuits are designed by series TL's and shunt MIM caps. The output matching circuit is achieved by a shunt TL and series TL. Small value resistors are usually added in series with the bypass caps to avoid out-of-band instability. However, this resistance will degrade the output power significantly. In this design, a large resistance (R_{stab}) is added in parallel to the bypass cap. At lower frequencies, the resistance damps any out-of-band instability. However, the impedance of the cap dominates at the operating frequencies and the effect of the stability resistance is negligible on the output power. Unfortunately, this resistance draws a lot of DC power consumption lowering the PAE but without any impact on the output power.

Design 2 (schematic not shown) uses a transmission-line network to combine two cells of the 204 GHz Design-1 stages into a higher-power amplifier. Design 2 also includes one more cell acting as a driver stage. Therefore, less than 10mW is required to drive the amplifier into saturation. Wiggling in the routing between the driver and the amplifier stage is done for a compact area design.

IV. Results

Fig. 4 shows IC photographs. S parameters were measured using an HP vector network analyzer with Oleson 220-325GHz

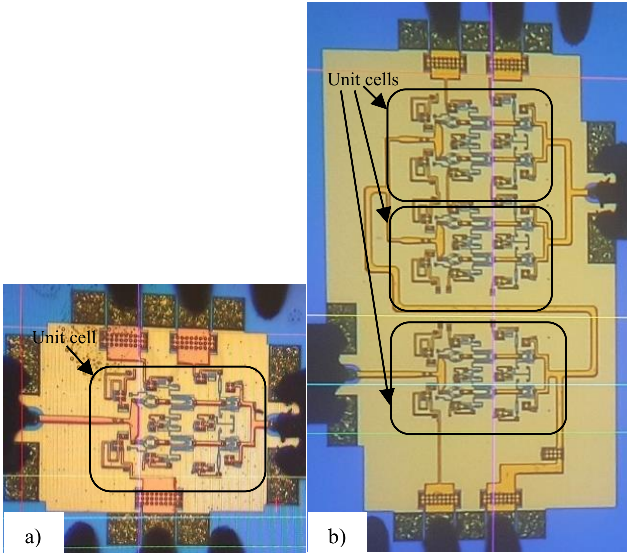

Fig. 4. (a) Die photo of design 1, and (b) Design 2, with 2:1 transmission-line combining. The die areas are 0.63 mm × 0.54 mm, and 0.7 mm × 1.3 mm respectively.

frequency extenders and GGB wafer probes. Calibration used LRRM standards on an external substrate. Fig. 5 shows measured S-parameters of the two designs. Design 1 shows 13.9 dB peak gain at 236 GHz and the 3-dB BW extends from 220GHz up to 247GHz. S11 is better than -10dB across the whole band. S22 is better than 6dB from 220GHz up to 240GHz. The reverse isolation (S12) is better than -34dB across the whole band. It is noted that the small signal gains of the measured designs are higher than the simulation. It means that the common lead impedances (Z_{common}) have more parasitic capacitances after the fabrication. This can be justified by the limited accuracy of the EM simulation or the transistor model miss some parasitic inductance. Stacked transistors with parasitic capacitances at their bases show higher small signal gain on the expense of the maximum saturated power. Design 2 has a 22.7 dB peak gain at 230 GHz and the 3-dB BW extends from below 220GHz up to 245GHz. S11 is better than -10dB across the whole band. S22 is better than -6dB below 236GHz. The reverse isolation (S12) is better than -42dB while the simulated one (not shown) is better than -85dB. The reverse isolation is critical in high gain amplifiers to avoid stability problems.

Large signal PA saturation characteristics were measured on-wafer using VDI ~204GHz frequency multipliers, driven by microwave synthesizers, GGB 220-330GHz probes, and an Erikson THz power meter. For the 204GHz measurements, the probe losses were determined by a probe-probe through measurement.

Power testing bias conditions for Design 1, were V_{CC}=5.9 V, V_{bias3}=4.9 V, and V_{bias2}=2.5 V. The collector current is 65mA where the total IC current (including the base currents) is 74 mA. For Design 2, V_{CC}=5.9 V, V_{bias3}=4.9 V, and V_{bias2}=2.5 V and the total collector for single cell is 61mA. The total IC current is 210mA for the three cells where two of them are connected in parallel and another one acts as a pre-driver stage.

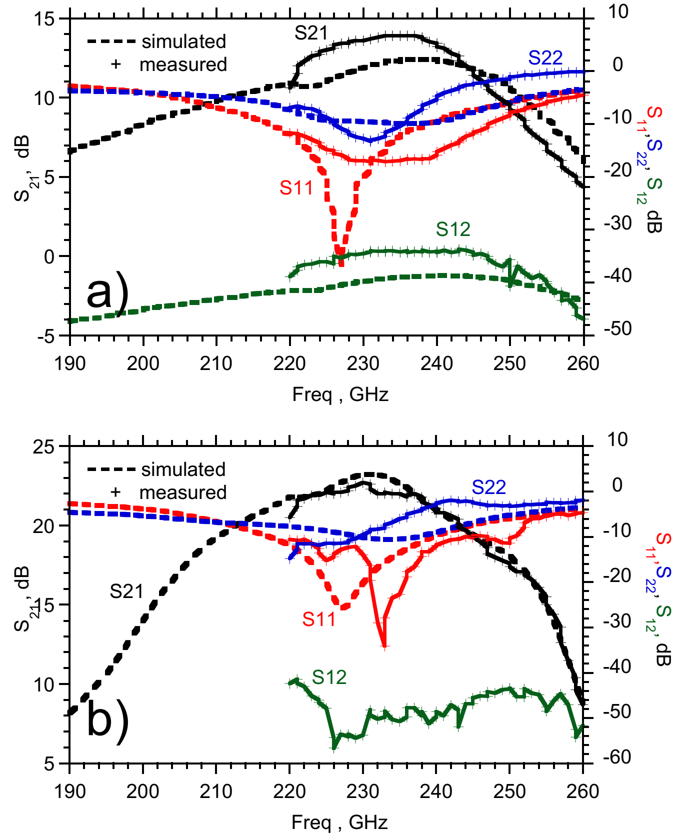

Fig. 5: Measured and simulated S-parameters of (a) Design 1, and (b) Design 2.

Fig. 6 shows the P_{in}-P_{out} characteristics of the two designs. For Design 1, at 204GHz, the saturated output power is 15.1 dBm, less than 1 dB below simulation. The DC currents are monitored at each sweep point to report any DC power increase due to the RF input power signal. However, it is noted that there is less than 1% increase in the DC power. The amplifier has a peak PAE of 5.8% at 15.1dBm and 5.8dB compressed gain.

For Design 2, the saturated output power is 18 dBm at 9.7dB compressed gain, and it matches the simulation well (less than 1dB difference). The DC currents are also recorded at each sweep point with less than 1% variations. The amplifier shows a 4.8% maximum PAE. The DC power of the driver is included in PAE calculations.

V. Conclusions

Medium and high-power PAs are key to emerging mm-wave systems. Efficient power combing techniques are required. The paper presented a rigorous way to design stacked power amplifier by 2-port techniques and it is working efficiently even at high mm-wave and sub-mm-wave frequencies. Table 1 shows a comparison between the state-of-the amplifiers. The stacked power amplifiers presented in the paper demonstrate compact area designs with high output power.

Table 1. Comparison between stat-of-the-art designs

Freq, GHz	Technology	S21, dB	P_{DC} mW	P_{out}, mW	PAE %	Dimensions, mm×mm	Ref
210	40nm CMOS	19.4	110	9.1	7.7	-	[10]
120	130nm SiGe BiCMOS	19	480	35.5	6.4	0.81×0.66	[11]
220	250nm InP HBT	26.8	3380	60		2.24×0.71	[12]
220	250nm InP HBT	14.8	4460	90	-	2.42×1.22	[13]
220	250nm InP HBT	10	-	48.8	-	0.7×0.65	[14]
190	250nm InP HBT	22.4	97	12.7	9.6	0.93×0.48	[15]
204	**130-nm InP HBT**	**11.7**	**436**	**34.6**	**5.8**	**0.63×0.54**	**This work**
204	**130-nm InP HBT**	**16.5**	**1180**	**63**	**4.8**	**0.7×1.3**	**This work**

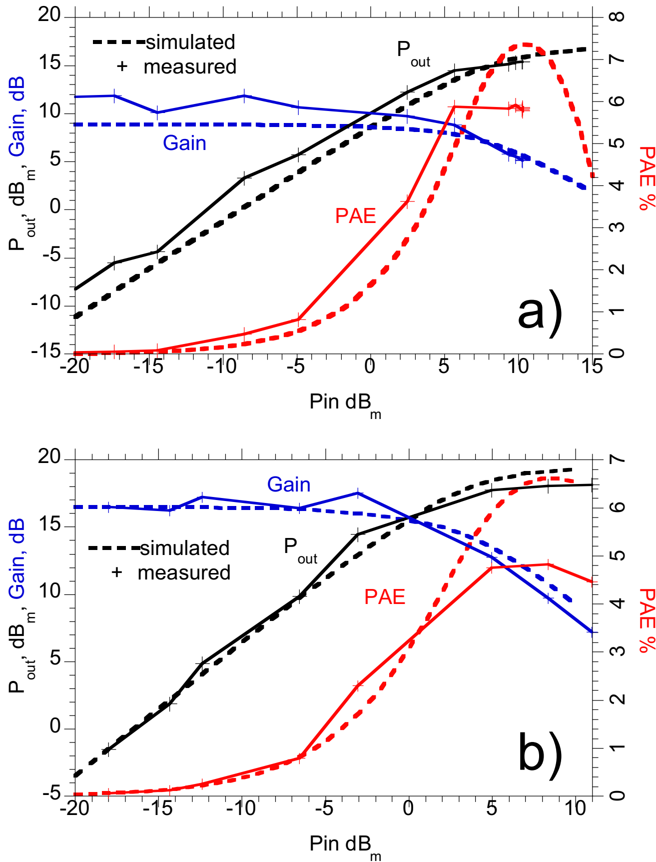

Fig. 6. Measured and simulated output power, PAE, and gain at 204GHz for a) Design 1and b) Design 2.

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