A High-Spurious-Harmonic-Rejection 32-53 GHz and 50-106 GHz Frequency Doublers using Digital Logic and DC Negative Feedback

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***Abstract* — We present two frequency doublers in 130 nm InP HBT technology. The doublers use digital logic and DC negative feedback to suppress unwanted harmonics. The single-ended output of the lower frequency doubler has -5 dBm output power over 32 GHz to 53 GHz output frequency range. First and third harmonic rejection is higher than 30 dBc. The delay control circuit with the feedback loop enables fourth harmonic rejection higher than 18 dBc. It consumes 0.94 W. The higher frequency doubler has -5 – -8 dBm single-ended output power over 50 to 106 GHz output frequency range with better than 25 dBc first harmonic rejection. It consumes 1.069 W.**

***Keywords* — frequency multiplier, frequency doubler, InP HBT, millimeter wave integrated circuits, MMICs.**

I. Introduction

Millimeter-wave systems are approaching widespread deployment in military systems and in mobile wireless. These require many low-phase-noise mm-wave local oscillators (LOs), particularly for systems using high-density constellations such as 64QAM. On-chip synthesizers are frequently used to generate LOs, but these can add considerable phase noise because low quality-factor (Q) passive devices and varactors at mm-wave frequency. The combination of a VCO with a frequency multiplier can enable the low-frequency VCO to work at mm-wave frequencies with low phase noise and wide tuning range. Frequency multipliers can be designed with little phase noise. As with a synthesizer within its PLL bandwidth, an ideal frequency multiplier increases phase noise by $20\log(N)$ compared with the input, where N is the multiplication ratio. However, frequency multipliers can generate substantial spurious harmonics. The harmonics will be closely spaced if N is large, as in a multiplier chain. These harmonics will generate out-of-band interference. In waveguide multipliers, spurious harmonics are readily suppressed by high-Q filters but, on ICs, filters consume large die area and have poor out-of-band rejection due to low passive element Q. In advanced near-THz SiGe and InP IC technologies, passive elements and filters remain poor but digital logic can operate well even at > 100 GHz [1, 2].

Here we report (Fig. 1) a broadband frequency multiplier architecture using digital logic and DC negative feedback. The architecture greatly suppresses spurious harmonics, hence little or no output filtering is required. The IC area is small. The doubler has first and third harmonic rejection better than 30 dBc and fourth harmonic rejection better than 18 dBc with 32 GHz to 53 GHz output frequency. The technique can be extended to at least 100 GHz output frequency.

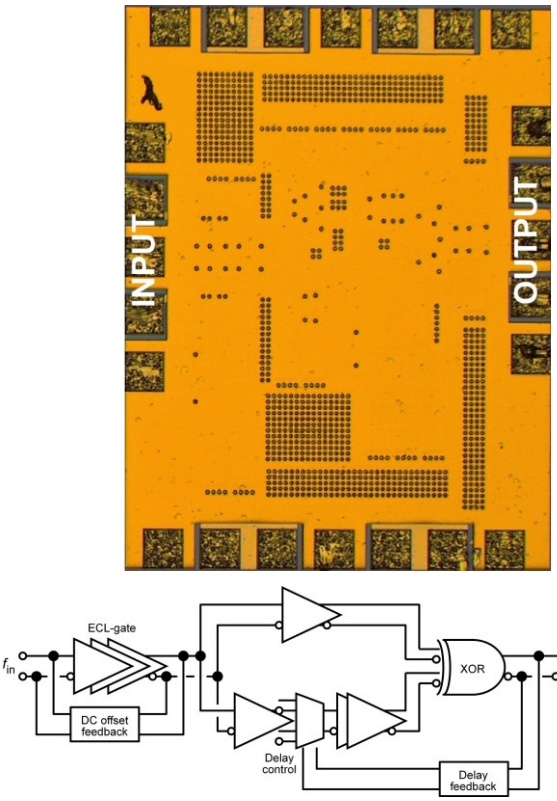

Fig. 1. Frequency doubler: chip photograph (top) and block diagram (bottom). Chip size: 750 × 990 um^2

II. InP HBT Technology

The ICs were designed into a 130 nm InP HBT process. The process provides 50 Ω/square thin film resistors, 0.3 fF/μm^2 MIM capacitors, and three-levels of gold interconnections (M1-M3). A 0.13 × 2 μm^2 HBT exhibits a current gain cut-off frequency f_τ = 520 GHz and a maximum

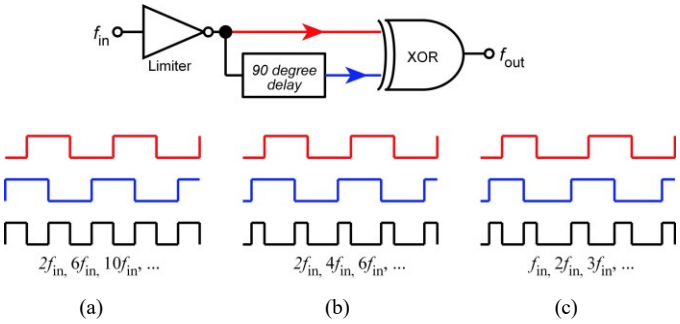

Fig. 2. Output harmonics of the doubler: (a) correct operation, (b) incorrect delay and (c) DC offset in the limiter.

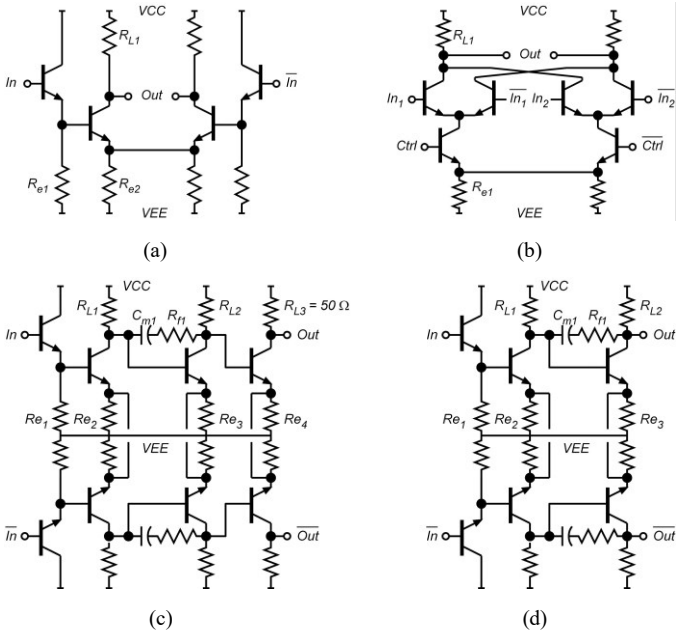

Fig. 3. Schematics of building blocks: (a) ECL-gate, (b) phase interpolator, (c) DC offset feedback and (d) delay feedback.

frequency oscillation f_{max} = 1.1 THz at I_C = 6.9 mA and V_{CE} = 1.6 V [3]. Low-loss normal and inverted microstrip lines are designed using M2 and M3 with a 5 μm thick BCB layer.

III. Doubler Design

A doubler consisting of a delay and an exclusive-OR (XOR) gate is sufficient to double the frequency of an input signal. Fig. 2 shows the origin of spurious harmonics. The doubler will have good harmonic rejection if the XOR gate is driven by a 50%-duty-cycle square-wave and if the delay is exactly 90 degrees. Given the wideband HBTs, the input ECL limiter converts even a 25GHz sinusoidal input into a square-wave output, but limiter DC offsets will cause the square-wave duty cycle to deviate from 50%, which generates limiter spurious outputs at DC, $2f_{in}$, $4f_{in}$, and above. Input to the XOR gate, the spurious DC, $2f_{in}$, $4f_{in}$,… inputs mix with the desired f_{in} input to produce spurious XOR outputs at f_{in} and $3f_{in}$. Similarly, if the delay differs from 90 degrees, the XOR output will have spurious outputs at DC, $4f_{in}$ and higher frequencies. Note that limiter DC offset produces a nonzero limiter DC output while an incorrect phase shifter delay

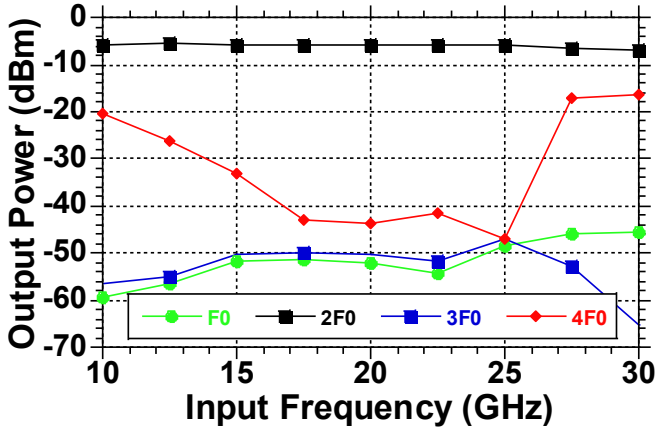

Fig. 4. Simulated output powers of harmonics.

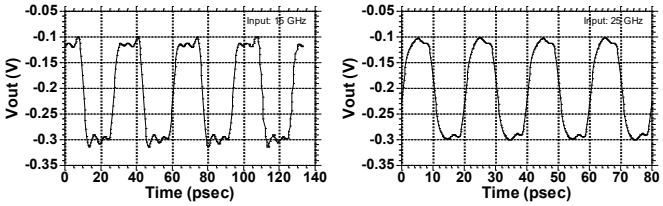

Fig. 5. Simulated waveforms at input frequencies: 15 GHz (left) and (b) 25 GHz (right).

produces a nonzero XOR gate DC output. We therefore sense these DC output voltages, and, with OP-amp negative feedback loops, use them to drive the limiter DC offset to zero and the phase-shifter to 90 degrees delay. These loops provide the doubler with excellent harmonic rejection over a broad bandwidth.

Fig. 1 shows the block diagram of the doubler. It consists of in/output buffer stages based on emitter-coupled logic (ECL) gates, the XOR gate, and the feedback-controlled delay circuit (Fig. 3). The doubler has differential in/output ports with 50 Ω thin film resistors. These resistors provide a broadband 50 Ω termination. The input buffer (Fig. 3a) with the DC offset feedback converts a sinusoidal input into a square-wave with 50%-duty-cycle. A single-ended sinusoidal input can therefore drive the multiplier. The output buffer provides constant output power over the wide tuning range. Both feedback loops have similar operation. The input buffer DC feedback circuit compares the DC levels of the limiter's non-inverting and inverting outputs. The input buffer DC feedback circuit (Fig. 3c) adjusts input DC voltages by controlling current flowing through R_{L3} (50 Ω) which is also the ECL-limiter's input termination resistor. The delay control loop (Fig. 3d) monitors the XOR gate DC output voltage, and, from this, adjusts the phase interpolator control voltage (Fig. 3b) until the XOR gate input signals have a 90-degree phase difference. Fourth harmonic rejection of the doubler is limited by the tuning range of the phase interpolator.

IV. Experimental Results

The ICs were characterized on-wafer. Fig. 1 shows a chip micro-photograph of the doubler with 32 GHz to 53 GHz

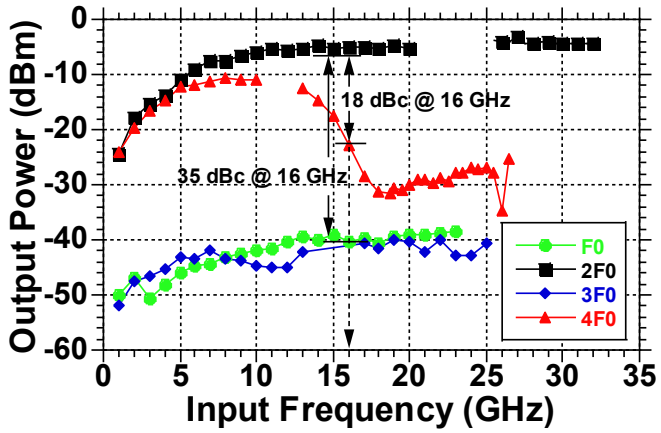

Fig. 6. Measured output powers of harmonics.

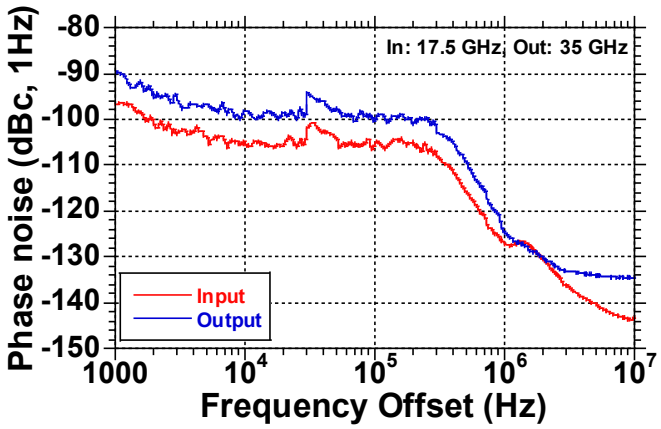

Fig. 7. Measured phase noise at 17.5 GHz input and 35 GHz output frequencies.

output frequency; the chip size is 750 × 990 um^2 including pads. The doubler with 50 GHz to 106 GHz has the same topology and chip size except different bias conditions and delay tunning range.

The doublers have differential outputs but only a single-ended output was measured. Power measurements were conducted with a Rohde & Schwarz FSU spectrum analyzer at low frequencies (< 46 GHz), an OML harmonic mixer (M15HWD, 50 – 75 GHz) and a Quinstar double balanced mixer (QMB, 75 – 110 GHz). Losses of cables and probes were de-embedded.

Fig. 4 and Fig. 5 show simulated harmonic output powers and voltage waveforms of the 32-53 GHz doubler. In simulations, within the delay control tuning range, the doubler has high harmonic rejection and 50% output duty-cycle. Fig. 6 shows measured output powers of the harmonics. The second harmonic has output power -5 – -8 dBm over a range of input frequencies. The output power corresponds to digital logic level in the design. The first and third harmonics rejection is better than 30 dBc. Fourth harmonic rejection is higher than 18 dBc within the delay tuning range from 16 GHz to 26.5 GHz. Doubler performance is insensitive to the input power, showing similar harmonic rejection with the input power from -3 to 3 dBm. The doubler consumes 284 mA from a -3.3 V

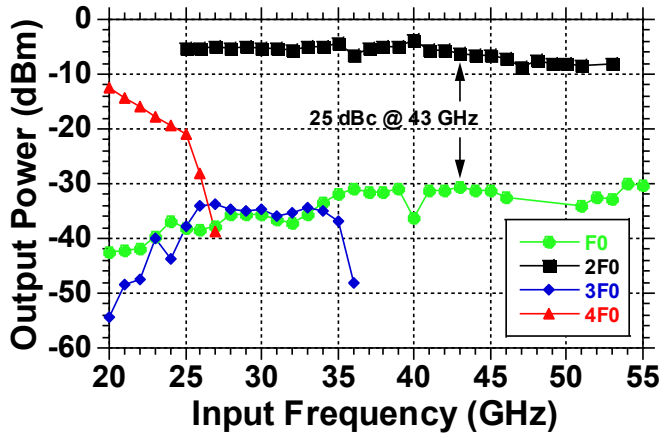

Fig. 8. Measured harmonic output powers of the doubler with 60 GHz to 100 GHz frequency.

supply. Fig. 6 shows the doubler can work at input frequencies higher than 26.5 GHz; harmonic rejection at such input frequencies was not tested because of the available test equipment. Fig. 7 shows measured phase noise of in/output signals. The spectrum analyzer's built-in function is used for phase noise measurements, and an Anritsu signal generator (MG3694C, < 40 GHz) is used for the input source. The multiplier adds about 6 - 7 dB, within experimental precision of the 20 log(N) increase of an ideal multiplier. This indicates that the DC feedback loops do not contribute significant added phase noise.

Measured harmonic output powers of the 50-106 GHz doubler are shown in Fig 8. It shows limited results at high frequency due to the available test equipment, but the doubler has similar behaviour as the lower frequency doubler. The second harmonic has output power -5 – -8 dBm and the first harmonic rejection is better than 25 dBc. It consumes 324 mA from a -3.3 V supply.

Table I summarizes the performance of the proposed frequency doubler and compares it with the previously reported doublers.

V. Conclusion

We presented broadband frequency doublers with 32 GHz to 53 GHz and 50 GHz to 106 GHz output frequencies with low phase noise, and excellent suppression of spurious harmonics. These frequency doublers offer greatly flexibility in designing frequency multiplier chains because strong spurious harmonic rejection enables a significantly relaxed filter requirement. This is particularly important in monolithic designs, as on-wafer filters are large and have poor out-of-band rejection.

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Table 1. Performance of the proposed and previously reported frequency doublers.

Ref.	Technology	Topology Input Output	Output BW (GHz)	Input Power (dBm)	Output Power (dBm)	Pdc (mW) @ V_{DC}	Fundamental Suppression (dB)	4th order Suppression (dB)	Area (mm^2)
[4]	0.18 um SiGe BiCMOS	Differential Differential	36 – 80	-7 @ 66 GHz 1 @ 80 GHz	1.7 @ 66 GHz -3.9 @ 80 GHz	137 @ 3.3	20 - 36	N/A	0.27
[5]	90 nm CMOS	Single Single	42 – 90	5	-6 – -3	20 @ 1	20 – 48	> 14	0.33
[6]	0.2 um InP DHBT	Differential Single	DC – 100	-5 @ 60 GHz	-10 @ 60 GHz	730 @ -4.5	24 – 32	N/A	2.24
[7]	0.13 um SiGe BiCMOS	Single Single	27 – 41	-15.5	1.3 – 4.3	17-22 @ 2	25.7 – 33	N/A	0.34
This work	0.13 um InP DHBT	Diff./Single Differential	32 – 53*	-3#	-5#	937 @ -3.3	35	> 18	0.74
This work	0.13 um InP DHBT	Diff./Single Differential	50 – 106*	-3#	-5 – -8#	1069 @ 3.3	25	> 15	0.74

* The doubler can work at higher input frequencies; harmonic rejection at such input frequencies was not tested because of the available test equipment.
#Single-ended measurement results.

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