A Dual-Conversion Front-End with a W-Band First Intermediate Frequency for 1-30 GHz Reconfigurable Transceivers

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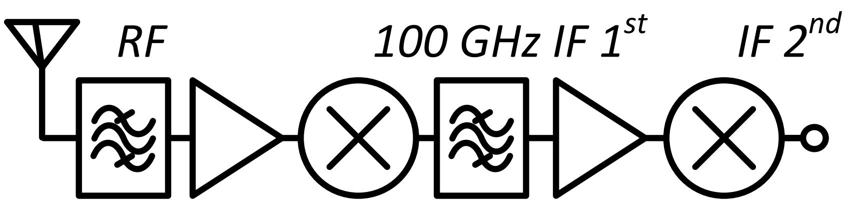
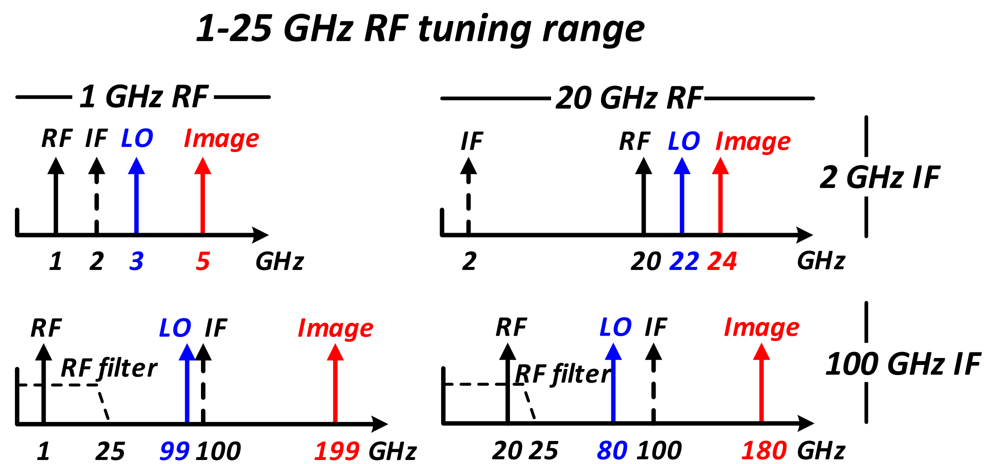
Outline

- Motivation
- Technology
- System Implementation
- Summary of the main IC blocks
  - High Dynamic Range Diode Mixer
  - Frequency Doublers (30-50 GHz, and 60-100 GHz)
  - x4 LO Multiplier Chain
- System Experiments

Dual-Conversion Receiver





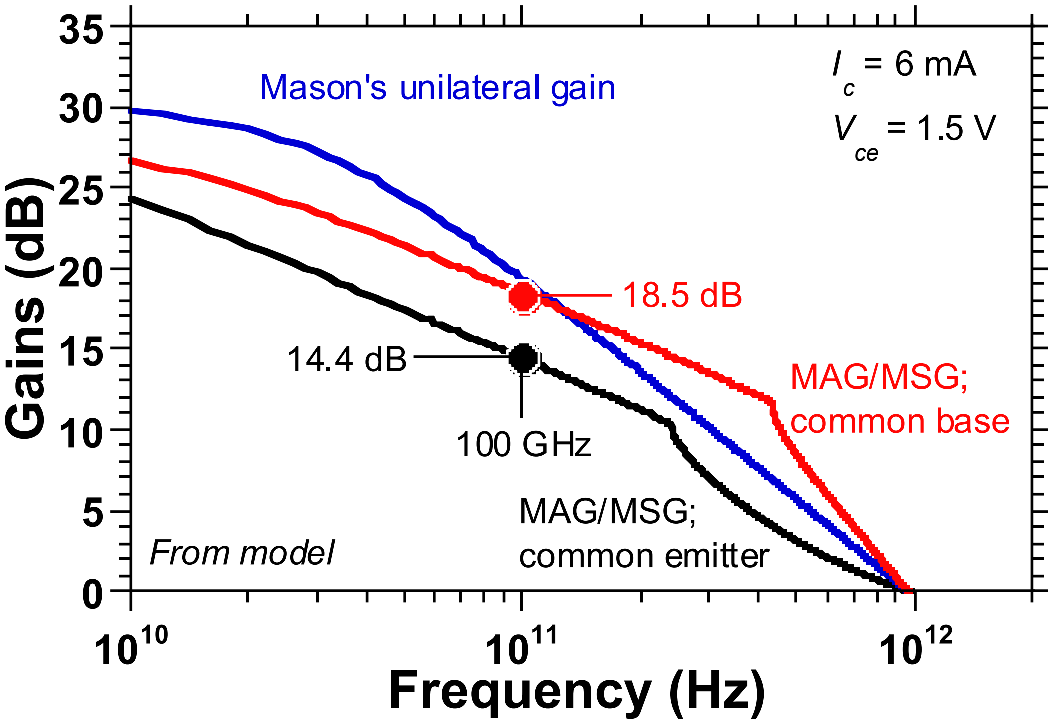
Classical RF architecture: extend to micro/mm-wave frequencies

- Up-convert to 1st IF (100 GHz), down-convert to 2nd IF (or baseband)
- Image response moved out-of-band
- Very wide tuning range, no image response.

Applications:

- Instrumentation
- Wideband surveillance: 1-25 GHz (possibly 1-50 GHz)
- Single IC serving many applications: application-specific LNA + common module

THz HBTs



Teledyne 130 nm InP HBT

- 1.1 THz f_{max}.
- CE: 14.4 dB MSG @100 GHz
- CB: 18.5 dB MSG @100 GHz

Process offers:

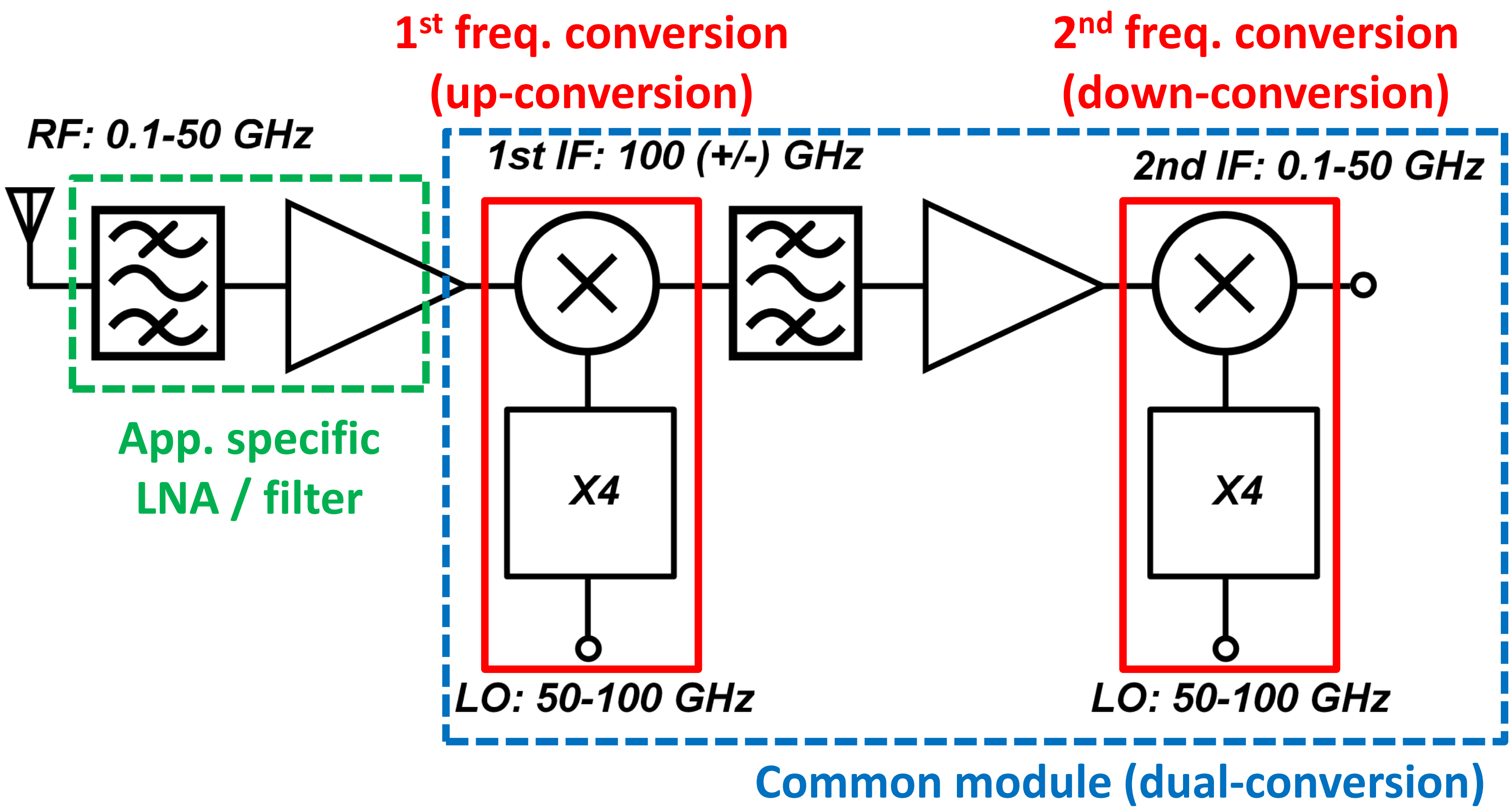
- 3 gold metal layers
- 50 Ohm/sq. thin film resistor
- 0.3 fF/um^2 MIM capacitors

Dual conversion at microwave:

- 100 GHz 1st IF would enable over 1-50 GHz spur-free tuning
- High speed IC technologies: 100 GHz IF feasible

THz transistors enable microwave dual-conversion receivers

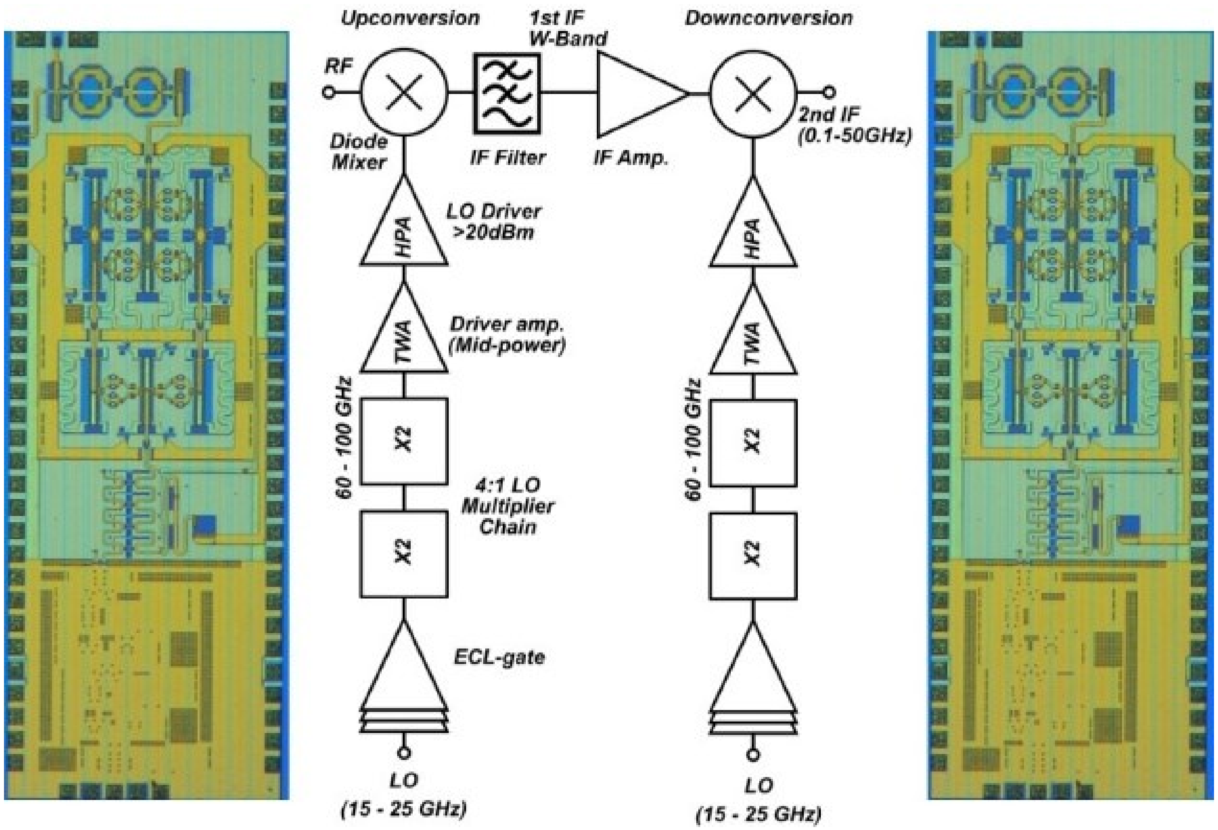
System Block Diagram – Dual Conversion



Need high dynamic range & wide tuning range

Spurious free multiplier chain & high dynamic range mixer

System Implementation – Dual Conversion



Up/down conversion ICs are same

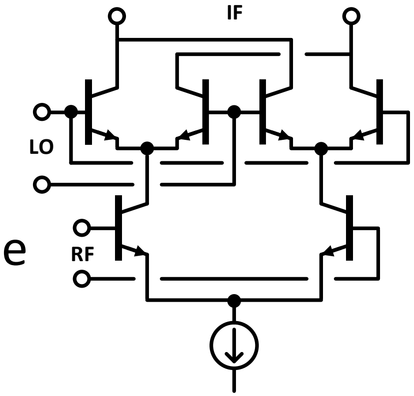
Used back to back to realize the proposed dual conversion receiver

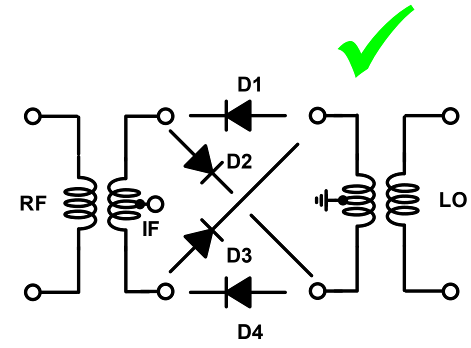
1st IF at W-band 94 GHz or 100 GHz (+/-)

High Dynamic Range Mixer

Transistor mixer:
Low IP3
High noise figure
Poor dynamic range

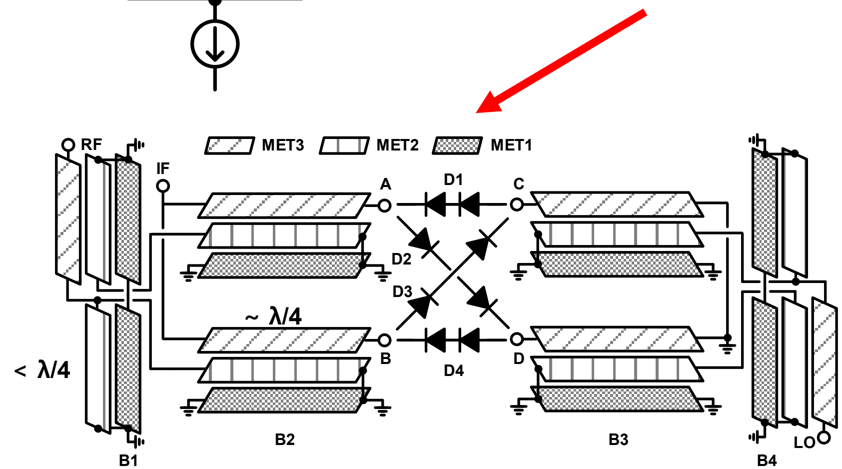
Diode mixer:
High IP3
Lower noise figure
Higher dynamic range





Design challenges:
High speed diode
Wide bandwidth balun
Wide tuning range + high power LO

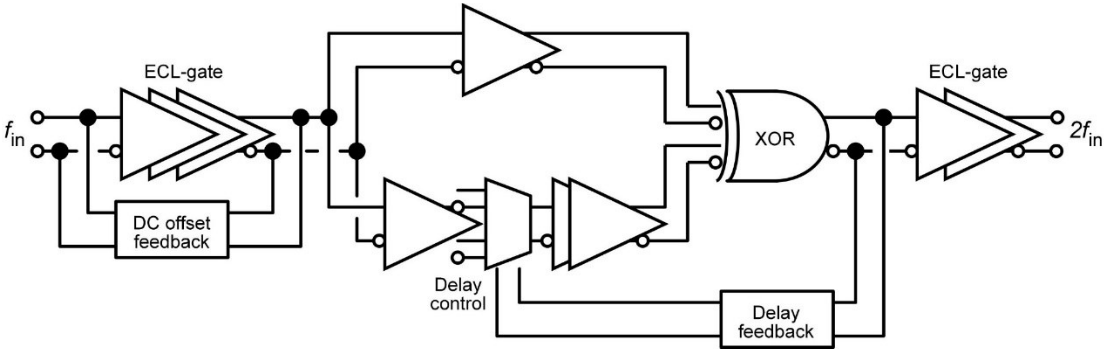
InP HBT offers high speed DHBT BC diode
(Schottky-like high-frequency characteristics)

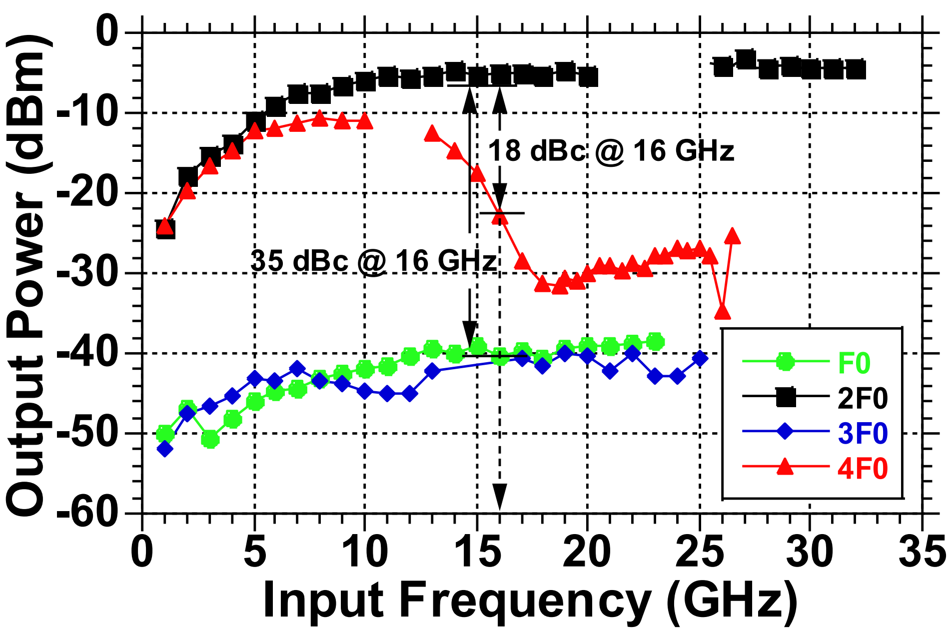


S.K.Kim et al, CSICS 2016

Four series-connected BC diode pairs
RF and LO baluns
Balun loss < 4 dB over W-band

1st Frequency Doubler (30-50 GHz)





<u>Uses digital logic</u>

<u>DC offset feedback</u>

Minimize dc offset of the ECL limiter output

<u>Delay feedback</u>

The phase shifter (delay circuit) to 90 degree delay

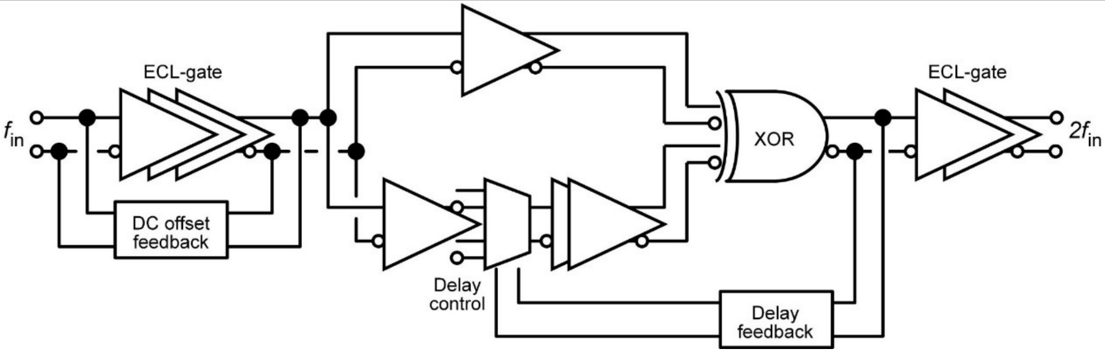
→ ***Suppress spurious harmonics***

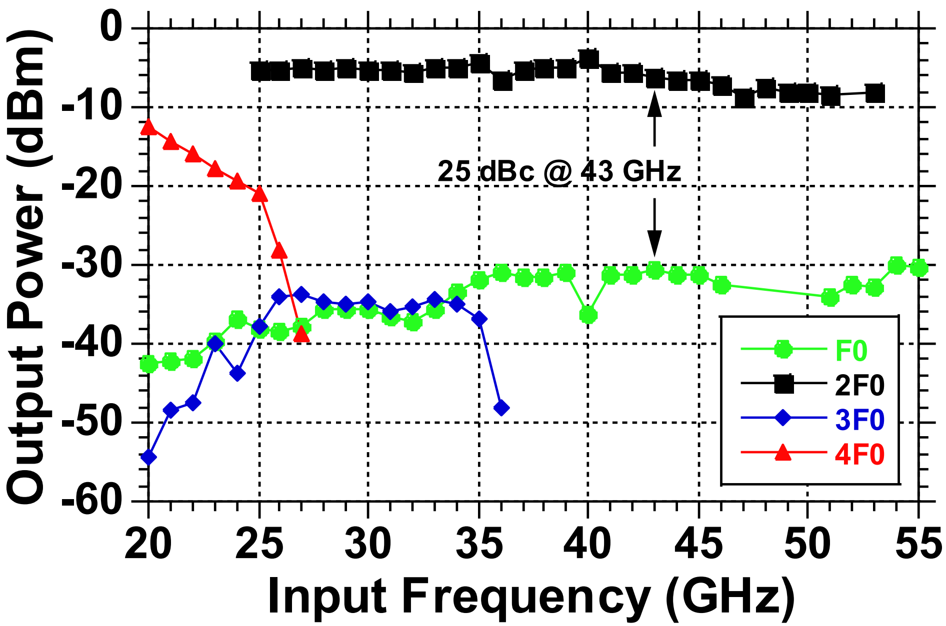
S.K.Kim et al, EuMW 2018

1st & 3rd harmonics rejection > 30 dBc.

4th harmonic rejection > 18 dBc within the delay tuning range

2nd Frequency Doubler (60-100 GHz)





Uses digital logic

DC offset feedback

Minimize dc offset of the ECL limiter output

Delay feedback

The phase shifter (delay circuit) to 90 degree delay

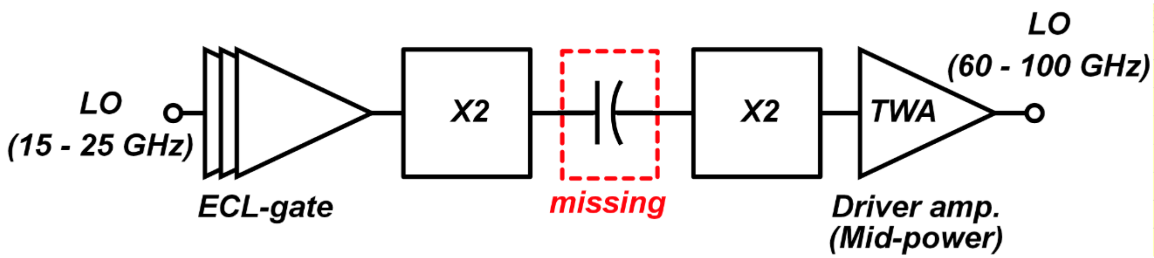
→ ***Suppress spurious harmonics***

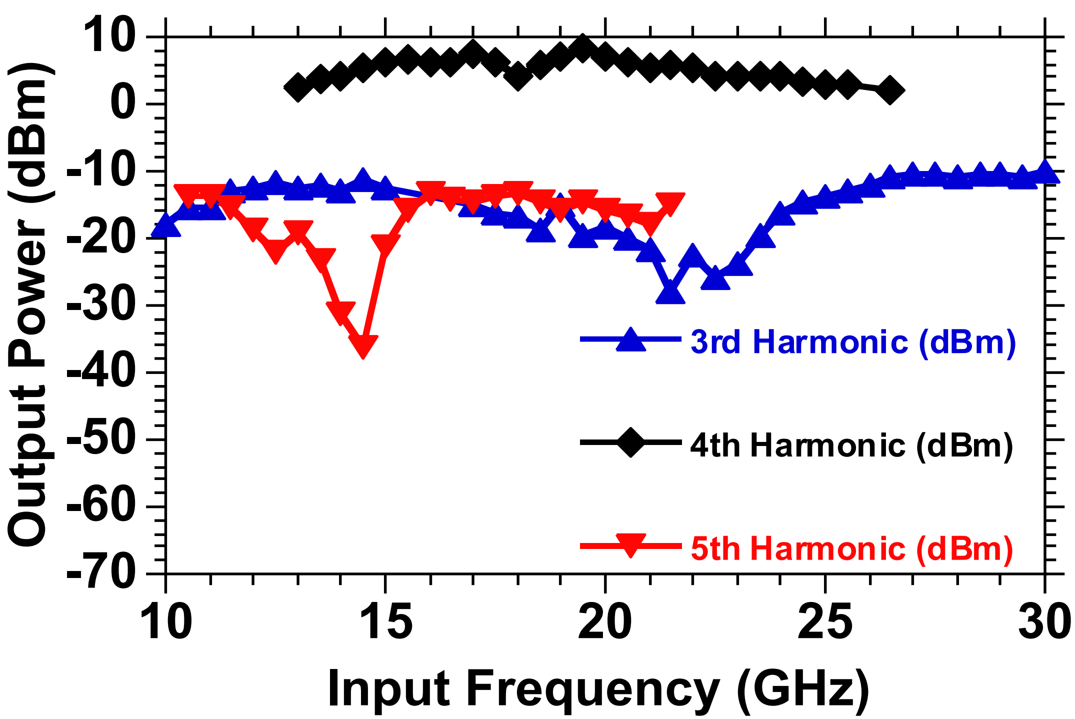
S.K.Kim et al, EuMW 2018

1st & 3rd harmonics rejection > 25 dBc.

4th harmonic rejection: similar behaviour, equipment limitation

x4 LO Multiplier Chain





x4 multiplier chain from two consecutive doublers

Problem: missing DC blocking cap between doublers

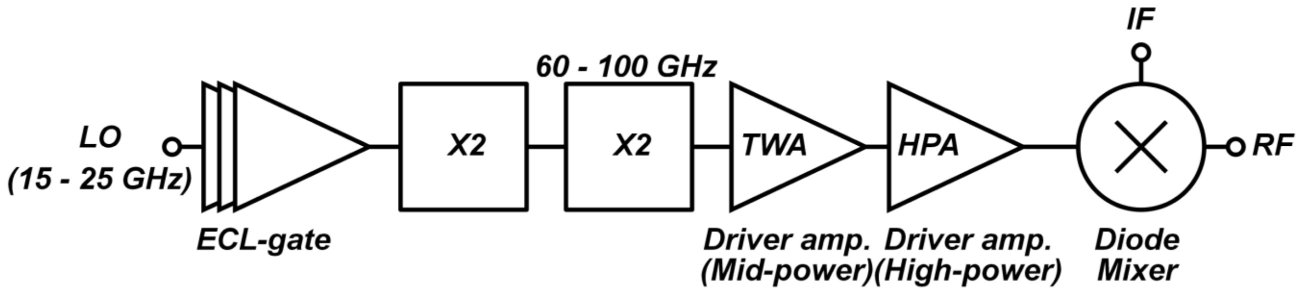
DC offset feedback affected

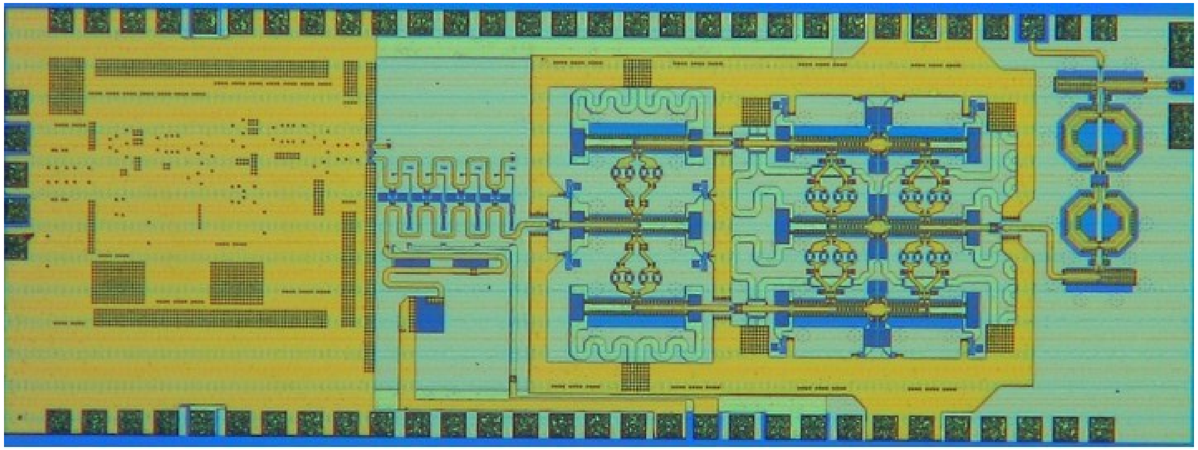
Travelling wave amplifier as driver with ~ 7-9 dBm Pout

3rd, and 5th harmonic rejection > 20 dBc

system performance degradation due to the multiplier harmonic rejection

Frequency Conversion IC





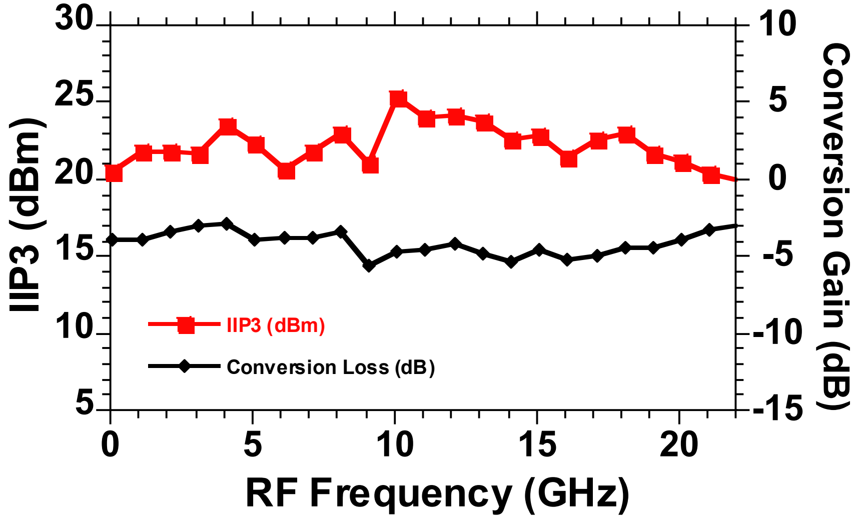
Integrated frequency conversion IC: Diode mixer, High power LO driver, x4 multiplier chain

Total power consumption: ~ 2.8 W - Multiplier chain and LO driver

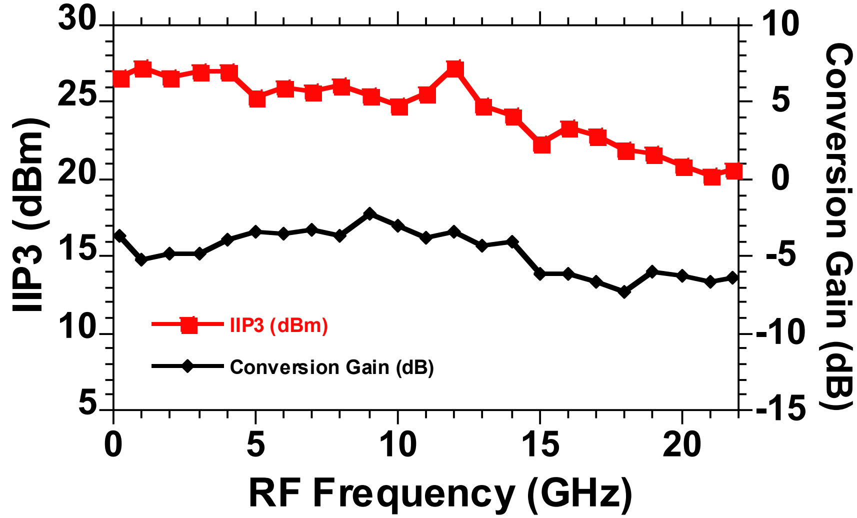
Size: 3.3 mm x 1.18mm

Up/Down-Conversion Measurements

Down-conversion



Up-conversion



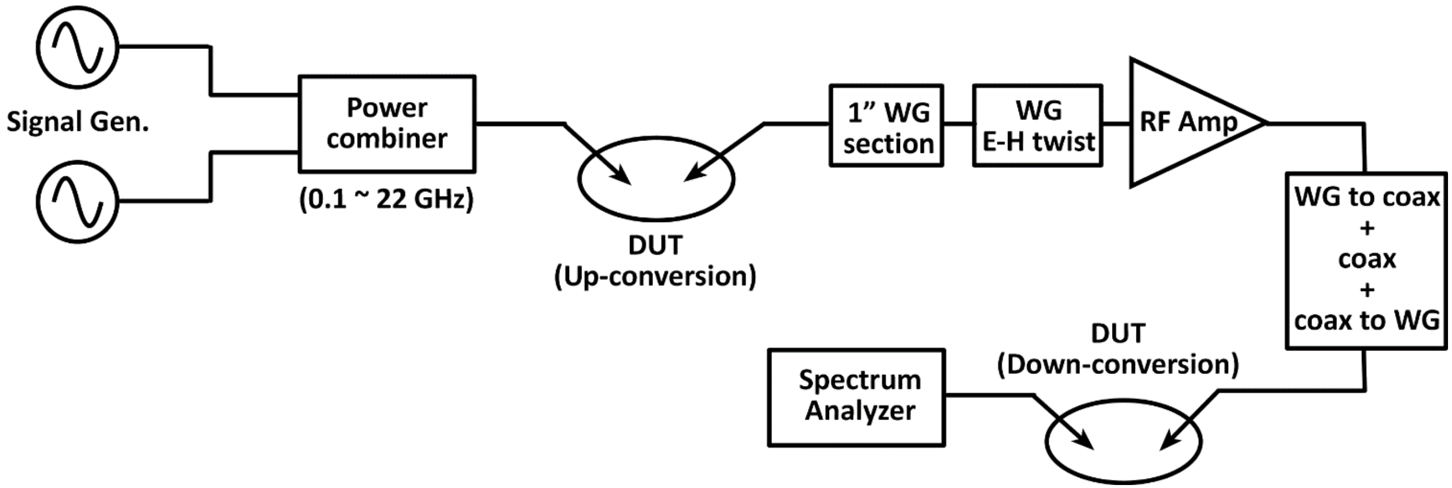
Down-conversion:

>20 dBm IIP3 and >-6 dB conversion loss

Up-conversion:

>20 dBm IIP3 and >-7 dB conversion loss

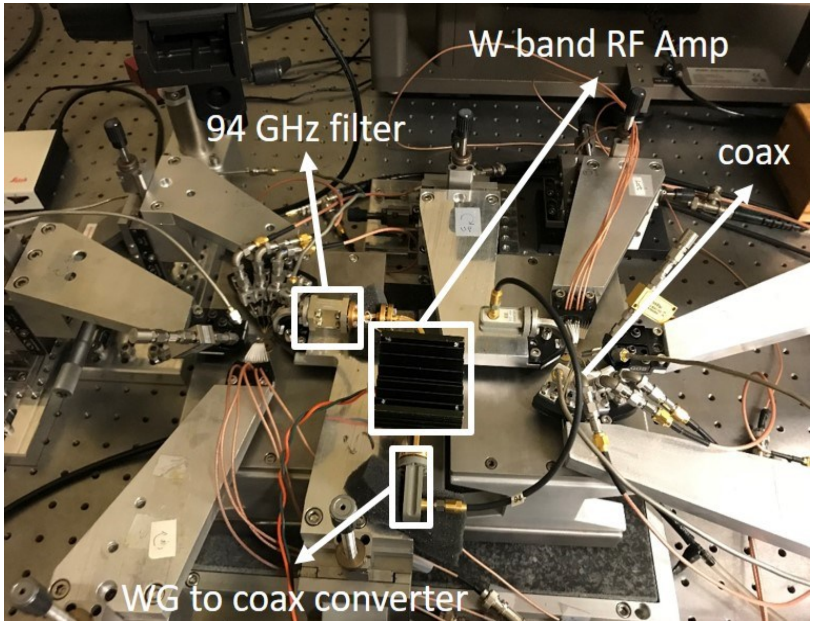
System Measurements - Experiment



2 freq. conversion ICs are connected thru

- **waveguide components**
- **W-band band-pass filter**
- **W-band amplifier**

2 probe stations, 8 probe arms



System Measurements - Procedure

Off-wafer IF section uses

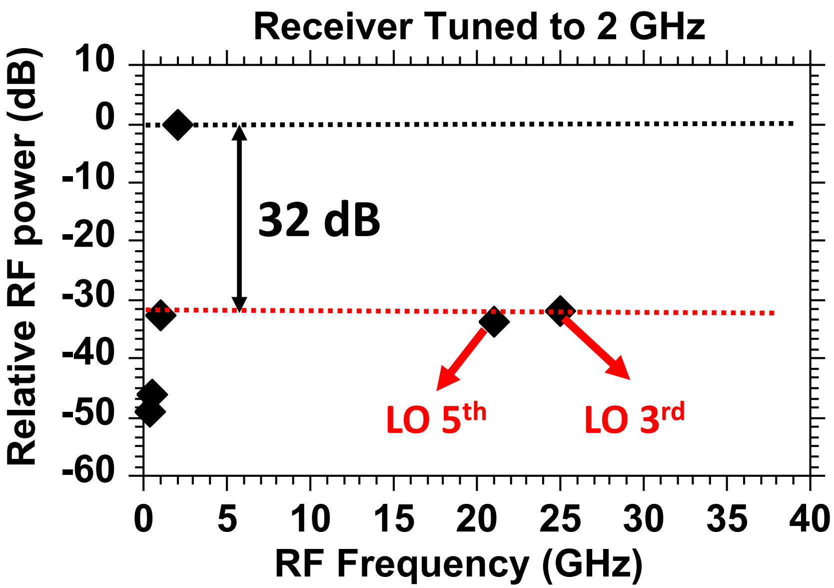
- 94 GHz Band-pass filter and
- commercial W-band amplifier

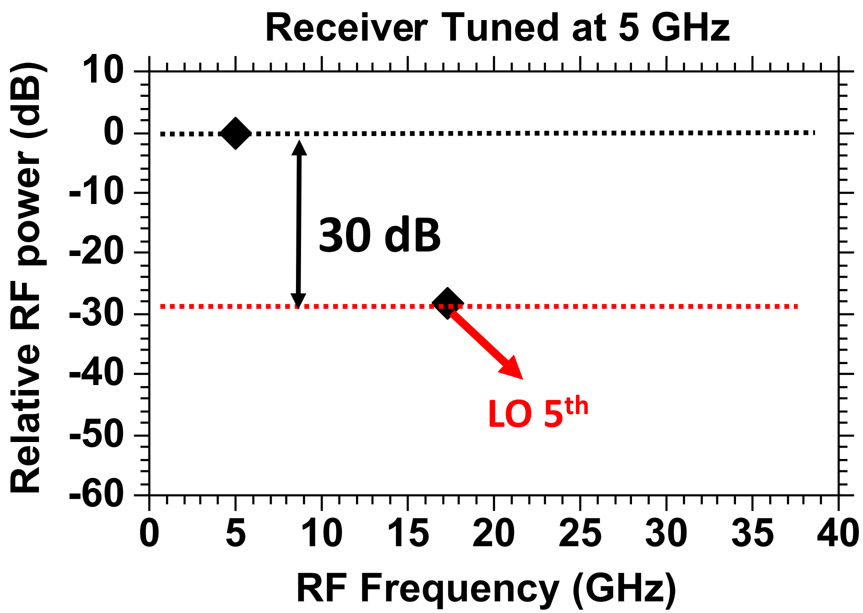
Available W-band amplifier had relatively high noise figure and low IIP3, total system NF and IIP3 limited by the off wafer IF amplifier and not reported here

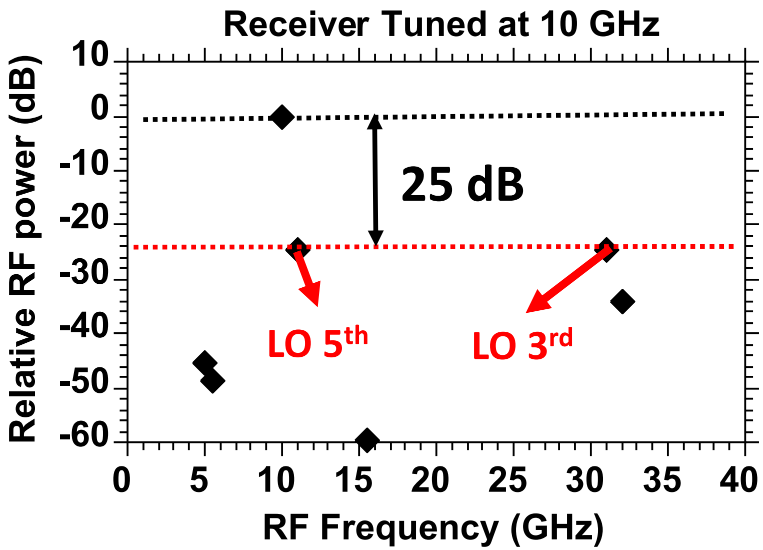
<u>Tuning range experiment:</u>

1. Receiver tuned at a particular desired RF frequency and LO held fixed
2. RF is swept over a targeted freq. range DC-40 GHz, while LO is fixed
3. Measurements performed at 2, 5, 10, 20 and 30 GHz RF freq.
4. Relative strength of the receiver spurious response measured as a function of input frequency.
5. Largest spurs come from LO 3rd and 5th harmonics.

System Measurements - Results





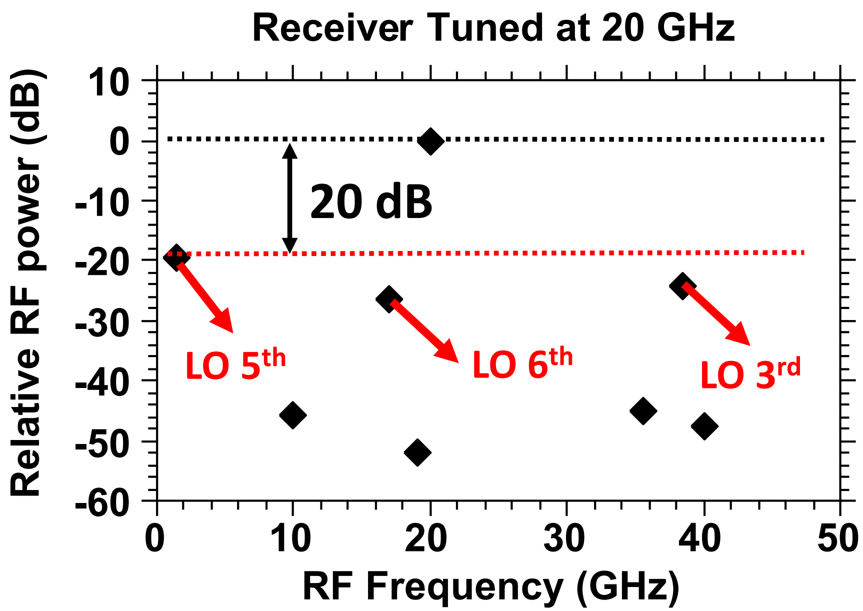


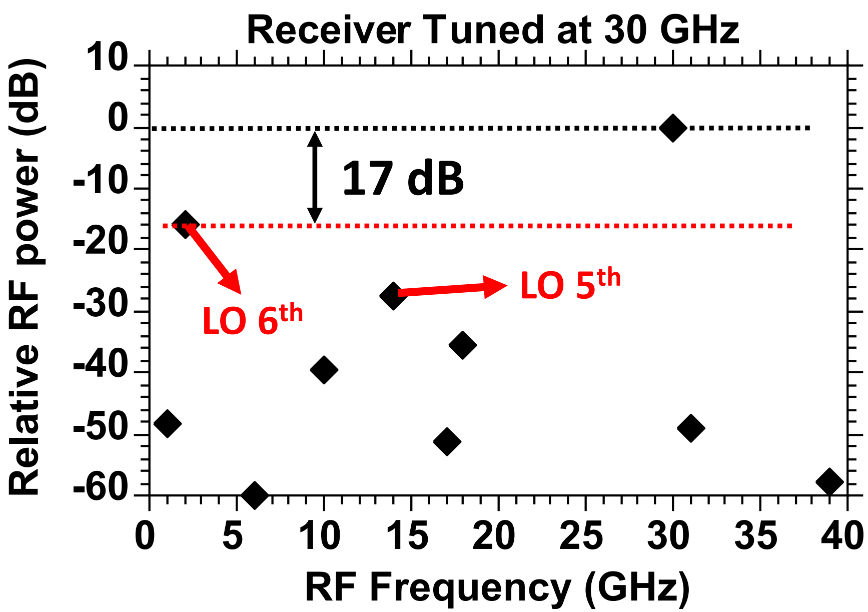
RF tuned at 2 GHz > 32 dB

RF tuned at 5 GHz > 30 dB

RF tuned at 10 GHz > 25 dB

System Measurements - Results





RF tuned at 20 GHz > 20 dB

RF tuned at 30 GHz > 17 dB

1-30 GHz Reconfigurable Transceivers

Dual conversion: classic widely-tunable RF receiver design
Extend to microwave (1-30 GHz) → Need ~100 GHz IF

Dual conversion: feasible with wideband (THz) transistors

100 GHz signal frequency is only 10% of transistor f_{max}
Enable high-dynamic-range mixers & amps.
4:1, 60-100 GHz LO multiplier using digital techniques

Summary of results:

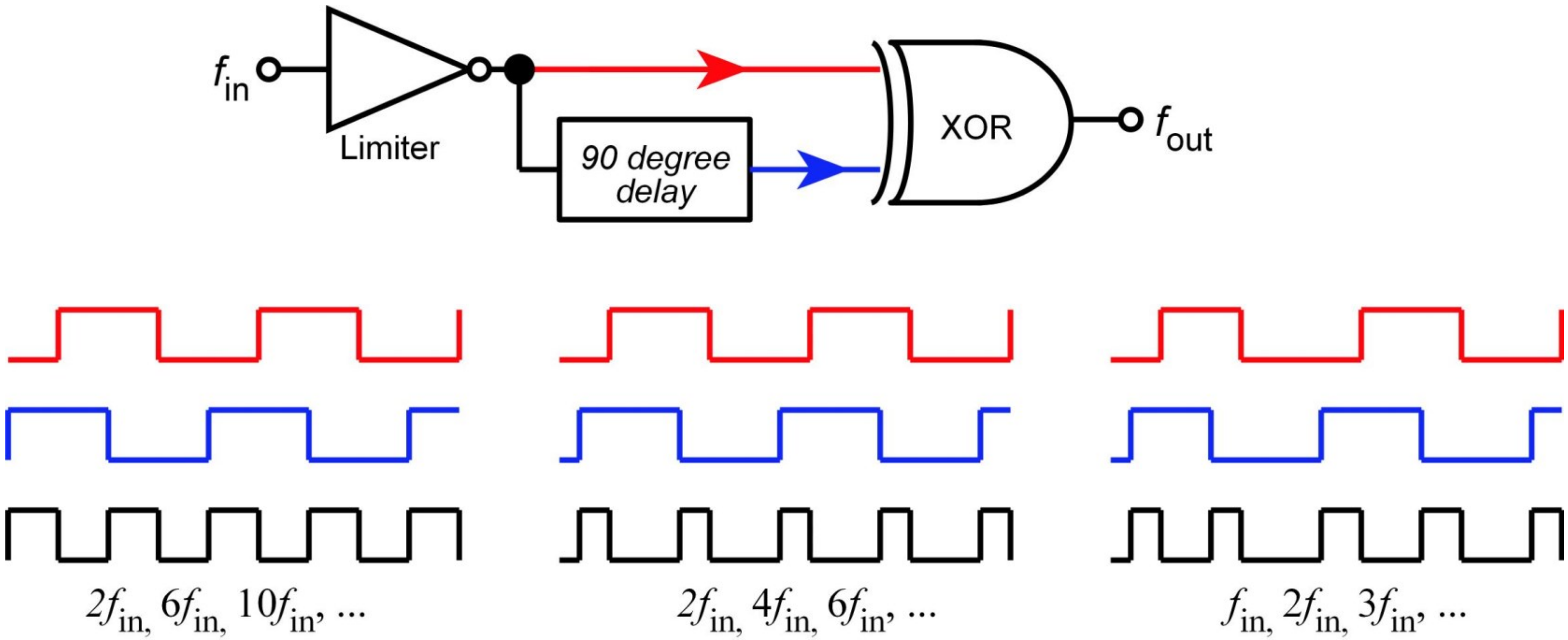
High dynamic range (6-8 dB loss ≈ noise figure, **>20** dBm IIP3)
Very wide tuning LO (15-25 GHz ↔ 60-100 GHz)
Spurious free tuning range of 1-30 GHz using dual conversion with IF at 94 GHz

We thank Teledyne Scientific & Imaging for IC fabrication

Thank you

Back-up Slides

Problems of Conventional Design



<u>Limiter DC offsets</u>

Spurious outputs at DC, $2f_{in}$, $4f_{in}$, ...

→ spurious XOR outputs at f_{in}, $3f_{in}$, $5f_{in}$, ...

➡

<u>High-Q filters are required</u>

large die area

poor out-of-band rejection

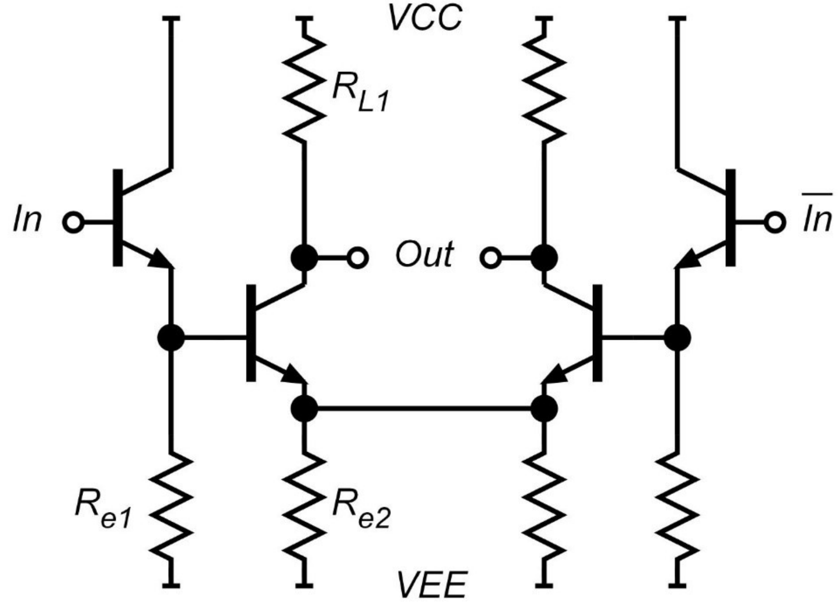
<u>Delay ≠ 90 degree</u>

Spurious XOR outputs at DC, 4fin, ...

<u>CMOS digital logic</u>

Cannot operate > 100 GHz

In/Output-stage: ECL-gate

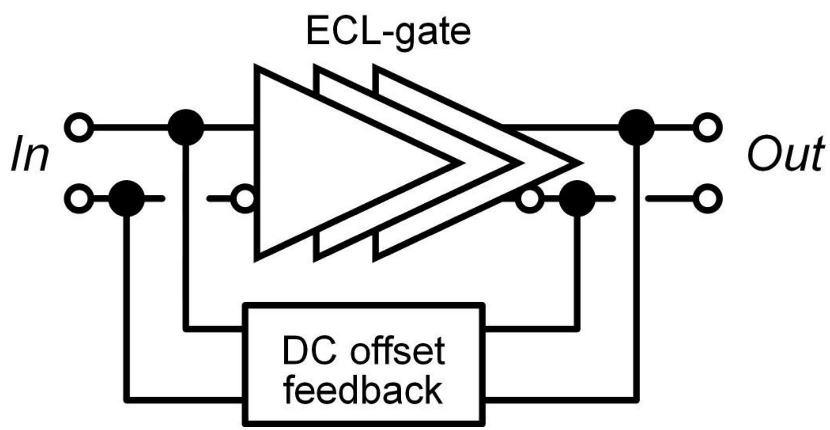


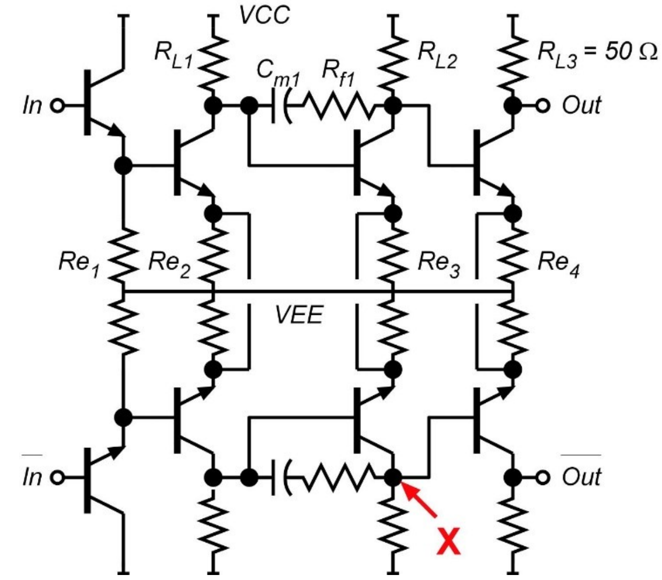
<u>Input</u>
Converts a sinusoidal input into a square-wave
Input can be driven single-endedly
Low input signal (-3 dbm) can drive

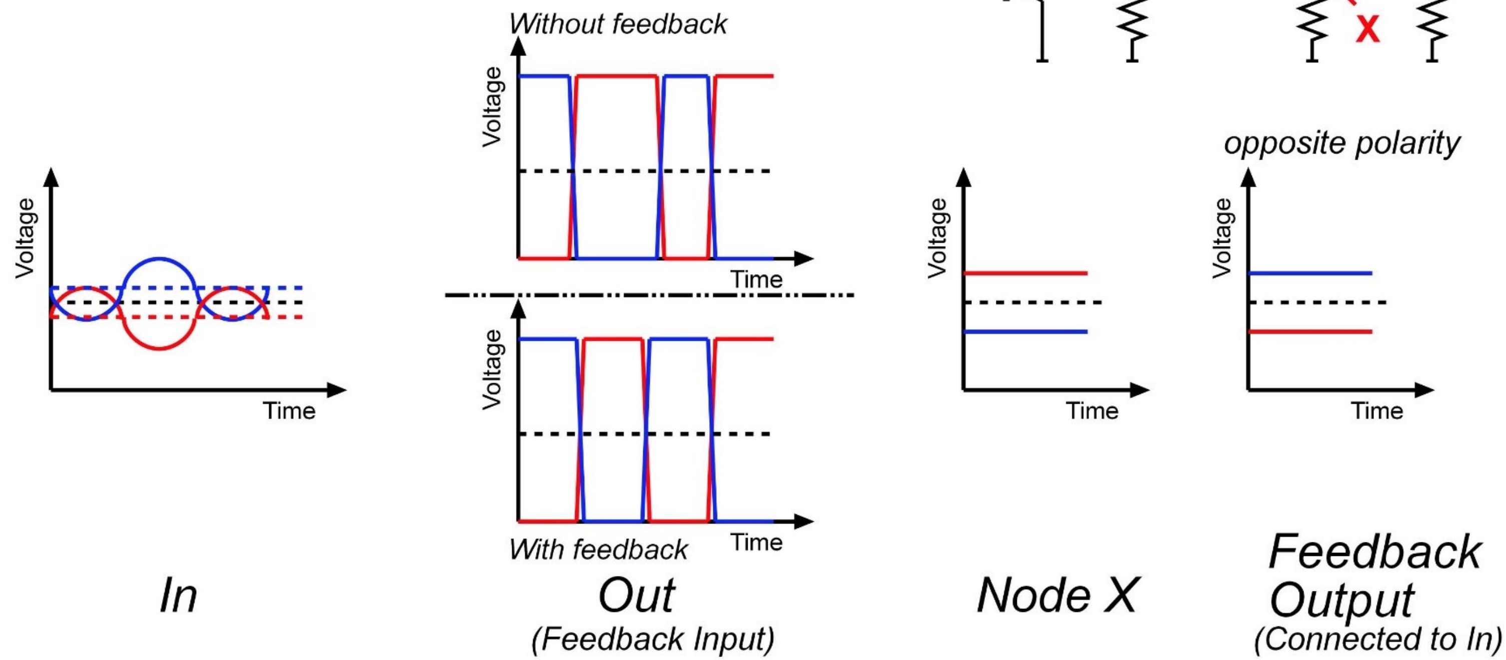
<u>Output</u>
Driver 50 Ω output load

ECL-gate can operate at > 100 GHz

DC-offset Cancellation

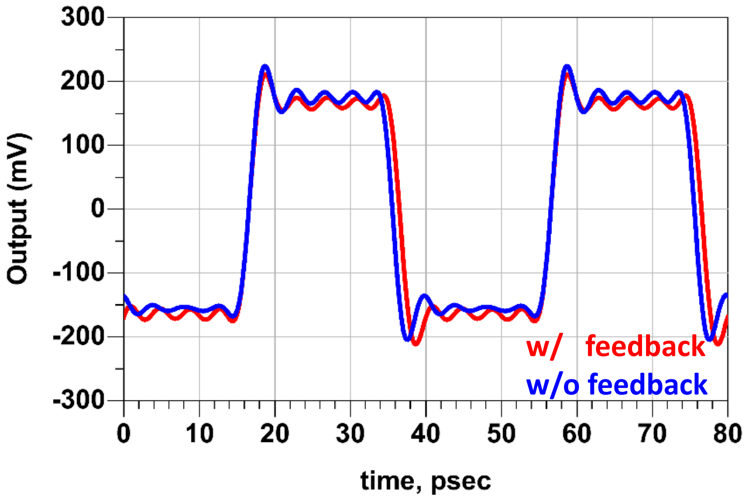


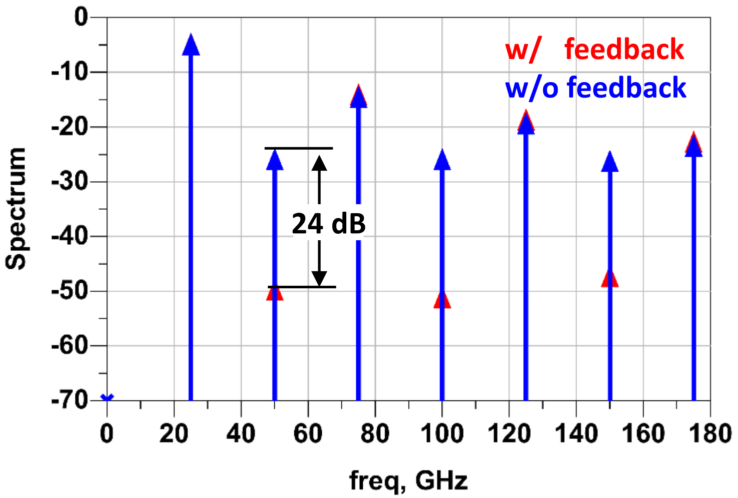




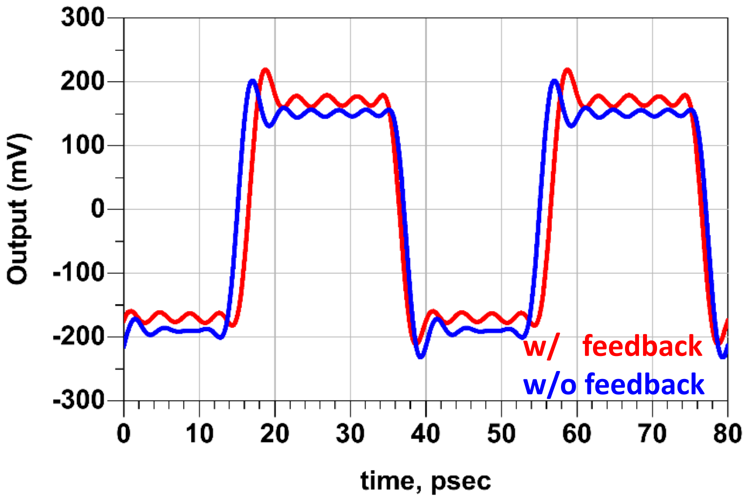
Simulation results: Input 25 GHz

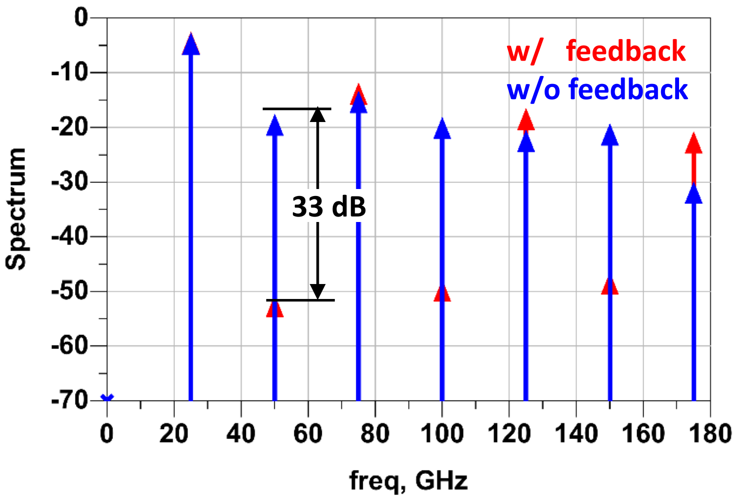
The second ECL-gate has 100 mV offset voltage



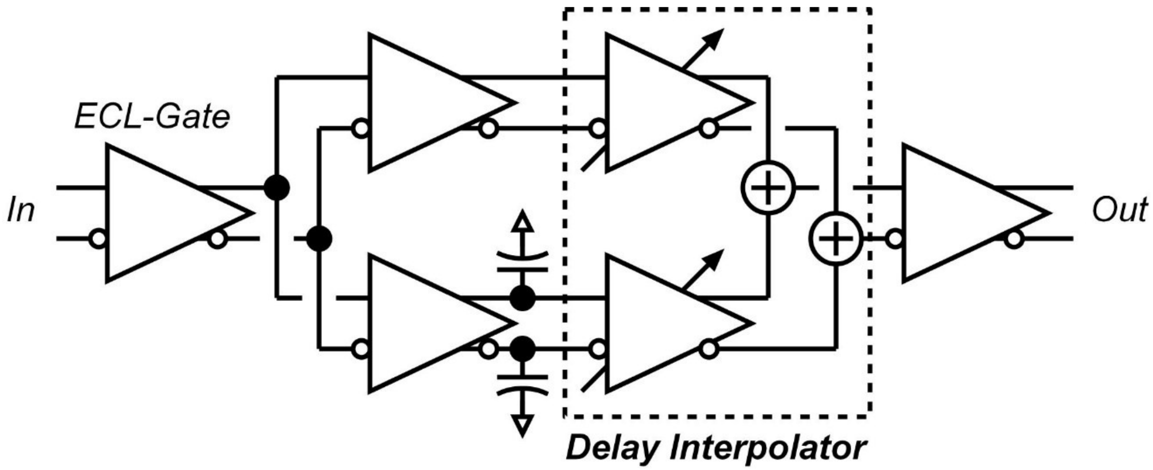


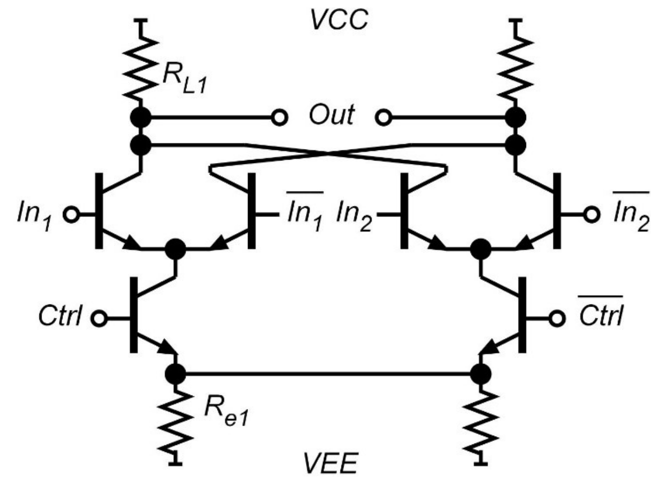
Each ECL-gate has 100 mV offset voltage





Delay Control



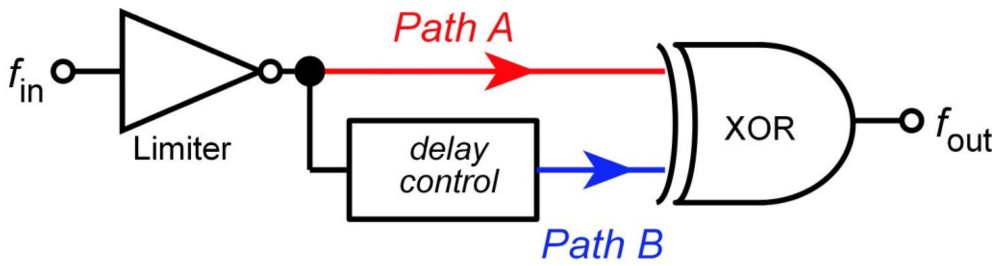


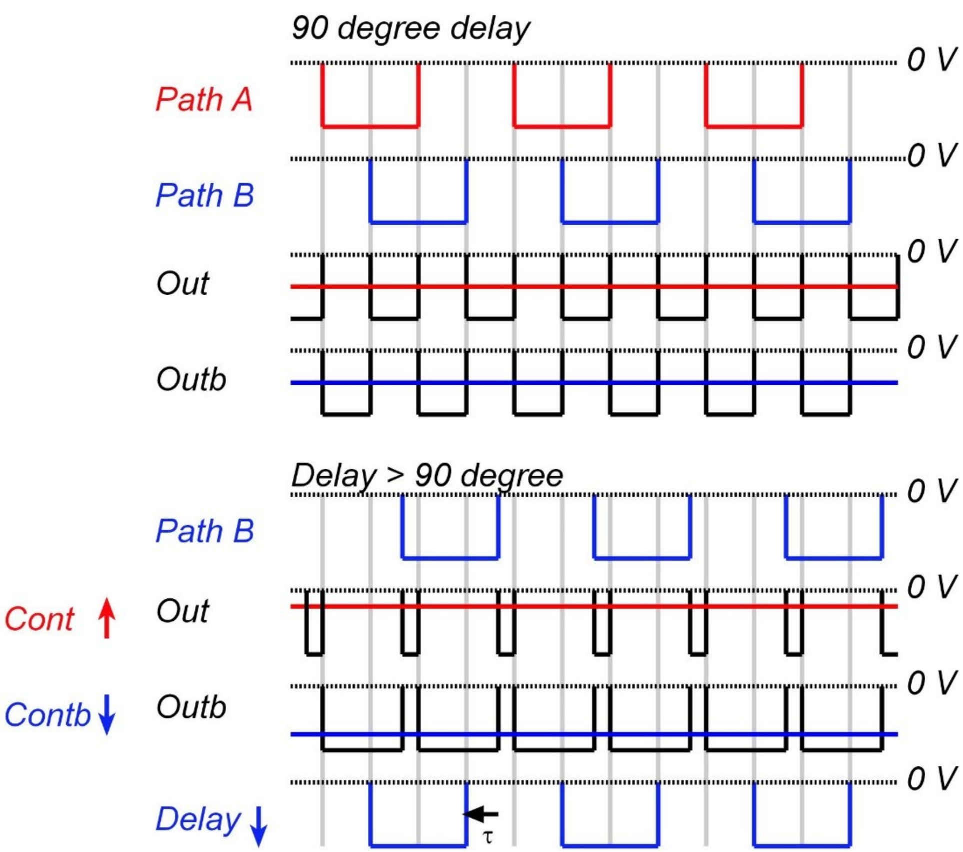
Delay interpolator

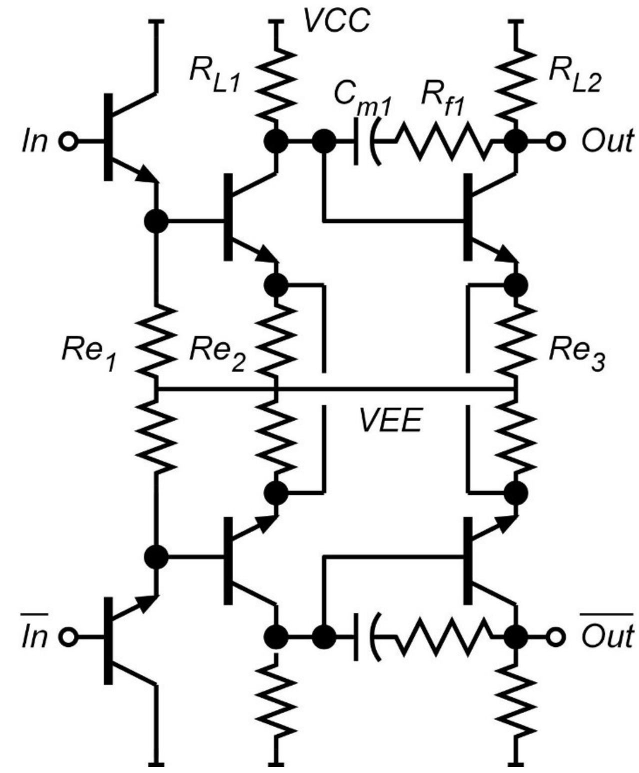
Optimum operating range is limited by the tunable delay range

XOR has same topology as the delay interpolator

Delay Feedback & Operation



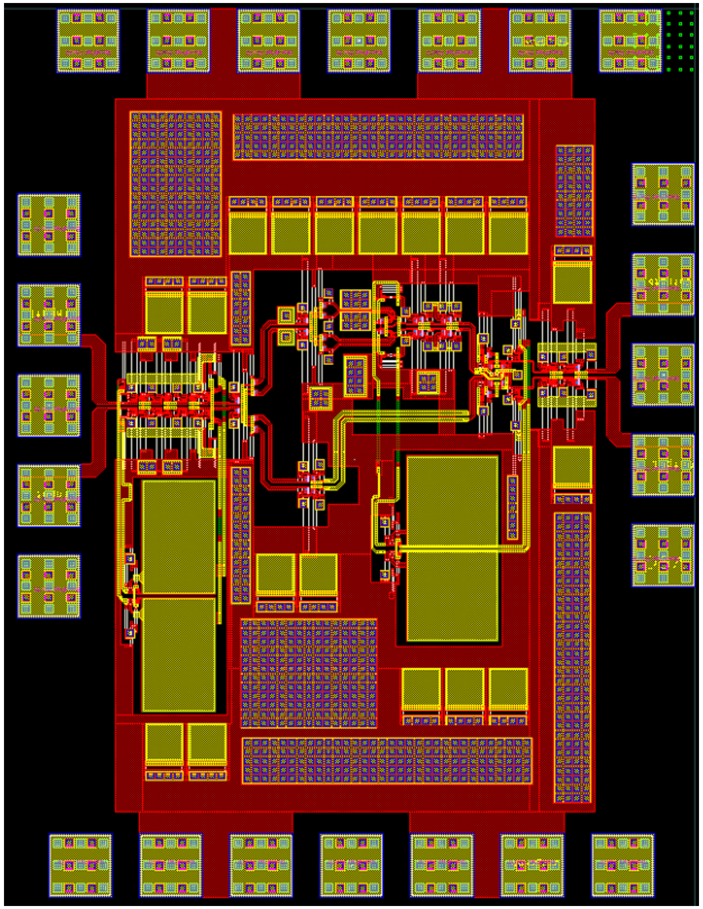


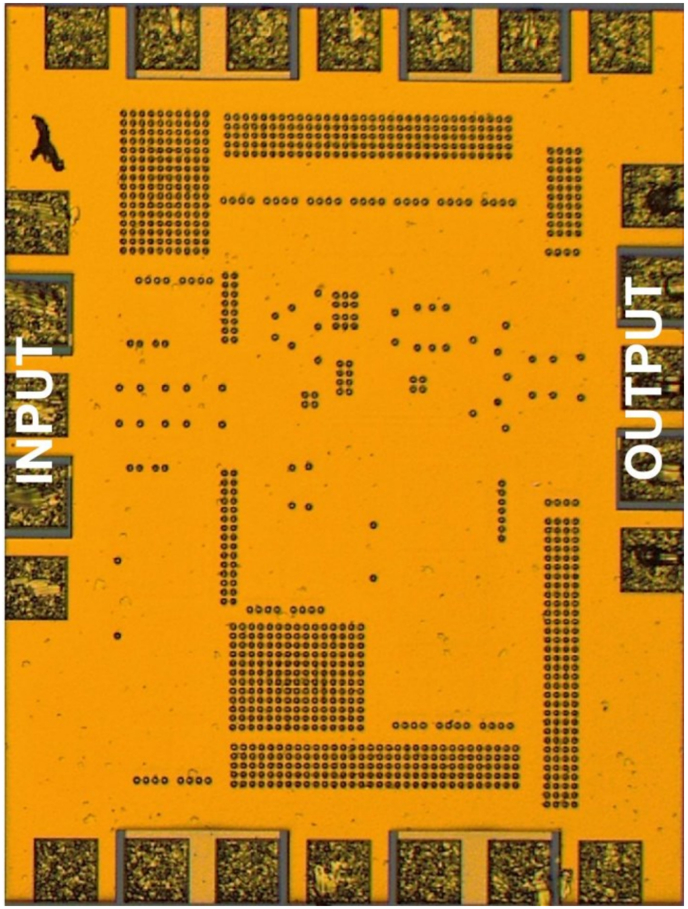


Input is connected to XOR outputs

Outputs are connected to Ctrl of the delay interpolator

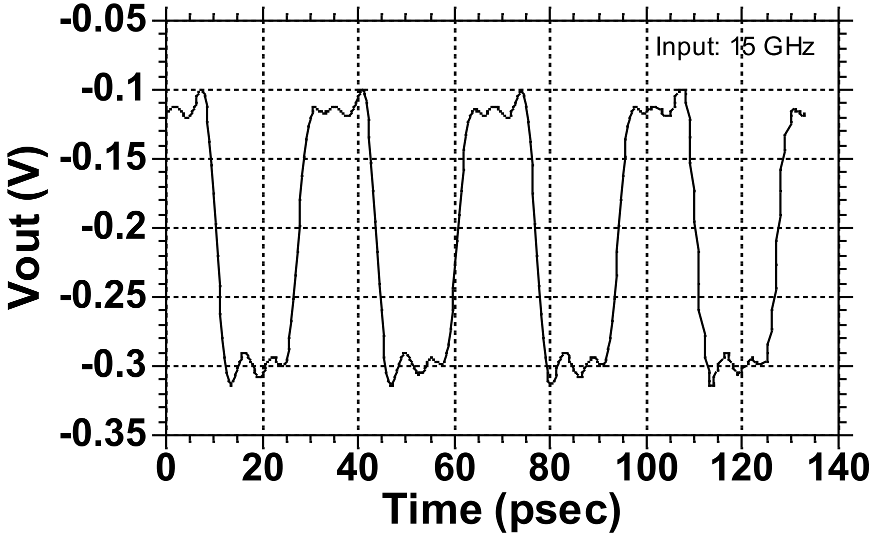
Layout & Chip Photo



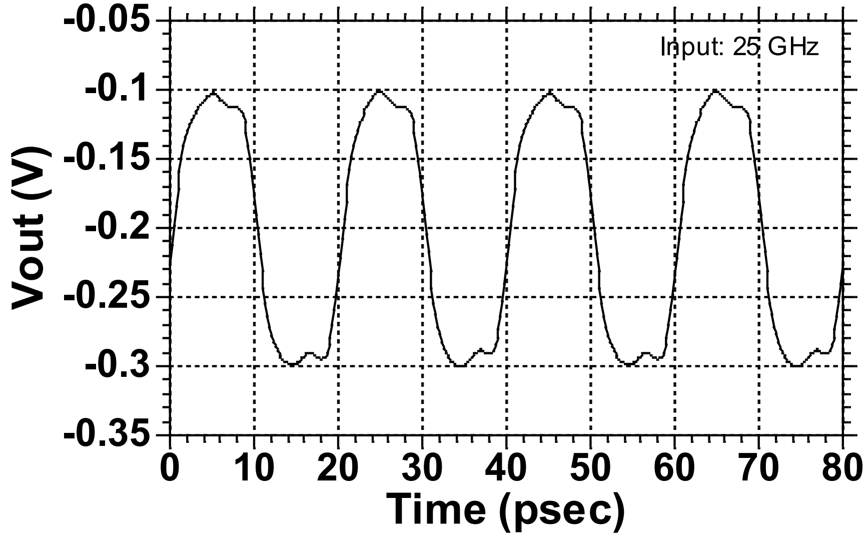


Chip size: 750 × 990 um^2 (area encloses active devices: 540 x 280 um^2)
Power consumption: 284 mA (32 – 53 GHz), 324 mA (60-100 GHz) @ 3.3 V

Simulation: Time-domain



Input 15 GHz → Output 30 GHz



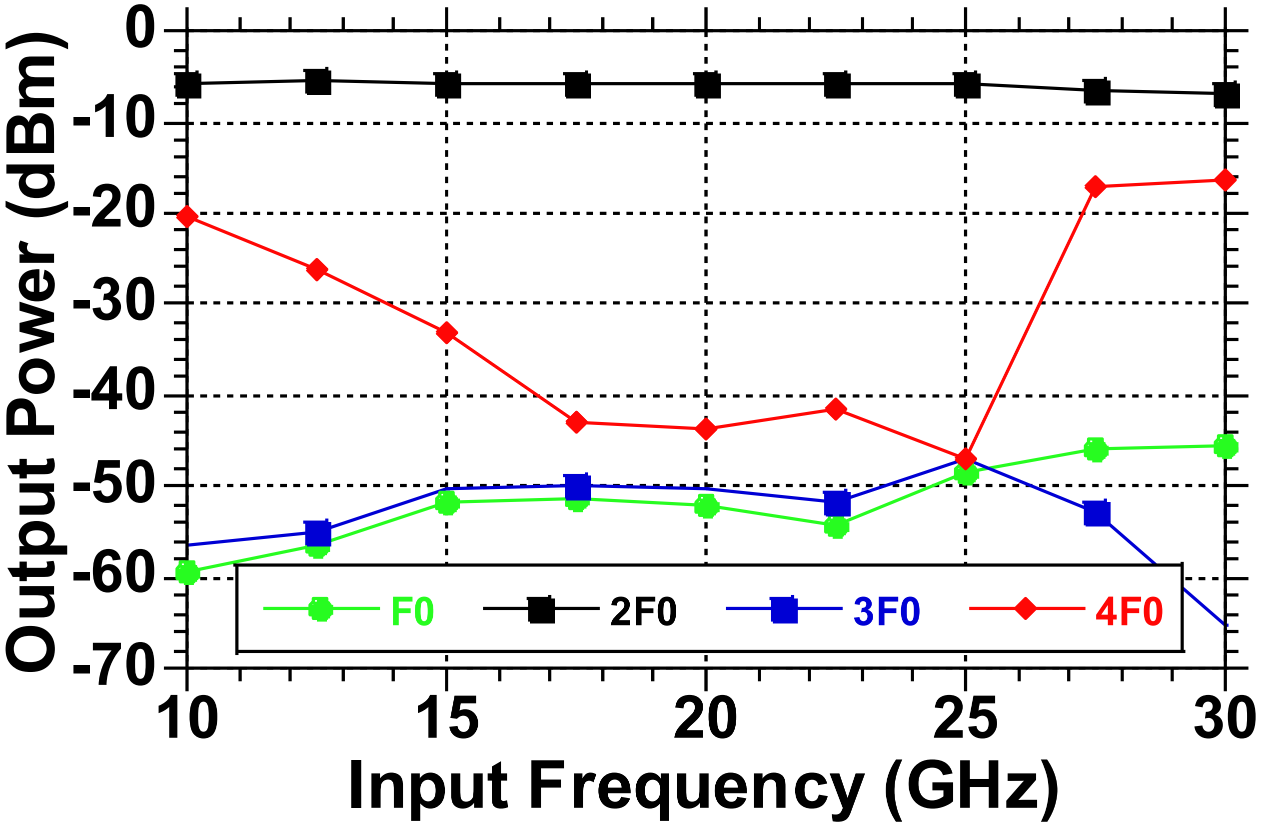
Input 25 GHz → Output 50 GHz

<u> single-ended simulation results</u>*

Waveforms have 50 % output duty-cycle

The amplitude correspond to digital logic level in the design

Simulation: Frequency-domain

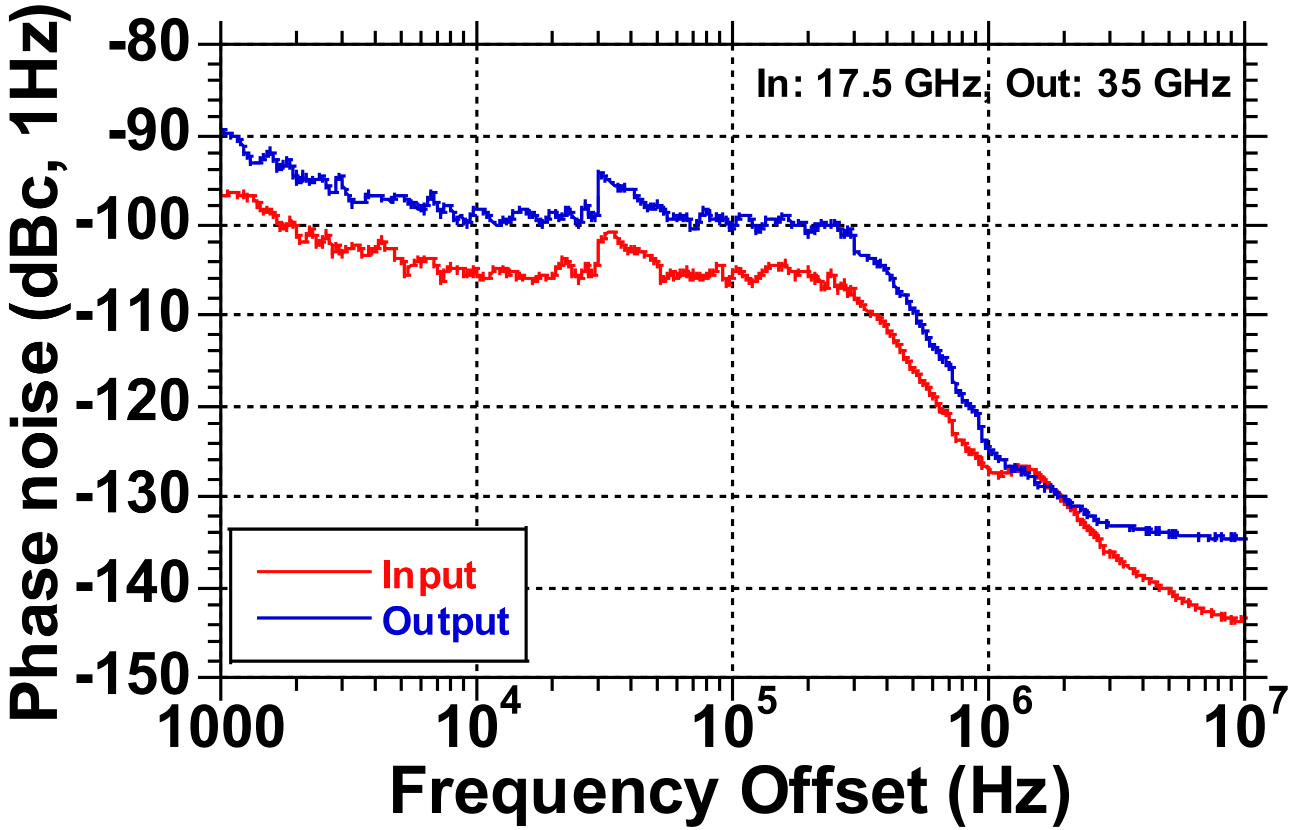


2^{nd} harmonic output power: -8 – -5 dBm

1^{st} & 3^{nd} harmonic rejection > 40 dBc

4^{th} harmonic rejection > 30 dBc

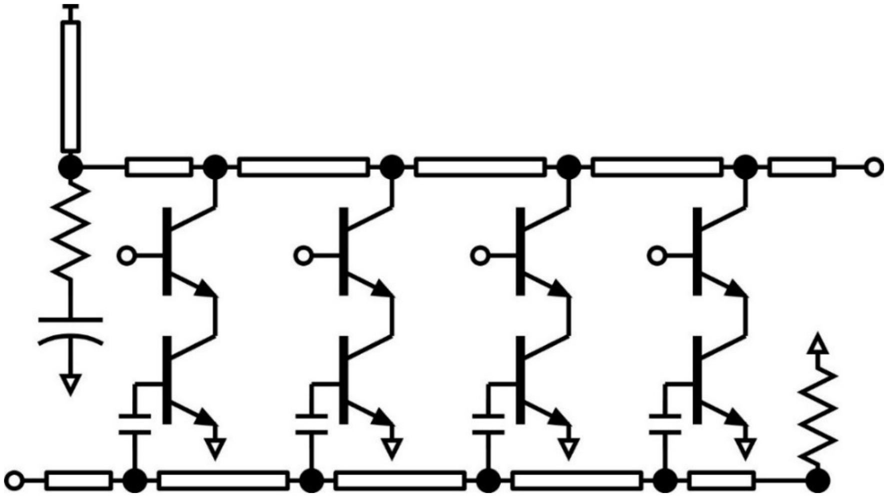
Phase Noise Measurements

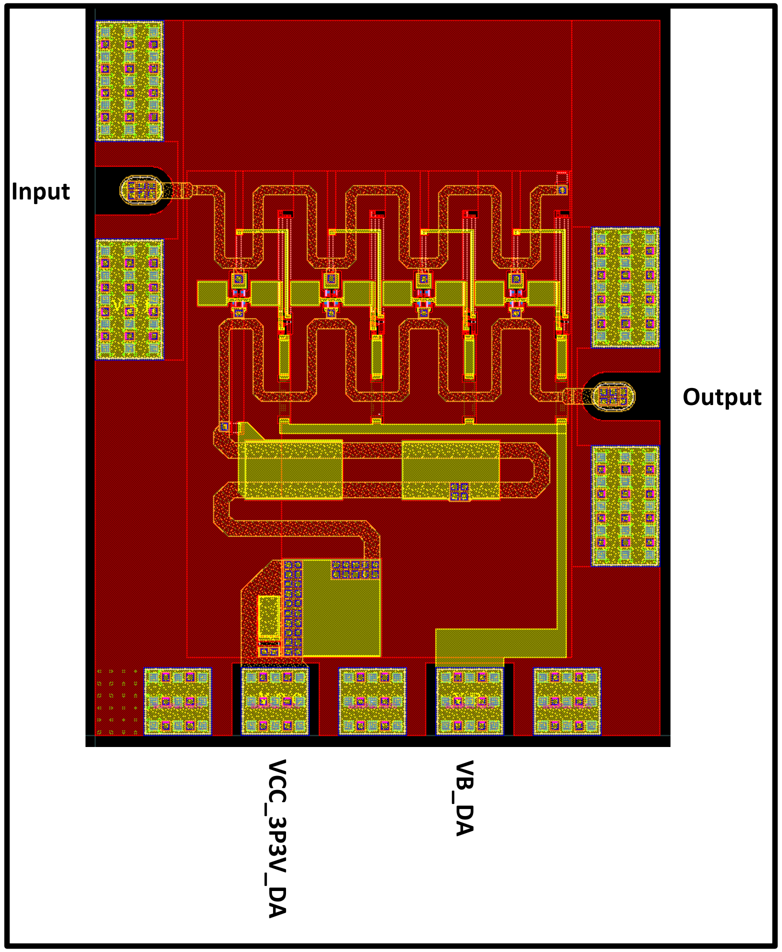


Input: 17.5 GHz, Output 35 GHz

Added phase noise: 6 – 7 dB (*ideal multiplier: 20*log(N)*)

Travelling Wave Amplifier (TWA)

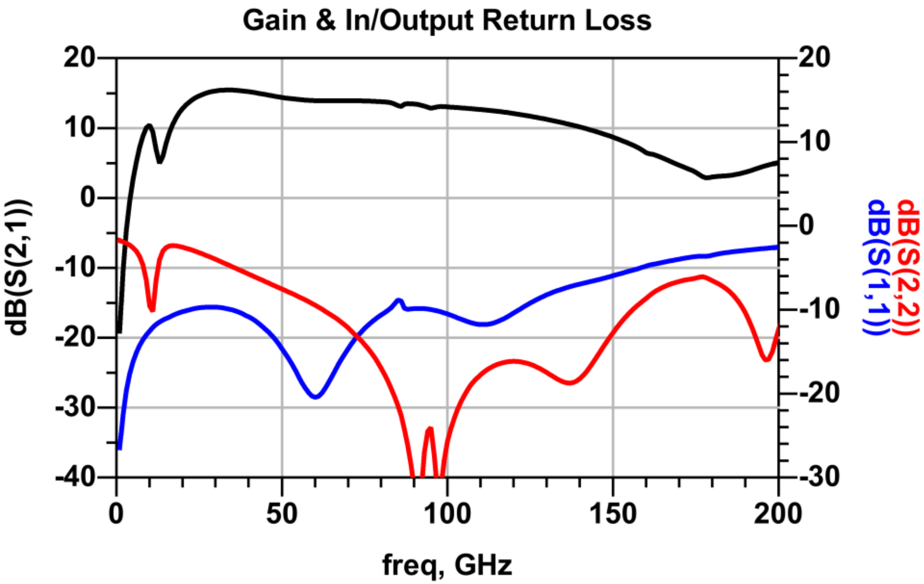


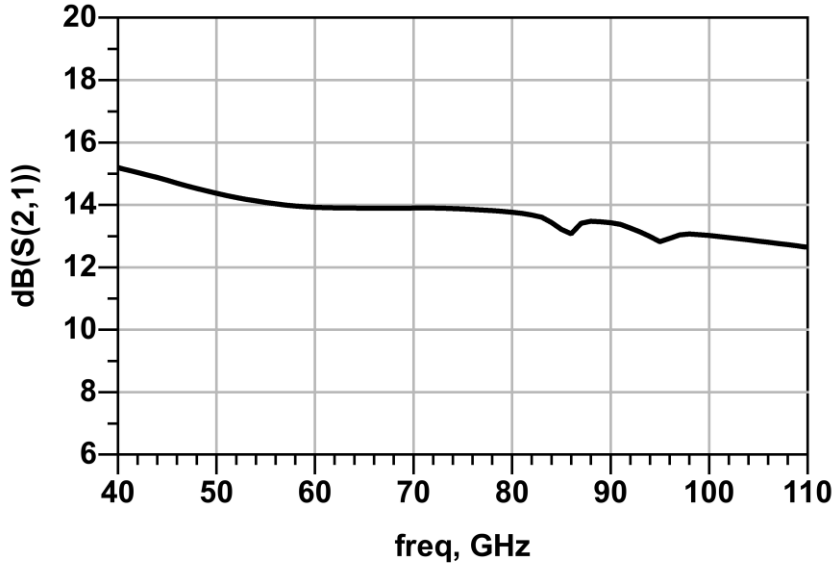


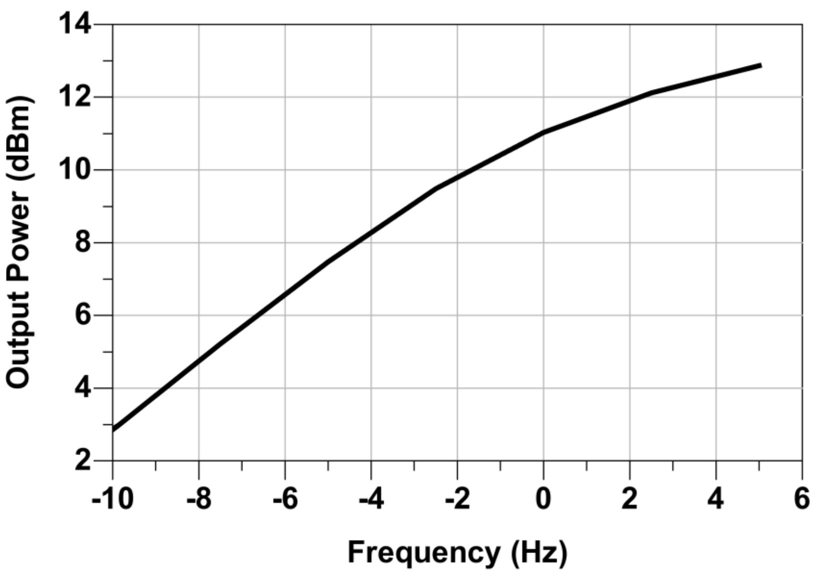
Size: 580 x 740 um^2

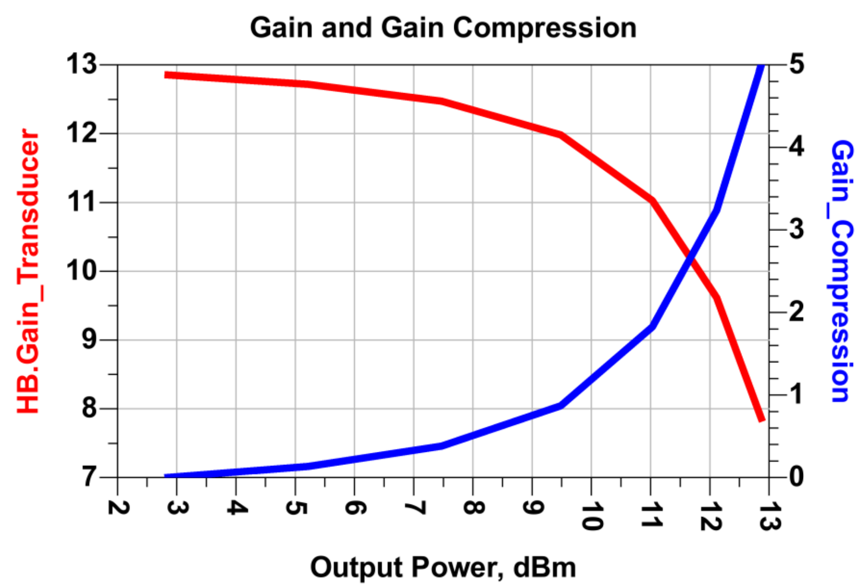
Bias	Probe	
VCC_3P3V_DA: 41.2 mA @ 3.3 V VB_DA: 13.6 mA @ 3.3 V	RF	GSG (W-band, 2)
	DC	PGP (1)

Travelling Wave Amplifier (TWA)

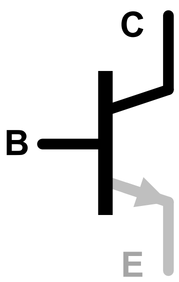




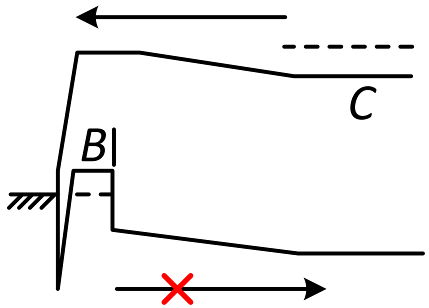




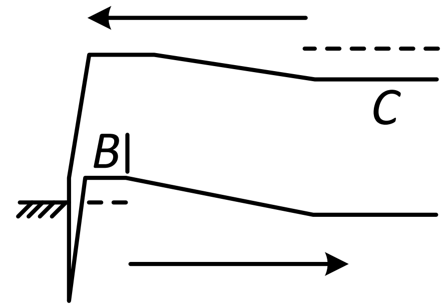
High Speed DHBT BC Diode



DHBT



Band diagram

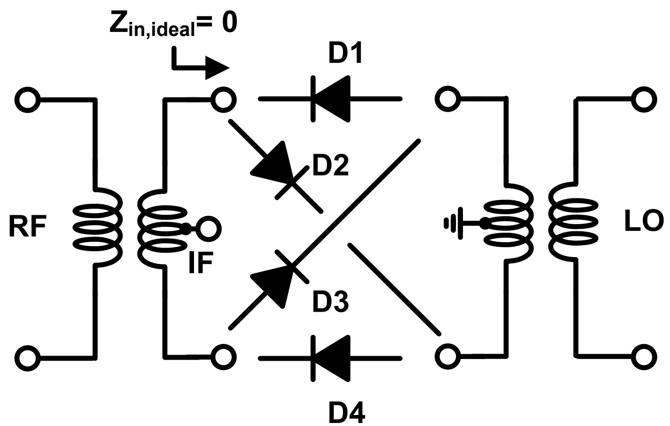


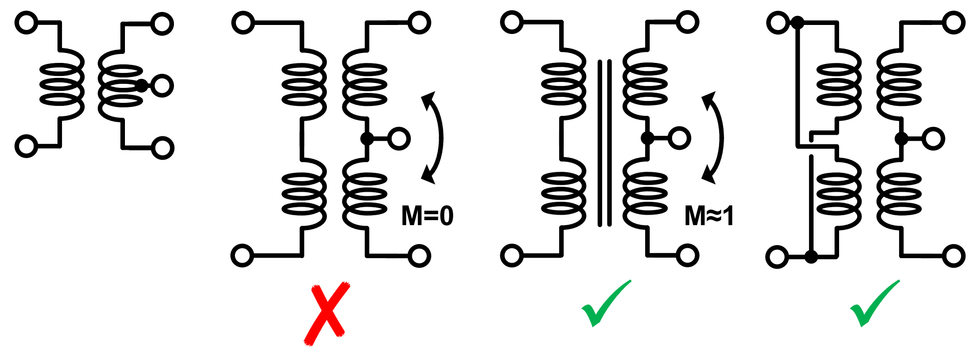
SHBT band diagram

Double-heterojunction base-collector diode
- Hole minority carrier storage is eliminated by large energy barrier to holes
- Electron minority carrier storage time is small

→ Schottky-like high-frequency characteristics

Balun For Diode Mixer





Common-mode impedance $Z_{cm,RF}$ must be zero

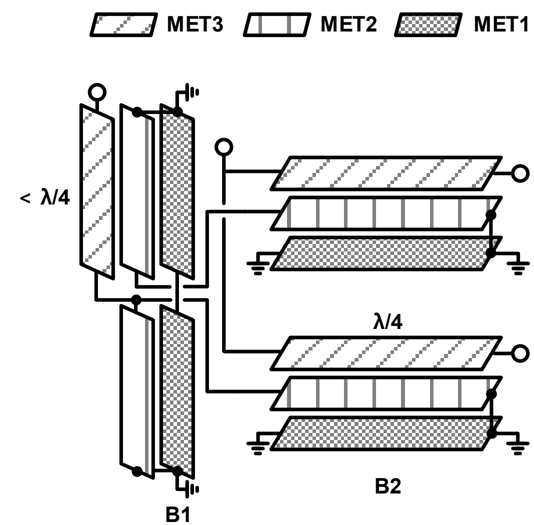
IF port is required

Simple center-tapped transformer has wrong Z_{cm}

- Two transformers in *series*.

Ferrite loading gives correct Z_{cm}; can't use on IC

Options: two *parallel* transformers, or balun.



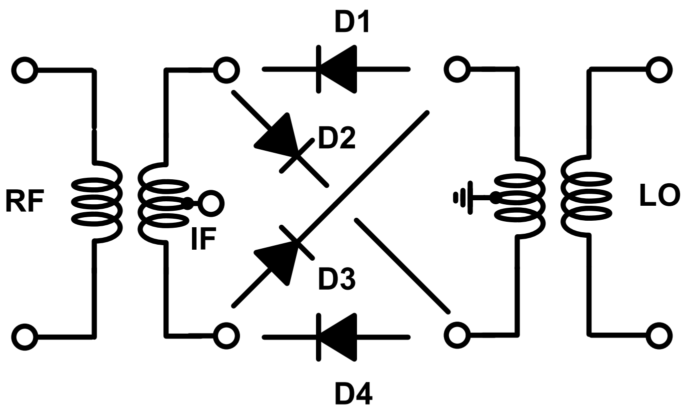
Proposed balun

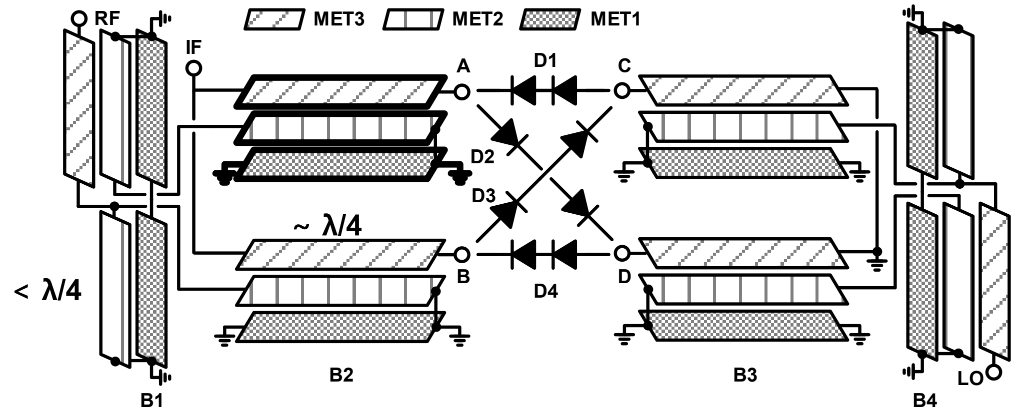
Proposed balun

- Sub-quarter wavelength balun (B1) [3]
- Section B2 provides the IF port and $Z_{cm,RF}$=0

[3] H. Park, et al., *IEEE J. Solid-State Circuits* (UCSB)

Diode Mixer

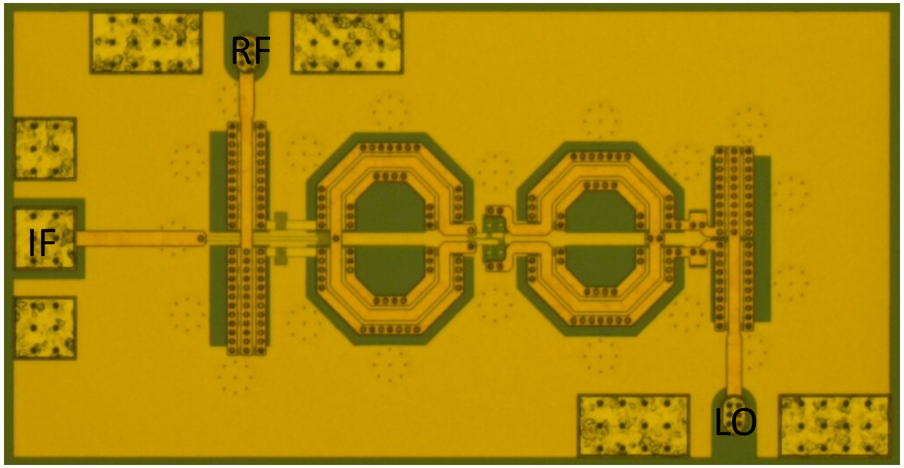




Four series-connected BC diode pairs

RF and LO baluns

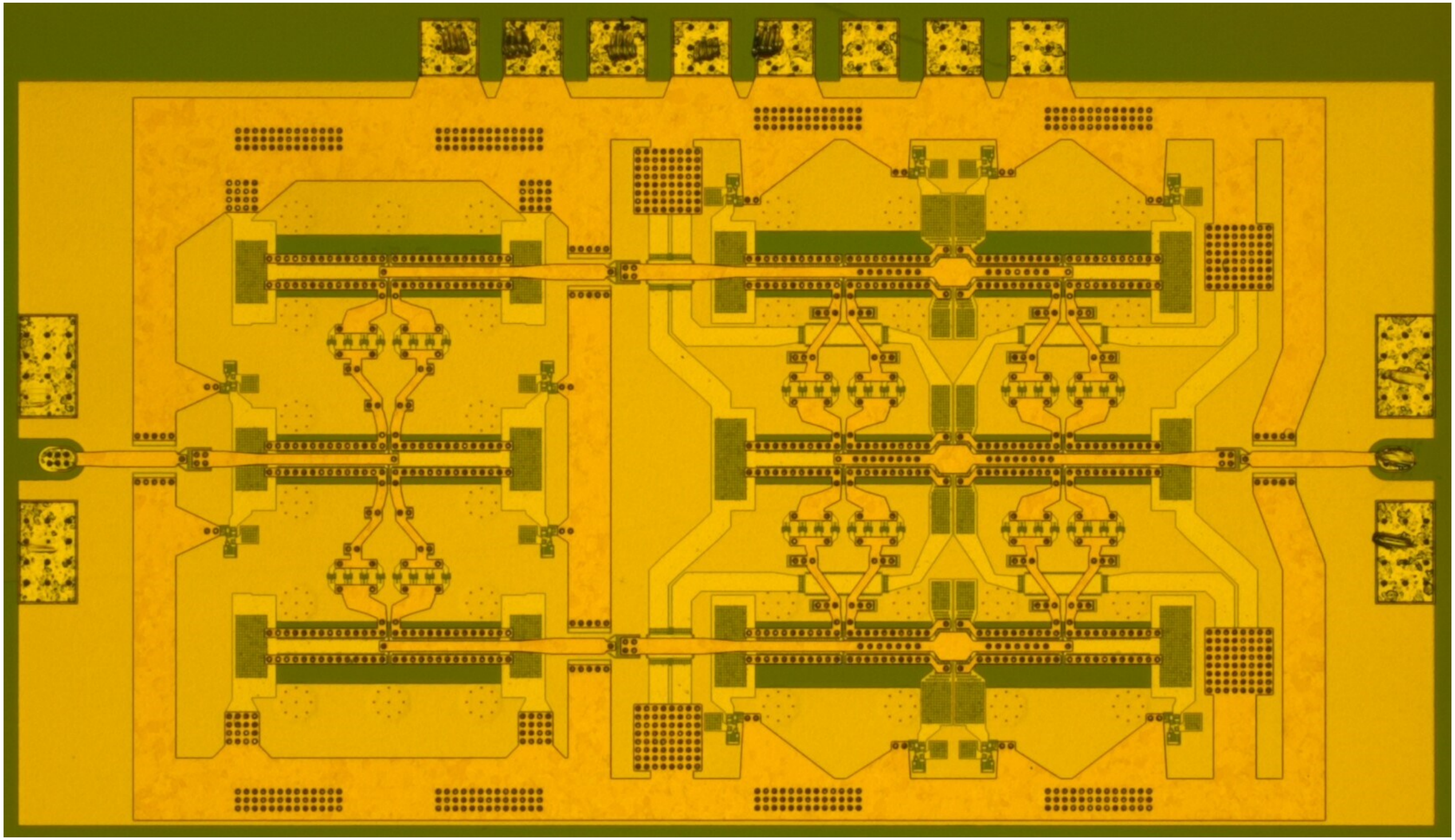
Balun loss < 4 dB over W-band



Size: 700 um x 300 um (excl. pads)

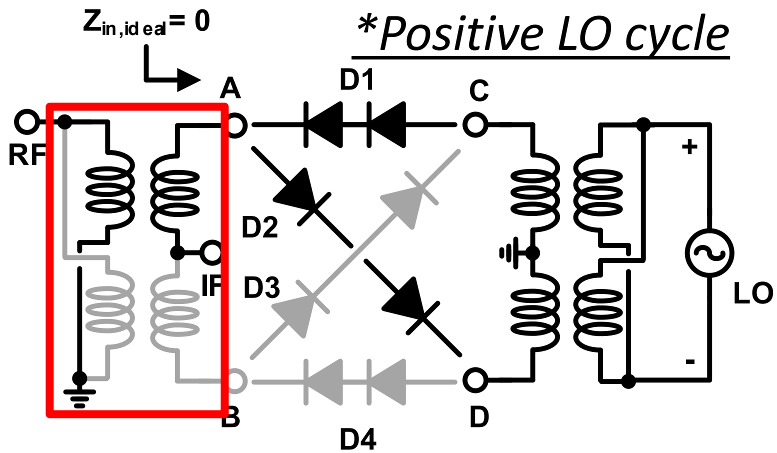
High-Power LO Driver

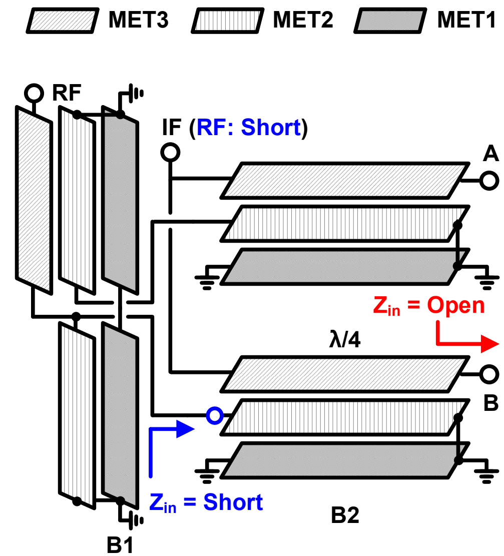
Wide bandwidth > 60-100 GHz, > 19 dBm output power

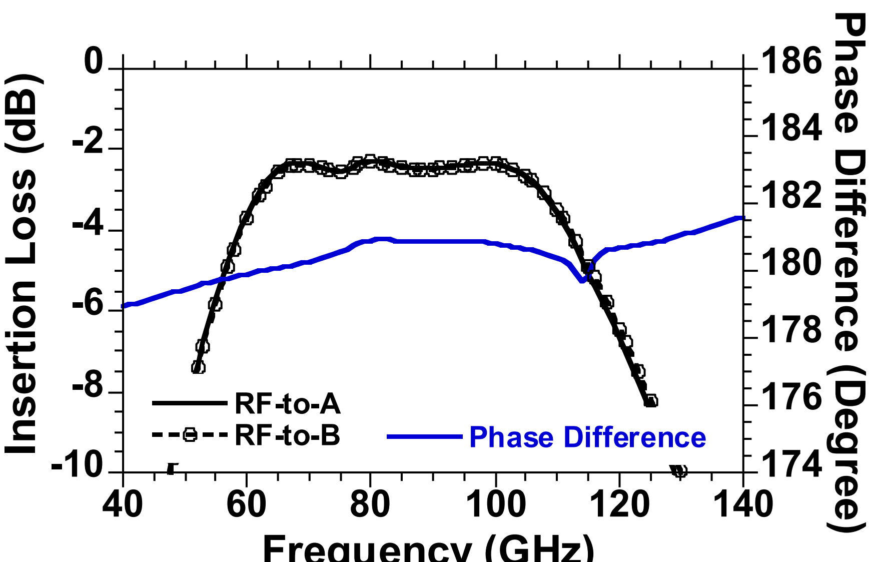


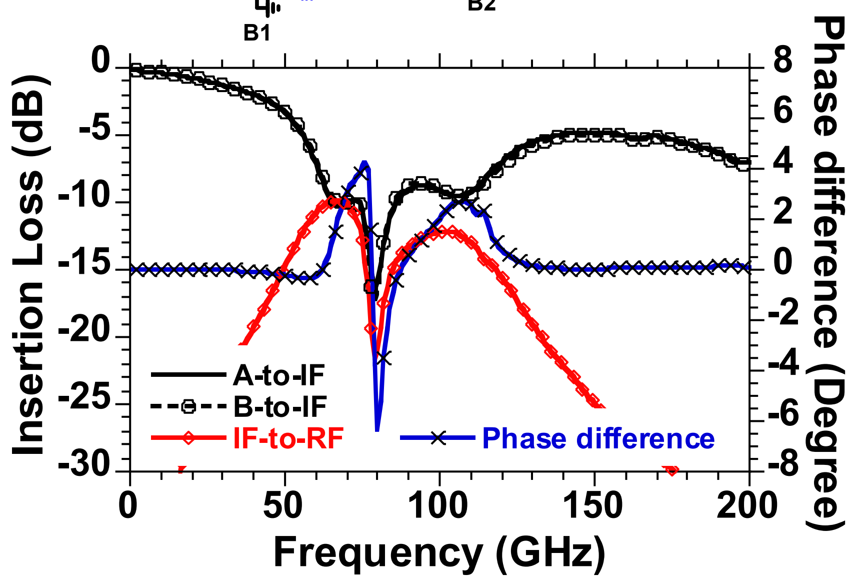
R. Maurer, et al., “Ultra-wideband mm-Wave InP Power Amplifiers in 130nm InP HBT Technology,” in *2016 IEEE CSICS*

RF Balun Design



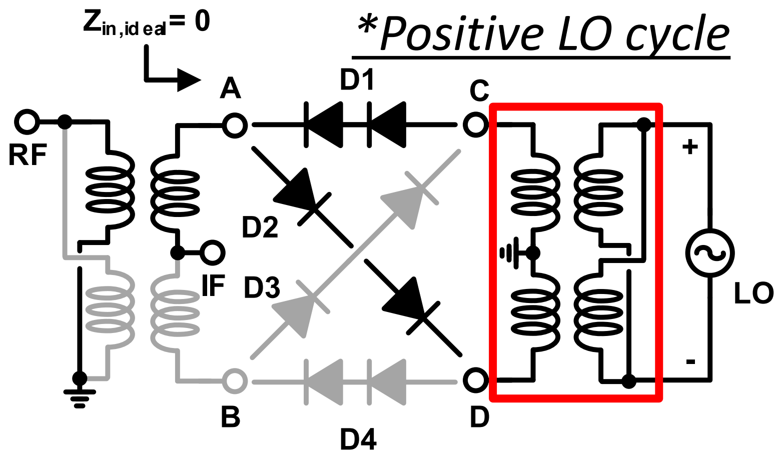


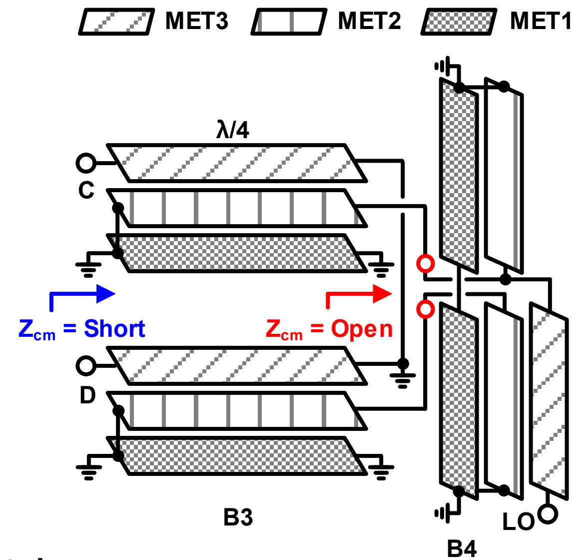


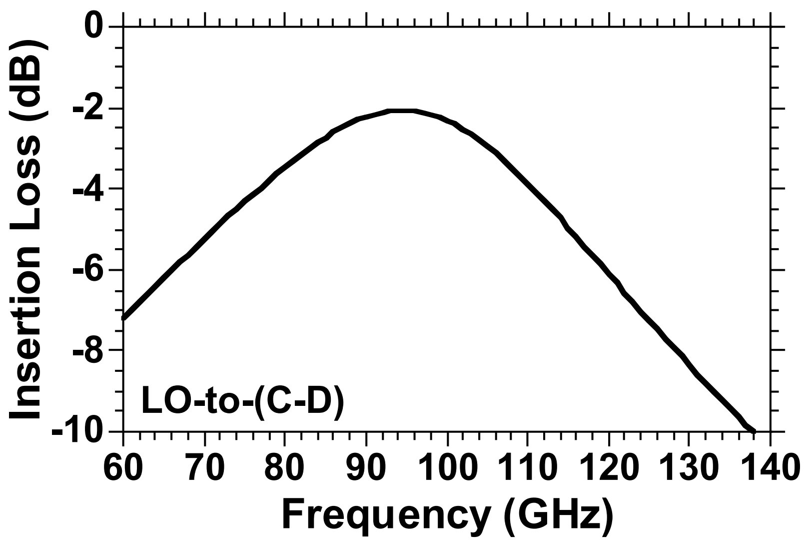


Insertion loss < 3.5 dB, phase error < 4°over W-band

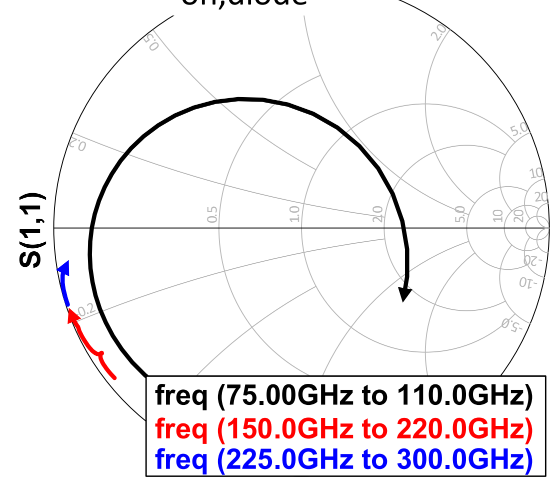
LO Balun Design







Z_{in} without $R_{on,diode}$



2-4 dB insertion loss over W-band

System Performance Assuming some LNAs

LNA with 18 dB and 12 dB gain

With 18dB gain LNA

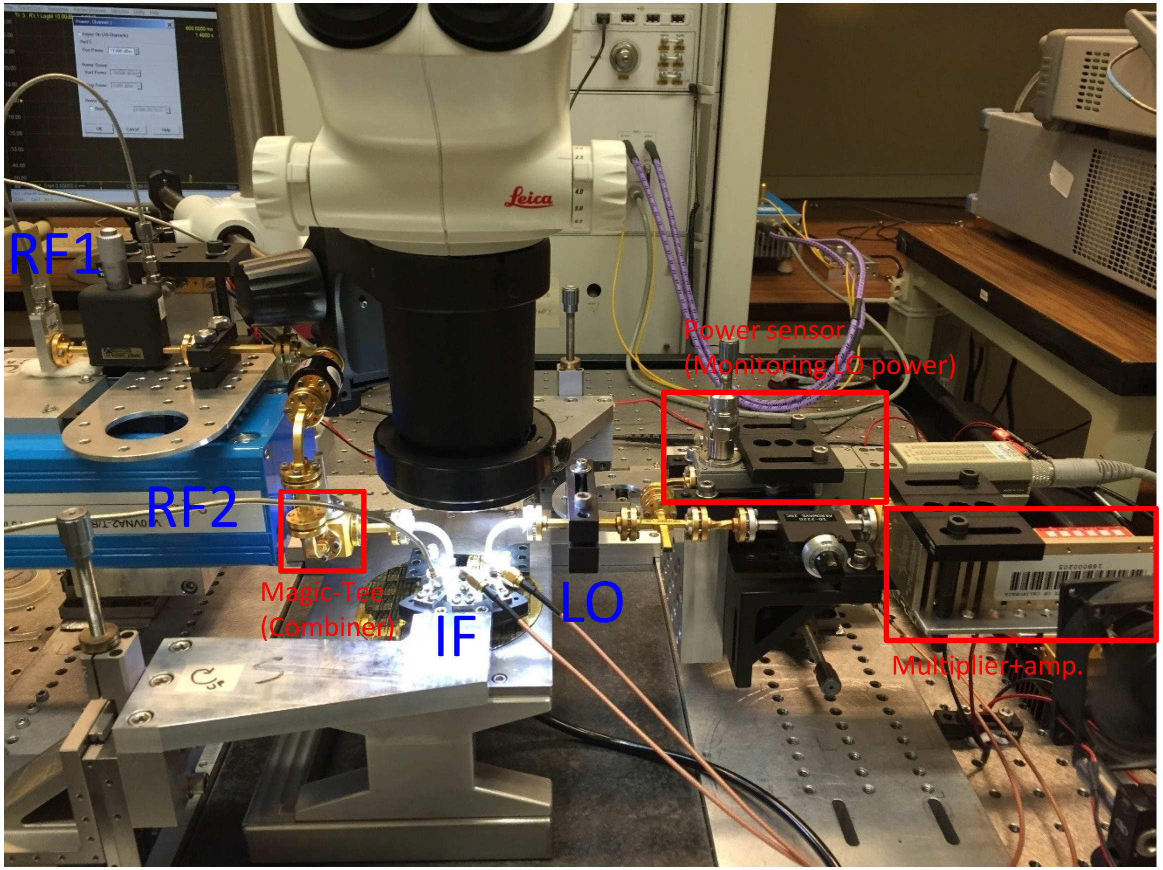
Receiver	units	overall	RFA1	M1	F2	IFA1	IFA2	~~IFA3~~	M2	F3	IFA4
Gain	dB	35	18	-8	-1	6.5	0	~~0~~	0.5	-1	20
Gain	linear	3162.28	63.1	0.16	0.79	4.47	1.00	~~1.00~~	1.12	0.79	100.00
Noise figure, component	dB		2	8	1	6.2	0.01	~~0~~	10	1	2
Noise factor, component	linear	2.37	1.58	6.31	1.26	4.17	1.00	~~1.00~~	10.00	1.26	1.58
IIP3, component	dBm	0	25	23	100	24.4	100	~~100~~	23	100	30
DC Power, component	mW										
antenna-referred IP3 of component	dBm		25	5	90	15.4	84.5	~~84.5~~	7.5	84	15
antenna-referred IP3 of system (in-band)	dBm	5									
antenna-referred IP3 of system (out-of-band)	dBm	5									
antenna-referred noise factor contribution	linear	2.37	1.58	0.08	0.03	0.4	0.00	~~0.00~~	0.25	0.01	0.02
system noise figure	dB	3.8									

With 12dB gain LNA

Receiver	units	overall	RFA1	M1	F2	IFA1	IFA2	~~IFA3~~	M2	F3	IFA4
Gain	dB	29	12	-8	-1	6.5	0	~~0~~	0.5	-1	20
Gain	linear	794.33	15.85	0.16	0.79	4.47	1.00	~~1.00~~	1.12	0.79	100.00
Noise figure, component	dB		2	8	1	6.2	0.01	~~0~~	10	1	2
Noise factor, component	linear	4.72	1.58	6.31	1.26	4.17	1.00	~~1.00~~	10.00	1.26	1.58
IIP3, component	dBm	0	25	23	100	24.4	100	~~100~~	23	100	30
DC Power, component	mW										
antenna-referred IP3 of component	dBm		25	11	96	21.4	90.5	~~90.5~~	13.5	90	21
antenna-referred IP3 of system (in-band)	dBm	11									
antenna-referred IP3 of system (out-of-band)	dBm	11									
antenna-referred noise factor contribution	linear	4.72	1.58	0.34	0.10	1.59	0.00	~~0.00~~	1.01	0.03	0.07
system noise figure	dB	6.7									

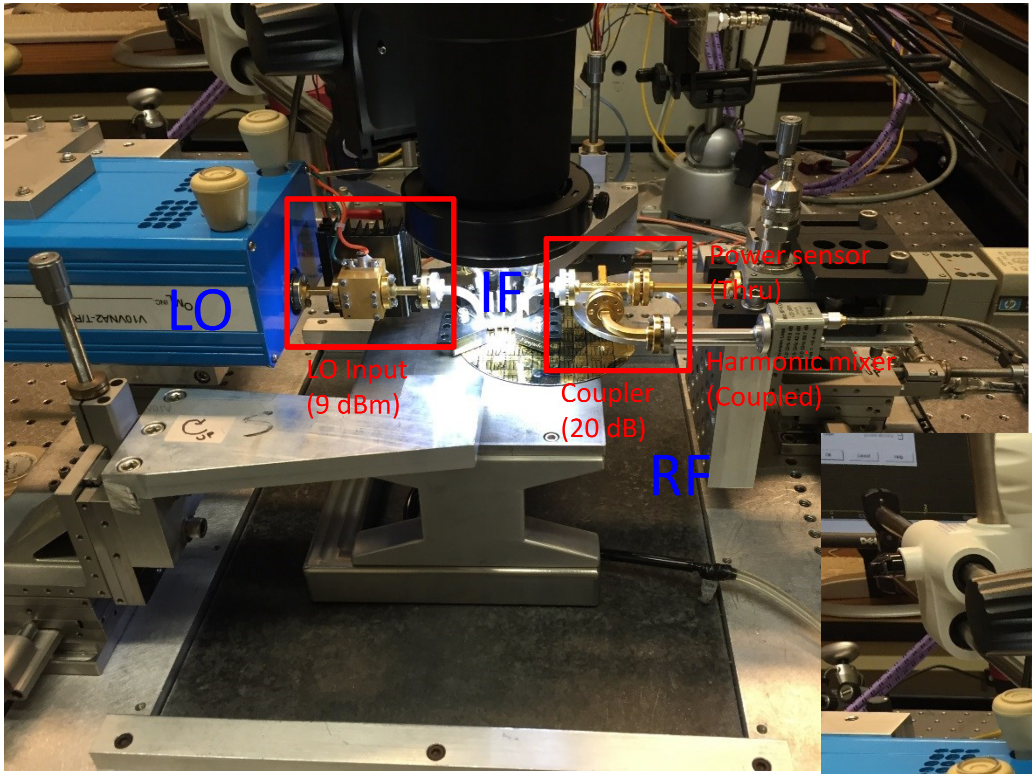
Figure 1: Receiver Dynamic Range Analysis with High-Gain and Moderate-Gain LNAs

IIP3 Measurement Setup



Up-conversion

Measurement Setup



Up-conversion

Spectrum and gain

Down-conversion