InP MOSFETs Exhibiting Record 70 mV/dec Subthreshold Swing

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Low InP/dielectric interface trap density D_{it} will enable low subthreshold swings (*SS*) in mm-wave MOSFETs [1] using InGaAs/InP composite channels [2] for increased breakdown and in tunnel FETs (TFETs) [3] using InAs/InP heterojunctions [4] for increased tunneling probability. Reducing D_{it} at the etched InP mesa edges of DHBTs and avalanche photodiodes will reduce leakage currents and increase breakdown voltages. While it can be difficult [5] to extract D_{it} of III-V interfaces from MOSCAP characteristics, D_{it} can be readily determined from the *SS* of long gate length L_g MOSFETs. Here we report InP-channel MOSFETs with record low *SS* indicating record low D_{it} at the semiconductor-dielectric interface. The devices use an AlO_xN_y/ZrO_2 gate dielectric and a 14nm channel thickness T_{ch}. A sample of 13 MOSFETs at 2 μm L_g shows *SS*=70mV/dec. (mean) ±3 mV/dec. (standard deviation), corresponding to a minimum D_{it} ~3×10^{12} $cm^{-2}eV^{-1}$. The lowest *SS* observed at 2 μm L_g is 66mV/dec. The results suggest that wide-bandgap InP layers can be incorporated into MOS device designs without large degradations in DC characteristics arising from interface defects.

Improved dielectric ALD processes on InAs, InGaAs, and GaSb has enabled high-performance TFETs [3] and digital [6,7] and mm-wave [1] InAs MOSFETs, with *SS*=61mV/dec. for InAs-channel MOSFETs [7]. Yet, the best reported work on high-k/InP interfaces showed *SS*=80-83 mV/dec [8].

The MOSFET structure is shown in **Fig. 1**. The channel, grown by MOCVD on a S.I. InP substrate, consists of a bottom 7 nm Zn-doped *P*-InP ($8\times10^{17}cm^{-3}$) layer to compensate growth interface donor impurities, and a top 7 nm UID-InP layer. Fabrication is similar to [6]. A 7 nm UID-InP vertical spacer, an 8nm Si-doped N^+-InP ($2\times10^{19}cm^{-3}$) and an 80 nm Si-doped ($4\times10^{19}cm^{-3}$) N^+-InGaAs S/D contact layer were selectively regrown by MOCVD. After regrowth, device mesas were isolated by wet etch. Prior to high-k deposition, a BOE etch and a 1-cycle digital etch in dilute HCl removed native oxides and prepared the surface. 4.5 nm ZrO_2 gate dielectric and the AlO_xN_y initiation layer were deposited by ALD. The dielectric was annealed in hydrogen at 350ºC for 30 minutes. The ALD and surface preparation are the same as in [7]. Ni/Au gate and Pd/Ni/Au S/D metal contacts were deposited by thermal evaporation. Separately, MOS capacitors (MOSCAPs) were fabricated on a 200 nm UID InP layer on N^+-InP substrate. These used the same surface cleaning, dielectric deposition, and hydrogen anneal as the MOSFETs. Gate and large-area body contacts were deposited in a single evaporation.

Fig. 2 shows the MOSCAP CV characteristic; the large increase in capacitance in accumulation at low frequencies is a measurement artifact due to gate leakage, arising when G/ω becomes comparable to the capacitance. The measured 1kHz-1MHz CV dispersion is considerably smaller than prior work on the high-k/InP interface [8,9].

Fig. 3 shows an SEM image of a 40 nm-L_g InP MOSFET. Note that the effective gate length is the horizontal channel length plus twice the vertical spacer thickness. **Fig. 4** shows the transfer characteristics of 40 nm, 100 nm, and 1 μm-L_g FETs. The threshold is ~0.7 V, determined by linear extrapolation. The on/off ratio is $>10^5$ for L_g>50 nm. Due to the 14nm thick channel, the output characteristics, **Fig. 5**, show severe short-channel effects at 40 nm L_g. I_{on} is 0.09, 0.1, 0.05 mA/um for 40 nm, 100 nm, 1 μm-L_g, respectively at V_{DS} = 0.6 V and V_{GS}-V_{TH}=0.5 V. 100 nm-L_g devices exhibit 0.31mS/μm peak g_m at V_{DS}=0.8 V. The N^+ S/D layer sheet resistance is 14 Ω, while the S/D contact resistivity is 7 Ω-μm^2, determined from TLM measurements.

Fig. 6 shows *SS* vs. L_g at V_{DS}=0.1 and 0.6 V. The record low SS of 70±3 mV/dec at V_{DS}=0.1 V is measured over 13 different 2 μm-L_g devices. D_{it} calculated from this *SS* is ~3×10^{12} $cm^{-2}eV^{-1}$. **Fig. 7** shows peak g_m vs. L_g at V_{DS}=0.6 V; **Fig. 8** shows DIBL vs. L_g at V_{TH}=1 μA/μm. Peak g_m reaches ~0.25 mS/μm at L_g<100 nm.

In this work we demonstrate record low trap density at InP/dielectric interfaces, these using ZrO_2/AlO_xN_y dielectrics. The results suggest that InP layers can be incorporated into gated MOS device structures without interface defects causing large degradations in DC characteristics. This work was supported by the Semiconductor Research Corporation (SRC) and the NSF under the E2CDA program.

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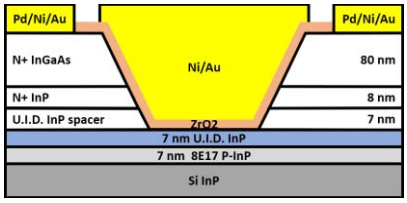

Fig. 1 Cross-sectional schematic of the InP channel MOSFETs.

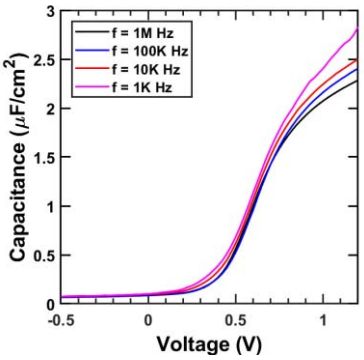

Fig. 2 CV characteristics of an InP MOSCAP with a ~4 nm ZrO_2/AlO_xN_y gate dielectric

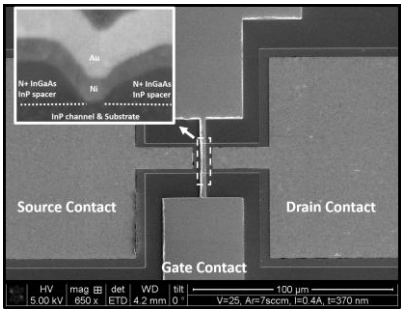

Fig. 3 Top view and cross-sectional SEM image of a device having ~40 nm L_g.

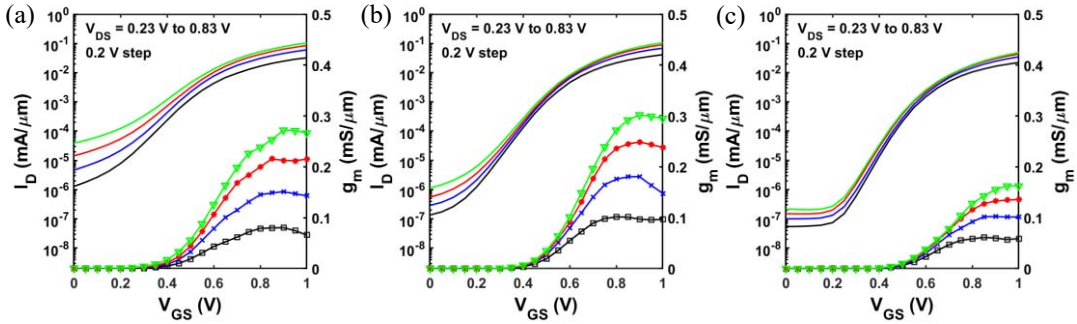

Fig. 4 Subthreshold characteristics and transconductance g_m vs. V_{GS} for L_g = 40 nm (a); 100 nm (b); 1 μm (c) FETs.

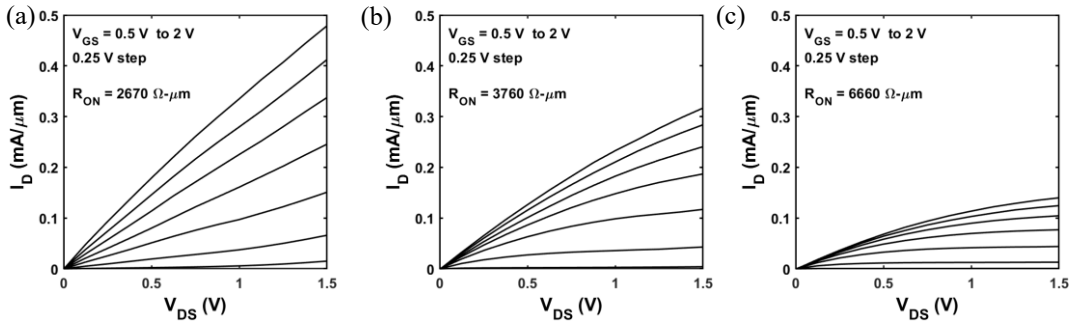

Fig. 5 Output characteristics for L_g = 40 nm (a); 100 nm (b); 1 μm (c) FETs.

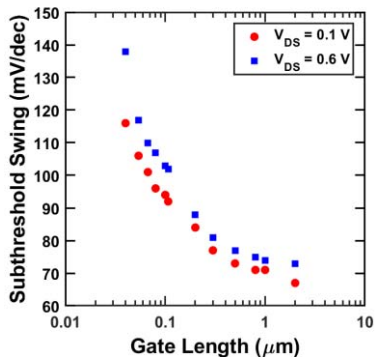

Fig. 6 SS vs. L_g .

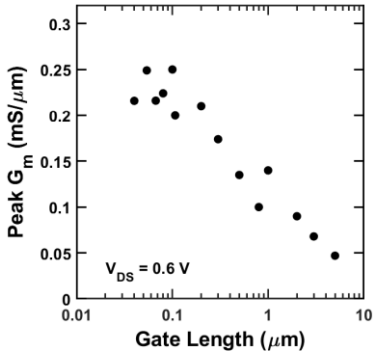

Fig. 7 Peak g_m vs. L_g .

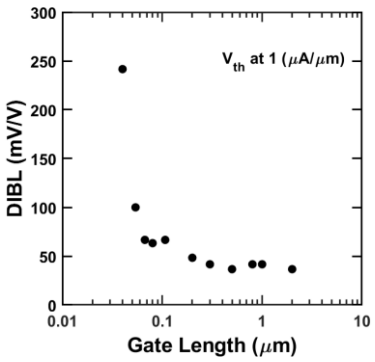

Fig. 8 DIBL vs. L_g .