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ABSTRACT

Selectively growing epitaxial material in confined dielectric structures has been explored recently as a pathway to integrate highly mismatched materials on silicon substrates. This approach involves the fabrication of a channel-like structure of dielectric material that from the growth atmosphere reaches down to a small exposed area of the substrate where subsequent growth via metal organic chemical vapor deposition (MOCVD) initiates. The technique, referred to as template assisted selective epitaxy, can also enable the development of novel nanoscale photonic and electronic device structures because of its ability to allow epitaxy to progress in a direction, final size, and aspect ratio defined by the dielectric template, and allows integration of horizontal heterojunction inside the channel. To date, most confined epitaxy work has been detailed on silicon. Due to the reduced chemical and thermal stability of InP compared to Si, additional steps for surface preparation are required. In this work, two different fabrication routes are described on InP substrates: one involving amorphous silicon as a sacrificial layer and deposited SiO_2 as top oxide, while the other involves spin coated photoresist and hydrogen-silsesquioxane sourced SiO_x. Both routes, leading to similar template structures, are demonstrated and discussed. Homoepitaxy of InP in both types of templates and the integration of an InAs horizontal heterojunction are demonstrated via MOCVD. An increase in growth rate with decreasing template length, increasing template width, and decreasing pattern density is observed.

I. INTRODUCTION

Recently, there has been interest in template assisted selective epitaxy (TASE) as a technique to integrate highly lattice-mismatched materials. TASE is a type of selective area growth (SAG) that involves epitaxial growth of semiconductor materials within a confined structure that is formed with patterned dielectric materials.[1] Gas phase precursors enter the confined structure through a "source hole" and are exposed to an area of the semiconductor substrate, referred to as a "seed," where growth selectively initiates. The confined nature of the growth enables known defect trapping mechanisms characteristic of high aspect ratio structures, thereby enabling heteroepitaxy.[2]

Early confined growth was investigated in Refs. 3 and 4 for silicon on insulator (SOI) applications, but limited devices were fabricated and the technique was not widely adopted.[3–5] More recently, IBM Research has demonstrated the integration of group III-V materials on silicon with TASE, sometimes also referred to as confined epitaxial lateral overgrowth (CELO).[1,6] Published results detailing TASE devices include MOSFETs,[1,7,8] tunnel field effect transistors (TFETs),[8,9] and gain material for lasers.[10] Limited studies regarding growth dynamics and template effects for TASE on Si have been published.[11–13] Additional work has leveraged TASE for defect trapping to grow GaN and has explored effects on a submicrometer scale using templates with a cavity thickness <0.2 μm.[14,15]

The technique, however, could also be leveraged to envision novel III-V nanoscale devices. TASE can rotate the direction of growth from vertical, typical of planar epitaxy, to being parallel with the substrate. Arbitrary orientation of the template allows subsequent growth to occur in a direction defined by the template and to a predetermined final size and aspect ratio. It would then be possible to exploit the anisotropy of the energy bands in III-V semiconductors to design devices in such a way that electrons are confined in a specific crystal direction while transport would occur in another direction. If at the growth front inside a TASE template we also were to find a flat, vertical facet, then heteroepitaxy would result in a horizontal heterojunction (HJ). Horizontal HJs in turn would benefit efficiency as is shown in high efficiency heterojunction (HJ) based devices,[16–20] while enabling simple planar gating. Studying homoepitaxy via TASE becomes then of interest to explore if this is possible. This work is focused on TASE in micrometer templates, with homoepitaxy of InP, which has seen limited published work in the literature.[21] Fabrication on InP substrates experiences additional process constraints compared to on-Si, with lower thermal and chemical stability. Here, two methods of fabricating horizontally oriented structures on InP substrates are explored. Particularly, a new process that does not include an amorphous Si (a-Si) sacrificial layer is detailed, allowing for etch damage due to the a-Si removal to be avoided. Additional process constraints for TASE on III-Vs are also included. Growth via metal organic chemical vapor deposition (MOCVD) of InP is executed on both types of templates, with good selectivity, and is characterized via scanning electron microscopy (SEM) and transmission electron microscopy (TEM). The reported results show an increase in growth rate with decreasing template length, increasing template width, and decreasing pattern density.

II. MATERIALS AND METHODS

A. Template fabrication

Templates of varying sizes were fabricated on (100) and (110) InP 2 in. wafers by two general methods. These two methods share some initial fabrication steps and then differ in the materials and deposition techniques used for the sacrificial layer and top dielectric. Both begin with an Al_2O_3 etch stop layer followed by a plasma enhanced chemical vapor deposition (PECVD) SiO_2 layer. Openings in the SiO_2 layer were then patterned by electron beam lithography (EBL) and inductively coupled plasma etched (ICP) in $CHF_3/CF_4/O_2$ exposing the small area of the InP, the "seed," where growth will selectively initiate.

Following this, a sacrificial layer was either deposited or spin coated and then patterned to define what will become the growth cavity. Finally, a top dielectric was either deposited or spin coated and patterned, exposing the sacrificial region to then be selectively removed. Specific details of each fabrication technique and their effects on growth are discussed later.

B. Growth via MOCVD

Processed wafers were diced into $7 \times 7\,mm^2$ samples, each containing four die and allowing for >1 mm of edge exclusion. Immediately before loading into the growth chamber, samples were dipped in 0.3% HF for 10 s and rinsed with DI water.

Metal organic chemical vapor deposition (MOCVD) was done in a horizontal reactor using trimethylindium (TMIn), tertiarybutylphosphine (TBP), and H_2 as carrier gas. Various growth pressures were explored in initial trials, ranging from 50 Torr to 350 Torr, showing an increase of selectivity with decreasing pressure. Acceptable growth selectivity was obtained with pressure $P = 50$ Torr and temperature $T = 580$–$640\,°C$ as measured with a thermocouple at the susceptor. The molar flow of TMIn was 1.3×10^{-6} mol/min for the initial 500 s of growth and then increased to 2.7×10^{-6} mol/min using a V/III ratio of 400. An *in situ* anneal was conducted before growth and consisted of two steps: 350 °C for 10 min in a hydrogen atmosphere, followed by 10 min at 660 °C under both hydrogen and TBP to avoid group V desorption from the InP surface.

C. Characterization

Scanning electron microscopy (SEM) was used to determine the success and amount of growth in the template as well as an initial estimate of crystal quality. The top oxide, while present, is thin enough to allow electron penetration and enough contrast between growth and empty cavity (Fig. 1).

Cross section transmission electron microscopy (TEM) images were taken after thinning down a lamella from the center of the template, to include the "seed" and the initial growth interface (Figs. 2 and 5). The samples were capped with sputtered Ir and Pt prior to milling. The TEM lamella thickness was ~100 nm. The samples were imaged at 200 kV in bright-field (BF) TEM mode, and high-resolution (HR) TEM mode.

III. RESULTS AND DISCUSSION

A. Template process

1. Dielectric mask (bottom oxide)

In this work, the fill factor (unmasked over masked area) is very low (<1%) compared to typical non-TASE selective area growth (SAG), enhancing the risk of parasitics (i.e., nucleation on the dielectric mask). Because growth inside the cavity occurs more slowly than growth on the surface, any parasitic will grow much faster than the desired confined growth. This fast surface parasitic growth impairs characterization and further processing. Additionally, it locally consumes precursors which changes the conditions inside nearby templates and renders control of the desired confined growth difficult. To minimize this, it is important to select dielectrics that provide the best growth selectivity/lowest sticking coefficient.

Thermal SiO_2, seen in previous TASE literature is not possible on non-Si substrates and thus deposited oxides must be used. Deposited oxides, however, are not stoichiometric which results in a wide range of sticking coefficients. In order to choose among the available oxides, InP growth trials were done on unpatterned substrates using typical SAG growth parameters and then characterized by SEM to compare parasitic nucleation. Plasma enhanced chemical vapor deposition SiO_x exhibited the lowest density of parasitic nucleation and was thus chosen for all future templates.

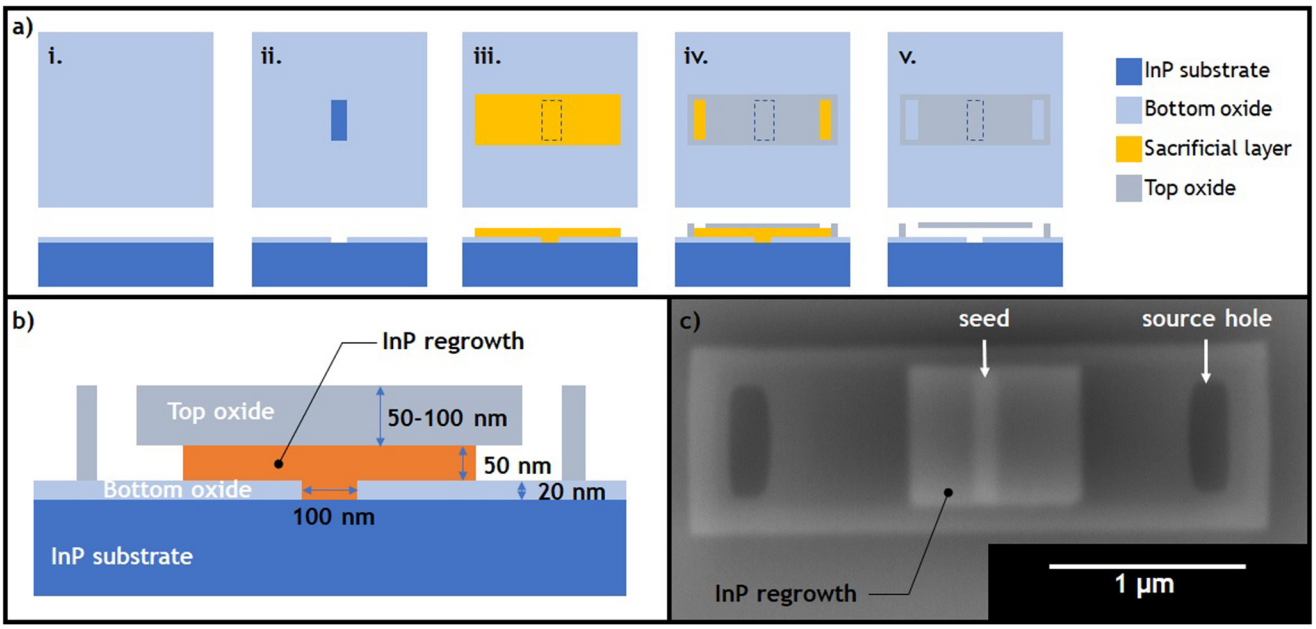

FIG. 1. (a) Illustration of general template fabrication. (b) Illustration of cross section of template after growth. (c) Top down SEM image of template after homoepitaxy of InP. The contrast allows seeing the seed location, the confined lateral overgrowth, and the unfilled cavity.

Oxide patterning must be considered to expose the "seed" areas of the. Silicon oxide is generally dry etched in fluorine chemistries and wet etched using hydrofluoric acid (HF). However, for VLSI relevant scaling, wet etching causes pattern size to be at least equal to twice the bottom oxide depth and thus dramatically reduces lateral spatial resolution and packing density. Dry etching is thus preferred; however, etching through SiO_x in fluorine chemistry will eventually expose InP to fluorine plasma, which will form nonvolatile InF_x, which is difficult to remove and known to be detrimental to growth initiation. In fact, exposing InP to any ion-energy damages the surface impairing epitaxy. While process induced damage can be removed by etching InP, it was found that 1–5× digital etch cycles (15 min UV-ozone +60 s 1:10 HCl) was not enough to sufficiently recover the surface. An $HCl:H_3PO_4$ 1:4 etch was attempted as well but found to cause severe undercutting of the seed hole, which can then trap later process materials. Cooling the $HCl:H_3PO_4$ solution to 6 °C reduces the etch rate and provided additional control but still resulted in a significant undercut. To eliminate this, a 3–5 nm atomic layer deposition (ALD) Al_2O_3 layer was used as an etch stop to protect the critical growth interface from

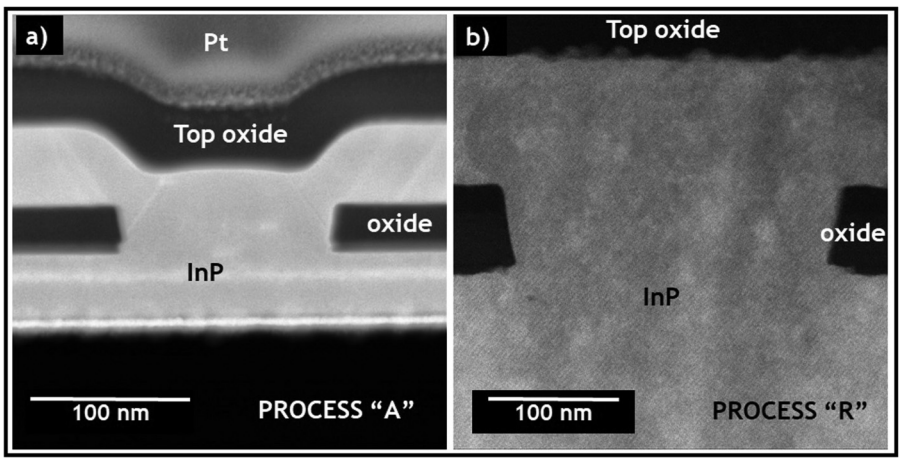

FIG. 2. TEM cross section images of TASE cavities with homoepitaxy of InP fabricated by (a) process A, where a dimple is present above the seed due to semiconformal deposition of a-Si. (b) Process R, where no dimple is present due to planarization via spin coating. Additional roughness in top oxide likely due to intermixing of CSAR and HSQ.

damage and selectively removed with tetramethylammonium hydroxide (TMAH) as the last step of the fabrication process.

2. Sacrificial layer

Choice of the sacrificial layer is critical because it must be selectively removable and, ideally, leave behind no residue or chemical modification of adjacent surfaces. Two materials were considered, each requiring a slightly modified fabrication process. Similar to Ref. 7, a-Si was investigated and, dissimilarly, the electron beam resist CSAR-62 was also investigated. We will refer to these as process A (a-Si sacrificial layer) and process R (photoresist sacrificial layer).

For process A, prior to a-Si removal, an oxide densification anneal >700 °C is useful to improve etch selectivity of a-Si/SiO_x in XeF_2. While achievable when using silicon substrates, annealing InP substrates at high enough temperatures would be impossible even with a phosphorus overpressure. Without an anneal, it was found that the XeF_2 modifies the oxide surface enough to cause severe parasitic nucleation during epitaxy. Recovering the surface damage, and thus selectivity, is although possible with an additional dilute HF dip that removes ~2–5 nm of oxide prior to growth. This has to be taken into account to avoid excessive thinning of the template sidewalls that could lead to mechanical failure.

For process R, CSAR, a common EBL resist was selected as the sacrificial layer. Deposition of this resist is done via routine spin coating. The roughness was evaluated by AFM after development and found to have an RMS of ~0.55 nm. The CSAR was finally removed in NMP-Rinse at 80 °C for 2 h, followed by a 3 min treatment in remote oxygen plasma at 350 °C. This resist based sacrificial layer did not show adverse effects on growth selectivity during SAG trials.

3. Template structure (top oxide)

Using the same material, PECVD SiO_2 for both bottom and top dielectric is possible in process A, but for process R, because PECVD is often done at temperatures $T \geq 250\,^{\circ}C$, concerns about organic contamination of the deposition chamber led us to choose hydrogen-silsesquioxane (HSQ) instead. By eliminating dry etch steps, the process time was reduced, however at the expense of additional EBL time due to the large (~1000 $\mu C/cm^2$) exposure dose of HSQ. By using HSQ and an expose/develop process rather than an etch process to form openings in the top oxide, a true "bridge" is realizable over the sacrificial layer. Dry-etching openings in process A leaves a sidewall and/or an additional "corner" for the MOCVD precursors to traverse.[11] Spin coating the CSAR sacrificial layer in process R also leads to planarization of the surface, eliminating the depression that typically forms above the seed by the semiconformal a-Si deposition of process A as shown in Fig. 2. Because sidewall deposition rate is often less than the normal deposition rate (in this case ~0.5×), this dimple behaves as a pinch point for gasses during the critical growth initiation and becomes more pronounced for thin cavities. One of the downsides of using HSQ over the spin coated CSAR is the resist intermixing that occurs at the interface. As observed in Fig. 2, the ceiling of the template is significantly rougher in process R than in process A, higher than what is measured on the spin coated CSAR only (0.55 nm RMS via AFM). We have not seen evidence of additional parasitic nucleation due to this roughness, but it is possible for it to induce additional crystal defects such as stacking faults during epitaxy, so additional material quality studies are desirable. In order to ensure that the HSQ itself properly planarizes, it is important that the HSQ is ~2× thicker than the underlying CSAR. This both limits the maximum cavity thickness and forces fairly thick top oxides. Other than that, processes similar to manufacturer recommended processes for both resists are used.

Completed templates were measured by AFM prior to and after growth to understand if a thermal cycle deforms the templates and "pinches" the cavity. Figure 3 shows the slight positive bowing of process R cavities prior to growth and negative bowing postgrowth—dependent upon the box width. The grown film was also measured after removing the oxide and exhibits similar bowing to the cavity suggesting that the template bows early in growth, likely during the initial heat up of the MOCVD chamber. Cavities formed by process A do not exhibit a significant change in bowing during growth. Because curing HSQ at $T > 600\,^{\circ}C$ induces compressive stress of −100 MPa[22] and the PECVD SiO_x has measured compressive stress of −250 MPa, the observed bowing in HSQ is unlikely due to stress. It has been reported that HSQ films shrink by >20% at $T > 600\,^{\circ}C$.[22] Additionally,

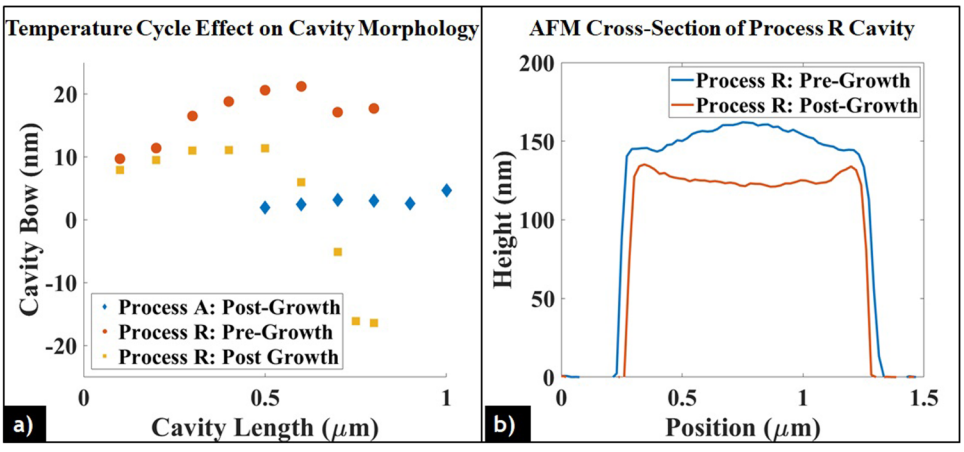

FIG. 3. Cavity bowing in process A and R templates measured by AFM (a) before and after growth as a function of body width and (b) AFM cross section perpendicular to growth direction at template center for 0.80 μm wide cavity before and after growth.

TABLE I. Summary of major benefits and limitations of the template fabrication processes.

	Process A	Process R
Growth selectivity	Good (with DHF dip)	Good (with *in situ* anneal)
Depression at seed	Present	Absent
Cavity thickness	Best for thick cavities Lower limit set by depression at seed	Best for thin cavities Upper limit set by resist processes
Cavity roughness	Low	High due to resist intermixing
Cavity width	High	Limited to <0.5 μm

when the width is >1 μm HSQ, boxes often become disconnected from the underlying oxide during development and CSAR removal, suggesting poor adhesion or pronounced mid-range electron scattering effects common in both InP and HSQ processes. So thermal properties, in conjunction with poor adhesion, suggest that the downward bowing is likely due to expansion/contraction of HSQ cavities on the oxide surface during growth. In conclusion, both process A and process R have benefits and downsides, summarized in Table I, which have to be considered.

B. Epitaxial growth

A V/III ratio of 400 was chosen which is high compared to typical MOCVD growth but is justified by some considerations. A morphological dependence of TASE growths on V/III ratio has been reported.[11,23] Additionally effective V/III ratio has been inferred to be lower deeper within a template.[11,23] As growth progresses, the template fills with grown material and the length of the remaining cavity is effectively shortened. As a result, the effective V/III ratio at the growth interface increases. A high V/III ratio is thus chosen to prevent local growth conditions at the growth interface from changing significantly with the progression of growth.

In the case of process R templates, significantly less unwanted parasitic nucleation was observed at template edges if the *in situ* anneal, as described in part III-B, preceded growth. It is possible that the HSQ is not fully transformed into SiO_2 at pattern edges, presenting either hydroxyl or other residual organic groups that can act as nucleation sites and are removed or saturated during the anneal.

After epitaxy, growth length was measured from the center of the seed to the growth front on either side and averaged. It is to be noted that while seeded growth occurs with 100% yield, not all templates are filled symmetrically. Possible residues from template fabrication at the growth seed have sometimes been observed to affect growth initiation and, consequently, final grown length.

To explore growth behavior on different crystal directions, templates were fabricated in two different orientations, rotated 90° from each other. When using (100) substrates, this results in cavities aligned along ⟨100⟩; when using (110) substrates, this results in cavities aligned along [010] and [−110]. Observing the grown material after MOCVD reveals how, even across identical templates, the growth front can present different crystal planes, with some templates showing single-faceted growth while others multifaceted. This is true for both (100) and (110) substrates. The yield of a specific facet though is influenced by growth conditions.[11] Notably, in this work, when using templates fabricated onto (110) wafers, in cavities developed along the [−110], we commonly observe flat vertical (−110) and (1−10) facets, as shown in Figs. 4 and 1(c). Having vertical facets normal to the direction of growth is of interest because it allows for the formation of horizontal HJs grown directly inside the cavity. This in turn could enable novel electronic and photonic devices.[16,19] The yield of this specific facet is primarily temperature related, appearing at 580–610 °C and disappears, favoring {111} facets, at higher temperatures. Shown in Fig. 5 is an initial result of 2 nm thick InAs HJ grown directly inside the channel, achieved in a single-step growth.

C. Growth rate vs length

As alluded above, the geometry of the templates affects the growth rate of the confined material. Because MOCVD growth rates are determined by diffusion of precursors to the growth surface, it is conceivable that template geometry and packing density could be used to tune growth length and/or composition

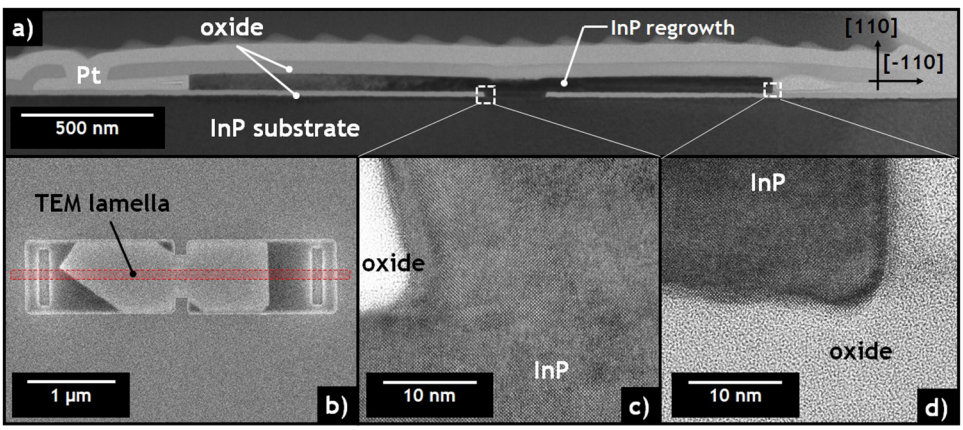

FIG. 4. Early InP homoepitaxy via TASE with a process A template. (a) Cross-sectional TEM. (b) Top view SEM of the TASE structure showing where the TEM lamella is taken. Inconsistency between the left and right facet can be observed. (c) HR-TEM at the initial growth interface. (c) HR-TEM at the growth front terminating on vertically oriented (−110) facet.

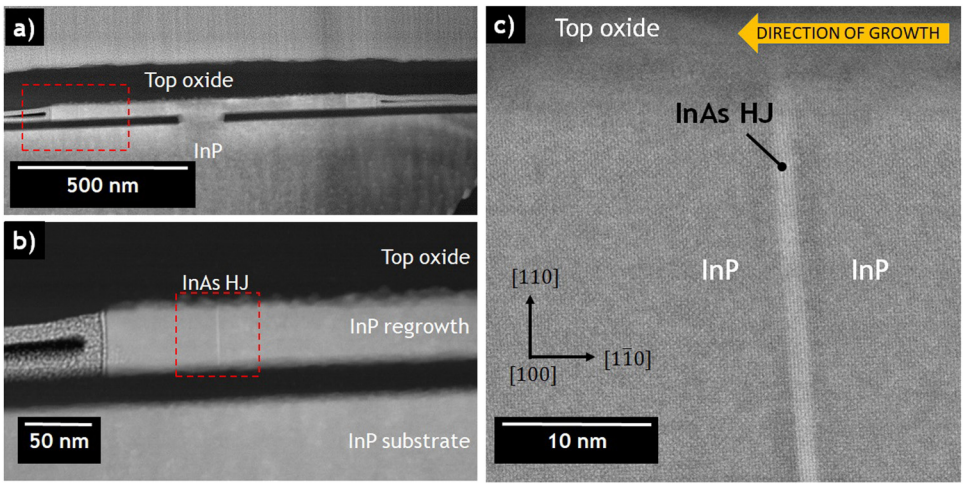

FIG. 5. Cross-sectional TEM at different magnifications of InP TASE with the inclusion of an InAs heterojunction. (a) and (b) BF-TEM imaging. (c) HAADF-STEM detailing the InAs HJ. The interface between the InP and the InAs looks abrupt and crystallinity is preserved.

across a wafer in a single growth. The effects of template width, length, thickness, and packing density were studied.

Because metal organic chemical vapor deposition (MOCVD) growth is generally limited by mass transport of precursors,[24] it is expected that in the case of high aspect ratio structures, the template geometry will directly affect growth rate.

An effect of template length on growth length was observed in both processes A and R templates. The length of the grown material inside the template was compared for structures of varying lengths, ranging from 2 μm to 4 μm, all simultaneously present on a die, with width and thickness fixed (Fig. 6). It was observed that the growth rate decreased as the template length increased. This growth rate reduction could be intuitively explained by the need for precursor material to cover longer distances, measured from the source hole to the growth front, to initiate/continue growth. The source hole is located at the sample surface where diffusion is dominated by lateral gas phase diffusion driven by partial pressure gradients, typical of SAG.[25] However, this pressure gradient might be diminished or absent at the growth front deep inside the template, as finite element simulations for other TASE growth suggest.[11]

D. Growth rate vs template width

Growth in templates of identical length but varying widths, ranging from 150 nm to 550 nm, was also conducted and exhibited an increase in the growth rate with increasing template width (Fig. 6). It should be noted that while all other template parameters are kept constant, the width of the source hole increases with the width of the template, thus allowing more precursors to reach the wider growth interface.

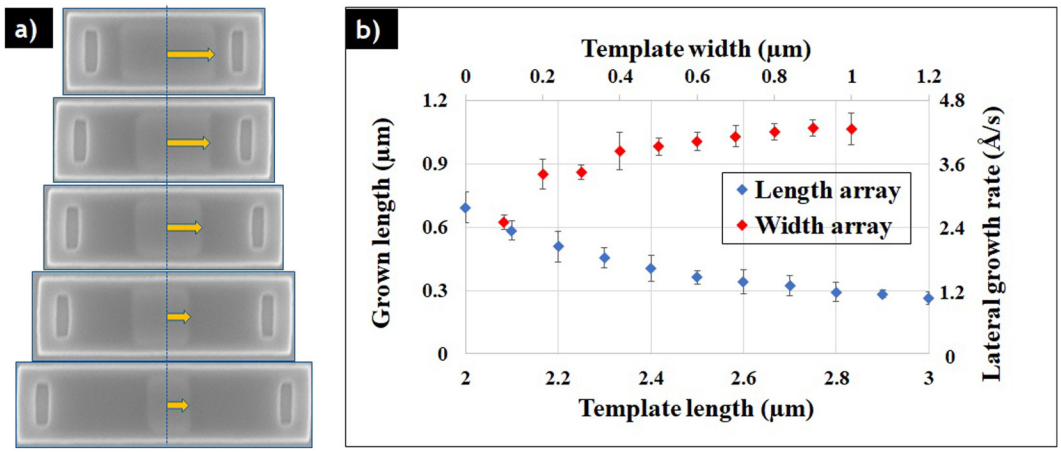

FIG. 6. Effect of cavity dimensions on growth rate. (a) Representative example of cavities of increasing length, exhibiting reduced growth in longer cavities. The arrows guide the eye to the growth front. (b) Growth length in cavities of varying width (L = 1.0 μm) and length (W = 0.35 μm). Each point is the average of 10–15 templates. Error bars show standard deviation.

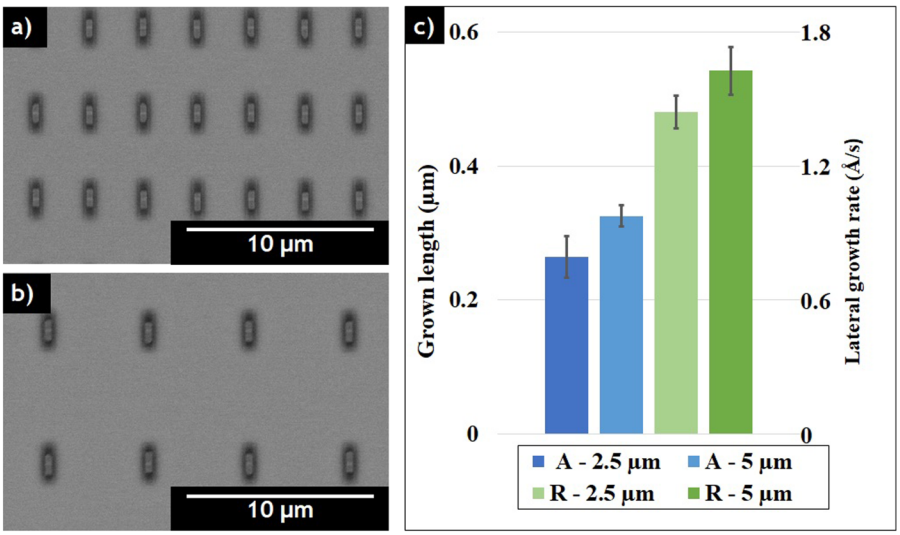

FIG. 7. Top down SEM images of process R TASE structures spaced by (a) 2.5 μm and (b) 5.0 μm. (c) Average growth length in cavities fabricated by techniques A and R where the widths of templates by the respective processes are W = 0.75 μm and W = 0.35 μm as process A can sustain wider templates without bowing.

E. Growth rate vs density of pattern

Identical templates (0.35 μm wide and 1 μm long) separated by 2.5 μm and 5 μm from template edge to edge, present on the same die, are shown in Fig. 7. For identical size template patterns, the growth rate decreases with increasing packing density (i.e., decreasing pitch/separation). This is expected considering loading effects present in SAG which causes growth rate enhancement as the masked/unmasked area ratio increases. It has been previously reported that TASE showed no change in growth rate with pattern density[11] where transport is dominated by surface diffusion. We note that differences in template geometry could be responsible for the discrepancy and hypothesize that the lower sidewall height in this work, compared to tall nanowire templates in Ref. 11, might allow for lateral gas phase diffusion mechanisms to still be noticeable. This effect could be used as an engineering tool to produce devices of different sizes or composition on the same wafer, simply by tuning template geometry.

IV. CONCLUSION

In this study, InP homoepitaxy was conducted by MOCVD using TASE. The effects of the template fabrication method, template geometry, and growth temperature were investigated. Templates were prepared on both (100) and (110) InP substrates using two methods, one of which is novel. The novel template fabrication method uses spin coated resist for both its sacrificial layer and the top oxide that defines the templates. This allows for planarization of the sacrificial layer and avoids a "dimple" at the seed while presenting a rougher ceiling due to resist intermixing and placing some limits on template size due to mechanical stability. After MOCVD epitaxy, it was found that both geometry and fill factor affect the growth rate: shorter, wider, thicker cavities enhance the growth rate, while longer, narrower, thinner cavities depress the growth rate. Growth parameters have been found that yield vertical {110} facets, when grown on (110) substrates, in templates oriented toward ⟨110⟩. This vertical faceting within TASE cavities could be exploited for horizontal heterojunction-based devices. To show this, an InAs horizontal heterojunction was demonstrated via single-step growth. This shows that TASE offers an interesting route to produce novel electronic and photonic structures as well as to cointegrate lattice-mismatched materials. However, careful attention must be paid to template fabrication and growth parameters in order to yield quality laterally overgrown material.

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