A 200mW D-band Power Amplifier with 17.8% PAE in 250-nm InP HBT Technology

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***Abstract* — We report a compact and high efficiency D-band power amplifier in 250nm InP HBT technology. A compact and low loss 8:1 transmission line power combiner is demonstrated. The three-stage power amplifier combines 8 capacitively linearized common-base power cells. The amplifier has 23dBm peak power with 17.8% power added efficiency (PAE) and 16.5dB associated large-signal gain at 131GHz. At 131GHz, the small-signal gain is 21.9dB. The small-signal 3dB-bandwidth is 125.8-145.8GHz. Over the 127-151GHz bandwidth, the saturated output power is greater than 22.3dBm with greater than 15% associated PAE. The amplifier occupies 1.34mm² die area and consumes 1.1W DC power. To the authors' knowledge, this result improves the state of the art peak PAE at 131GHz by 2.5:1 for comparable saturated output power.**

***Keywords* — D-band, millimeter wave, high efficiency, power amplifiers, 250-nm InP, low loss, compact, transmission-line combiner.**

I. INTRODUCTION

100-300GHz wireless systems benefit from wide available spectrum, while the short wavelengths facilitate large MIMO arrays simultaneously radiating many signal beams for high total high capacity. Unfortunately, at 100-300GHz, free space (λ^2/r^2) path loss and weather attenuation are high. High-capacity outdoor 100-300GHz systems may thus require ~100mW power amplifiers [1]. Above 100GHz, CMOS amplifiers have limited output power [2] while reported SiGe amplifiers have higher output power but relatively low efficiency ([3]-[5]). GaN has high output power to 120GHz, but efficiencies are generally limited ([6], [7][6]). To date, above 120GHz InP HBTs [8] demonstrate a superior combination of output power, efficiency, and bandwidth ([9]-[12]).

Output power is increased by combining. Though successful at lower frequencies, series combiners are challenging to design at higher mm-wave frequencies [9]. Parallel combining, using transmission lines networks, is more easily implemented at D-band. Though Wilkinson combiners [10] have wide bandwidths, at the expense of reduced bandwidth, more general corporate transmission-line combiners can be designed for lower losses and smaller die area, ([3], [4], [12]).

Here we report a compact, highly efficient D-band power amplifier. The amplifier uses a compact, low loss 8:1 power combiner, and capacitively linearized common-base power and driver cells. At 140GHz, the amplifier has 22.8dBm saturated output power with 16.7% PAE and 16.1dB associated gain. At 140GHz and 1dB gain compression, the output power is 20.2dBm with 9.4% PAE and 20.3dB associated gain. The peak saturated output power is 23dBm with 16.5dB associated gain and 17.8% PAE at 131GHz. Over 127-151GHz, the saturated output power is greater than 22.3 dBm with greater than 15% associated PAE. The amplifier consumes 1.1W DC power and the die area is 1.34mm².

II. POWER AMPLIFIER DESIGN

A. Technology Description

ICs were fabricated in the Teledyne 250nm InP technology [8], which has four Au interconnect layers, 0.3fF/µm² MIM capacitors and 50Ω/square thin film resistors. The HBT has a maximum 650GHz power gain cut-off frequency (f_{max}), a maximum 3mA/µm current density and 4.5V BV_{CEO}.

B. Power and Driver Cells Design

We recently reported a design comparison between common emitter (CE) and capacitively degenerated (Fig. 1) common base (CB) stages [12], the latter using a significant capacitive reactance between the base and ground, this reducing the gain. Under optimum load termination for maximum saturated output power, and independent of the value of the base capacitive reactance, the saturated (peak) PAE of the CB stage is identical to that of the CE stage [12]. However, decreasing the base capacitance C_E reduces the fractional variation of the input impedance $Z_{in} \cong kT/qI_E+(\tau_b+\tau_c)/C_E$ with variations of the

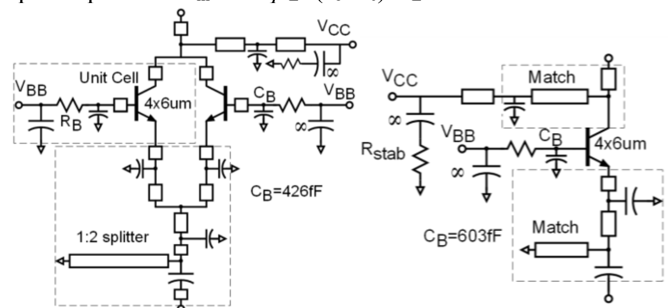


Fig. 1. Schematic diagram of: a) two combined power amplifier cells. The pair of power cells are driven by a single driver cell. b) driver cell with input and output matching networks.

emitter current I_E over the RF signal cycle. This linearizes the stage and thus increases the output power and PAE at 1dB gain compression. The base capacitive reactance also improves the CB stability factor. The external base resistance provides stable control of the DC collector bias current only a slight increase in DC power. The driver and power cells are similar to [12]; two power cells, each having 4 emitter fingers of 6µm length, share a common shunt inductor that tunes the transistor collector-base capacitances. Once C_{cb} is shunt-tuned, each 4×6µm cell requires a 50Ω load for optimum PAE. To sustain high PAE, each pair of output stages is driven by a stage having 4 emitter fingers of 6µm length.

The two cascaded driver stages (Fig. 1b) have similar design. The input and output tuning networks are stagger-tuned to broaden the amplifier bandwidth. For increased gain, these stages use a larger base capacitance than the output stage. To reduce design effort, the first stage uses the same 4×6µm transistor cell as the second stage; overall amplifier PAE could have been slightly improved by using smaller transistors, with a correspondingly smaller DC bias current, in the first stage. MIM capacitors isolate DC bias between stages. All matching circuits and interconnects are simulated by ADS momentum and verified by HFSS.

C. Low Loss Transmission Line Combiner

The output power combiner must be low-loss for high PAE and compact for small die area. Wilkinson combiners [10] are broad bandwidth, but an 8:1 Wilkinson combiner requires 14 transmission-lines, each having $\lambda/4$ length and Z_0=71Ω. This requires substantial die area. The high-impedance lines are narrow, limiting the maximum current. Losses are high because the signal must propagate through three cascaded narrow hence lossy $\lambda/4$ lines. At the expense of narrower bandwidth, abandoning the Wilkinson design permits the transmission-line combiner to be designed for less loss and a smaller die. In [12] we demonstrated a 4:1 combiner with low loss, simulated 0.92dB including shunt inductive tuning of C_{cb} but not including probe pad losses. Here, the combining ratio is increased to 8:1, yet low low loss is maintained, simulated 0.98dB including shunt inductive tuning of C_{cb} but without probe pad losses. The resulting amplifier has nearly 2:1 greater output power than [12] yet maintains a similar high PAE.

Fig. 2a shows the combiner. For clarity, the shunt inductive lines tuning C_{cb} are not shown. For the first combining level, short 50 Ω transmission line sections (TL_1) combine the outputs of two 4×6µm cells. The required load impedance for each cell (Z_1) is 50Ω while the required load impedance (Z_2) for two parallel cells combined by TL_1 is 25Ω. The impedance transformation does not depend on the lengths of TL_1 and TL_2, hence these lengths are minimized for smallest losses. Four combined cells require a load impedance (Z_3) of 12.5Ω, this achieved by a $\lambda/4$ transmission line (TL_3) having $25\times\sqrt{2}\ \Omega$ characteristic impedance. Die area is reduced because only two $\lambda/4$ lines are required. Losses are reduced because TL_3 is wide, and because the signal passes through only a single $\lambda/4$ line, though these improvements are slightly offset by the increased loss associated with the high VSWR on TL_3. The wide lines permit high currents. In simulations (Fig. 2c), the proposed 8:1 combiner, without shunt elements, has a loss of 0.63dB at 140GHz, compared to 0.96dB for the 8:1 Wilkinson combiner, without shunt elements, (Fig. 2b). The loss remains smaller than that of the Wilkinson over a 47.5GHz bandwidth.

The power amplifier is designed to be packaged. A dense array of through-substrate vias (TSVs) provides a low-inductance connection between the ground planes on the top and bottom surfaces of the IC substrate, as only the latter connects to the package ground system. The TSVs also suppress dielectric substrate modes. The RF I/O pads are relatively large, 55µm×57.5µm, and use all wiring planes to improve pad adhesion during wire bonding. The pad impedance was simulated in HFSS and the line parameters of the output combiner were then adjusted to compensate for the pad parasitics. The final combiner parameters are: TL_3 (17Ω, 90°), TL_2 (23Ω, 17°), TL_1 (61Ω, 7.2°). The total combiner loss including the pad is 1.3dB (0.98dB for series TL and shunt tuning inductors, and 0.32dB for the pad).

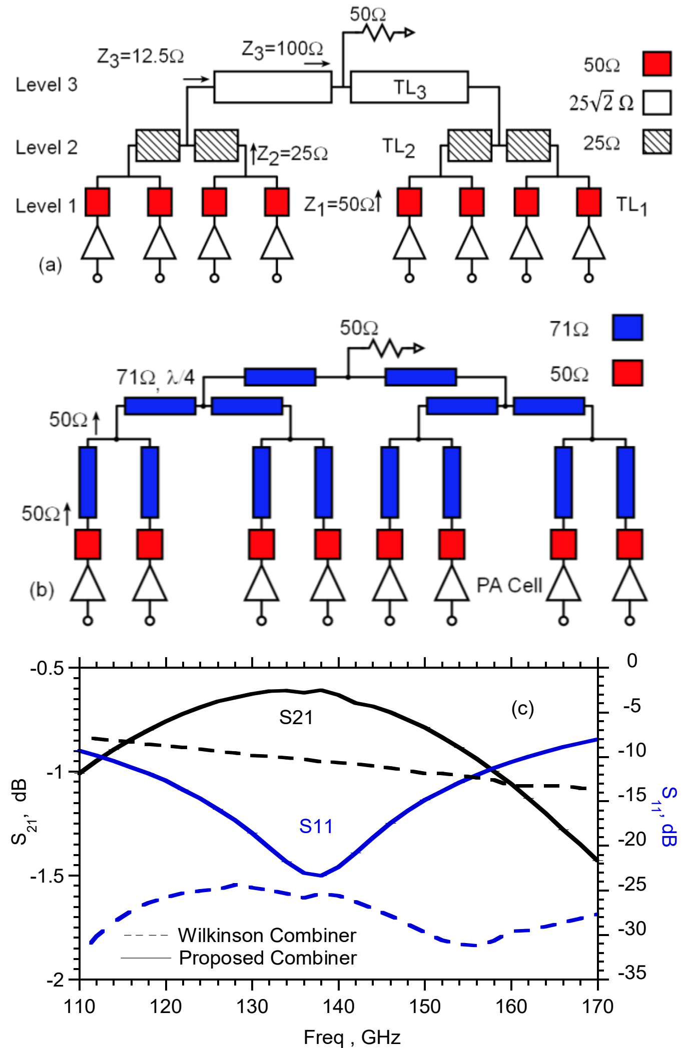
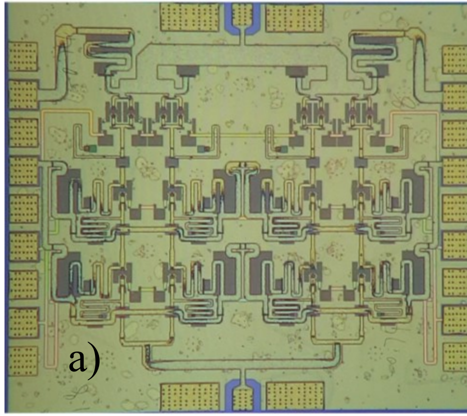


Fig. 2. (a) Proposed 8:1 transmission-line combiner for 50Ω load, (b) an 8:1 Wilkinson combiner (with bridging resistors omitted) and (c) simulations comparing the insertion losses and input reflection coefficients of the two designs.



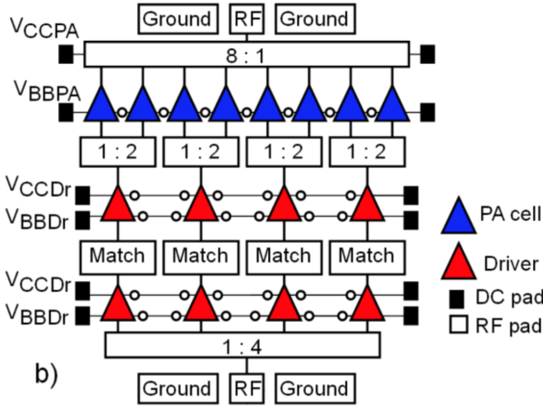


Fig. 3. a) Chip micrograph of the power amplifier. The area is 1.23mm× 1.09mm including the pads. b) amplifier block diagram.

III. Measurement Results

Fig. 3a shows the IC micrograph and Fig. 3b its block diagram. S-parameter are measured using an HP network analyzer with VDI 110-170GHz frequency extenders and 140-220GHz GGB wafer probes with WR-5 to WR-6 waveguide adapters. To avoid driving the amplifier into gain compression, an attenuator is added to the port 1 frequency extender output. This attenuation degrades the network analyzer directivity, producing the small ripples observed in the S11 measurement.

The analyzer was calibrated to the probe tips using SOLT standards on an external CS-15 calibration substrate. DC bias was provided to the DC pads on both sides of the IC die to minimize *IR* drops. The DC probes have bypass capacitors

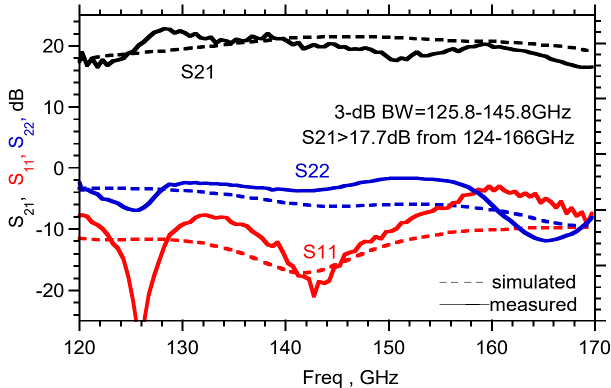


Fig. 4. Measured (solid) and simulated (dashed) S-parameters

mounted near the probe tips to suppress supply-induced oscillations. Identical bias conditions are set for the two driver stages (V_{CCDr}=2.43V, V_{BBDr}=1.5V, I_{CCDr}=221mA, I_{BBDr}=8.6mA) while the output stage is separately biased at (V_{CCPA}=2.43V, V_{BBPA}=1.5V, I_{CCPA}=221mA, and I_{BBPA}=9mA). The peak small signal gain (Fig. 4) is 22.8dB at 128.3GHz while S21 is flat within 3dB between 125.8-145.8GHz. The amplifier is designed for maximum saturated output power which differs, by necessity, from gain matching, resulting in poor S_{22}.

Large-signal power characteristics were measured on the 3-mil-thick die without any external cooling. The input signal source is a 110-170GHz VDI frequency extender, with ~10dBm output power, followed by a variable attenuator. The output is measured by an Eriksson power meter. Losses of the D-band probes were separately measured, and the reported data is corrected for the probe losses.

The driver stages have V_{CCDr}=2.43V, V_{BBDr}=1.41V, the total driver collector current I_{CCDr}=212mA, and the total driver base current is I_{BBDr}= 7.7mA. The output stage is biased separately, with V_{CCPA}=2.65V, V_{BBPA}=1.41V, the total collector current I_{CCPA}=219mA and the total base current I_{BBPA}=8mA. Fig.5 shows the power measurement at 140GHz. At each RF drive level, the base bias voltages are adjusted to keep constant the

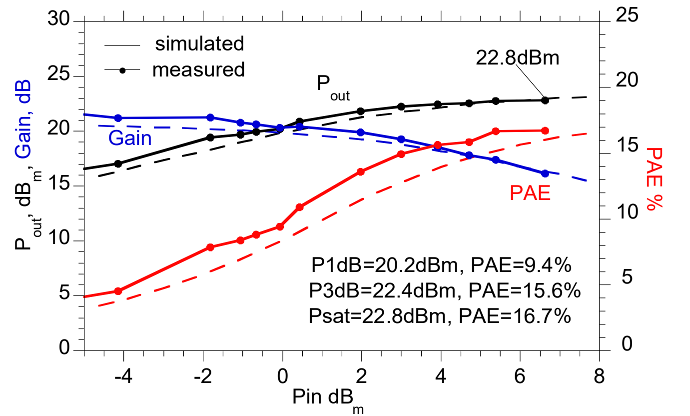


Fig. 5. Measured and simulated output power, PAE, and gain versus the input power at 140GHz.

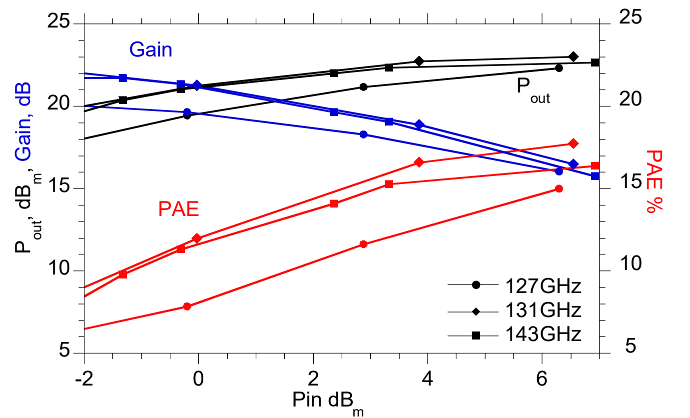


Fig. 6. Measured P_{out}, PAE, and gain versus the input power at 127, 131, and 143GHz.

collector bias currents, with values as stated above. At 140GHz, the saturated output power is 22.8dBm with 16.1dB associated gain and 16.7% PAE. The amplifier OP_{1dB} is 20.2dBm with PAE=9.4% and 20.3dB associated gain. Fig. 6 shows the power measurement at different frequencies and Fig. 7 shows the peak PAE, the associated gain, and the output power versus frequency. Over 127-165GHz, the saturated output power is within its 3dB of its maximum at 131GHz.

IV. Conclusion

A high-efficiency, and compact D-band power amplifier has been demonstrated in 250nm InP HBT technology. Eight power cells are combined by a compact and low-loss transmission line network. The number of power cells is doubled compared to [12], resulting in almost twice the output power while maintaining almost the same PAE. Capacitive grounding linearizes the common-base stages, providing increased efficiency at the 1dB gain-compression point. The three-stage amplifier shows 200mW saturated output power with 17.5% PAE at 130GHz. The saturated output power is 20-23dBm from 125-165GHz. Drivers share the same V_{CC} and V_{BB} to reduce the number of pads. However, the PAE will increase by controlling each driver's supply independently or scaling the first driver. Table 3 compares the state-of-the-art D-band amplifiers: PAE is improved ~2.5:1 for amplifiers of comparable saturated output power.

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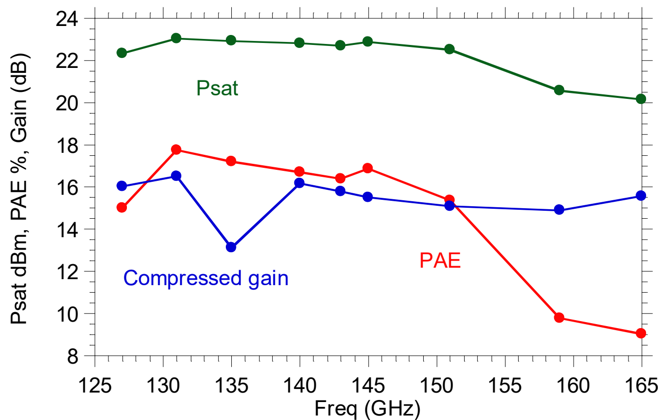

Fig. 7. Measured saturated output power, PAE and the compressed gain vs. frequency

Table 1. Comparison between state-of-the-art D-band amplifiers.

Ref	[7]	[5]	[10]	[12]	This work
Tech.	GaN	90-nm SiGe	250-nm InP HBT		
Freq, GHz	98-122 -	120 130	110-150 131	140 130	**127-151** **131**
P_{sat}, dBm	24.6-27	22 21*	23.2-24 23.8	20.5 19.8	**>22.3** **23**
BW_{3dB} GHz++	11*	35	32.7	43	**20**
Gain at P_{sat} (dB)	12-19*	3* -	14-16 16	15 15.9	**13-16.5** **16.5**
Peak PAE %	14% at 102GHz	3.6 -	5.8-7.0 6.9	20.8 17.1	**>15** **17.8**
Size (mm^2)	6.98	0.62	1.89	0.69	**1.34**
P_{DC} (W)	-	2.2	3.46	0.52	**1.1**
P_{sat}/Area mW/mm^2	124+	254 202.9+	134 126.4+	162 138	**149**

*Graphically estimated, ++small signal bandwidth, +calculated

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