Power Consumption Analysis for Mobile MmWave and Sub-THz Receivers

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***Abstract*—Power consumption is one of the most significant technical barriers for practical millimeter wave (mmWave) communication devices for mobile applications. Communication in the higher mmWave bands above 100 GHz will face even greater challenges. This paper attempts to provide initial power estimates for mobile mmWave devices under realistic parameter values and state-of-the-art device performance characteristics to understand the performance of such systems today and guide research for the future. Power is estimated for a user equipment in a multi-carrier New Radio (NR) system for both a 4×100 MHz system at 28 GHz similar to current 5G deployments as well as a hypothetical 8×200 MHz system at 140 GHz that may be used in future 6G systems. Importantly, the analysis considers power consumption of both the RF front-end components as well as portions of the digital baseband processing. Both analog and fully-digital beamforming are also evaluated.**

I. Introduction

The vast spectrum available in the millimeter wave (mmWave) bands offers the potential for massive throughput and low-latency communication [1], [2] and is now a key component of the 5G New Radio (NR) standard from 3GPP [3]. A key challenge for these systems is power consumption, particularly in handheld and mobile devices. Due to the high isotropic path loss, mmWave systems rely on communication in narrow, electrically steerable beams. To enable the beam steering, front-ends must support large numbers of antennas at very wide bandwidths [4].

In addition, research is now considering transmissions in the higher mmWave bands above 100 GHz [5], sometimes referred as the sub-THz frequencies. Energy consumption in these bands is likely to be an even greater challenge as systems will require support of even wider bandwidths and greater numbers of antenna elements. In addition, as we will see in our analysis, power efficiency for components above 100 GHz remains considerably less favorable than devices in the lower mmWave range.

This paper attempts to provide initial estimates of the power consumption for potential mmWave devices in mobile settings. The broad goal is to assess the feasibility of such devices with current technologies, and identify future areas of research.

To make the analysis more realistic, we consider user equipment (UE) in a 3GPP New Radio (NR) standard [3]. Although the NR standard was defined for 5G systems, the standard is extremely flexible and provides an excellent baseline for 6G evaluation as well. In order to support wide bandwidths expected in the mmWave range, we assume a NR system with carrier aggregation with multiple component carriers [6]. We compare the system with two carrier frequencies: (a) a 28 GHz system with parameters similar to 5G deployments today [7]; and (b) a hypothetical 140 GHz system for potential 6G systems. The 140 GHz band is the most likely sub-THz frequency for future 6G systems [8]. At both carrier frequencies, we estimate the power consumption for a UE receiver under realistic system parameters and state-of-the-art device characteristics. Importantly, unlike previous analyses such as [9], we attempt to estimate the power for both the RF front-end and digital baseband.

One key focus of the study is to compare beamforming architectures, specifically analog beamforming and fully-digital beamforming. To reduce power consumption, most initial 5G commercial systems on mobile devices employ analog phased arrays – see the survey in [10]. Analog arrays typically perform beamforming in the RF chain and require only one mixer and A/D converter per digital stream. While analog beamforming may reduce the front-end power, the systems can only steer in a limited number of directions at a time, greatly reducing the responsiveness of the arrays.

In contrast, fully digital architectures digitize all signals from all antennae and perform beamforming digitally. Fully digital architectures offer dramatically faster search by being able to look in all directions simultaneously [11], [12]. For example, fully digital architectures can reduce the initial access time by an order of magnitude in [13], [14]. Fast search is essential scenarios with high mobility [15], need to support low latency recovery from blocking [16]–[18], and aggressive use of idle and DRX modes [19].

However, fully digital architectures requires one mixer and A/D converter (ADC) per antenna, potentially significantly increasing the power consumption over traditional phased arrays. To compensate, the ADCs in fully digital designs must be typically run at very low resolutions (e.g. 3-4 bits) [9], [11], [12], [20]. To assess digital beamforming our analysis will also include bit-width optimizations in the relevant digital

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TABLE I: System parameters used in the analysis.

Parameter	Value		Remarks
Carrier frequency f_c	28 GHz	140 GHz	
Number RX antennas, N_{rx}	8	64	Assume a single array, typically UPA.
Subcarrier spacing (SCS), kHz	120	240	
Number component carriers, N_{CC}	4	8	
Bandwidth per CC, B_{CC} (MHz)	95.04	190.08	Based on 66 occupied RBs per CC [22]
FFT size per CC, N_{FFT}	1024	1024	
Total bandwidth, $B_{CC}N_{CC}$ (GHz)	0.380	1.52	
Sample rate, f_{samp} (GHz)	0.491	1.966	Based on FFT size, SCS and N_{CC}
OFDM symbol duration, T_{sym} (μs)	8.92	4.46	Derived from SCS
Number digital streams per CC, N_{str}	2	2	More streams not needed due to lack of spatial diversity

components.

II. System Assumptions

The parameters for the analysis at 28 and 140 GHz system are shown in Table I. For the 28 GHz system, we assume a UE array with $N_{\mathrm{rx}} = 8$ antennas, consistent with capacity simulations in [21] as well as recent UE designs in [18]. Note, as described in [18], UE devices may have multiple arrays for 360 degree coverage, but we assume here that only one such array is on at a time. For the 140 GHz system, we assume $N_{\mathrm{rx}} = 64$ antennas. Due to the smaller wavelength, a 64 element array (e.g. 8×8 UPA) at 140 GHz can occupy a smaller total area compared to an 8 element array (e.g. 2×4 UPA) at 28 GHz.

As stated in the Introduction, we consider a 3GPP NR type system [3] with carrier aggregation [6]. We let N_{CC} denote the number of component carriers (CCs), and assume each component carrier has a sample rate of f_{CC} and occupied bandwidth of B_{CC}. The total sample rate is $f_{\mathrm{samp}} = N_{CC} f_{CC}$.

Following the 3GPP NR standard, we assume each component carrier uses an OFDM processing with an FFT size N_{FFT}. For the 28 GHz system, we assume $N_{CC} = 4$ components carriers with configuration as described in [22] with commonly used 5G parameters today. Specifically, the carriers are spaced at 100 MHz with an occupied bandwidth of $B_{CC} = 95.04$ MHz (66 resource blocks). We assume a sub-carrier spacing of 120 kHz and $N_{FFT} = 1024$ FFT size, also standard for 28 GHz deployments. For the 140 GHz systems, we assume a sub-carrier spacing of 240 kHz. We also assume $N_{CC} = 8$ component carriers spaced at 200 MHz with an occupied bandwidth of $B_{CC} = 190.08$ MHz each, providing a total signal bandwidth of 1.6 GHz, four times the bandwidth of the 28 GHz (roughly scaling the bandwidth with the carrier frequency). For both systems, the sample rate is derived from the FFT size, number of component carriers, and sub-carrier-spacing.

As a final key assumption, for the data plane, we assume that a mobile device needs to support $N_{\mathrm{str}} = 2$ digital streams in each component carrier. Larger numbers of streams are likely not needed since the channels will lack spatial diversity (although polarization diversity is still possible)

III. Architecture

We analyze the power for both fully digital and analog receivers as shown in Fig. 1. In the **fully digital receiver (top panel)**, each RX antenna has an independent LNA, mixer and A/D pair with the A/D running at the full wideband sampling rate f_{samp}. In each antenna and each component carrier, a CC selection filter is used to extract the N_{CC} component carriers. Each CC filter consists of an numerically controlled oscilator (NCO) to select the correct CC, a low pass filter and $1/N_{CC}$ downsampler. The output of each CC filters runs at a sample rate of $f_{CC} = f_{\mathrm{samp}}/N_{CC}$.

The key idea for the remaining component processing is that the data plane must support a limited number of streams at a wide bandwidth, while the directional search can be performed on a narrowband with all directions. To this end, for the data plane in the fully digital design, the output of the N_{rx} ADCs in each CC is fed to a N_{rx}-input N_{str}-output linear digital beamformer where N_{str} is the number of digital streams required per CC. Each of the N_{str} streams is then fed to an FFT engine for the OFDM processing. The digital BF thus eliminates the need to run one FFT on each antenna – instead it is run on each stream.

For the directional search, we exploit the fact that the search in the NR standard can be performed on a narrowband primary synchronization signal (PSS), which would fit in a single CC [14]. We thus run a PSS searcher on each antenna, but in only one CC. In addition, the PSS searcher runs at a low SNR and can therefore benefit from very low bit widths. In fact, simulations in [13] suggest two bits is sufficient.

For the **analog receiver architecture (lower panel)**, each RX antenna is first passed through an LNA and then one RF phase shifter for each stream to perform the analog beamforming. This produces a total of N_{rx} RF signals for each stream. The streams are then combined and a mixer is used to downconvert to baseband where there is one ADC pair for each stream. In each stream, there are N_{CC} CC selection filters to extract the component carriers. There is one OFDM FFT for each stream in each CC. Also, on one CC, we run a PSS searcher.

IV. Power Consumption Estimation

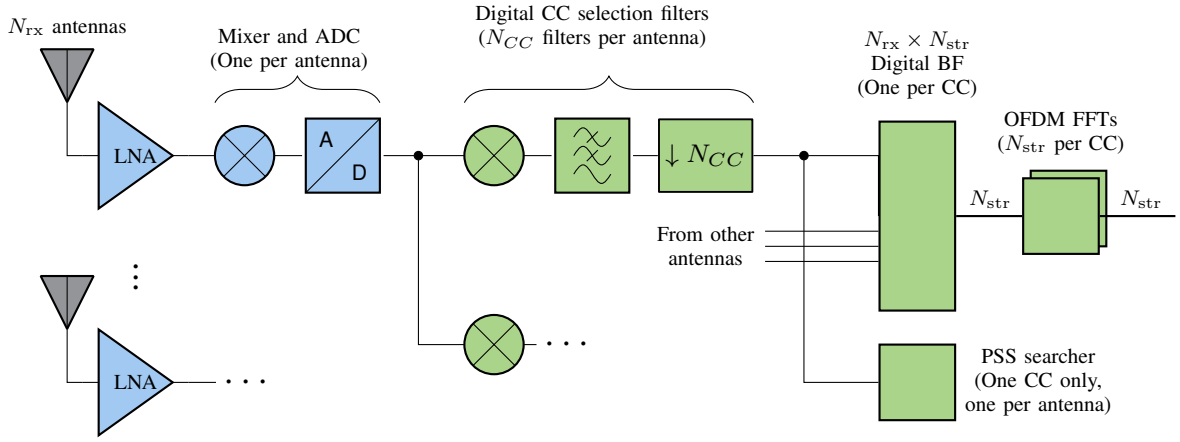
In this section, we model the power consumption of the analog and fully digital beamforming receiver systems at mmWave and sub-THz frequencies. The power consumption of the receiver can be modeled as follows.

Low Noise Amplifier: In mmWave and sub-THz frequencies, the LNA design is very challenging due to the low noise figure requirements [23]. The DC power drawn by the LNA P_{LNA} can be calculated as [24],

$$P_{LNA} = \frac{G}{\mathrm{FoM}(\mathrm{NF} - 1)}, \tag{1}$$

where G is the gain, FoM is the figure of merit in mW^{-1}, and NF is noise figure of the LNA.

(a) **Fully digital RX**



(b) **Analog RX**

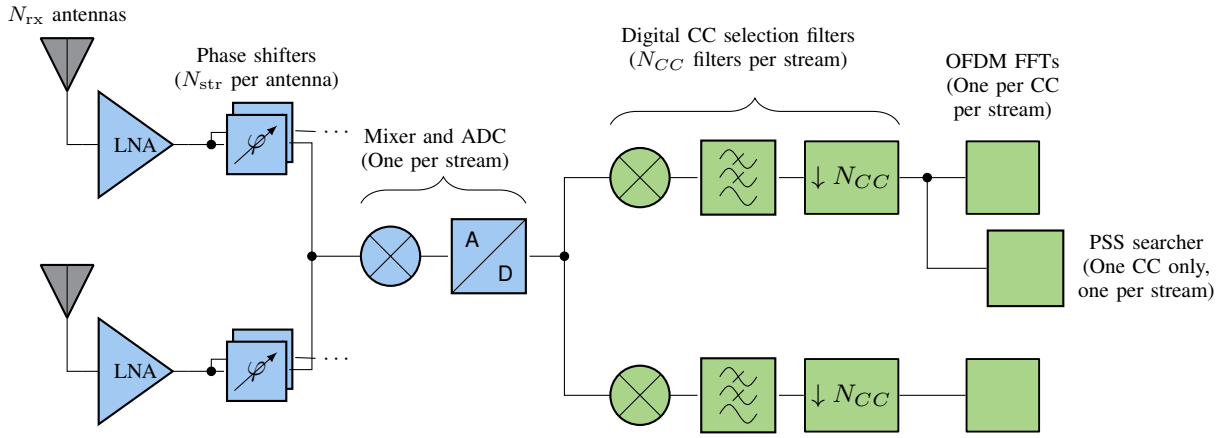


Fig. 1: High level architecture for the fully digital receiver (top panel) and analog receiver (bottom panel) to be analyzed. Each architecture supports N_{rx} antennas, N_{CC} component carriers and N_{str} digital streams per component carrier. The blue boxes represents components in analog, and the green boxes are components in digital. In the RF front-end, some components such as filters and the VGA are not shown.

In Table II, we compare the fully digital and analog architectures taking into consideration the insertion loss of the RF phase shifters in the above equation. In both architectures, there are N_{rx} LNAs. Similar to [9], for the fully digital design we assume that the LNA must supply a gain of $G = 10$ dB. For the analog case, we assume that the LNA gain must be increased by a factor of $IL_{PS} = 10$ dB for the insertion loss of the phase shifters [25]. Additionally, in the analog case, each antenna requires one phase shifter for each digital stream, so the gain requirement will increase by a factor of N_{str}, the number of digital streams. For the 28 GHz systems, we take into consideration a BiCMOS LNA reported in [26], with a minimum noise figure $NF = 3.1$ dB, and $\text{FoM} = 8.46$ mW^{-1}. For the 140 GHz system, we use the parameters of the CMOS LNA described in [27], which has a minimum noise figure $NF = 5.2$ dB, and $\text{FoM} = 0.87$ mW^{-1}. See also [25].

Mixer LO: In the power analysis, we consider mixers as passive components that introduce IL and do not draw any power. The power drawn by the mixers is due to the local oscillator. In Table II we report the $P_{LO} = 10$ dBm for the 28 GHz systems based on the analysis of an I/Q modulator in [28]. For the 140 GHz systems we consider the $P_{LO} = 19.9$ dBm based on the LO design in [27]. In the digital design, there are N_{rx} mixers, one for each antenna. In the analog design, there are N_{str}, one for each digital stream.

A/D converters: In the fully digital beamforming case, we need one ADC pair for each of the N_{rx} antennas. The ADC pair has one ADC for the in-phase (I) component and a second for quadrature (Q) component. In the analog beamforming case, we need only one ADC pair for each of the N_{str} digital streams. The power consumption of each ADC is given by [11],

$$P_{ADC} = \text{FoM}_{ADC} f_{\text{samp}} 2^n, \tag{2}$$

where f_{samp} is the sampling rate, n is the number of bits and and the FoM_{ADC} is a figure of merit of the data conversion, sometimes called the energy per conversion step.

To reduce the power consumption in the analog case, we can lower bit resolution with the assumption that the degradation in

TABLE II: Power consumption estimates (in mW) for the fully digital and analog receiver architectures with parameters in Table I.

Component	**Fully Digital**		**Analog**		**Remarks**
	28 GHz	140 GHz	28 GHz	140 GHz	
LNA	9.05	325	180	6515	$N_{\rm rx}$ LNAs required for both designs, but the power consumption is increased in the analog case since each LNA drives $N_{\rm str}$ phase shifters at IL=10 dB.
Mixer LO	80	6272	20	196	LO drives the mixers which is itself passive. The LO supplies $N_{\rm rx}$ mixers for the digital case and $N_{\rm str}$ mixers for the analog case.
ADC	8.18	261	16.4	65.4	$N_{\rm rx}$ 4-bit ADC pairs for digital and one 8-bit ADC pair for analog.
CC LPF	51.12	818	22.72	45.44	$N_{\rm rx}N_{\rm CC}$ filters for digital and $N_{\rm str}N_{\rm CC}$ filters for analog.
Digital BF	6.4	204.8	0	0	$N_{\rm CC}$ units each performing $N_{\rm rx} \times N_{\rm str}$ beamforming. Not used in analog case.
Total	**155**	**7881**	**239**	**6822**	

SNR can be compensated with beamforming. Prior simulations [9], [11], [12], [20] have indicated that 4 bits is sufficient for most cellular data and control plane operations. In Table II, we consider an ADC with FoM = 65 fJ/conv, based on the 4-bit flash-based ADC designed in [29]. We consider $N_{\rm rx}$ 4-bit ADC pairs for the fully digital architecture, and $N_{\rm str}$ 8-bit ADC pairs for the analog architecture. As shown in Table I, the sampling frequency for the 28 GHz systems is $f_{\rm samp} = 0.491$ GHz, and $f_{\rm samp} = 1.6$ GHz for the 140 GHz system.

Component carrier downsampling filters: Carrier aggregation with multiple component carriers (CCs) requires filters to extract the samples from the different CCs. We assume each CC is processed with $1/N_{CC}$ of the samples, where N_{CC} is the number of CCs. We assume a standard CC channel selection filter: The samples from the ADC are first passed through a numerically controlled oscillator (NCO) to shift the CC to be centered around DC. The shifted samples are then passed through a digital finite impulse response (FIR) low pass filter (LPF) to remove out-band noise in the adjacent CCs. The FIR filter outputs are then downsampled by $1/N_{CC}$ resulting in a sample rate of $f_{CC} = f_{\rm samp}/N_{CC}$ per CC.

The power analysis of any digital component will depend strongly on the bitwidths in the processing. For the CC selection filter, we considered a filter with 6-bit coefficients and $L = 65$ taps. The 6-bit coefficients were multiplied by 4-bit ADC outputs and accumulated with 12 bits. The MATLAB DSP toolbox was then used to find a filter with a maximum ripple in the passband up to $B_{CC}/2$ and maximum stopband rejection for frequencies beyond $f_{\rm samp}/N_{CC}/2$. The optimized filter response for the 28 GHz system is shown in Fig. 2 and we observe a stopband rejection of $A_{\rm st} = 29.19$ dB.

To estimate the power of the filter, observe there are $2L$ multiply-and-accumulate (MAC) operations in each filter output (the factor of 2 due to I and Q). Each filter outputs at a rate of $f_{\rm samp}/N_{CC}$. In the digital design, there are $N_{\rm rx}N_{CC}$ filters. Thus, the power consumption for the CC filters in the fully digital case is

$$P_{\rm LPF} = 2E_{\rm MAC}LN_{\rm rx}f_{\rm samp}, \tag{3}$$

where $E_{\rm MAC}$ is the energy per real MAC. Similarly, for the analog beamforming case, we need one filter per digital stream and CC, and we obtain the power,

$$P_{\rm LPF} = 2E_{\rm MAC}LN_{\rm str}f_{\rm samp}. \tag{4}$$

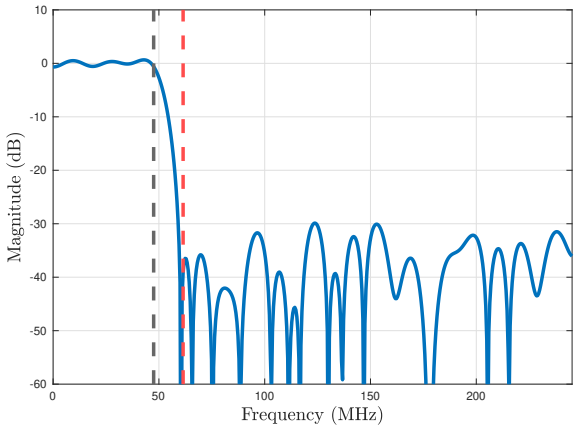


Fig. 2: Frequency response of a possible CC downsampling filter for the 28 GHz system. The filter is implemented with 6-bit coefficients and 65 taps. The passband is $B_{CC}/2$ shown in the black dashed line and the stop-band begins at $f_{\rm samp}/N_{CC}/2$ shown in the the red dashed line.

Initial power estimations with the TSMC 28nm process show that the fully-digital design needs $E_{\rm MAC} \approx 100$ fJ per MAC at 28 GHz, and $E_{\rm MAC} \approx 50$ fJ per MAC at 140 GHz, and the analog design needs $E_{\rm MAC} \approx 178$ fJ per MAC at 28 GHz and $E_{\rm MAC} \approx 88$ fJ per MAC at 140 GHz (the analog design has a larger number of input bits from the ADC, and the 140 GHz requires less since the SNR per antenna is lower).

Digital beamformer: The fully digital design also requires a digital beamformer multiplying the inputs from $N_{\rm rx}$ antennas to $N_{\rm str}$ digital streams. In each sample, it must perform $N_{\rm rx}N_{\rm str}$ MACs. Since the total sample rate across all CCs is $f_{\rm samp}$, the total power consumption is $P = E_{\rm MAC}N_{\rm rx}N_{\rm str}f_{\rm samp}$, where $E_{\rm MAC}$ is the energy per complex MAC. Again, initial power estimations with the TSMC 28nm process show that $E_{\rm MAC} \approx 1$ pJ per complex MAC was possible with 6-bit real inputs from the CC filters. The resulting power is shown in Table II.

PSS searcher: The PSS is essentially a matched filter for the PSS sequences from the base station. Similar to results in [13], we found that the PSS searcher can be implemented in very low number of bits (1-2). At this resolution, the PSS is most efficiently implemented directly in time-domain (not via

convolution), and our initial calculations show the results are negligible and are not shown in the table.

OFDM FFT engines: The OFDM processing in the NR standard requires FFT engines. Both the analog and fully digital designs require $N_{\rm str}N_{\rm CC}$ FFTs in each OFDM symbol period. We are still evaluating the power consumption for this processing, but it is the same for both designs.

V. Conclusions

We have attempted to assess the power consumption of multi-carrier receivers for both 28 GHz and 140 GHz systems using realistic parameter values and state-of-the-art device characteristics. Three key conclusions can be seen:

- *Mixer and phase shifter power are dominant:* The power in the mixer (in the fully digital case) and phase shifter (in the analog case), is overwhelmingly dominant. These components must be the focus of future research if power consumption is to be significantly reduced.
- *Fully digital vs. analog:* Although fully digital architectures offer considerable benefits over analog beamforming in high mobile scenarios, the power consumption is comparable assuming aggressive bit-width optimization.
- *Applications and outlook:* Our initial estimates show that a 64 element 140 GHz receiver consumes approximately 7 Watts which is prohibitive for handsets that generally have a maximum peak power of 1 to 4 Watts. However, it is possible that this power may be available in other scenarios including robotics, cars, UAVs and point-to-point links (e.g. cellular front-haul). In addition, much of the devices in the 140 GHz are in their infancy. For example, the FoM for the 140 GHz LNA is almost ten times worse than the 28 GHz part. This suggests that there is considerable scope to improve power consumption in high frequency devices, potentially widening their applicability.

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