A 140GHz power amplifier with 20.5dBm output power and 20.8% PAE in 250-nm InP HBT technology

Ahmed S. H. Ahmed[#1], Munkyo Seo[*], Ali A. Farid[#], Miguel Urteaga[$],
James F. Buckwalter[#], and Mark J. W. Rodwell[#]
[#]Department of Electrical and Computer Engineering, University of California, Santa Barbara, USA
[$]Teledyne Scientific Company, Thousand Oaks, CA 91360, USA
[*]Department of Electrical and Computer Engineering, Sungkyunkwan University, South Korea
[1]a_s_ahmed@ucsb.edu

***Abstract*—We report a high-efficiency D-band power amplifier in 250nm InP HBT technology. The design has three common-base stages and a low-loss 4:1 transmission-line output power combiner. The amplifier has 20.5 dBm peak saturated output power with 20.8% PAE and 15dB associated large-signal gain at 140GHz. At 1dB gain compression, the output power is 17dBm with 9.7% PAE. The amplifier's peak small-signal gain is 20.3dB at 140GHz, and the small-signal 3-dB bandwidth is 120-163GHz. Over a 125-150GHz bandwidth, the saturated output power is within 2dB of its 140GHz maximum, with an associated PAE greater than 14.3%. The amplifier consumes 0.52W DC power and occupies 0.69mm^2 area. To the authors' knowledge, this result improves the state-of-the-art peak PAE at 140GHz by 1.6:1 for amplifiers of comparable saturated output power.**

***Keywords*—D-band, millimeter wave, high efficiency, power amplifiers, InP, transmission-line combiner.**

I. Introduction

There is an increasing demand for high-capacity mobile communication [1]. Considering millimeter frequencies for the next communication generation provides increased frequency spectrum and the shorter wavelengths support massive spatial multiplexing in hub and backhaul systems. Unfortunately, λ^2/R^2 path loss and weather attenuation are high. Given the assumptions of [1], at 140GHz, to serve 128 users at 100m range and 10Gb/s/user using a 256-element MIMO array, the required operating output power per element is 16.5dB$_m$ and the 1dB gain compression point must be ~2.5dB greater than this. Given the large array, efficient power amplifiers are critical, generating less heat and simplifying package design.

140GHz CMOS power amplifiers [2] and transmitters [3] are feasible, but have limited output power and efficiency. SiGe technologies have higher output power ([4]-[6]) and good efficiency. InP technologies ([7], [8]) have simultaneously superior output power and efficiency.

Here we report a 140GHz, 20.5dBm amplifier with 20.8% PAE and 15dB associated large signal gain. The key features in the design are a low-loss transmission-line power-combining network, a common base architecture, and driver scaling to sustain good PAE. The amplifier has a peak measured small signal gain of 20.3dB at 140GHz with a 3dB BW of 43GHz. The 140GHz OP$_{1dB}$ is 17dBm with 9.7%PAE. Over a 125-150GHz bandwidth, the saturated output power is within 2dB of its 140GHz maximum, with an associated PAE greater than 14.3%. The amplifier demonstrates low DC power dissipation of 0.52W and compact area of 0.69mm^2.

II. Power Amplifier Design

ICs were fabricated in the Teledyne 250nm InP technology [9], which has four Au interconnect layers, 0.3fF/μm^2 MIM capacitors and 50Ω/square thin film resistors. The HBT has a maximum 650GHz power gain cut-off frequency (f_{max}), a maximum 3mA/μm current density and the 4.5V BV$_{CEO}$.

A. Unit Cell design

Both common-emitter (CE) and common-base (CB) designs were considered. In power amplifiers, the output tuning network is designed for maximum saturated output power, not for maximum small-signal gain [10]. Large-signal simulations for CE (Fig. 1a), CB with a grounded base (Fig. 1b), and CB with a finite base capacitance (Fig. 1c) are performed under loading for maximum saturated output power, for a device having 4 emitter fingers each of 6μm length, biased at 1.4mA/μm and V_{CE}=2.5V. The CB stage with grounded base (Fig. 1d) has ~2.4dB greater gain than CE, but biasing requires a negative supply V_{EE} and system efficiency is degraded by the voltage drop across the necessary emitter bias stabilization resistor R_e or DC current source. We instead use a CB stage with a base bypass capacitor (Fig. 1c). The base resistor R_b provides stable control of I_C; DC power wasted in R_b is small because I_B is much smaller than I_C. The maximum base capacitance is limited by physical layout and the resulting self-resonance. The capacitor's impedance is nonzero, there is a significant AC base voltage swing, and the gain is reduced. However, the PAE is almost constant despite this gain reduction, (Fig. 1d): the CB stage with finite base capacitance, coupled with its driver stage, can be analyzed as a generalized series-power-combined stage ([11]-[13]), with the output power being the sum of power contributed by the output transistor and input power from the driver stage.

Though the CE and capacitively-bypassed CB stages show similar saturated PAE, the capacitively-bypassed CB stage was selected because the latter shows greater PAE at the 1dB gain compression point. This is a consequence of gain linearization provided by the impedance presented to the base. The OP$_{1dB}$ for CB with a 600fF base capacitance is 15.2dB$_m$ with 29.7% PAE compared to 12dB$_m$ with 15.4% PAE in CE and 13.5dB$_m$ with

22.4% PAE for the grounded-base CB stage. OP_{1dB} is highest for the finite-base-capacitance CB stage simply because of the contribution of the driver stage power.

Though not documented here, the 4-finger CB layout also presented smaller parasitic interconnect impedances than did the 4-finger CE design, providing larger gain once electromagnetic analysis of multifinger layout parasitics were included in the simulations. Multifinger transistor layout design is critical in mm-wave power amplifiers. The transistor footprint is similar to [14], except that the bases are grounded through a 426fF MIM capacitor. The power unit cell has 2 emitter fingers, each 12μm length, with base contacts at each end; in terms of parasitic base metal inductance and resistance, this layout is equivalent to 4 fingers each 6μm emitter length.

The transistor collector capacitance (Fig. 2a) is tuned by a shunt inductive transmission-line section, terminated by a bypass capacitor. This network also supplies the collector DC bias. The base DC bias is routed between cells using the transistor collector contact metallization layer, which, because it lies below the metal-1 ground plane, reduces coupling between DC and RF signal lines. The microstrip lines use a metal-1 ground plane and metal-4 RF conductor. The inputs of two unit cells inputs are combined and matched to the driver optimum load impedance by L-C sections. Staggered matching provides wide band operation. Input shunt stubs provide both RF impedance tuning and a DC path for the emitter current. DC bias is isolated between stages using series MIM coupling. ADS momentum and HFSS tools are used to simulate all routing and matching circuits.

B. Driver design

Two driver stages are added to increase the gain. Their architecture (Fig. 2b) is similar to the PA cell. The base capacitance is increased to 603fF, increasing the gain to ~7dB. The driver output power is sufficient for one driver cell to drive two PA output cells. The driver's input and output impedances are matched close to 50Ω. As with the output cells, matching network tunings are staggered for increased bandwidth. The transistor base bias is distributed on the collector contact metal layer, while DC collector bias is distributed on metal 4. All DC bias lines are by bypassed using MIM capacitors with 10Ω series damping resistors. The first driver stage uses the same transistor size as the 2nd driver stage, but uses reduced DC bias, V_{CC3} and V_{BB3}, for higher PAE.

C. Combiner design

Four 50Ω power cells are combined to achieve the required power. For 50 Ω load, cascaded Wilkinson combiners (Fig. 3b) can provide 4:1 combining, this requires two cascaded $\lambda/4$ sections and results in a simulated 0.66dB loss at 140GHz and large die area. The proposed combiner (Fig. 3a), similar to ([15], [16]), uses only one $\lambda/4$ section, which is more compact and has 0.48dB at 140GHz simulated losses for 50 Ω load. Two 50Ω cells are combined using transmission line sections with Z_1=50Ω. The length of Z_1 is kept small for minimum loss but the length does not impact the impedance transformation. The required load impedance for two combined cells is 25Ω. This is

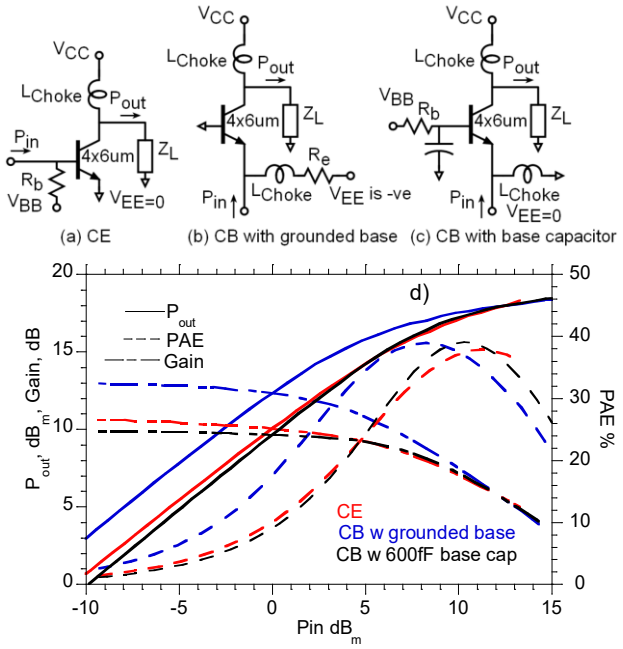

Fig. 1. Schematic diagram of: (a) CE (b) CB with grounded base; (c) CB with 600fF base capacitor; (d) P_{out}, gain, and PAE for CE, grounded CB, and CB with base capacitor.

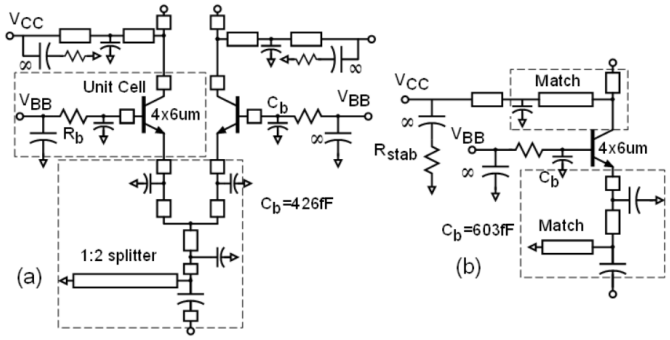

Fig. 2. Schematic diagram of: (a) two combined power amplifier cells driven by a single driver cell; (b) driver stage with input/output matching circuits

achieved by the $\lambda/4$ section, Z_2, which transforms the 100Ω presented at its load to 25Ω.

The amplifier is designed for packaging. The IC uses a dense array of through-substrate vias (TSVs) to connect the chip and backside ground planes and to suppress substrate modes. The RF I/O pads are relatively large, 55μm×57.5μm, to be compatible with wirebonds. To tune the resulting pad capacitance, Z_2 is adjusted to 31 Ω. This increases the 4:1 combiner loss to 0.93dB (including the shunt inductive tuning elements and without the pad losses). The simulated pad loss is ~0.32dB at 140GHz.

III. Measurement Results

Fig. 4a shows the IC micrograph and Fig. 4b the IC block diagram. S-parameter are measured using an HP network analyzer with VDI 110-170GHz frequency extenders and 140-220GHz GGB wafer probes with WR-5 to WR-6 waveguide adapters. Probe-tip calibration is done using SOLT standards

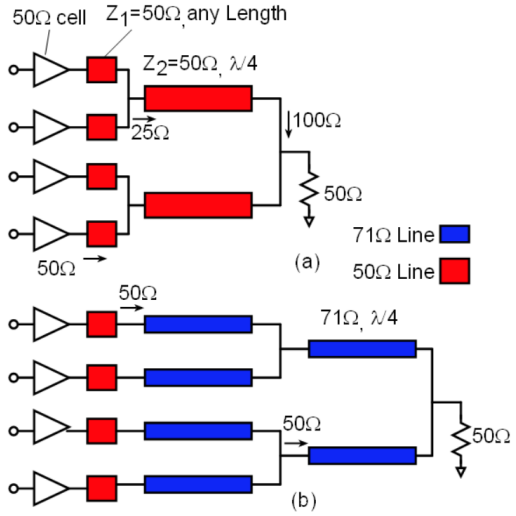

Fig. 3. Schematic diagram (a) 4:1 low loss transmission line combiner for 50Ω load; (b) 4:1 Wilkinson power combiner (with bridging resistors omitted) for 50Ω load

on an external CS-15 calibration substrate. Table 1 summarizes the DC biases. The DC biases of the drivers are optimized to improve the PAE; the IC dissipates 0.52W.

The IC has 20.3dB peak measured small-signal gain (Fig. 5) at 140GHz. The agreement between the measurement and simulation results is best when the foundry-recommended base inductance is neglected. As the impedance presented to the HBT base involves a series combination of this inductance and the MIM base bypass capacitance, we believe that this disparity is due to small errors in modelling the MIM base capacitance.

The gain S_{21} is flat to within 1dB between 126-146GHz and to within 3dB gain between 120-163GHz. The input reflection coefficient S_{11} is better than -10dB from 138GHz to 157GHz and at better than -8.4dB from 120 to 170GHz. As the output is tuned for maximum saturated output power, S_{22} is necessarily poor, but is better than -6dB from 120-145GHz.

Power was measured on the 3-mil die without bonding to a heat sink. A 110-170GHz VDI frequency extension module with an added output attenuator delivers up to ~10dBm, sufficient for power measurement. 140-220GHz wafer probes were used with WR6 to WR5 adaptors. An Ericson meter measured the output power. Probe losses were measured to move the power reference plane to the probe tips.

Table 2 summarizes the DC bias condition. The RF input signal changes slightly the bias current and the base voltage is adjusted at each power sweep to keep a constant current. The output stage is biased at 130mA and 2.5V for V_{CC1}. Bias for the first stage was reduced (V_{CC3}=1.5V, I_{CC3}=32mA) for increased PAE. Fig. 6 shows the large- signal power measurement and simulation results. There is a good agreement between measurement and simulation. At 140GHz, the amplifier has a peak saturated output power of 20.5dBm with 20.8% PAE and 15dB associated gain. At 1-dB gain compression, the amplifier has 17dBm output power and 9.7% PAE. Over a 125-150GHz bandwidth, the saturated output power is within 2dB of its 140GHz maximum, with an associated PAE greater than 14.3% as shown in Fig. 7.

IV. Conclusion

A high-efficiency D-band power amplifier has been demonstrated in 250nm InP HBT technology. The compact amplifier utilizes 3 gain stages and a low-loss output power combiner. Capacitive grounding linearizes the common-base stages, providing increased efficiency at the 1dB gain-compression point, yet this linearized stage design maintains gain comparable to a common-emitter stage. The amplifier shows 112mW saturated output power with 20.8% PAE. The amplifier provides wide band operation with 43GHz small signal BW and low DC power consumption. Table 3 compares the state-of-the-art D-band amplifiers: PAE is improved 1.6:1 for amplifiers of comparable saturated output power.

Table 1. DC biases for S-parameters

V_{CC1}	V_{CC2}	V_{CC3}	V_{BB1}	V_{BB2}	V_{BB3}
2.5V	2.5V	1.5V	1.94V	1.36V	1.1V
I_{CC1}	I_{CC2}	I_{CC3}	I_{BB1}	I_{BB2}	I_{BB3}
121mA	52mA	31.8mA	4.1mA	1.7mA	0.95mA

Table 2. DC biases for Power measurement

V_{CC1}	V_{CC2}	V_{CC3}	V_{BB1}	V_{BB2}	V_{BB3}
2.5V	2.5V	1.5V	1.95V	1.4V	1.1V
I_{CC1}	I_{CC2}	I_{CC3}	I_{BB1}	I_{BB2}	I_{BB3}
130mA	56mA	34mA	5mA	2mA	1mA

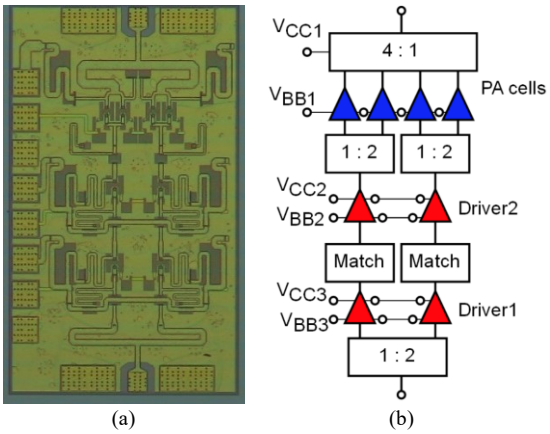

Fig. 4. (a) Chip micrograph of the power amplifiers. The area is 1.08mm × 0.63mm including the pads. (b) amplifier block diagram.

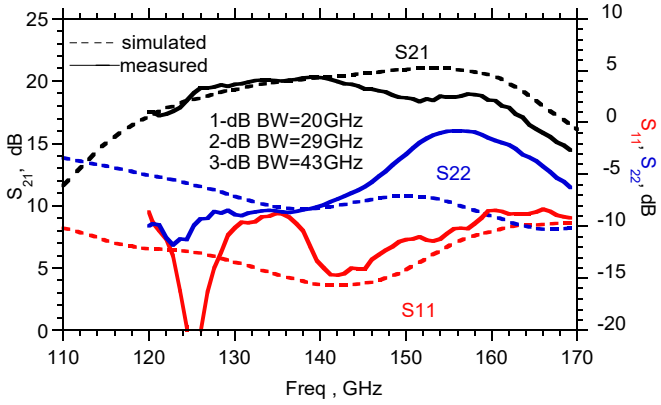

Fig. 5. Measured (solid) and simulated (dashed) S-parameters

Table 3. Comparison between state-of-the-art D-band amplifiers.

Ref	Technology	Freq (GHz)	P_{sat} (dBm)	BW_{3dB} GHz^{++}	Gain at P_{sat} (dB)	Peak PAE %	Size (mm^2)	P_{DC} (W)	P_{sat}/Area mW/mm^2
[2]	40 nm CMOS	140	14.8	17	13**	8.9	0.34	0.3	88.8
[4]	130-nm SiGe HBT	155-180	18.0	25	23.5**	4.0	0.85	1.57*	74.2
[5]	130-nm SiGe HBT	1s-142	17$^+$	16	29**	13$^+$	1.06	0.39*	47.2
[6]	130-nm SiGe HBT	131-180	14	49	22**	5.7	0.48	0.44*	52.3
[7]	250-nm InP HBT	110-150	23.2-24.0	32.7	14-16	5.8-7.0	1.89	3.46	134
[8]	250-nm InP HBT	115-150	21-21.8	34.8	15-17.5	8.2-10.5	0.75	1.54	205
This work	**250-nm InP HBT**	**125-150**	**18.9-20.5**	**43**	**12.3-15.9**	**14.3-20.8**	**0.69**	**0.52**	**162**

*Estimated from maximum PAE, P_{sat}, and compressed gain. ** graphically estimated. +Balun loss de-embedded. ++Small signal BW

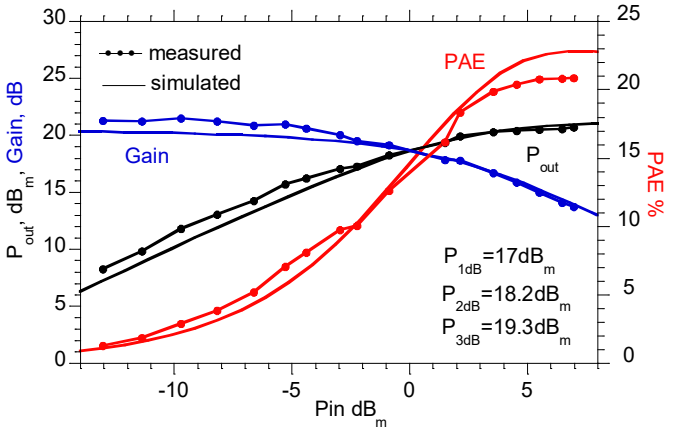

Fig. 6. Measured and simulated output power, PAE, and gain versus the input power at 140GHz.

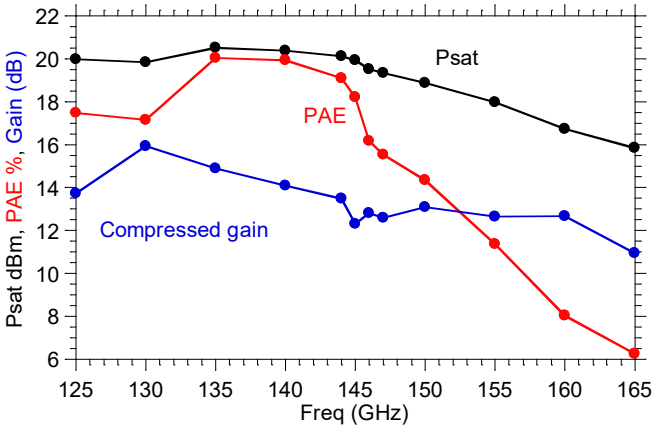

Fig. 7. Measured saturated output power, PAE and the compressed gain vs. frequency

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